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A Figure of Merit for Optimization of Nanocrystal Flash Memory Design

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Nanocrystals can be used as storage media for carriers in flash memories. The performance of a nanocrystal flash memory depends critically on the choice of nanocrystal size and density as well as on the choice of tunnel dielectric properties. The performance of a nanocrystal memory device can be expressed in terms of write/erase speed, carrier retention time and cycling durability. We present a model that describes the charge/discharge dynamics of nanocrystal flash memories and calculate the effect of nanocrystal, gate, tunnel dielectric and substrate properties on device performance. The model assumes charge storage in quantized energy levels of nanocrystals. Effect of temperature is included implicitly in the model through perturbation of the substrate minority carrier concentration and Fermi level. Because a large number of variables affect these performance measures, in order to compare various designs, a figure of merit that measures the device performance in terms of design parameters is defined as a function of write/erase/discharge times which are calculated using the theoretical model. The effects of nanocrystal size and density, gate work function, substrate doping, control and tunnel dielectric properties and device geometry on the device performance are evaluated through the figure of merit. Experimental data showing agreement of the theoretical model with the measurement results are presented for devices that has PECVD grown germanium nanocrystals as the storage media.

Keywords: Nanocrystals, Germanium, PECVD, Germanosilicate, Capacitance Spectroscopy, Memory, Retention.

1. INTRODUCTION

Nanocrystals (NCs) formed by annealing silicon dioxide films having excess Si or Ge has attracted much attention due to optical and electronic properties of such nanostructures.[1–3] In particular, NCs embedded in silicon oxide films have been subject of study for their potential applications in memory devices.[4] Among various methods of synthesis of the NCs are, ion implantation into oxide, co-sputtering of oxide and germanium (Ge), low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD) followed by appropriate annealing of the grown films.[5,6] Since many parameters of NCs such as density, size, and composition can be adjusted by proper choice of deposition parameters, NCs offer flexibility in design of flash memory cells. However, understanding of charge storage mechanisms is important in optimization of device performance.

In this paper, we analyze nanocrystal memory charging and retention dynamics by assuming carrier storage in NC energy levels instead of deep traps. Based on this assumption, we present a theoretical model that includes the effect of NC dimensions and density to calculate the charging and discharging dynamics. Gate work function, substrate doping and tunnel dielectric properties are inherently included. This study is restricted to electron storage in Ge NCs for the sake of simplicity. The analysis can be extended to Si NCs by adjustment of material parameters, and can further be extended for hole storage in Si and Ge NCs with proper adjustment of the band-bending model.

2. THEORETICAL MODELLING

A typical nanocrystal metal-oxide-semiconductor (NC-MOS) memory element consists of a standard MOS capacitor with a layer of NCs embedded in the oxide between the gate and the substrate as shown in Figure 1.

Based on the assumption that only NCs are responsible for charge storage and that a single electron per NC is

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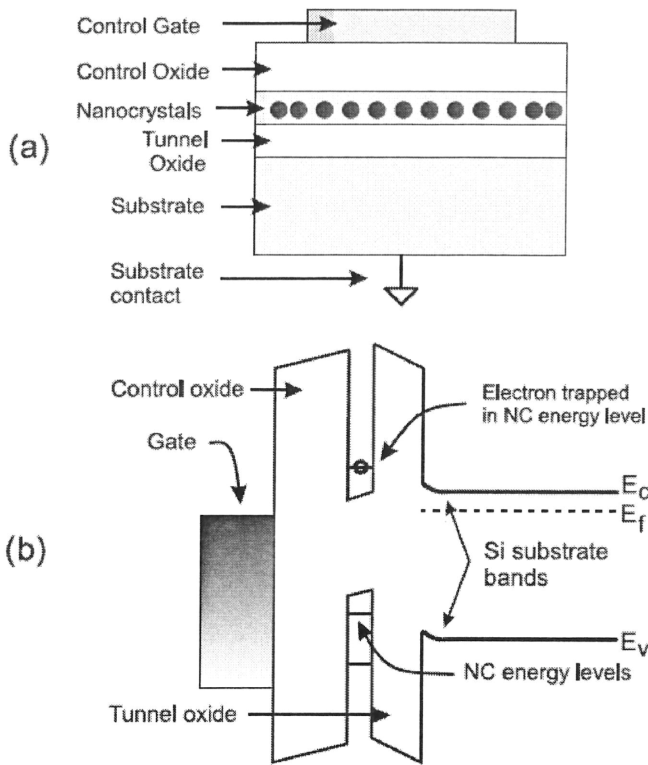

Fig. 1. Typical nanocrystal MOS capacitor memory test element with an n-type substrate. (a) Cross-section and (b) band diagram of charged element under 0 V bias.

stored for a total of n_{NC} NCs, the flat-band voltage shift ΔV_{FB} is approximately given by[7]

$$\Delta V_{FB} = \frac{q n_{nc}}{\epsilon_{ox}}\left(t_{cox} + \frac{\epsilon_{ox}\, t_{nc}}{2\,\epsilon_{ge}}\right) \tag{1}$$

where q is the electronic charge, t_{cox} is the control oxide thickness, t_{nc} is the average diameter of the NCs, ϵ's are the dielectric constants of respective materials.

In order to evaluate dynamical properties of such memory elements, charging and discharging currents must be calculated taking into account tunnelling through the barrier for a given electric field within the tunnelling region. The currents also depend on availability of source and target states. Since there are many device parameters that collectively determine the charge-discharge currents, a simple closed form formula can not be obtained that covers all cases. Therefore, in the following subsections, charge and discharge currents are studied separately, and intuitive formulas are given whenever possible.

2.1. Charging of the NC-MOS Element

It is best to capture the essential features of charging dynamics with a minimally complex model. During the write cycle, the device is in accumulation and initially there is no stored charge in the device. In this case, the oxide field F_{tox} will be determined by the gate voltage during writing, V_{write}, approximately as $F_{tox} \simeq V_{write}/t_{ox}$, where t_{ox} is the total effective oxide thickness. The tunnelling current through a trapezoidal barrier can be calculated in two different limits, the direct tunnelling and Fowler-Nordheim limits. It should be noted that, it is desirable to have low fields in flash memory devices in order to increase device reliability. In the case of direct tunnelling, charging current density can be calculated using a transmission coefficient which can be calculated by the WKB approach for direct tunneling. The charging current density then becomes[8]

$$J_c = \frac{AF_{tox}^2}{V_B} \times \exp\left[-\left(1-\left(1-\frac{F_{tox}t_{tox}}{V_B}\right)^{3/2}\right)\frac{BV_B^{3/2}}{F_{tox}}\right] \tag{2}$$

where $A = q^2 m_{si}/16\pi^2 m_{ox}\hbar$, $B = 2\sqrt{8m_{ox}q}/3\hbar$, F_{tox} is the tunnel oxide field during charging, m_{ox} is the tunnel effective mass and V_B is the barrier height between the oxide and the substrate. At high fields ($F_{tox}t_{tox} > V_B$) the tunnelling is through a triangular barrier (FN regime) and the tunnel transparency term in Eq. (2) must be rewritten, resulting in a charging current density given by[9]

$$J_c = \frac{AF_{tox}^2}{V_B} \times \exp\left[-\frac{BV_B^{3/2}}{F_{tox}}\right] \tag{3}$$

The actual charge deposited will depend on the availability of final states. This can be accounted for by including a capture cross section per nanocrystal. The differential charge deposited per unit area $d\sigma$ in a time interval $d\tau$ can be calculated through

$$d\sigma = p_c D_{trap} J_c(F_{tox}) d\tau \tag{4}$$

where p_c is the average capture cross section, and D_{trap} is the available density of target states. The capture probability may depend on NC shape and $D_{trap} \approx N_{NC}$ is the NC areal density.

2.2. Discharging of the NC-MOS Element

During retention, the device is in depletion and $V_{gate} = 0$. If NC bound states are responsible for storage of carriers, discharge occurs by tunnelling from the NC ground state to the substrate, either by direct or trap assisted tunnelling. For the case of direct tunnelling, the current density describing the discharge of the NCs is different than Eq. (2) mainly because available source states are not a bulk continuum but are the NC states. Assuming a delta-function distribution for the NC states $D_{NC}(E) = N_{NC}\delta(E - E_{NC})$ located at the quantization energy E_{NC} and a single stored carrier for every NC, the discharge current density can be given as

$$J_d = qN_{NC}T_t(E_{NC})\upsilon_{NC} \tag{5}$$

where $\upsilon_{NC} \simeq \hbar\pi/2m_{ge}d^2$ is the semi-classical escape attempt rate for NCs of diameter d.[10]

The transmission probability $T_t(E, F_{tox})$ for a single electron at energy E can be calculated through the WKB approximation as

$$T_t(E) \approx 4\exp\left[-\left(1-\left(1-\frac{F_{tox}t_{tox}}{V_B(E)}\right)^{3/2}\right)\frac{BV_B(E)^{3/2}}{F_{tox}}\right] \quad (6)$$

The tunnel oxide field is determined by the amount of stored carriers as well as by the band-bending. For a given stored charge, the oxide field therefore depends on the tunnel oxide thickness, total oxide thickness, substrate doping, gate work-function and dielectric constants. In order to obtain an intuitive result, we consider the case where stored charge is small and tunnel oxide field is proportional to the stored charge (or flat-band shift), $F_{tox} \approx \Delta V_{FB}/2t_{ox}$.

For the calculation of the discharge current through Eqs. (5) and (6), the barrier height must also be calculated. The barrier height is a function of the NC ground state energy given by $V_B(E) = V_{B0} - E_{NC}$, where V_{B0} is the bulk barrier height. The energy levels of uncapped germanium NCs have recently been measured directly as a function of size, using scanning tunnelling spectroscopy.[11] An empirical formula for the conduction band minimum of Ge NCs as a function of size is given by

$$E_{CBM}(d) = E_{CBM}(\infty) + \frac{11.86}{d^2+1.51d+3.3936} \quad (7)$$

where the energies are in eV, d is the nanocrystal diameter in nm. Equation (7) can be used to estimate E_{NC}, which can be used in the estimation of the tunnelling barrier observed by the NCs during discharge.

The size distribution of NCs leads to a distribution of energies. Considering a Gaussian size distribution, a density of states (DOS) can be calculated (Fig. 2). The DOS can also be approximated by a Gaussian. In this case, the stored charge is distributed to the available NC states according to Fermi-Dirac distribution with a local quasi-Fermi level. For a Gaussian density of states with peak energy E_p and half width of σ_E, the quasi-Fermi level of the nanocrystal ensemble is given in the zero temperature limit by

$$E_F = E_P + \sqrt{2}\sigma_E \times Erf^{-1}\left(\frac{2n_c}{N_{NC}} - 1\right) \quad (8)$$

where Erf^{-1} denotes the inverse of the error-function, n_c is the total number of stored carriers and N_{NC} is the total number of nanocrystals. The quasi-Fermi depends strongly on the ratio of total stored charge to number of NCs.

Escape of carriers near or above the quasi-Fermi level dominates the discharge current. Therefore, discharge current depends on the number of stored carriers which is proportional to the flat-band voltage shift through Eq. (1). This feature of the escape current is the reason of super-exponential charge decay in NC memory elements. A more intuitive, closed-form formula for the discharge current is

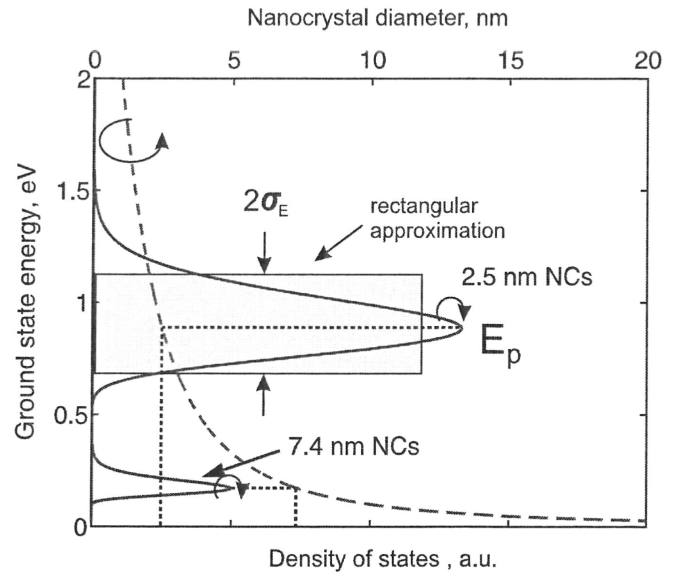

Fig. 2. Schematic description of density of states (solid curves) for the ground states of nanocrystals with two representative average diameters of 2.5 and 7.4 nm. Minimum of energy corresponds to the conduction band edge of bulk germanium. Dotted curve shows electron ground state of NCs as a function of size as described by Eq. (7). Areas under the curves are equal to the NC areal density.

desirable to compare the effect of design parameters on charge retention. However, a simple closed-form expression can not be obtained without further simplifying assumptions. A closed-form formula can be obtained by assuming a rectangular shaped density of states, neglecting band bending effects, assuming a gate work-function that is aligned with the substrate Fermi level and calculating in the zero temperature limit. Then Eq. (8) can be approximated by

$$E_F = E_P + \sqrt{2}\sigma_E\left(\frac{2n_c}{N_{NC}} - 1\right) \quad (9)$$

Under these assumptions, Eqs. (5), (6), and (9) can be used to calculate a closed form for the discharge current at zero gate bias. The discharge current is then given as a function of the flat-band voltage shift ΔV_{FB} due to stored carriers as

$$J_d \simeq \frac{4qN_{NC}\pi\hbar\sqrt{V_p}\exp[-\frac{3}{2}Bt_{tox}\sqrt{V_p}]}{3m_{ge}d^2Bt_{tox}\sigma_E} \times \left(\exp\left(\frac{3Bt_{tox}\sigma_E}{2\sqrt{V_p}}\frac{\Delta V_{FB}}{\Delta V_{max}}\right) - 1\right) \quad (10)$$

where $V_p = V_B - E_p/q$ is the barrier height observed by the average size NC, σ_E is the width of the rectangular energy distribution, t_{tox} is the tunnel oxide thickness, m_{ge} is the electron mass in the nanocrystal, $\Delta V_{max} \simeq qN_{NC}t_{ox}/\epsilon_{ox}$ is the maximum flat-band voltage shift when all nanocrystals carry an electron, and $B = 4\sqrt{2m_{ox}q}/3\hbar$, m_{ox} being the electron tunnelling mass. Note that V_p and σ_E are normalized by q, to have units of Volts.

The approximate discharge current density given by Eq. (10) includes the effects of NC density, size distribution, flat-band voltage shift as well as tunnel oxide thickness and tunnel barrier height.

2.3. Temporal Decay of Stored Charge

The time decay of the NC charge can be calculated through integration of Eq. (10) which is of the form $J_d(\Delta V_{FB}) = J_{d0}(\exp(\beta \Delta V_{FB}) - 1)$. The retention time τ_{ret} is found as a function of initial and final flat-band voltage shifts as

$$\tau_{ret} = \frac{C_{ox}}{J_{d0}\beta} \ln\left(\frac{e^{\beta V_i} - 1}{e^{\beta V_f} - 1}\right) - C_{ox}\frac{V_i - V_f}{J_{d0}} \tag{11}$$

where V_i is the initial flat-band shift before decay, V_f is the final flat-band shift at time τ_{ret}, $\beta = 3Bt_{tox}\sigma_E / 2\sqrt{V_p}\Delta V_{max}$ is as given in Eq. (10). The factor J_{d0} can be referred from Eq. (10) and C_{ox} is the device capacitance per unit area.

2.4. Figure of Merit for a Nanocrystal Memory Cell

The figure of merit (FOM) definition chosen in this article is

$$\text{FOM} = \log_{10}\left(\frac{\tau_{ret}}{\tau_{charge}}\right) \simeq \log_{10}\left(\frac{J_c}{J_d}\right) \tag{12}$$

where τ_{ret} and τ_{charge} are the retention and charging times for a given set of device parameters. The FOM depends on many design parameters such as the write voltage V_{write}, desired retention time τ_{ret}, desired flat-band voltage shift at the end of retention time V_f, tunnel barrier properties such as width, dielectric constant and barrier height, control dielectric properties such as width and dielectric constant, substrate doping, gate work-function, nanocrystal size distribution and material composition. The effects of some of the parameters are interrelated through non-linear equations and only a numerical result for the FOM can be obtained without simplifying assumptions. Using numerical calculation, the FOM can be calculated for a given device geometry (control and tunnel barrier thicknesses) and nanocrystal size distribution. A greater FOM will mean a faster device writing time, τ_{charge}. A FOM of about 18 is desirable which means a nanosecond write time for 10 year data storage.

3. EXPERIMENTAL DETAILS

3.1. Sample Preparation

The oxide-germanosilicate-oxide trilayer films were grown in a PECVD reactor (model PlasmaLab 8510C) on Si substrates using 180 sccm SiH_4 (2% in N_2), 225 sccm NO_2 and varying flow rates of GeH_4 (2% in He) as precursor gases, at a sample temperature of 350 °C, a process pressure of 1000 mTorr under and an applied RF power of 10 W. The samples were then annealed in N_2 atmosphere in an alumina oven at temperatures ranging from 650 °C to 950 °C for 5 minutes. The samples were loaded and unloaded with ramp times of 1 minute.

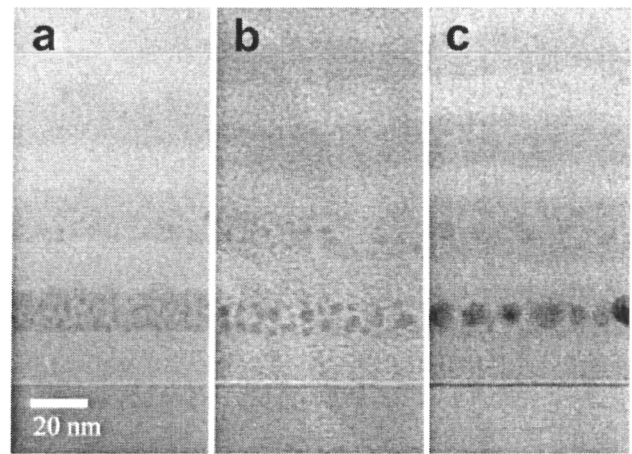

Fig. 3. Formation of Ge NCs as a function of anneal temperature and GeH_4 flow rate as observed by TEM. Multi-layer structures of germanosilicate with flow rates of 120, 110, 100, and 90 sccm are seen away from the substrate (bottom to top) after annealing at (a) 650 °C, (b) 770 °C, and (c) 850 °C for 5 minutes.

Transmission electron microscopy (TEM) images of a multilayered test sample show the formation of NCs as a function of annealing temperature as seen in Figure 3. The layers contain increasing amounts of Ge in layers away from the silicon substrate. High density NC formation is observed only in the bottom-most layer which has a composition of $Si_{0.6}Ge_{0.4}O_2$ as determined by XPS analysis. The NC diameter increases nonlinearly from 2.5 nm to 7.4 nm as the annealing temperature is increased from 650 °C to 850 °C as tabulated in Table I. For fabrication of the devices, first a thermal tunnel oxide of thickness 4 nm was grown using dry oxidation, followed by PECVD growth of germanosilicate layer of 10 nm thickness and composition of $Si_{0.6}Ge_{0.4}O_2$ were grown on n-type silicon substrates with resistivity of 1–10 Ω cm. This germanium rich layer is where NCs form upon annealing. On top, a $t_{con} = 17$ nm control oxide was deposited. Backside ohmic metallization was done by AuSb evaporation for the n-type substrates followed by rapid thermal annealing in forming gas. Gate metallization was done by shadow evaporation of aluminium.

3.2. Flat-Band Voltage Measurement

Capacitance measurements were performed using a capacitance meter (HP 4278A) using 1 MHz AC excitation with 25 mV amplitude. The flat-band voltage shift can be tracked quasi-real-time for small changes in the flat-band shift by using a digital feedback loop that we developed. The feedback loop operates by measuring the capacitance and using successive approximation to find the value of the

Table I. Average nanocrystal size and width of size distribution for different annealing temperatures as observed by TEM. Equation (7) is used to estimate peak ground state energy and width of density of states distribution for the nanocrystal ensemble.

Annealing temperature (°C)	Diameter (nm) average size	2σ (nm) size width	E_p (eV) peak energy	$2\sigma_E$ (eV) energy width	N_{nc} (cm^{-2}) areal density	ΔV_{max} volts
650	2.5	0.6	0.88	0.55	8×10^{12}	16.9
770	3.2	1.0	0.64	0.53	3.2×10^{12}	6.3
850	7.4	1.6	0.17	0.17	8×10^{11}	1.7

gate bias required to observe a given set-point capacitance value and eliminates the need of tracing the whole CV curve and post-processing of the data to access the value of the flat-band voltage shift. During write/erase pulses, the loop can be momentarily turned off, and after the pulse it can be restarted at the same bias voltage. This method allows rapid monitoring of the changes in the flat-band voltage shift (within few tens of msec) after a write or erase pulse. The flat-band voltage difference can be measured rapidly and can be used to extract the discharge or charge currents.

3.3. Charging of Nanocrystals

Dynamic CV measurements have been performed on NC-MOS capacitors, by measuring the CV as a function of time near the flat-band voltage between applied pulses of varying pulse voltage and a fixed pulse duration 50 msec.

As can be seen in Figure 4, the total accumulated charge measured through flat-band voltage shift follows the nanocrystal density, which is proportional to $1/d_{nc}^3$.

The charging currents are extracted from flat-band voltage shift measurements, by applying a 12 V write pulse to previously uncharged three devices with properties shown in Table I. The experimental values of J_c are 8.68 nA, 4.76 nA, and 0.73 nA per cm^2 for devices with NC densities of 8×10^{12}, 3.2×10^{12}, and 8×10^{11} cm^{-2} respectively. The current density calculated using Eq. (2) is 21 nA cm^{-2} using oxide properties found in literature.[9,12] Remarkable proportionality of charge current density to NC density shows that capture cross section p_c is rather independent of NC size for our NCs and has a value of about 5×10^{-14} cm^2.

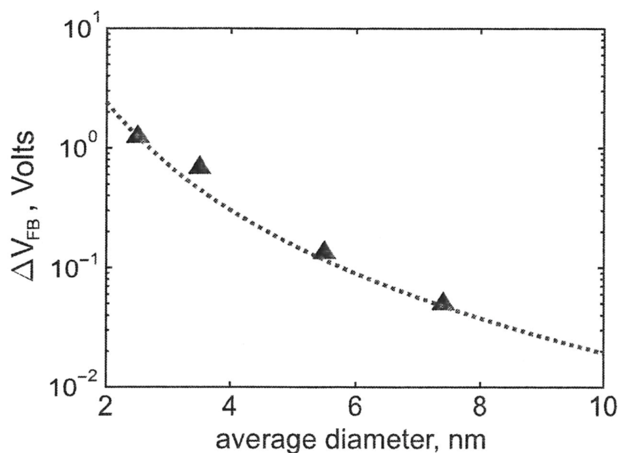

Fig. 4. Flat-band voltage shift as a function of nanocrystal diameter (filled triangles) and for the as deposited sample (horizontal dotted line) after a 7 V write pulse of duration 500 msec. The dotted curve is drawn to aid the eye.

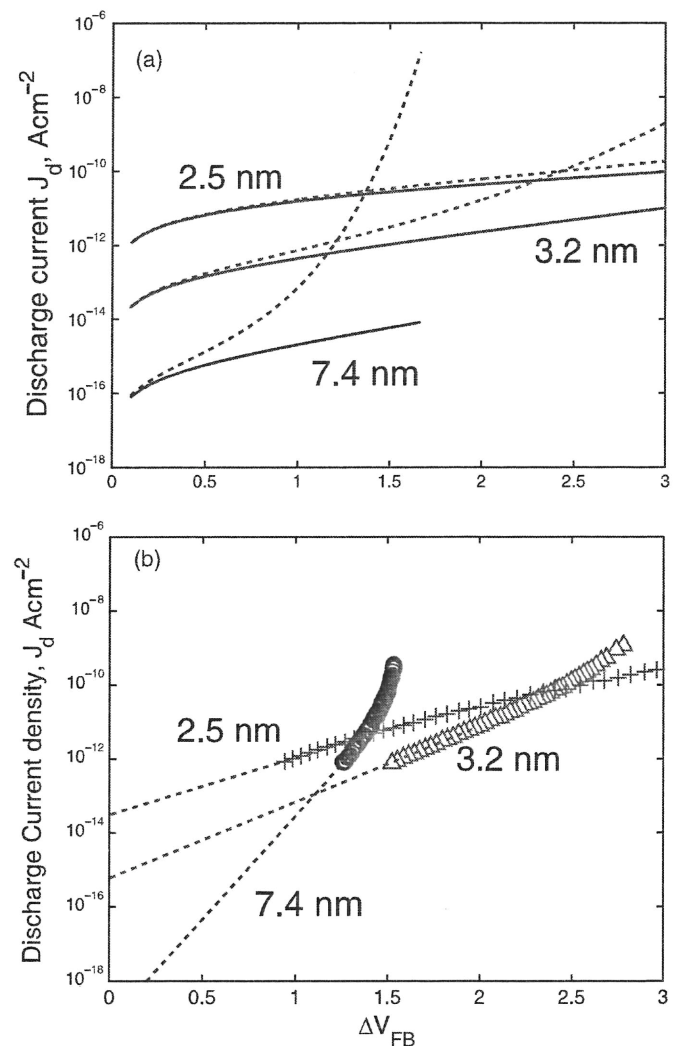

Fig. 5. (a) Discharge currents as a function of flat-band voltage shift calculated for NC-MOS devices under zero gate bias. A tunnel oxide thickness of 4 nm and total oxide thickness of 31 nm is assumed. Bulk barrier height of oxide-silicon interface is taken as 3.3 eV. Nanocrystal parameters are based on experimental values given in Table I. Solid curves are the currents for the rectangular DOS approximation given in Eq. (10) and dashed curves are numerical results assuming Gaussian DOS. (b) Experimental discharge current densities at zero gate bias plotted as a function of flat-band voltage shift for 2.5, 3.2, and 7.4 nm nanocrystals. Dashed lines are linear interpolations drawn to aid the eye.

3.4. Discharging of Nanocrystals

The discharge currents have been measured through decay of stored charge for the three devices as shown in Figure 5(b).

The discharge current densities are plotted in Figure 5(a). It is seen that Eq. (10) agrees reasonably well with a more accurate numerical calculation for small ratios of $\Delta V_{FB}/\Delta V_{max} < 0.2$. If charging ratio is large, i.e., when $\Delta V_{FB}/\Delta V_{max} \rightarrow 1$, the rectangular DOS approximation breaks down. Still, Eq. (10) can be used to estimate effect of design parameters on the retention performance by careful consideration of the value of $\Delta V_{FB}/\Delta V_{max}$ for the desired memory window. For example, noting the dependence of E_p given in Eq. (7), it can be seen from Eq. (10) that an increasing NC diameter increases the average barrier height and reduces the discharge current. It can also be seen that, increasing NC density but keeping other parameters constant increases ΔV_{max}, which in turn gives a lower quasi-fermi level for carriers in NCs for the same memory window, and reduces the escape current.

The smaller NCs can hold more charge due to increased NC density but they also decay faster. Comparison of Figures 5(a, b) shows that the numerical solution predicts the discharge currents rather accurately. For example, it is seen that, as the flat-band voltage nears 1.7 volts (ΔV_{max} for the 7.4 nm device), there is a sharp increase in the experimental discharge current. This is in accordance with the numerical solution. Also, size dependence of the discharge currents are similar for theory and experiment. Therefore, we conclude that the model describes the behavior of the NC-MOS device and at smaller charging ratios of $\Delta V_{FB}/\Delta V_{max} \ll 1$, Eq. (10) can be used to qualitatively compare devices with different NC properties.

The decay of the charge stored in the NCs has also been recorded for the NC-MOS capacitors with different NC diameters as a function of time. The decay of the flat-band voltage shift is fitted using Eq. (11) as seen in Figure 6. A rapid initial decay followed by a slower decay is in accordance with the predictions of Eqs. (10) and (11). The data can be fitted accurately for short and long time periods by using two adjustable parameters J_{d0} and β.

4. DISCUSSION

The model agrees well with experiment and can be used to estimate effect of various design parameters on device performance. Based on the theoretical model described in the theoretical section, the FOM has been calculated for various device parameters. The dependence of the FOM on the control dielectric thickness to tunnel dielectric thickness is given in Figure 7.

It can be seen that, a decreasing control oxide thickness improves FOM. This can be understood through two mechanism, one being the increase of the charging current at a given write voltage, and the other being reduction of the tunnel dielectric field during retention due to better screening of the NC charge by the gate contact. It is desirable to choose a thin control dielectric with high dielectric constant to enhance these effects and achieve a higher FOM. The FOM has also been calculated for different dielectric materials (material properties from[13]) with same effective oxide thickness, keeping other device parameters the same, as shown in Figure 8.

It is seen that, higher dielectric constant materials enhance device performance. This effect can be understood by the fact that, the actual dielectric thickness is greater for higher dielectric constant, reducing the escape tunnelling

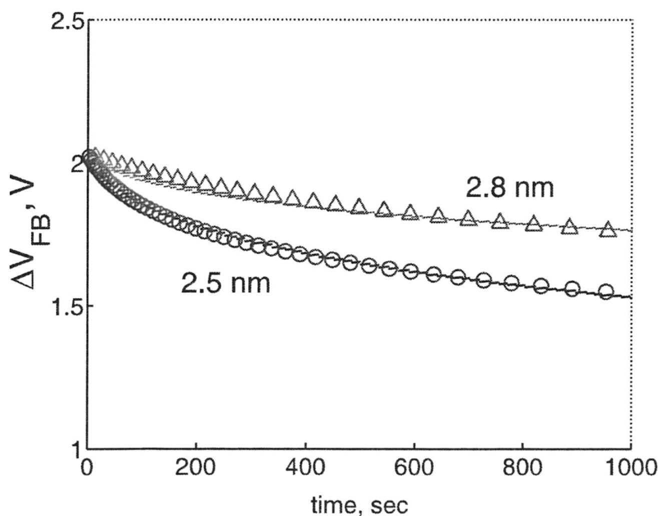

Fig. 6. Experimental flat-band shift as a function of time for two capacitors with different average nanocrystal diameters. Smaller NCs with an average diameter of 2.5 nm (triangles) decay faster than those with an average diameter of 2.8 nm (circles). Data is fitted using Eq. (11).

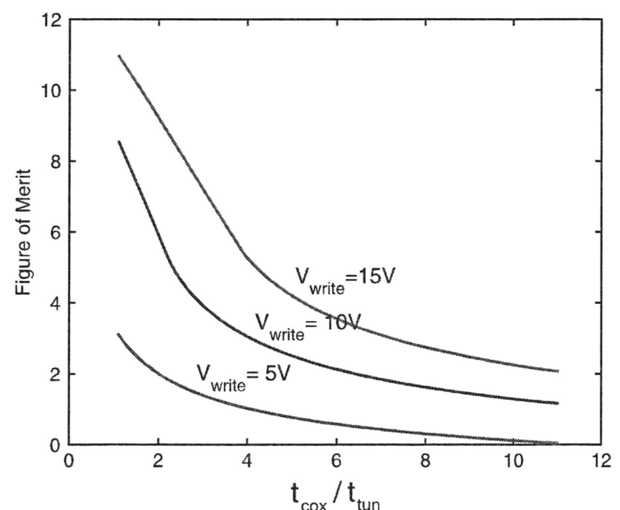

Fig. 7. Figure of Merit (FOM) for a device with 6 nm diameter Ge nanocrystals and 3 nm thick SiO_2 tunnel dielectric, plotted for $V_{write} = 5$, 10, and 15 Volts as a function of control oxide thickness (t_{cox}) to tunnel oxide thickness (t_{tun}). Memory window is 0.5 Volts. Decreasing control oxide thickness enhances the FOM by enhancement of write current.

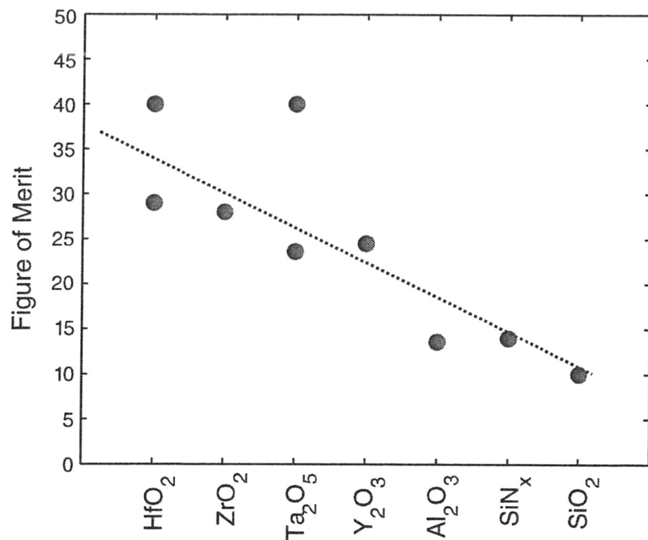

Fig. 8. Figure of merit for different control and tunnel dielectric materials for nanocrystal diameter of 6 nm, write voltage of 10 V, and effective oxide thickness of 4 nm. Dotted line is drawn to guide the eye.

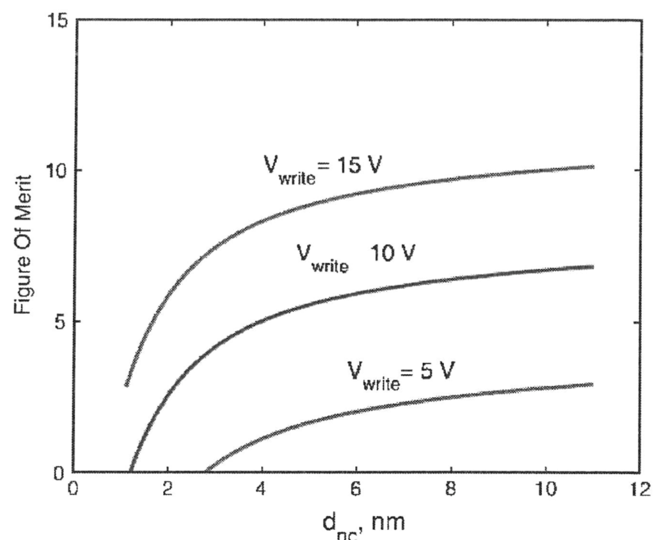

Fig. 10. Figure of merit as a function of nanocrystal diameter, suming a nanocrystal density of $N_{nc} = 10^{12}\text{cm}^{-2}$.

rate. It must be noted that, there is a minimum nanocrystal size for a high-K dielectric, as smaller nanocrystals have a higher quantization energy. Smaller nanocrystals observe smaller barriers and high-K dielectrics generally have smaller conduction band barriers on silicon. The figure of merit is also plotted as a function of substrate doping and gate work-function as seen in Figure 9. It is seen that there is a weak dependence on doping density and work-function of the gate. Numerical calculations were used to calculate the band bending for a given set of parameters.

The figure of merit depends strongly on the nanocrystal properties. Smaller nanocrystals can be made with higher areal density but decay faster due to tighter quantum

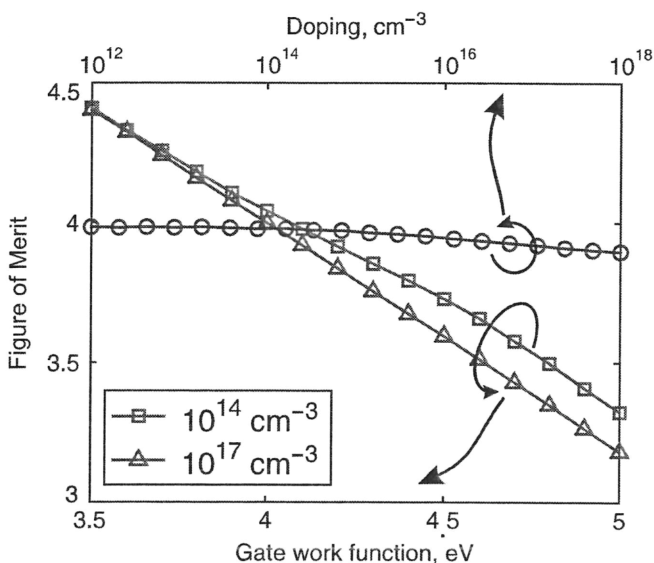

Fig. 9. Figure of merit as a function of gate work-function and substrate doping density for 3 nm diameter nanocrystals, 4 nm tunnel oxide and 20 nm control oxide. Write voltage is 10 V.

confinement. The effect of average nanocrystal diameter is plotted in Figure 10, and it is seen that devices with larger and high density nanocrystals perform better.

5. CONCLUSIONS

In this article, we have proposed a charge storage and retention model for NC-MOS memory devices and compared it with experimental results. The model envisions storage of carriers in quantized energy levels of NCs. The escape of carriers is modelled by direct tunnelling out of the NCs to the substrate. The tunnelling rate depends on the field in the tunnel oxide, which is a function of total number of stored carriers as well as the surface potential of the substrate at a given gate bias. The model can be used to predict the effect of various design parameters such as nanocrystal size and composition, total flat-band voltage shift on write speed and retention time. The model predicts the super-exponential time decay commonly observed in NC-MOS elements. For NC-MOS capacitors containing Ge NCs fabricated by the PECVD technique, NC size related quantum confinement is found to play a role in the storage of charges. The model agrees well with the experimental results, and gives useful insight to NC-MOS memory device design. Theory suggests that high-K dielectric devices with large and dense nanocrystals perform better in terms of retention time and write speed.

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