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Citation: Appl. Phys. Lett. **104**, 013112 (2014);
View online: https://doi.org/10.1063/1.4861590
View Table of Contents: http://aip.scitation.org/toc/apl/104/1
Published by the American Institute of Physics

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(Received 4 November 2013; accepted 18 December 2013; published online 9 January 2014)

A low power zinc-oxide (ZnO) charge trapping memory with embedded silicon (Si) nanoparticles is demonstrated. The charge trapping layer is formed by spin coating 2 nm silicon nanoparticles between Atomic Layer Deposited ZnO steps. The threshold voltage shift (ΔV_t) vs. programming voltage is studied with and without the silicon nanoparticles. Applying −1 V for 5 s at the gate of the memory with nanoparticles results in a ΔV_t of 3.4 V, and the memory window can be up to 8 V with an excellent retention characteristic (>10 yr). Without nanoparticles, at −1 V programming voltage, the ΔV_t is negligible. In order to get ΔV_t of 3.4 V without nanoparticles, programming voltage in excess of 10 V is required. The negative voltage on the gate programs the memory indicating that holes are being trapped in the charge trapping layer. In addition, at 1 V the electric field across the 3.6 nm tunnel oxide is calculated to be 0.36 MV/cm, which is too small for significant tunneling. Moreover, the ΔV_t vs. electric field across the tunnel oxide shows square root dependence at low fields (E < 1 MV/cm) and a square dependence at higher fields (E > 2.7 MV/cm). This indicates that Poole-Frenkel Effect is the main mechanism for holes emission at low fields and Phonon Assisted Tunneling at higher fields. © *2014 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4861590]

Reprogrammable nonvolatile memory represents an essential element in most of the modern electronic devices. While Silicon-Oxide-Nitride-Oxide-Silicon (SONOS)-type memory devices are still holding the largest share of nonvolatile memory devices due to their high data retention, high endurance, and fast program/erase (P/E) speed,[1] a demand for an alternative memory technology is rapidly growing because of the excessive power consumption of SONOS memories, which is mainly caused by the high operating voltage required (typically > 10 V) to inject charge carriers into the charge trapping layer.[2] This is due to the high electric field needed for tunneling.[3] At lower electric fields, emission of charges over a reduced potential barrier is possible via Poole-Frenkel Effect (PFE).[3–5]

Recently, a technology that has been attracting a growing attention is ZnO-based memory devices because they can provide high performance as well as low cost, high environmental stability, and optical transparency.[6–8] In parallel, the charge-trapping layer can be engineered to improve the trapping and retention characteristics of the memory, allowing for lower operating voltages and thinner tunnel oxides. Embedding nanoparticles (NPs) in the charge trapping layer could be one way to achieve this goal.[9,10] In this work, the effect of using 2 nm Si NPs in the charge trapping layer on the performance of a ZnO-based memory device is studied. The physical mechanisms of emission and capture of holes are studied by extracting electric field profiles and plotting the ΔV_t vs. square root and vs. square of electric field across the tunnel oxide and by investigating the energy band diagram of the structure.

Silicon nanoparticles (Si-NPs) are fabricated in a two-stage process. Initially, production of Si-NPs were achieved by focusing a femtosecond pulsed laser of $\lambda = 800$ nm with pulse duration of 200 fs, an average output power of 1.6 W at a pulse repetition rate of 1 kHz on a silicon wafer immersed in deionized water. Next, Si-NPs of predominately 2 nm in size (ranging from 1 to 5.5 nm) were synthesized by performing sonification at 40 KHz for 200 min then filtration of the NPs colloidal using filters with a pore size of 100 nm.[11] A TEM image of the synthesized ultra-small non-agglomerate Si NPs is depicted in Fig. 1.

The channel-last memory cells were fabricated on highly doped (10–18 mΩ cm) p-type (111) Si wafer which is used as a back-gate electrode. First, a 15-nm-thick Al_2O_3 blocking oxide is deposited by Atomic Layer Deposited (ALD) using a Savannah 100 system, followed by a 2-nm-thick ZnO charge trapping layer. Then, Si-NPs were spun on the ZnO at a speed of 700 rpm and an acceleration of 250 rpm/s for 10 s. Again, a 2-nm-thick ZnO charge trapping layer was ALD deposited so that the Si-NPs are embedded within the charge trapping ZnO. This was followed by ALD deposition of a 3.6-nm-thick Al_2O_3 tunneling oxide and an 11-nm-thick ZnO channel at 250 °C. A solution of 98:2 H_2O:H_2SO_4 is used for 2 s to etch the channel after patterning by optical lithography. The source and drain contacts were created by depositing 100 nm Al by thermal evaporation followed by lift off. Using Plasma Enhanced Chemical Vapor Deposition (PECVD), a 360-nm-thick SiO_2 layer is deposited for device isolation. Finally, Rapid Thermal Annealing (RTA) in forming gas (H_2:N_2 5:95) for 10 min at 400 °C was performed on the samples. Fig. 2 shows a

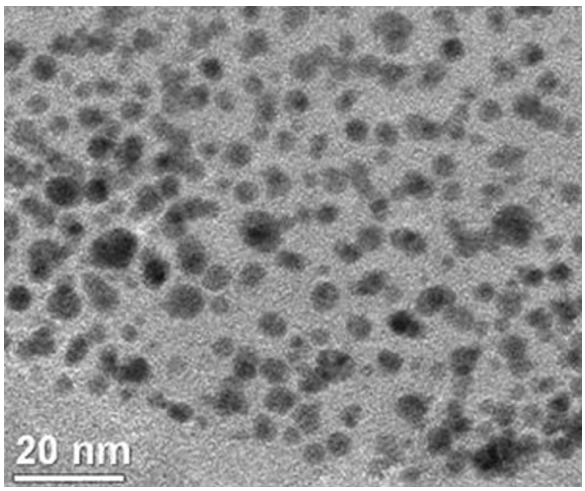

FIG. 1. TEM image of the laser-synthesized ultra-small Si nanoparticles.

cross-section of the final device structure with the Si nanoparticles.

In an attempt to study the effect of the Si-NPs on the performance of the memory device, the memory cells were probed using the Agilent-Signatone probe station. In order to program and erase the memory cell $-10\,V/10\,V$ is applied on the gate for 5 s with the source and drain being grounded. In order to read the state of the cell, the gate voltage is swept from 0 V up to 20 V with a drain voltage V_d of 10 V and the source being grounded. It was found that the memory cells were being programmed by applying a negative gate voltage and erased by applying a positive gate voltage, which suggests that holes are being trapped. The measured $I_{drain} - V_{gate}$ curves of the programmed and erased states of memory devices with and without Si NPs are plotted in Fig. 3 and the ΔV_t is extracted at a drain current of 4×10^{-5} A, which is near the extrapolated turn on of the device. The ΔV_t is increased by an amount of ~3.7 V (from 2.6 V) with the Si NPs. This shows that the Si nanoparticles behave as charge trapping centers with a high trapping density within the bandgap of ZnO.[12] Additionally, the samples were programmed and erased (P/E) at different voltages to see the effect of the programming voltage. As expected, the V_t shift in both cases increases with the program and erase voltages. Also, at a very low program/erase voltage of $-1\,V/1\,V$, the V_t shift can be as high as 3.4 V due to the Si-NPs, which suggests that a mechanism other than tunneling can cause the holes emission from channel to trapping layer. Fig. 4 shows the mean and standard deviation of the measured V_t shifts.

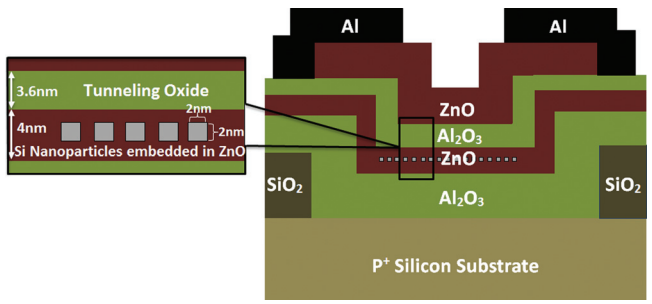

FIG. 2. Schematic cross-section of the fabricated charge trapping memory cell with embedded Si nanoparticles.

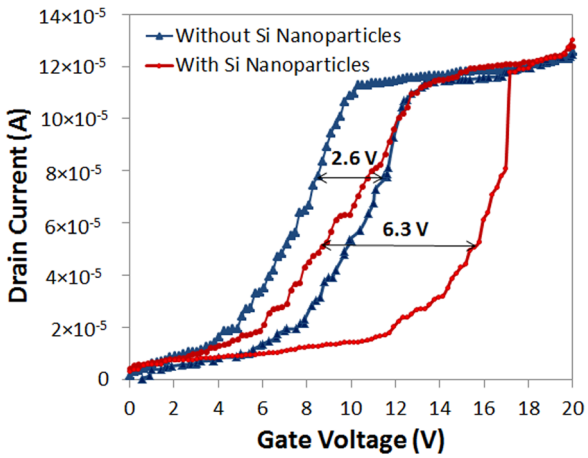

FIG. 3. $I_d - V_g$ showing the obtained V_t shift with and without Si nanoparticles $V_d = 10$ V. The memory is programmed by applying $V_g = -10$ V for 5 s with source and drain being grounded, and erased by applying $V_g = 10$ V for 5 s.

The plot shows that the variation obtained with Si-NPs is larger than without nanoparticles. The reason for this larger deviation could be due to the different number and size of the nanoparticles embedded within each memory cell. In fact, the Si nanoparticles size ranges from 1 to 5.5 nm, which makes it very difficult to obtain a uniform distribution of Si-NPs in all the devices. Additionally, the deposition method of the silicon nanoparticles by spin coating can lead to non-uniform distribution.

In addition, the retention characteristic with and without nanoparticles is studied. Fig. 5 shows the V_t shift versus time after a single programming event at -10 V. The plot shows that the memory with Si NPs loses 36% of its initial charge in one year while that takes only 70 min in devices without NPs; also 41% of the charge of the memory device with NPs is lost in 10 yr while that only takes 100 min for devices without NPs. The plot indicates that the slope of the retention time curve is improved with NPs, which means that the rate of charge loss is reduced due to Si-NPs better confinement. As shown in Fig. 5, the memory with Si-NPs still exhibits a large V_t shift of 3.6 V after 10 yr while the memory without nanoparticles has a retention time which is much less than 10 yr. The good retention characteristic of the memory cell is attributed to the large barrier, good confinement of holes in the Si NPs, and large tunnel oxide thickness which makes

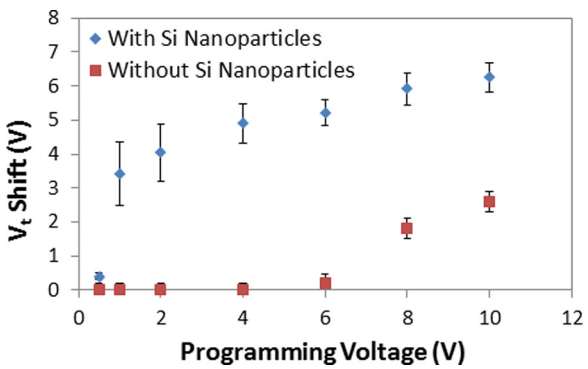

FIG. 4. Threshold voltage shift vs. programming voltage with and without Si nanoparticles.

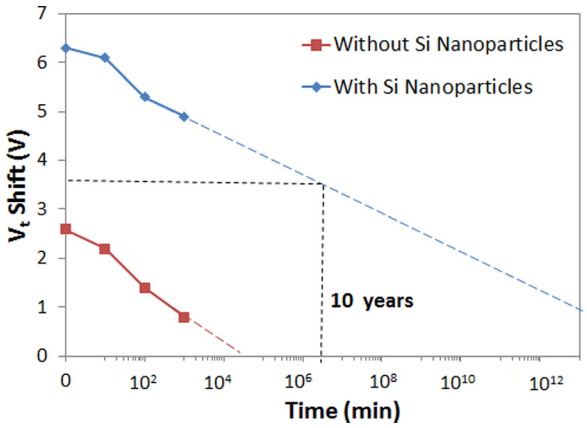

FIG. 5. V_t shift vs. time measured for the memory structures with and without Si nanoparticles.

it difficult for holes to be emitted back without an applied bias or large reverse electric field. Assuming the threshold voltage shift is mainly due to the stored charge in the trapping layer, the charge trap states density can be calculated using the following equation:[13]

$$Q = \frac{C_t \times \Delta Vt}{2 \times q}, \quad (1)$$

where C_t is the capacitance of the charge trapping layer per unit area and q is the elementary charge. At a programming voltage of -10 V and with $C_t = 560\,\mathrm{nF/cm^2}$, the ΔVt is 6.3 V which corresponds to a charge trap states density of $1.1 \times 10^{13}\,\mathrm{cm^{-2}}$ or equivalently $1.67 \times 10^{-6}\,\mathrm{C/cm^{-2}}$, and at a programming voltage of -1 V, the ΔVt is 2.6 V which corresponds to a charge trap states density of $5.95 \times 10^{12}\,\mathrm{cm^{-2}}$ or $9.52 \times 10^{-7}\,\mathrm{C/cm^{-2}}$.

To understand more about the charge transport mechanism, the energy band diagram of the memory cell with Si-NPs is constructed and shown in Fig. 6 using the material properties for ZnO, Al_2O_3,[14–16] and 2 nm Si nanoparticles.[17–20] As a matter of fact, it has been shown that as the Si nanoparticles size shrinks their bandgap increases due to quantum confinement in 0-D,[17] their dielectric constant decreases,[18] their work-function increases,[19] and their electron affinity decreases. Additionally, the charging energy is increased to 1.1 eV for a 2-nm Si NP.[19]

It is shown in Fig. 6 that the conduction band offset between channel and tunnel oxide ($\Delta E_c = 1.92$ eV) is larger than the valence band offset ($\Delta E_v = 1.36$ eV), which makes the holes more prone to overcoming the barrier than electrons. Additionally, because of the small electron affinity of the Si-NPs, the conduction band minimum of the Si-NPs is above that of the adjacent ZnO which may inhibit electrons storage, but the valence band minimum of the Si-NPs is above that of the adjacent ZnO so a quantum well is formed for holes, which supports the observed holes storage in the memory cell.

In order to determine the mechanism of holes emission, ΔV_t versus the square root and vs. the square of the electric field are studied and plotted in Figs. 7 and 8, respectively. The electric field across the tunnel oxide is calculated using Physics Based TCAD simulations.[3,4,21] With 1 V gate voltage; the electric field across the tunnel oxide is 0.36 MV/cm, and with a 10 V gate voltage; the electric field is 3.6 MV/cm. At an electric field of 1 MV/cm; tunneling over a potential barrier of 1.36 eV is negligible.[3,22,23] In fact, when a very small negative gate voltage is applied in order to program it, the holes (charged particles) in the channel gain enough energy and drift towards channel/tunnel oxide interface, but their energy is not enough for tunneling through the 3.6-nm-thick tunnel oxide to the charge trapping layer due to the large barrier ($\Delta E_v = 1.36$ eV). However, at lower electric fields, thermal emission of holes over the barrier is dominant. This barrier can be further reduced by the electric field in square-root dependence via the Poole-Frenkel Effect.[3–5] In 1938, Frenkel explained the increase of the carriers thermal emission rate in an external electric field by the barrier lowering associated with the Coulomb potential of the carriers: as the applied field increases, the barrier height decreases further, and due to this barrier lowering, the thermal emission rate of charges exponentially increases.[22,24,25] This effect has often been assigned to a donor trap, which is neutral when it contains an electron and is positively charged when the electron is absent so that a Coulombic attraction exists. In the ZnO memory described in this Letter, the ZnO

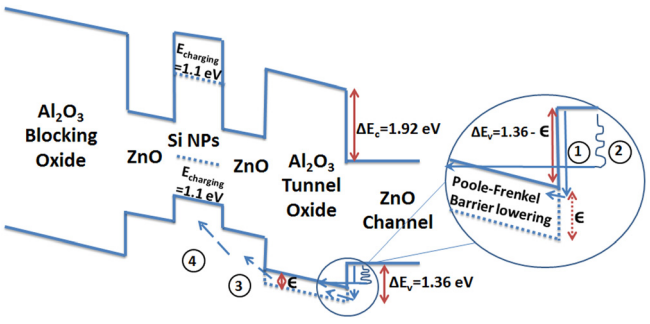

FIG. 6. Energy band diagram of the ZnO memory with Si nanoparticles with applied negative bias. The changes due to quantization and coulomb charging energy of the 2 nm Si nanoparticles are included. (1) The Poole-Frenkel Effect reduces the barrier for holes allowing them to overcome the potential barrier and be emitted to Al_2O_3. (2) Holes are thermally excited and tunnel via PAT. (3) Holes in Al_2O_3 tunnel oxide drift to the ZnO due to the electric field in the oxide. (4) Holes are trapped in the available quantum states in the ZnO bandgap and in the quantum well formed due to valence band offset between the Si nanoparticles and ZnO trapping layers.

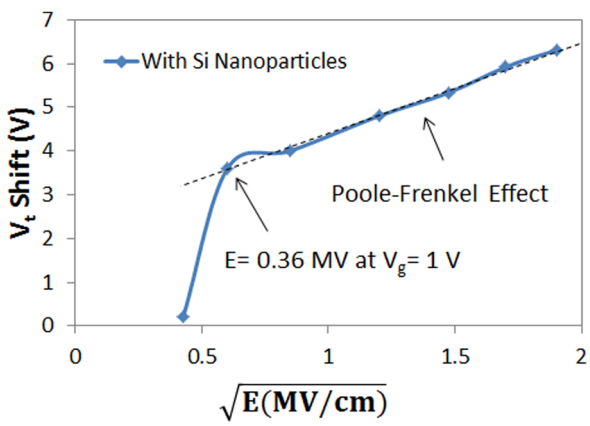

FIG. 7. V_t shift vs. square root of the electric field across the tunnel oxide. Linear trend indicates that Poole-Frenkel Effect is the mechanism for holes emission and capture.

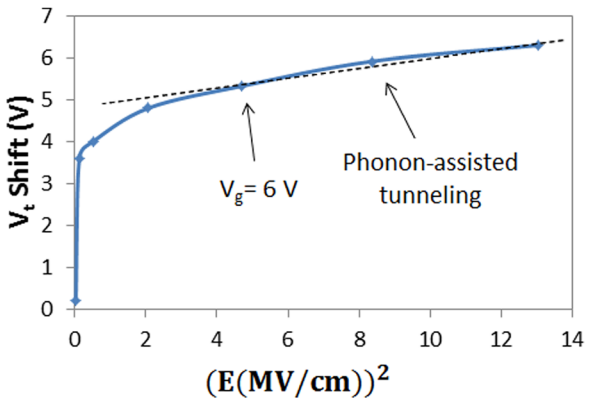

FIG. 8. V_t shift vs. square of the electric field across the tunnel oxide. Linear trend indicates that PAT is the mechanism for holes emission and capture.

channel is n-type due to native crystallographic defects, such as interstitial zinc and oxygen vacancies, which behave as electron donors and the holes are minority carriers.[7] So a Coulombic attraction is present and when an external electric field is applied Poole-Frenkel mechanism is applicable. In fact, Fig. 7 shows a linear dependence of V_t shift on the square root of the electric field. This indicates that Poole-Frenkel Effect is the dominant mechanism of emission of holes from channel to charge trapping layers at low electric fields.[4,5,22] This also explains why large V_t shifts are obtained with low program/erase voltages.

In fact, due to Poole-Frenkel Effect, the smaller barrier height for the holes ($\Delta E_v = 1.36$ eV) is further lowered in the presence of an electric field by an amount ϵ given in Eq. (2)[26]

$$\in = \sqrt{\frac{q^3 E}{\pi \epsilon_0 \epsilon_r}}, \tag{2}$$

where ϵ_r is the dielectric constant of the tunnel oxide, q is the coulomb charge, and E is the electric field across the tunnel oxide. The barrier lowering is calculated at a gate voltage $V_g = 1$, 2, and 10 V to be 0.16 eV, 0.23 eV, and 0.5 eV, respectively. The barrier lowering exponentially increases the amount of holes which will overcome the barrier as depicted in Fig. 6.

Additionally, Fig. 8 shows a linear dependence of V_t shift on the square of the electric field at $E > 2.7$ MV/cm, which indicates that Phonon-Assisted Tunneling (PAT) is the dominant mechanism for hole transmission where holes are thermally excited. This excitation increases the holes tunneling probability through the tunnel oxide as shown in Fig. 6.[3,22] The electric field allows the holes to drift to the ZnO charge trapping layer and some holes will be captured by Si nanoparticles since there is no barrier for the holes as shown in Fig. 6. Once there, they are confined within the nanoparticles or within the available energy states in the quantum well formed by the valence band offset between Si-NPs and adjacent ZnO layers.[12]

In summary, a low power ZnO-based charge trapping memory with Si nanoparticles is fabricated and studied. With 2 nm Si-NPs, the memory cells show a much higher V_t shift and a longer retention time (>10 yr). The results show that Poole-Frenkel Effect is the dominant mechanism for hole emission at low electric fields allowing for low voltage programming. The large V_t shifts obtained with Si nanoparticles at low voltages and the excellent retention highlight a promising technology for future ultra-low power memory devices.

We gratefully acknowledge financial support for this work provided by the Advanced Technology Investment Company (ATIC). This work was supported in part by TUBITAK Grant Nos. 109E044, 112M004, 112E052, and 113M815.

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