

Charge retention in quantized energy levels of nanocrystals

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Abstract

Understanding charging mechanisms and charge retention dynamics of nanocrystal (NC) memory devices is important in optimization of device design. Capacitance spectroscopy on PECVD grown germanium NCs embedded in a silicon oxide matrix was performed. Dynamic measurements of discharge dynamics are carried out. Charge decay is modelled by assuming storage of carriers in the ground states of NCs and that the decay is dominated by direct tunnelling. Discharge rates are calculated using the theoretical model for different NC sizes and densities and are compared with experimental data. Experimental results agree well with the proposed model and suggest that charge is indeed stored in the quantized energy levels of the NCs.

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1. Introduction

The observation of formation of nanocrystals (NCs) by annealing of silicon dioxide films having excess Si or Ge has attracted attention due to optical and electronic properties of such nanostructures [1–4]. In particular, Ge NCs embedded in amorphous silicon oxide (a-SiO) films have been subject of study, because of low temperature of formation, compatibility with standard integrated circuit fabrication processes and for their potential applications in optoelectronic and memory devices. The NCs are candidates as storage media for electron storage cells in flash memory devices [5,6]. Since many parameters of NCs such as density, size and composition can be adjusted by proper choice of fabrication parameters, they offer flexibility in design of NC flash memory cells. However, a better understanding of charge storage mechanism is important in optimization of device performance. Recent studies have proposed a model describing the storage of carriers in NC-

MOS devices assuming storage in deep-traps [7–9] associated with NCs and trap energy level engineering was investigated to improve device performance.

In this paper, we investigate an alternative mechanism for carrier storage by assuming carrier storage in NC energy levels instead of deep traps. Based on this assumption, we present a theoretical model that includes the effect of NC dimensions and density to calculate the discharge dynamics. Germanium NC-MOS capacitors have been fabricated and characterized using capacitance measurements. Results are compared with theory, showing agreement on size and density-related discharge properties.

2. Theoretical modelling

A typical NC memory element cross section is shown in Fig. 1. Based on the assumption that only NCs are responsible for charge storage, the flat-band voltage shift ΔV_{FB} is approximately given by [10]

$$\Delta V_{FB} = \frac{q_{nc}}{\epsilon_{ox}} \left(t_{cox} + \frac{\epsilon_{ox} t_{nc}}{2\epsilon_{Ge}} \right), \quad (1)$$

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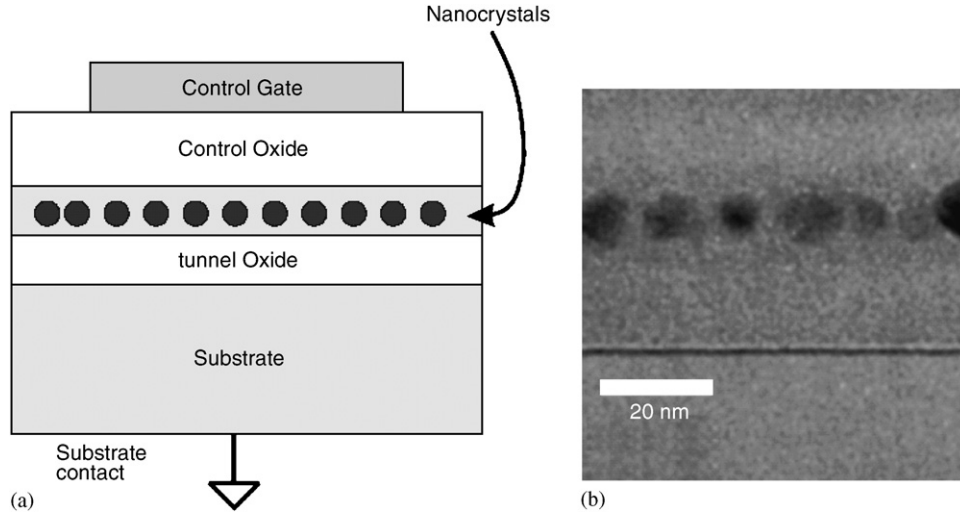


Fig. 1. (a) Schematic cross-section of a NC-MOS capacitor, and (b) example TEM micrograph of a calibration sample showing germanium nanocrystal band with 7.4 nm average diameter NCs.

where q_{nc} is the total stored charge in the NCs, t_{cox} is the control oxide thickness, t_{nc} is thickness of the layer containing the NCs, ϵ 's are the effective dielectric constants of respective materials. An important parameter of the NC-MOS device is the maximum flat-band voltage shift ΔV_{max} . This is the flat-band voltage shift when all available NCs of density N_{nc} carry an electron i.e. $q_{nc} = qN_{nc}$. It is seen that ΔV_{max} depends on device geometry through Eq. (1) and also on NC density. Due to large Coulomb charging energy, average number of electrons per NC can be assumed to be smaller than one.

In order to evaluate retention properties of NC-MOS memory elements, discharging currents must be calculated. Since there are many device parameters that collectively determine the charge–discharge currents, a simple closed-form formula cannot be obtained that covers all cases. Therefore, retention and erase currents are addressed separately.

During retention, the device is in depletion and $V_{gate} = 0$. If NC bound states are responsible for storage of carriers, discharge occurs by tunnelling from the NC ground state to the substrate, either by direct or trap-assisted tunnelling. For the calculation of the discharge current, the barrier height of tunnelling carriers must be calculated. The barrier height is a function of the NC ground state energy given by $V_B(E) = V_{B0} - E_{nc}$, where V_{B0} is the bulk barrier height and E_{nc} is the energy of electron stored in the NC. The energy levels of uncapped germanium NCs have recently been measured directly as a function of size, using scanning tunnelling spectroscopy [11]. The conduction band minimum of Ge NCs as a function of size is given by

$$E_{CBM}(d_{nc}) = E_{CBM}(\infty) + \frac{11.86}{d_{nc}^2 + 1.51d_{nc} + 3.394}, \quad (2)$$

where the energies are in eV, d_{nc} is the NC diameter in nm and $E_{CBM}(\infty)$ is the conduction band minimum for bulk

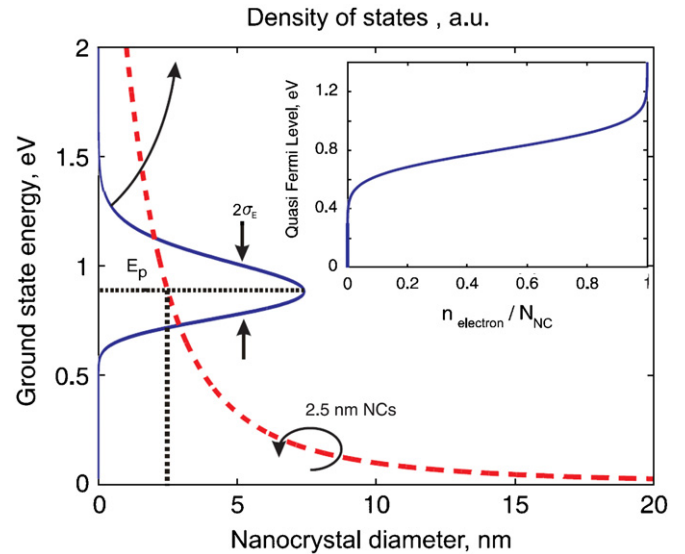


Fig. 2. Schematic description of density of states (solid curve) for the ground states of NCs with average diameter of 2.5 nm. Dotted curve shows electron ground state of NCs as a function of size as described by Eq. (2). Inset shows the quasi-Fermi level as a function of number of electrons per NC.

germanium. If we assume a Gaussian size distribution for the NCs, the density of states, $D_{nc}(E)$, can then be calculated through Eq. (2) for electrons as plotted in Fig. 2.

Assuming thermal equilibrium within the NC layer, the quasi-Fermi level can be calculated implicitly (inset of Fig. 2) for a given total stored charge. Escape of carriers near or above the quasi-Fermi level dominates the discharge current. As a result of reduced barrier height at the quasi-Fermi level for a large number of carriers per NC, discharge current increases with the number of stored carriers (or the flat-band voltage shift). This reduction in barrier height, along with the increase in the tunnel oxide field, results in the super-exponential charge decay

commonly observed in NC-MOS memory elements [12]. By super-exponential we mean the exponentially increased discharge current at the initial stage of decay due to non-linear nature of discharge current on the total stored charge.

The current density describing the discharge of the NCs can be calculated assuming direct tunnelling. For carriers stored in NCs with density $n(E)$ all at an energy E , the discharge current density J_d can be given as

$$J_d = qT_t(E, F_{\text{tox}})v_{\text{nc}}n(E), \quad (3)$$

where $v_{\text{nc}} \approx \hbar\pi/2m_{\text{Ge}}d_{\text{nc}}^2$ is the semi-classical escape attempt rate for NCs of diameter d_{nc} [13]. Here $T_t(E, F_{\text{tox}})$ is the barrier transparency, for electrons with energy E and tunnel oxide field F_{tox} . The actual discharge current must be obtained by integration of Eq. (3) multiplied by the density of states (DOS). The resulting current will be dominated by tunnelling of carriers near the quasi-Fermi level. The transmission probability $T_t(E, F_{\text{tox}})$ can be calculated through the WKB approximation as [14–16]

$$T_t(E) \approx \exp\left[-\left(1 - \left(1 - \frac{F_{\text{tox}}t_{\text{tox}}}{V_B(E)}\right)^{3/2}\right) \frac{BV_B(E)^{3/2}}{F_{\text{tox}}}\right], \quad (4)$$

where $B = 4\sqrt{2m_{\text{ox}}q}/3\hbar$, m_{ox} being the electron tunnelling mass. The tunnel oxide field F_{tox} is determined by the amount of stored carriers as well as by the band bending. If band-bending and gate-substrate work function difference is ignored, the tunnel oxide field is approximately proportional to the flat-band shift (or the total stored charge). Tunnel oxide field is then given roughly by $F_{\text{tox}} \approx \Delta V_{\text{FB}}/2t_{\text{ox}}$, where t_{ox} is the total dielectric thickness. The factor 1/2 is approximate for our device parameters. Exact value of F_{tox} depends on device geometry and properties as well as band bending. During the erase cycle, V_{gate} is negative and the device is in inversion. The discharge current is determined by Eqs. (3) and (4). However, the oxide field is determined by the applied gate voltage and flat-band voltage shift and is given approximately by $F_{\text{tox}} \approx (-V_{\text{gate}} + \Delta V_{\text{FB}}/2)/t_{\text{ox}}$. A more accurate description of F_{tox} as a function of gate bias can be obtained in a numerical calculation by taking into account the band bending of the substrate. Using the discharge currents given in Eq. (3) and a standard band-bending model [17], the charge and discharge currents can be calculated numerically.

3. Experimental

The oxide–germanosilicate–oxide trilayer films were grown in a PECVD reactor (model PlasmaLab 8510C) on Si substrates using 180 sccm SiH_4 (2% in N_2), 225 sccm NO_2 and varying flow rates of GeH_4 (2% in He) as precursor gases, at a sample temperature of 350 °C, a process pressure of 1000 mTorr, under an applied RF power of 10 W. The samples were then annealed in N_2

atmosphere in an alumina oven at temperatures ranging from 650 to 950 °C for 5 min. The samples were loaded and unloaded with ramp times of 1 min. For fabrication of the devices, first a thermal tunnel oxide of thickness 4 nm was grown using dry oxidation on n-type silicon substrates with resistivity of 1–10 Ωcm , followed by PECVD growth of germanosilicate layer of 10 nm thickness and composition of $\text{Si}_{0.6}\text{Ge}_{0.4}\text{O}_2$ as determined by XPS analysis. On top, a $t_{\text{cos}} = 27$ nm control oxide was deposited. After annealing, backside ohmic metallization and gate metallization was done by metal evaporation.

Transmission electron microscopy (TEM) was used to characterize the formation of NCs as a function of annealing temperature. High-density NC formation is observed for layers with a composition of $\text{Si}_{0.6}\text{Ge}_{0.4}\text{O}_2$. The NC diameter increases nonlinearly from 2.5 to 7.4 nm as the annealing temperature is increased from 650 to 850 °C as tabulated in Table 1 for four devices. The average quantized energy, energy distribution width and maximum flat-band voltage shifts are calculated using Eqs. (1) and (2) and are given in Table 2 for the devices described in Table 1. The volume of the NC layer was calculated for a unit surface area using the thickness of the layer containing NCs (10 nm) and volumetric density of the NCs inferred from TEM micrographs was used to calculate the effective areal density. The effective dielectric constant of the NC layer is assumed to be $\epsilon_{\text{ge,eff}} = 9$ (mean of oxide and bulk germanium dielectric constants), the thickness of the NC layer is assumed to be 10 nm, and the dielectric constant of SiO_2 is assumed to be $\epsilon_{\text{ox}} = 3.8$.

Capacitance measurements were performed using a capacitance meter (HP 4278A) with 1 MHz AC excitation of 25 mV amplitude. The flat-band voltage shift can be tracked quasi-real time for small changes in the flat-band shift by using a digital feedback loop that eliminates the

Table 1

Average NC size and width of size distribution for different annealing temperatures as observed by TEM

Anneal temperature (°C)	Average diameter (nm)	Size distribution width (nm)	Nanocrystal density (cm^{-2})
650	2.5	0.6	8×10^{12}
700	2.8	0.7	5.3×10^{12}
770	3.2	1.0	3.2×10^{12}
850	7.4	1.6	8×10^{11}

Table 2

Calculated properties of NCs based on size distribution data

Anneal temperature (°C)	E_p (eV)	σ_E (eV)	ΔV_{max} (V)
650	0.88	0.55	11.9
700	0.78	0.52	7.9
770	0.64	0.53	4.5
850	0.17	0.17	1.2

need of tracing the whole $C-V$ curve to estimate the value of the flat-band voltage shift. During write/erase pulses or zero bias wait cycles, the loop can be momentarily turned off. This method allows rapid monitoring of the changes in the flat-band voltage shift (within few tens of ms) after a write or erase pulse or during retention under a fixed gate bias.

4. Results and discussion

Dynamic $C-V$ measurements have been performed on NC-MOS capacitors, by measuring the $C-V$ as a function of time near the flat-band voltage between applied pulses of varying voltage and durations. Cumulative charge deposition has been measured for three capacitors annealed at different temperatures as shown in Fig. 3 by applying pulses of 50 ms duration and by sweeping the pulse voltage. The discharge currents have been measured through free time decay of flat-band voltage shift under zero bias for three devices as shown in Fig. 4, after the capacitors were charged to a certain voltage by applying a long pulse (few tens of seconds) at a voltage of 15 V. The ΔV_{FB} measured using the feedback setup is used to calculate the stored charge using Eq. (1) and the amount of charge escaped during the interval was divided by the time duration between measurements to calculate the current. The discharge current is seen to increase with increasing flat-band voltage shift (or stored charge). Curves for different NC sizes show a cross-over behavior. This feature is a strong evidence for size-related discharge of the NC-MOS elements. Smaller NCs decay faster than larger NCs at a given charging ratio of $\Delta V_{FB}/\Delta V_{max}$ due to reduction of the tunnel barrier height as they have a higher average quantization energy. However, if the flat-band voltage shift is close to ΔV_{max} or $n_e/N_{NC} \approx 1$, the quasi-Fermi level increases rapidly as shown in the inset of Fig. 2. As ΔV_{max}

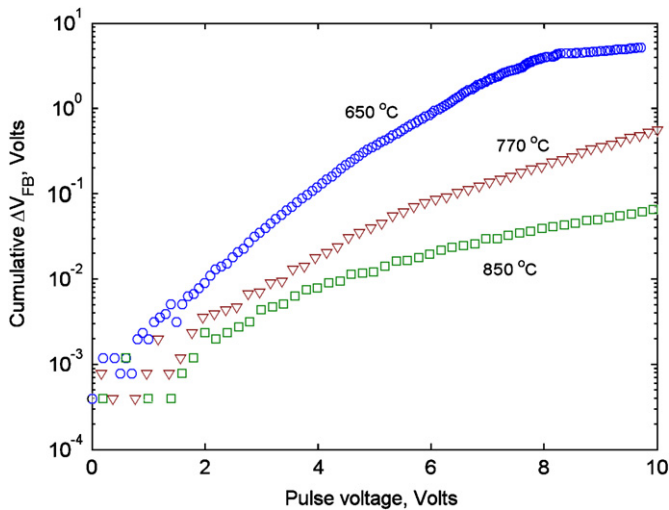


Fig. 3. Cumulative flat-band voltage shift of NC-MOS capacitors measured using the capacitance feedback technique. Smaller NCs with larger effective areal density can be charged to larger voltages in a shorter time.

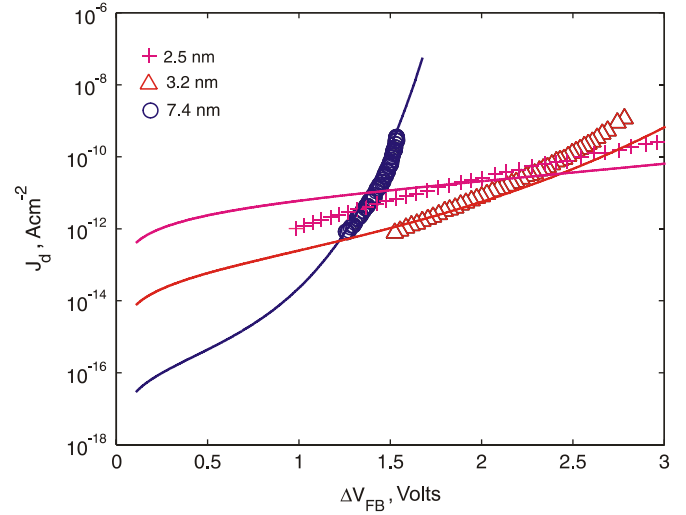


Fig. 4. Theoretical (solid lines) and experimental discharge current densities for three devices with different average NC diameters and NC densities as a function of flat-band voltage shift.

is proportional to the effective areal NC density $N_{NC} \propto 1/d_{nc}^3$, smaller NCs have higher density and ΔV_{max} . The reason for the density being proportional to $1/d_{nc}^3$ instead of $1/d_{nc}^2$ is the way the effective areal density was calculated as explained in the experimental section. At a given ΔV_{FB} , stored charge per NC is larger for lower density (large diameter) NCs. Therefore at a given ΔV_{FB} , large NCs may have a larger quasi-Fermi energy than smaller NCs although the average quantization energy is lower. Since carriers near the quasi-Fermi level dominate the discharge, the discharge current increases rapidly when $\Delta V_{FB} \rightarrow \Delta V_{max}$ as is clearly seen in the data for the device with 7.4 nm diameter NCs, for which $\Delta V_{max} = 1.2$ V. This is roughly in accordance with the numerical solution shown in solid curves of Fig. 4. The cross-over behavior shows that NC size and density as well as total stored charge play an important role in determination of the charge decay rate. Charging above the calculated $\Delta V_{max} = 1.2$ V is possibly related to multiple electron charging of the NCs which are not included in the model, or due to uncertainty in the thicknesses of the layers and actual values of the dielectric constants which were used in the calculation of ΔV_{max} .

NC discharge currents have been measured as a function of erase pulse voltage. After NC-MOS devices with NC diameters of 2.5 and 2.8 nm have been charged by 5 V write pulses to a flat-band voltage shift of 1.6 V, erase pulses of duration $\tau_e = 1$ s have been applied and flat-band voltage shift has been recorded. The discharge currents are shown in Fig. 5. The increased currents for smaller NCs quantitatively confirm the prediction of numerical calculation. The data of Fig. 5 suggest that the discharge is indeed dominated by direct tunnelling.

The decay of the charge stored in the NCs has also been recorded under zero bias for the NC-MOS capacitors with different NC diameters as a function of time. The decay of

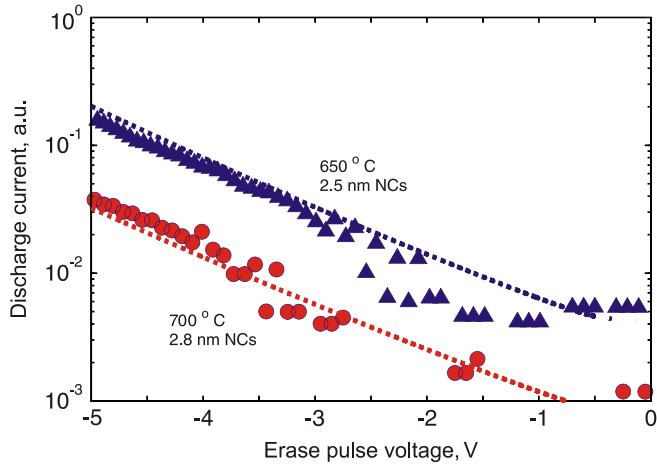


Fig. 5. Normalized discharge currents for 2.5 nm (triangles) and 2.8 nm (circles) diameter NC-MOS devices. Smaller NCs can be erased faster due to reduced tunnel barrier. Dotted lines are numerical simulations obtained by only changing the NC size after fitting the barrier height and width for one of the curves.

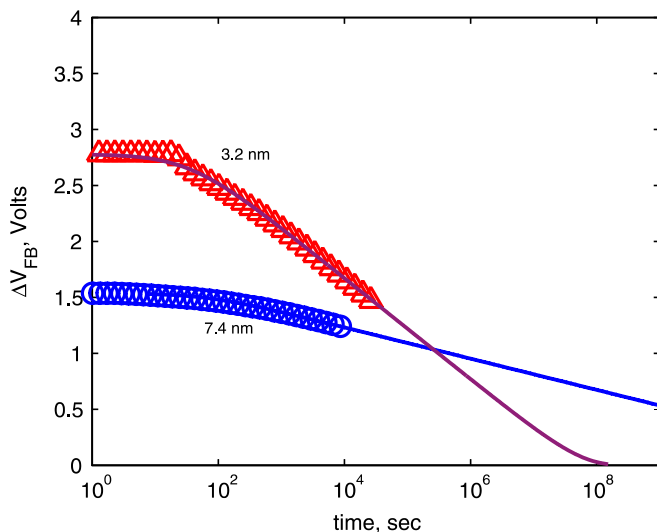


Fig. 6. Smaller NCs with an average diameter of 3.2 nm (triangles) decay faster than those with an average diameter of 7.4 nm (circles). Solid lines are numerically calculated curves based on the presented model.

the flat-band voltage shift is fitted using numerically calculated discharge currents and numerical integration of the decay of stored charge as shown in Fig. 6. The model predicts the decay of charge for both short and longer time scales. It is seen in the time domain also that smaller NCs decay faster than larger NCs. The data shown in Fig. 6 were fitted with slightly different parameters than for Fig. 4, to obtain a better fit for the two curves.

5. Conclusions

In conclusion, we have proposed a charge storage and retention model for NC-MOS memory devices and

compared it with experimental results. The model envisions storage of carriers in quantized energy levels of NCs. The escape of carriers is modelled by direct tunnelling out of the NCs to the substrate. The model can be used to predict the effect of various design parameters such as NC size and density on retention time. The model also correctly predicts the super-exponential charge decay commonly observed in NC memory devices. For NC-MOS capacitors containing Ge NCs fabricated by the PECVD technique, NC size-related quantum confinement is found to play a role in the retention of charges. This is an alternative model to surface trap related carrier storage. Although there are multiple fitting parameters in the model, it predicts essential features of the experimental results such as crossing-over of discharge current densities and time dependence of stored charge during decay. The model therefore gives useful insight to NC-MOS memory device design.

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References

- [1] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbe, K. Chan, *Appl. Phys. Lett.* 68 (1996) 1377.
- [2] X.X. Wang, J.G. Zhang, L. Ding, B.W. Cheng, W.K. Ge, J.Z. Yu, Q.M. Wang, *Phys. Rev. B* 72 (2005) 195313.
- [3] S. Okamoto, Y. Kanemitsu, *Phys. Rev. B* 54 (1996) 16421.
- [4] J. Xu, Z.H. He, K. Chen, X. Huang, D. Feng, *J. Phys. Cond. Mat.* 11 (1999) 1631.
- [5] C. Miesner, T. Asperger, K. Brunner, G. Abstreiter, *Appl. Phys. Lett.* 77 (2000) 2704.
- [6] Z. Yu, M. Aceves, J. Carrillo, F. Flores, *Nanotechnology* 14 (2003) 959.
- [7] M. She, T. King, *IEEE Trans. Elec. Dev.* 87 (2003) 1934.
- [8] W.K. Choi, V. Ng, S.P. Ng, H.H. Thio, Z.X. Shen, W.S. Li, *J. Appl. Phys.* 86 (1999) 1398.
- [9] B.H. Koh, E.W.H. Kan, W.K. Chi, W.K. Choi, D.A. Antoniadis, E.A. Fitzgerald, *J. Appl. Phys.* 97 (2005) 124305.
- [10] T.Z. Lu, M. Alexe, R. Scholz, V. Talelaev, M. Zacharias, *Appl. Phys. Lett.* 87 (2005) 202110.
- [11] Y. Nakamura, K. Watanabe, Y. Fukuzawa, M. Ichikawa, *Appl. Phys. Lett.* 87 (2005) 133119.
- [12] P.F. Lee, X.B. Lu, J.Y. Dai, H.L.W. Chan, E. Jelenkovic, K.Y. Tong, *Nanotechnology* 17 (2006) 1202.
- [13] A. Nauen, I. Hapke-Wurst, F. Hohls, U. Zeitler, R.J. Haug, K. Pierz, *Phys. Rev. B* 66 (2002) 161303(R).
- [14] M. Lenzlinger, E.H. Snow, *J. Appl. Phys.* 40 (1969) 278.
- [15] M. Depas, B. Vermeire, P.W. Mertens, R.L. Van Meirhaeghe, *Sol. Stat. Elect.* 38 (1995) 1465.
- [16] A. Gehring, S. Selberherr, *IEEE Trans. Dev. Mat. Rel.* 4 (3) (2004) 306.
- [17] E.H. Nicollian, J.R. Brews, *MOS Physics and Technology*, Wiley, New York, 1981.