A KU-BAND PHEMT MMIC HIGH POWER AMPLIFIER DESIGN

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND

ELECTRONICS ENGINEERING

AND THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Ahmet DEĞİRMENCİ

July, 2014

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah ATALAR (Advisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. Vakur Behçet ERTÜRK

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assist. Prof. Dr. Aykutlu DANA

Approved for the Graduate School of Engineering and Science:

Prof. Dr. Levent Onural
Director of the Graduate School

ABSTRACT

A KU-BAND PHEMT MMIC HIGH POWER AMPLIFIER DESIGN

Ahmet DEĞİRMENCİ
M.S. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Abdullah ATALAR
July, 2014

Power amplifiers are regarded as the one of the most important part of the radar and communication systems. In order to satisfy the system specifications, the power amplifiers must provide high output power and high efficiency at the same time. AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMT) provides significant advantages offering high output power and high gain at RF and microwave frequencies. Considering the electrical performance, cost and the reliability issues, pHEMT monolithic microwave integrated circuit (MMIC) high power amplifiers are one of the best alternatives at Ku-band frequencies (12-18 GHz portion of the electromagnetic spectrum in the microwave range of frequencies).

In this thesis, a three-stage AlGaAs/InGaAs/GaAs pHEMT MMIC high power amplifier is developed which operates between 16-17.5 GHz. Based on 0.25 μm gate-length pHEMT process, the MMIC is fabricated on 4-mil thick wafer with the size of 5.5 x 5.7 mm^2. Under 8V drain voltage operation, 26.5-24 dB small signal gain, 10-W (40 dBm) continuous-wave mode output power at 3 dB compression with %25-30 drain efficiency is achieved when the base temperature is 85°C.

Keywords: MMIC, power amplifier, GaAs-based PHEMT, 0.25μm, Ku-Band.

ÖZET

PHEMT TEKNOLOJİSİ KULLANARAK YÜKSEK GÜÇLÜ MMIC YÜKSELTEÇ TASARIMI

Ahmet DEĞİRMENCİ
Elektrik ve Elektronik Mühendisliği, Yüksek Lisans
Tez Yöneticisi: Prof. Dr. Abdullah ATALAR
Temmuz, 2014

Güç yükselteçleri, radar ve haberleşme sistemlerinin en önemli parçalarından biri olarak gösterilmektedir. Sistem gereksinimlerini sağlamak adına, güç yükselteçleri yüksek güç ve kazancı aynı anda sağlamalıdır. RF ve mikrodalga frekanslarında, AlGaAs/InGaAs/GaAs tabanlı sahte biçimli yüksek elektron mobiliteli transistorler yüksek güç ve kazancı aynı anda sağlayarak önemli avantajlar sunmaktadır. Elektriksel performans, maliyet ve güvenilirlik açısından bakıldığında, pHEMT MMIC yüksek güç yükselteçleri Ku bant frekansları için en iyi alternatiflerden birisi olarak görülmektedir.

Bu tezde, 3-katlı AlGaAs/InGaAs/GaAs tabanlı, 16-17.5 GHz bandında çalışan bir pHEMT MMIC yüksek güç yükselteci geliştirilmiştir. MMIC 4 mil kalınlığında bir wafer üzerine 0.25 mikron kapı uzunluğuna sahip bir pHEMT prosesi kullanılarak 5.5x5.7 mm^2 büyüklüğünde ürettirilmiştir. 8V drain gerilimінde, 85°C taban sıcaklığında, 26-24.5 dB küçük sinyal kazancı ile 3 dB doyum noktasında sürekli çalışma modunda 10-W (40 dBm) çıkış gücü, %25-30 drain verimliliği ile birlikte elde edilmiştir.

Anahtar sözcükler: MMIC, güç yükselteç, GaAs tabanlı PHEMT, 0.25μm, Ku-Bant.

Acknowledgement

I would like to thank my supervisor Prof. Dr. Abdullah ATALAR for his valuable guidance and support throughout this thesis study and my graduate education. I am also thankful to Assoc. Prof. Dr. Vakur Behçet ERTÜRK and Assist. Prof. Dr. Aykutlu DANA for taking part in my thesis committee.

I would also like to express my gratitude to Ahmet AKTUĞ for his great support and valuable advices on my MMIC design. I learned a lot from his experience in this area. I am grateful to Şebnem SAYGINER for her encouragement during this study and giving me chance to work in this area.

I am thankful to Turkish Scientific and Technological Research Council (TÜBİTAK) for the financial support during my graduate education.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 General Introduction

Power amplifiers (PAs) can be defined as the circuits that convert DC input power into a significant RF/microwave output power. Since signal amplification is one of the most important concepts in RF and microwave systems such as transmitter/receiver (T/R) modules, power amplifiers are regarded as the vital components of these systems. In recent times, RF/microwave applications have gained considerable diversity that forces the technology used in the design of power amplifiers progress in order to satisfy the challenging requirements of these applications. In addition to the challenging performance requirements, component size, cost and reliability issues are also carefully considered due to the high volume productions. Monolithic Microwave Integrated Circuit (MMIC) technology plays an important role in such applications since MMICs offer lower cost, more compact size, higher performance and reliability. Due to all these advantages, MMIC amplifiers have become one of the most vital parts of the military and commercial applications.

Over the past twenty years, many technologies have been introduced such as MESFETs, HBTs and HEMTs which are suitable to fabricate MMIC amplifiers. Although each technology has its own benefits, AlGaAs/InGaAs/GaAs based pseudomorphic high electron mobility transistor (PHEMT) technology is one of the best candidates to provide high power level with high gain due to its superior properties at RF/microwave frequencies.

1.2 HEMT Technology

At the beginning of 1970s, silicon bipolar transistors and GaAs MESFETs were introduced. While most of silicon bipolar transistor amplifiers were designed for below C-band frequencies, GaAs MESFETs were used in the amplifiers whose operation band were above L-band frequencies [1]. Then, at late 1980s and 1990s, new solid state devices have been introduced including HEMT, pHEMT, HFET and HBT using new materials such as InP, SiC and GaN offering amplification at frequencies up to 100 GHz or more [2]. Each device technology has its own advantages but HBT and HEMT devices differ from other technologies due to their superior performance at RF/microwave frequencies. For instance, HEMTs have the highest operation frequency, lowest noise figure and high output power (high breakdown voltage) and power added efficiency (PAE) capability [1]. HBT is another popular device technology especially for low-cost power applications. They offer better linearity and lower phase noise than HEMTs [1]. However, due to the fact that HEMT devices have excellent millimeter-wave power performance at high frequency operation, it can be said that the invention of GaAs HEMTs in 1979 was one of the cornerstones in the electronics world [3].

After the invention of GaAs HEMTs and pseudomorphic HEMTs (pHEMT), GaAs MESFETs have started to lose its role in the applications that require low noise figure, high gain and high power at millimeter wave frequencies. Despite the fact that MESFETs and HEMTs have very similar working principles, the major difference is their epitaxial layer structures. Both MESFET and HEMT device structures are grown on semi-insulating GaAs substrate. However, GaAs HEMT devices have a compositionally different layer (AlGaAs) in order to increase the performance of the device. This additional layer grown on GaAs buffer layer forms heterojunction which offers unique properties for the HEMT device [4].

Due to the energy-band gap difference between AlGaAs and GaAs layers, a band-bending occurs at the heterojunction interface [1]. This band-bending is very critical because it forms a two dimensional electron gas (2DEG) which is close to the interface between GaAs and AlGaAs layers. The 2DEG contains the free electrons that diffuse from AlGaAs layer (higher energy band gap layer) to GaAs layer (lower energy band gap layer). Thanks to the formation of 2DEG, while donor atoms reside in the AlGaAs layer, the electrons stay in GaAs layer where the channel occurs. Due to this separation between donor atoms and free electrons, chance of collision is minimized and the drift velocity of the electrons is also enhanced which offers higher carrier mobility in comparison with the bulk material [1]. Since the conduction channel is well confined at the interface between GaAs-AlGaAs layers and HEMTs show higher saturated velocity, HEMT devices exhibit higher transconductance [4]. High carrier mobility and high saturation velocity are critical features to achieve high currents and high frequency of operation for HEMT devices. Therefore, HEMT devices exhibit very good power performance at millimeter-wave frequency operations.

As the other improvement in HEMT structures, pHEMT devices that have superior RF properties have been developed. In pHEMT devices, a InGaAs layer is additionally grown between undoped AlGaAs spacer and undoped GaAs buffer layer [4]. InGaAs has lower energy band-gap than AlGaAs and GaAs materials. Therefore, unlike HEMT structure, the lowest energy quantum well resides in InGaAs layer and the free electrons are confined to this layer since there are higher energy band levels on both sides [4]. Ability of pHEMTs to operate at high frequencies is attributed to 2DEG electron gas channel formed in heterojunction barrier because InGaAs layer grown between AlGaAs and GaAs layers has different lattice constant [5],[6]. This difference creates larger band-gap discontinuity. Consequently, more charges reside in 2-DEG, thus increasing the transconductance and output power performance [7]. Therefore, pHEMT devices have superior RF/microwave features compared to GaAs HEMTs and MESFETs.

In recent times, AlGaN/GaN HEMTs have become an important option for RF and microwave power amplifiers due to their high power handling capabilities [8],[9],[10],[11]. Due to the superior material properties of Gallium Nitride (GaN), they have higher breakdown voltages, higher thermal conductivity and higher saturated drift velocity which leads to high saturation current densities compared to GaAs [12]. Due to all these properties, GaN HEMTs offer higher power densities, higher efficiency levels and higher output impedance levels which makes the output matching easier, less complex and cost-efficient [13]. All these properties make GaN HEMTs more advantegous than GaAs HEMTs except for the cost. Although GaAs MMICs still lead the MMIC market, it is expected that GaN MMICs will enhance its role in the market for the following years [14]. To sum up, considering the superior RF/microwave properties of HEMT devices, it can be apparently said that HEMT technology dominates the power amplifier applications at RF/microwave frequencies.

1.3 Thesis Outline

In this thesis, design and measurement of a 3-stage, 10-W continuous-wave (CW), 16-17.5 GHz monolithic microwave integrated circuit (MMIC) high power amplifier is presented. Considering output power and gain requirements, we used WIN Semiconductors (Taiwan) 0.25 μm, AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (pHEMT) technology since they can provide sufficient power and gain at Ku-band frequency.

In chapter 2, some of the power amplifier concepts and the techniques used in the design procedure is explained. Chapter 3 consists of the design procedure and the simulation results. Design phase is explained in detail in this chapter. Consequently, measurement results are presented in chapter 4.

Chapter 2

Power Amplifier Fundamentals

Power amplifiers (PAs) are one of most critical components in many modern systems from radar and communication systems to medical imaging systems. Due to the fact that the application area is such diversified, the requirements of applications must also differ in the noise figure, bandwidth, efficiency, linearity, output power and gain performance. Therefore, various PA design techniques have been developed in order to satisfy the requirements of the broadband RF/microwave applications area.

Basically, the performance a power amplifier is determined by a DC quiescent point which is called Q-point, the source and load impedances. Choosing a proper DC quiescent point plays key role in the design of a power amplifier since it directly determines the class of the power amplifier. In addition to the class of operation, the source and load impedances also characterize the response of the amplifier. Consequently, power amplifiers are optimized for the system requirements such as noise figure, efficiency, output power, gain by choosing a proper Q-point, source and load impedances. In this chapter, these key performance parameters and some important concepts are presented.

2.1 Efficiency

Basically, in order to measure how an RF power amplifier performs the energy conversion from DC to RF, the concept of efficiency is introduced. Efficiency is extremely significant for the performance of an RF power amplifier since it also influences other system parameters such as output power. Besides, higher efficiency also enhances the thermal performance of the power amplifier that is also significant especially for mobile applications. For a given output power, higher efficiency implies less supply power usage which directly enhances the operating lifetime of batteries in the mobile applications. From this point of view, efficiency is regarded as one of the key parameters in the power amplifier design. There are more than one efficiency definition such as drain efficiency, power added efficiency (PAE), overall efficiency. In this thesis, drain efficiency definition is used. Drain efficiency defines how much DC power is converted to RF output power. In this definition, RF input power level isn't taken into account. Omitting the RF input power doesn't cause a problem for the multistage designs which have high gain. To sum up, drain efficiency is defined as the delivered RF output power over the DC power consumed by the amplifier:

$$Drain\ Efficiency = \frac{P_{RFout}}{P_{DC}} \tag{2.1}$$

2.2 Power Amplifier Classes

Power amplifier classes are basically classified as transconductance amplifiers and switch-mode amplifiers. Class A, AB, B and C amplifiers are defined as transconductance amplifiers, whereas class D, E and F amplifiers are defined as switch mode amplifiers. The major trade-off in the classification of the classes is between linearity and efficiency. Figure 2.1 shows the comparison of the linearity and efficiency performances of transconductance and switch mode amplifiers.

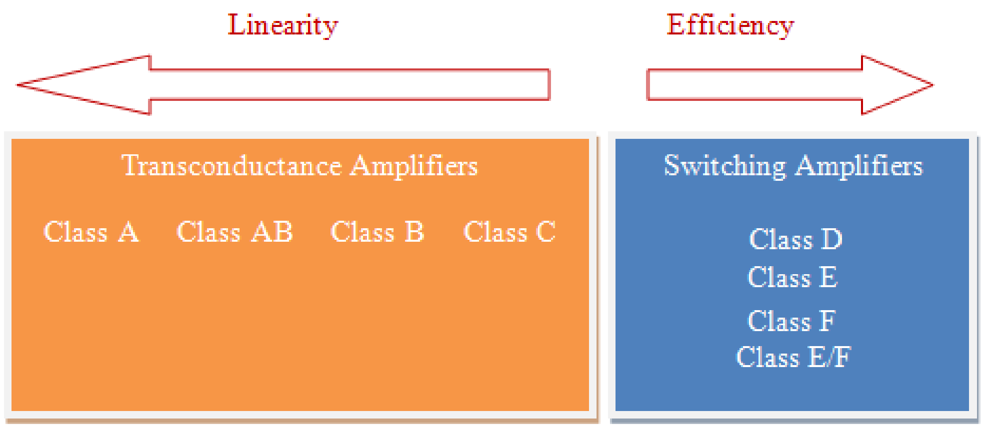


Figure 2.1: Linearity-Efficiency performance comparison of PA classes [15].

As Figure 2.1 summarizes, switching mode amplifiers exhibit more efficient performance than transconductance amplifiers, whereas they sacrifice from linearity. In switch mode amplifiers, the power amplifiers are considered as a DC-to-RF converter rather than an amplifier since the main motivation behind them is to enhance the efficiency [16].

The major characteristic of conventional class D and E amplifiers is the switch mode in which the transistor operates. Under class D and E operations, the voltage and the current waveforms at the output show a 180° phase difference [1]. In theory, %100 drain efficiency is achievable in class D and E amplifiers. However, the non-ideal switch performance of the transistors results in reduced efficiency.

In class F amplifiers, the impedance matching networks are optimized to control harmonic power levels. By showing desired loads at harmonic frequencies, drain voltage waveform is shaped to a square wave, whereas drain current waveform is a half-sine wave. In theory, % 100 drain or collector efficiency is also achievable for class F amplifiers. However, since it is only possible to control finite number of harmonics, class F amplifiers cannot reach %100 drain efficiency, either. Consequently, switch mode amplifiers benefit from nonlinear behavior of the transistor by using the device as a switch or manipulating harmonic loads in order to enhance the efficiency performance. Therefore, it results in less linear amplifiers compared to transconductance amplifiers as Figure 2.1 shows. However, in order to provide high efficiency and high linearity at the same time, some linearization techniques are implemented such as Envelope Elimination and Restoration (EER) technique, Doherty, Chireix and digital pre- and post- distortion techniques [15].

Conventional class A, AB, B and C amplifiers are also defined as linear amplifiers. They basically differentiate from each other with their bias conditions. In other words, class A, AB, B and C amplifiers are identified by their current conduction angles (CCA). Figure 2.2, 2.3, 2.4 and 2.5 show the drain current waveform of class A, AB, B and C.

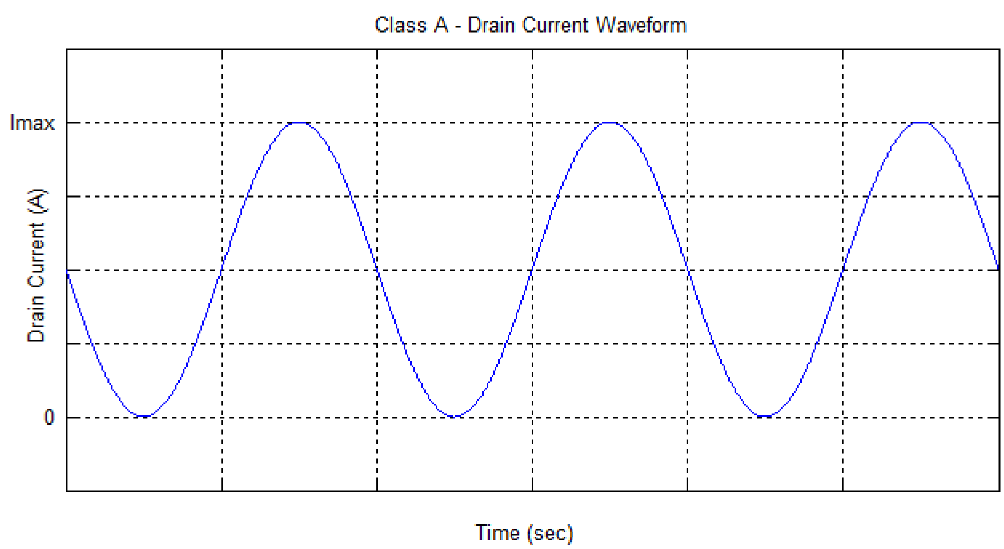


Figure 2.2: Drain current waveform of class A. The transistor operates for full cycle. The current is never zero.

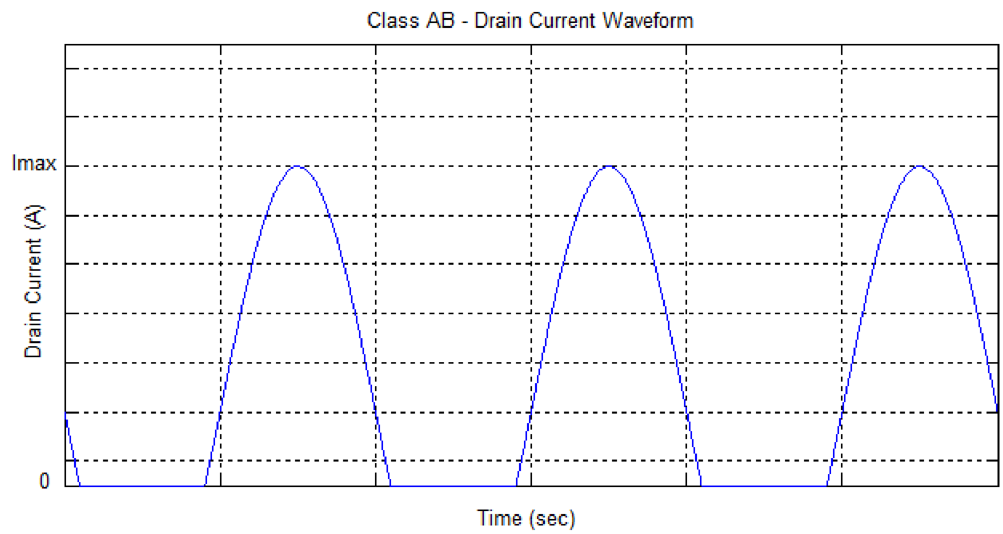


Figure 2.3: Drain current waveform of class AB. The current is zero less than half cycle.

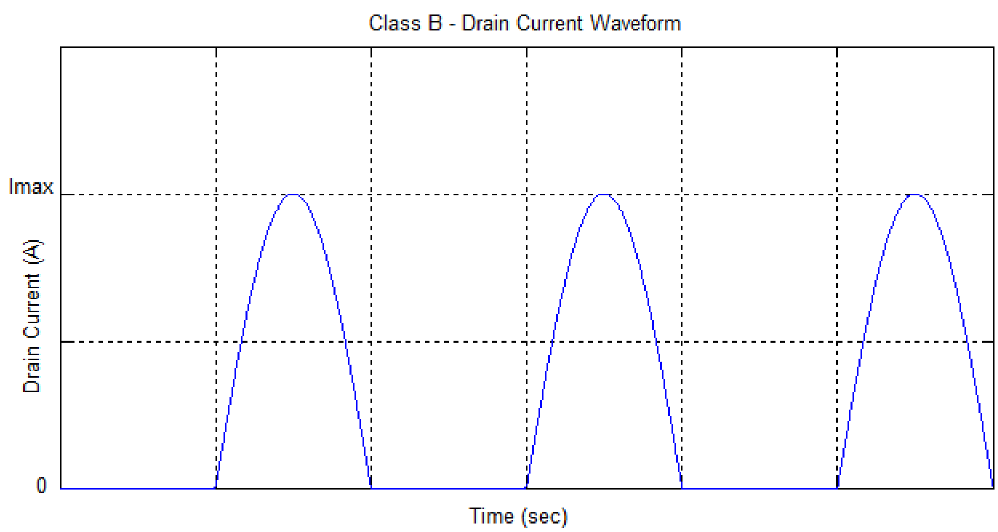


Figure 2.4: Drain current waveform of class B. The current is zero for half cycle.

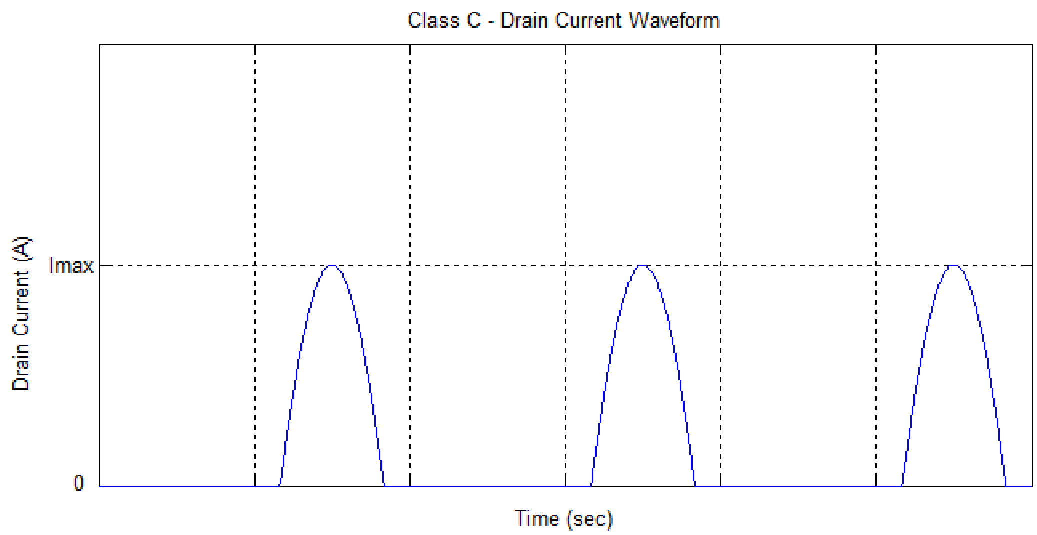


Figure 2.5: Drain current waveform of class C. The current is zero for more than half cycle.

Class A amplifier is always in conduction mode which means that drain current of class A amplifier is never zero for full cycle (360°) of the input sinusoidal signal. Therefore, class A amplifiers are known as the least efficient class compared to other classes. Theoretically, a class A amplifier can have %50 drain efficiency at most and provides the highest linearity, assuming there is no saturation [1].

Class B amplifiers are biased at the pinch-off voltage of the device where there is no current without RF signal. In this class, the transistor is in conduction mode for only half cycle (180°) of the input signal. Class B amplifiers have less linearity but higher efficiency than class A amplifiers. In theory, the maximum drain efficiency of %78.5 can be achievable [1]. There is also a mid-class between class A and B amplifiers which is called as class AB. In class AB amplifiers, Q-point is set at between the transistor pinch-off and mid-point of saturation region and pinch-off. In this case, the transistor stays ON more than half cycle. Thanks to this mid-point bias condition, class AB amplifiers can provide higher efficiency than class A amplifiers and better linearity than class B amplifiers.

In class C amplifiers, the transistor is biased at below the pinch-off. In other words, the transistor is kept in the conduction mode less than a half-cycle. Therefore, class C amplifiers provide higher efficiency than class A, AB and B amplifiers whereas they have the worst linearity performance compared to other transconductance amplifiers. Figure 2.6 shows the tuned load theoretical performance as a function of current conduction angle. Output power and gain curves are given as normalized to the power and gain of the Class A amplifier.

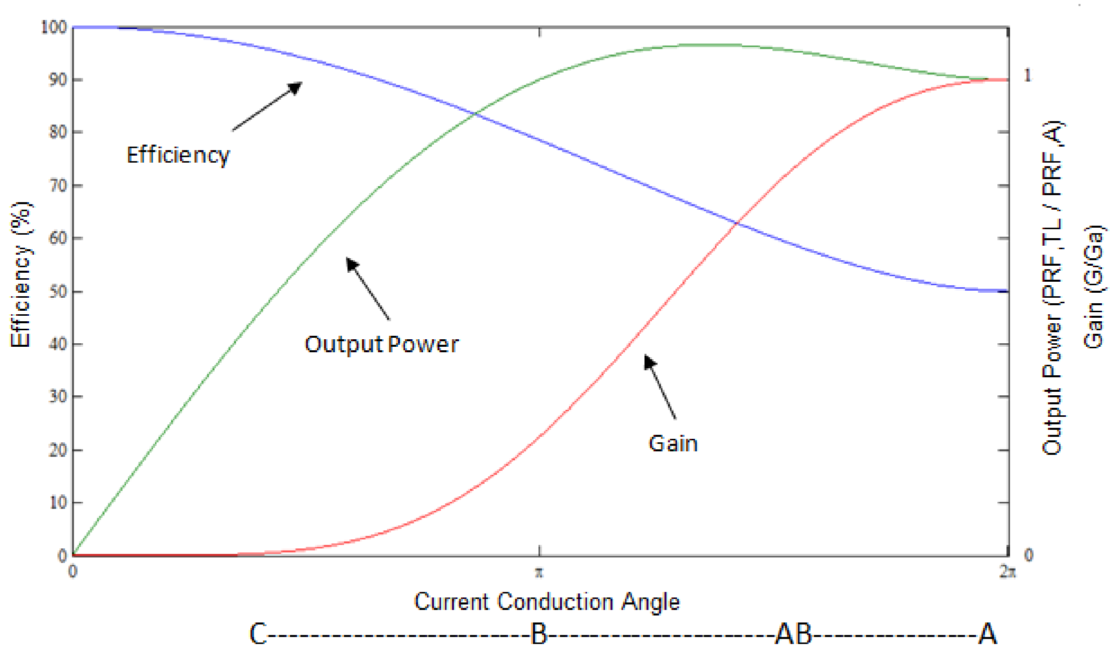


Figure 2.6: Tuned load theoretical performance comparison of transconductance amplifiers [6].

As Figure 2.6 summarizes, there is not much difference in the maximum output power performance while the conduction angle changes between 2π to π. However, while efficiency decreases, the gain performance enhances when the conduction angle increases to 2π. As Figure 2.6 shows, class AB amplifiers provide high output power and high gain at the same time while the efficiency is also high enough compared to class B and C amplifiers. Therefore, the transistors are operated under class AB operation in this thesis study.

2.3 Load-Pull Data and Output Matching

Apart from the DC quiescent point of the transistor, the load impedance shown to the device has a considerable influence on output power, PAE, gain and linearity performances of the amplifier. Each of these performance parameters has its own optimum load and source impedance conditions at not only the fundamental but also the harmonic frequencies. In order to maximize the output power, load matching is designed to match the output of the transistor to the optimum load impedance. The optimum load impedance that let to achieve maximum current and voltage swing can be approximated by the following equation:

$$R_{opt} = \frac{V_{max}}{I_{max}} \tag{2.2}$$

However, determination of the optimum load for maximum power requires further analysis apart from this approximate equation due to the parasitic effects of the transistor. The exact optimum load and power contours can be determined by either load pull simulations or load pull measurements. In these simulations and measurements, the load shown to the output of the transistor is swept using a tuner and the output power level is measured for each of the load impedance. This process provides us the power contours on the Smith chart that show the necessary load levels for desired output power. Load-pull simulations require a very good and detailed nonlinear modeling of the device since load-pull results are prone to be manipulated by the nonlinear characteristics of the device. Therefore, an accurate measured load-pull data is more trustworthy than the simulations. Especially for MMIC applications, the design success at first iteration is significant not to increase the cost by changing the design at 2nd iteration. Therefore, we used measured load-pull data of the device in this thesis study in order to achieve the required performance at first iteration.

Considering the fact that the load impedance has great influence on the performance of the power amplifier, the output matching network design requires a special attention to achieve the requirements. In addition to the load impedance, the bandwidth, loss and the complexity of the matching network are also taken into account and the optimum matching technique is chosen looking at the performance requirements.

2.3.1 Cluster Matching Technique

In MIC and MMIC applications, it is not easy to match the high power amplifiers low optimum impedance value to 50 ohm over a wide bandwidth [1]. Therefore, the cluster matching technique is used to design output matching network. Figure 2.7 shows an example of this matching technique with 4-FET combining.

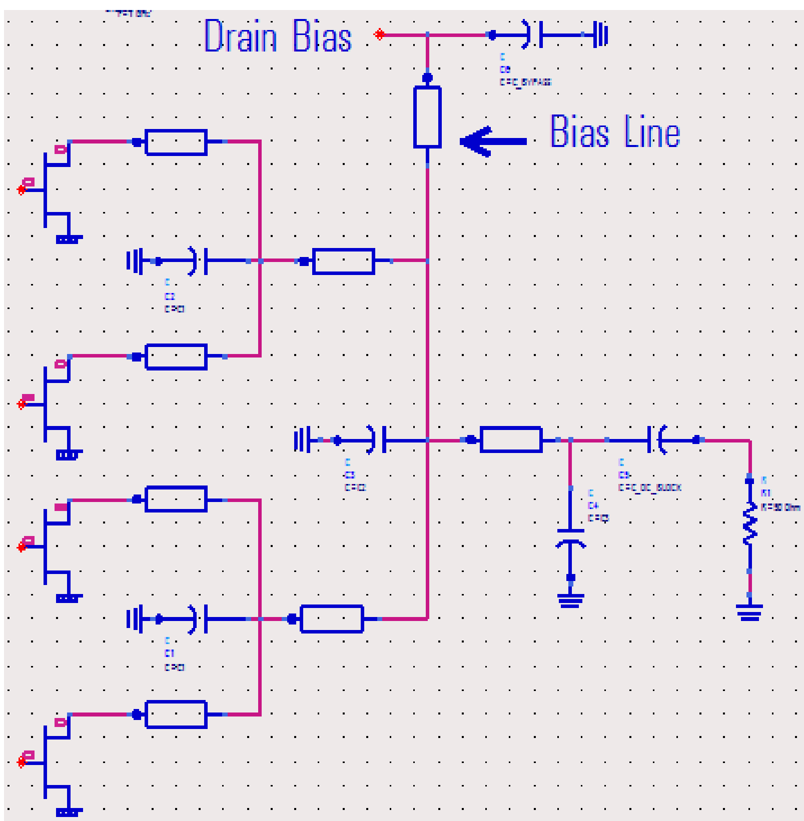


Figure 2.7: Schematic of a typical cluster matching technique [1].

Cluster matching network has two main functions. First of all, it provides the optimum load to the transistors. In addition to that, it combines the output power provided from the transistor. Matching network transforms 50 ohm to the optimum load by using intermediate load values at each combination junction. Thanks to this technique, wider bandwidth matching is realizable for high power amplifier designs. There are three major advantages of this type of matching network [1]: higher impedance levels, efficient power combining due to in-phase feeding the devices and lower thermal resistance due to the distribution of the devices over a larger area.

2.4 Stability

Stability analyses must be carefully conducted in a RF/microwave amplifier design since any unwanted oscillation may cause serious effects on the RF/microwave performance of the design. Even-mode, odd-mode and parametric oscillations are the most serious types that can be encountered with in a MMIC power amplifier design.

Even-mode oscillations can be prevented by providing unconditional stability for all frequencies. There are mathematical expressions that test the stability conditions of the systems, such as K factor and μ factor related to S-parameters. According to K-Δ test, for all passive source and load terminations, a device is unconditionally stable if the following two conditions are simultaneously satisfied [17].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \tag{2.3}$$

$$\Delta = \ |S_{11}S_{22} - S_{12}S_{21}| > 1 \tag{2.4}$$

In addition to the even-mode stability, multidevice and multistage amplifier designs require further stability analyses. Odd-mode oscillation is also another important concept that must be carefully investigated during the design procedure. In most MMIC high power amplifier (HPA) applications, the transistors at the output stage are combined by using the cluster matching network. Although, the matching network seems symmetrical and fed the transistor in-phase, each transistor can see different load due to the coupling issues at the output matching network. This asymmetry at the output stage may cause odd-mode oscillations which must be analyzed and taken proper precautions during the design phase.

The multistage power amplifier design also triggers the generation of parametric oscillations which show up as a function of input power or input frequency due to the presence of multiple nonlinear devices and loops [18]. Parametric oscillations occur at multiple of the subharmonics (f/2, 3f/2 ...) and they are mostly caused by the nonlinear behavior of the device. Therefore, parametric oscillations usually occur when the amplifier is driven to compression where the nonlinearity of the device increases. Primarily, the nonlinearity in Cgs and Cgd generate subharmonic oscillations [19]. Since the capacitances of Cgs and Cgd are dependent to input power, mostly subharmonic oscillations occur only under large signal conditions.

2.5 Design Procedure

2.5.1 Technology and Transistor Type Selection

After the determination of the design requirements, technology and transistor type must be decided since it directly affects the amplifier performance. Different transistor technologies have different advantages and disadvantages depending on the frequency of operation, power, efficiency and noise figure performance. Therefore, it is critical to choose the optimum process by evaluating the cost and performance requirements of the application. For instance, for high power amplifier applications at microwave and millimeter-wave frequencies, GaAs and GaN HEMTs are the best candidates due to their superior output power, gain and efficiency performances.

2.5.2 Transistor Size Selection

Transistor size selection is another significant step in a power amplifier design. It must be carefully chosen since it directly determines the output power, gain, efficiency, output matching loss and size of the chip. For the multistage power amplifiers, transistor size and the number of transistors used in the driver stage are also critical in order to keep the efficiency high and prevent the problems such as early driver saturation. Considering either load-pull measurements or simulations, transistor size and bias conditions must be selected in accordance with the application requirements.

2.5.3 Design Topology and Circuit Optimization

At this step, the topology of the matching network, biasing networks and the number of stages are decided regarding the power, gain, efficiency and bandwidth requirements. In this step, input, interstage and output matching networks are designed and optimized considering the requirements. During the design of matching and biasing networks, stability must be also simultaneously analyzed and matching networks must be optimized in order to assure the stability for all frequencies.

2.5.4 Layout Design

Despite the fact that layout design phase follows the design topology step, these two phases must be simultaneously operated since all the design movements made in previous step must be physically applicable. In addition to that, depending on the type of application, cost also can be the first consideration and the design must be optimized in size even sacrificing from the performance. Therefore, layout design must be always taken into account while designing the matching and biasing networks. After layout design is completed and the design rule check is performed, MMIC is ready to be fabricated.

Chapter 3

A Ku-Band pHEMT MMIC Power Amplifier Design

In this chapter, the design of a Ku-band 3-stage AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility (pHEMT) MMIC high power amplifier is discussed. This MMIC power amplifier was fabricated on WIN Semiconductor's 0.25 μm gate-length pHEMT technology (PP-2521) with 4-mil wafer thickness. In this thesis work, we aimed to achieve at least 22 dB small-signal gain with ± 1 dB gain ripple and minimum 10-W continuous-wave (CW) operation output power at 3 dB compression under 8V operation. In order to provide required output power, 16 transistors in common-source configuration were combined at the output stage. The challenging part of this thesis work is to achieve 10-W continuous-wave (CW) output power, even when the base temperature of MMIC reaches 85°C, since high current levels result in thermal problems which directly degrade output power, gain and efficiency performances of the chip.

The design of amplifier was performed using the design kit of selected process (PP2521). Although, the design kit includes small-signal and large-signal models of the transistors, we used small-signal and load-pull measurements performed at ASELSAN, due to the reliability concerns about the large-signal model of the design kit. All simulations and layout design were completed using Agilent's

Advanced Design System (ADS) Simulation Tool. Design steps are given in the following sections step by step.

3.1 Process Selection

After we determined the design requirements and decided to use pHEMT technology, we started down selection phase between possible processes. The key motivation behind this down selection is to select optimum process with high power density, high gain and compact cell structures. From this point of view, we chose WIN Semiconductor (Taiwan) Foundry in the design of this work and the foundry presents two different processes that are available for Ku-band power applications: PP25-01 and PP25-21. When the power densities and gain performances of these two processes are compared, we decided to use 0.25 μm power pHEMT Ku-band 8V PP25-21 process since it offers higher output power density and gain compared to PP25-01 at Ku-band. In fact, PP25-21 process is based on PP25-01 technology but while PP25-01 uses 7V operation, PP25-21 is operated under 8V. In other words, PP25-21 is the process of qualified version of PP25-01 for higher output power performance. Therefore, PP25-21 was selected for this thesis work.

3.2 Transistor Size Selection

GaAs MMIC foundries define the transistors by their number of fingers, gate width and number of ground via. Figure 3.1 shows an example of PP25-21 pHEMT layout in common-source configuration.

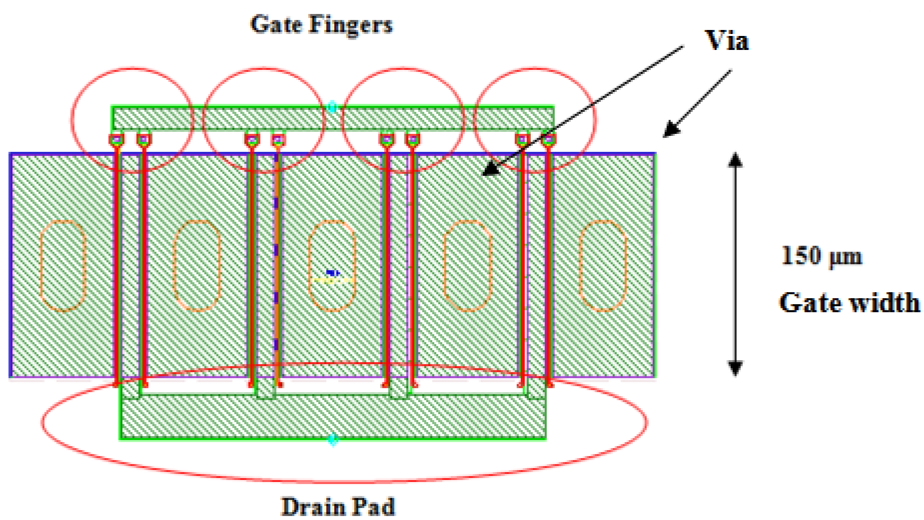


Figure 3.1: Layout of 8x150 μm with 5 via PP25-21 transistor.

A transistor periphery is defined by the multiplication of the number of gate fingers and gate width. Power density is also calculated using this term. Therefore, both the gate width and number of fingers determine the output power of a transistor. Besides, the number of via used in the transistor play considerable role in the thermal performance which also influences the amplifier's performance parameters such as power, gain and efficiency. Therefore, transistor selection process is performed considering these three transistor parameters: gate width, number of gate fingers and number of via.

There are three major points to be noted in choosing the optimum transistor size: output power, gain and size which are interrelated, as well. To begin with, the designer must put extra effort in order to keep the chip dimensions as small as possible due to the cost issues. From this point of view, the size of the transistors must be carefully chosen because y-dimension of MMIC is determined by the number of fingers of the transistors at the output stage. Therefore, increasing the number of fingers results in increased y-dimension of MMIC which is not a cost-effective solution to enhance the output power. Additionally, the number of via is also another significant transistor parameter. From the RF performance point of view, using large number of vias for each transistor is desirable to have better thermal performance and electrical performance but in the expense of larger chip dimensions. Encircled part in Figure 3.2 shows how the size of the transistors at the output stage sets the y-dimension of the chip.

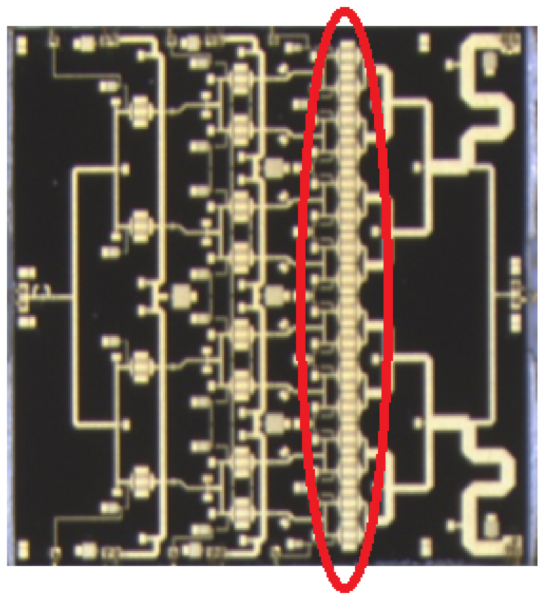


Figure 3.2: Photograph of a fabricated PHEMT MMIC PA

Gate width is another important transistor-size parameter that influences the performance of the transistor. In some cases, gate width of the transistor is also increased in order to obtain larger periphery and improve the output power performance. However, there are two major drawbacks about increasing the gate width. First of all, there is a process limitation about increasing output power using larger gate periphery because when the device reaches a certain size, scaling ratio starts to drop. As an example, when the transistor size is doubled from 2x75 μm to 4x75 μm, output power is almost doubled but this relation is distorted for scaling between larger devices such 8x150 μm and 8x300 μm. In other words, power densities start to drop after exceeding a certain size limit. Consequently, output power scaling saturates for larger devices. In addition to that, increasing the gate width results larger output capacitance which both decreases the gain and lowers the optimum impedance. As a consequence of this, the loss of output matching network increases which means using larger devices may not be solution for enhancing the output power when the device size exceeds a certain limit.

In order to determine the required transistor size to be used at the output stage, we used load-pull measurements performed at 16 GHz. Load pull measurements were performed at 8V drain voltage and 150 mA/mm. Figure 3.3 shows the photograph of a 6x150 μm (3 via) sample. Figure 3.4 and 3.5 show the power density and gain performance graphs of the transistors with different peripheries and via configurations.

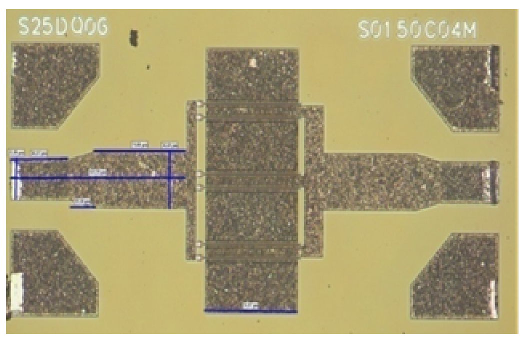


Figure 3.3: Photograph of a 6x150 μm (3 via) transistor sample.

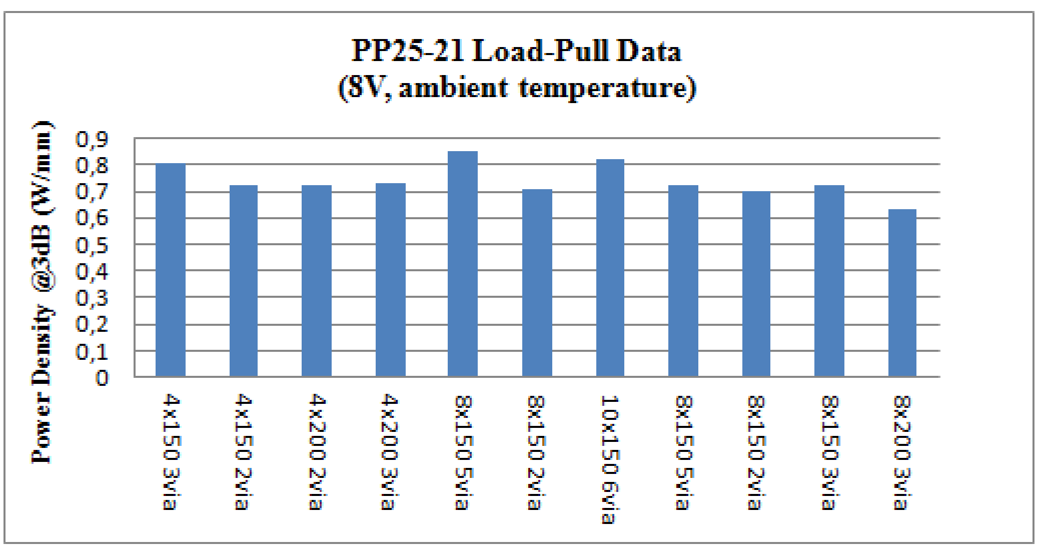


Figure 3.4: Power densities of different size transistors at 3 dB compression.

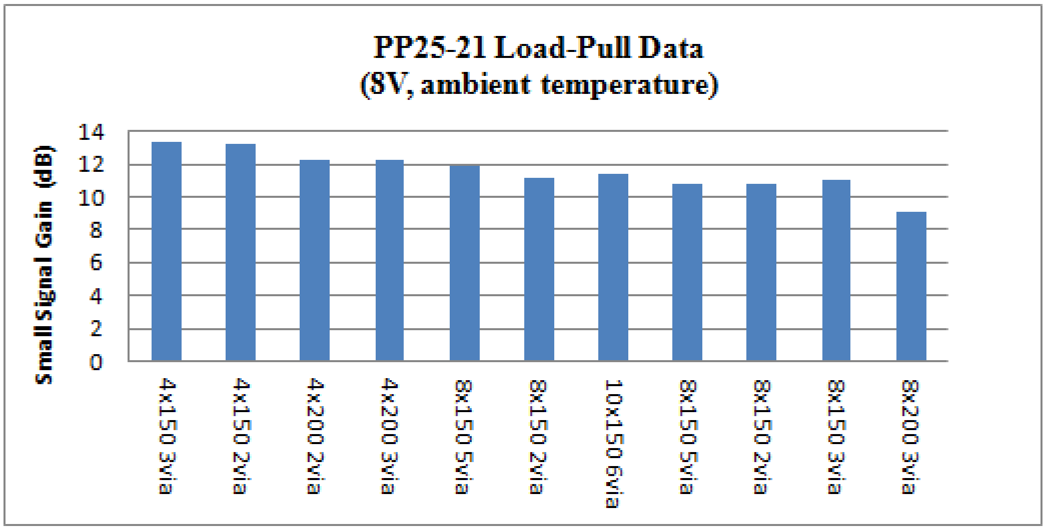


Figure 3.5: Small signal gain measurement of different size transistors.

Load-pull measurements show that PP25-21 process exhibits 0.7-0.85 W/mm at 3-dB compression for all peripheries at 16 GHz. Considering these measurements, we decided to combine 16 cells at the output stage in order to meet 10W level of output power at 3 dB compression. Figure 3.6 shows the possible via and combinations of 150 μm gate-width transistors. Each configuration has its own benefits in terms of output power, thermal management and die size.

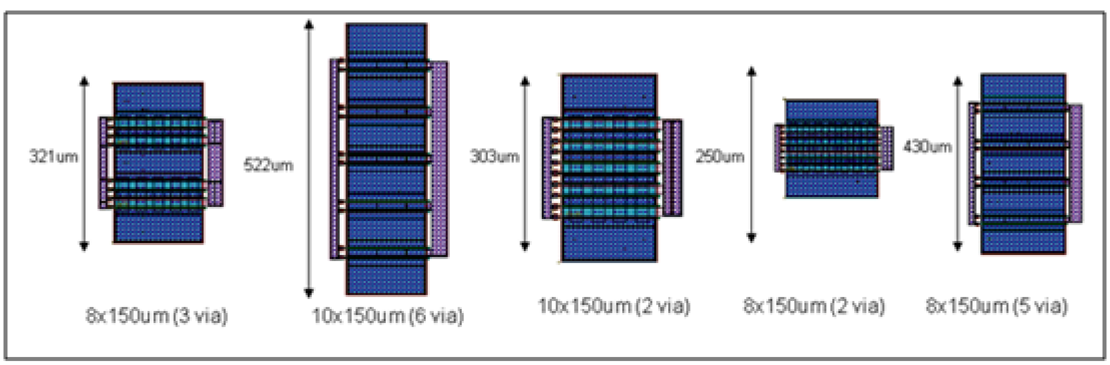


Figure 3.6: Layout configurations of 150 μm transistors.

To begin with, we decided to use one of these 3 via configurations considering both thermal performance and die size. Using this configuration with 321 μm length in y-axis, we set y-dimension of MMIC to 5.7 mm. As the second step, we decided to use 150 μm gate width device since 8x150 μm (3 via) transistor is able to provide 30.3 dBm output power at 3 dB compression when the device is matched for maximum output power. Maximum drain efficiency is %48 if the device is matched to maximize efficiency. Figure 3.7 shows measured power and efficiency contours at 16 GHz. Load-pull measurements were done using the samples that WIN provided us but there was 10° (at 10 GHz) transmission line at the output of the transistors as it can be seen on Figure 3.3. Contours are plotted referenced at probes. Therefore, we added the effect of the transmission line to the power and efficiency contours. Table 3.1 and Figure 3.8 show the optimum loadings for both power and efficiency after the effect of this transmission line is de-embedded.

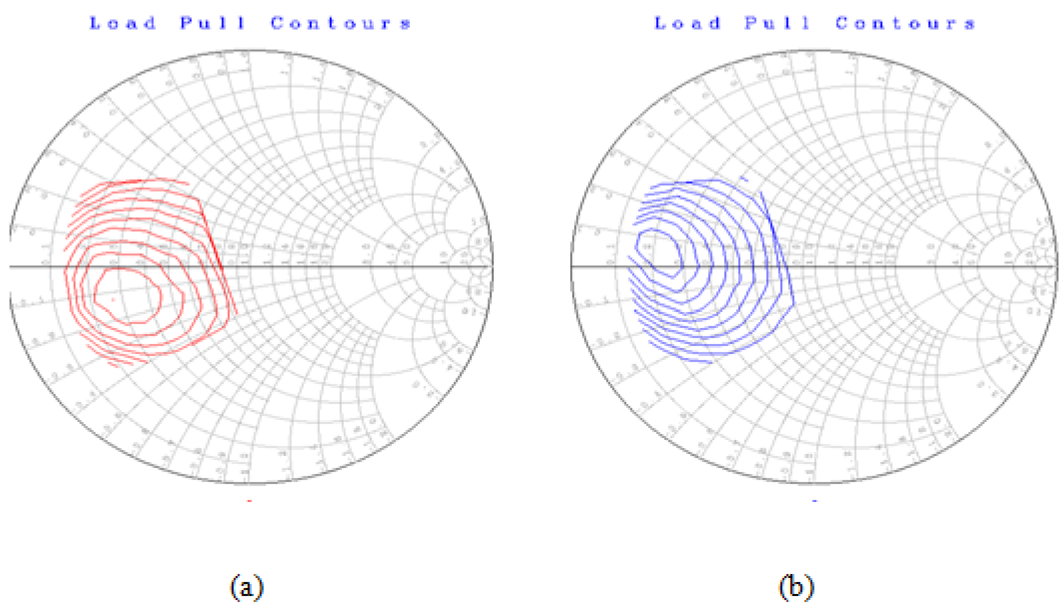


Figure 3.7: (a) Power contours of 8x150 μm (3 via) transistor at 16 GHz. Maximum power is 30.3 dBm and contours are separated by 0.5 dB. (b) Efficiency contours of same device. Maximum efficiency is %48 and contours are separated by %3. In order to reach real optimum loadings, 10° (at 10 GHz) transmission line is de-embedded.

$Z_{optpower}$	$13.590 + j * 6.828$
Z_{opteff}	$11.102 + j * 16.436$

Table 3.1: Optimum loadings for power and efficiency at 16 GHz when 10 ohm-10° line is de-embedded.

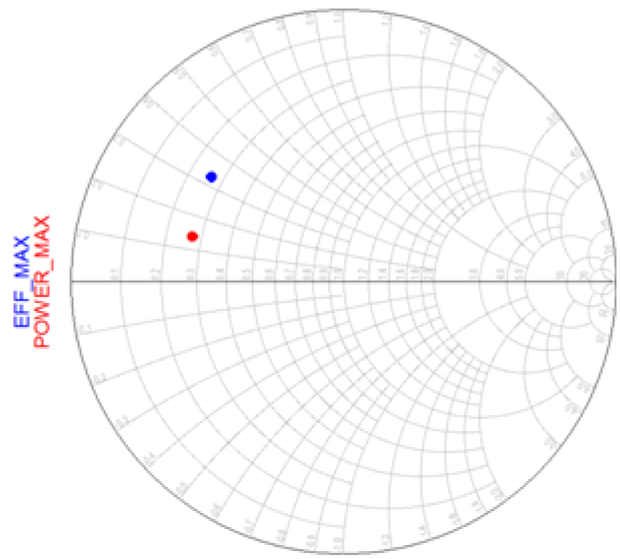


Figure 3.8: Optimum loadings for power and efficiency when the line at the output of the transistor is de-embedded.

Using load-pull measurement result, when each of 16 cells at the output is matched for maximum power, we expected to obtain 42.3 dBm output power. Table 3.2 approximately summarizes how much we may lose from this power when the loss, mismatch, thermal performance and process spread are considered.

Loss in output matching network	1 dB
Loss due to mismatch	0.2 dB
Change in output power due to temperature	0.5 dB
Change due to process spread	0.3 dB
Total Loss	**2 dB**

Table 3.2: Approximate loss calculation in the worst case scenario.

This approximate estimation gives 2 dB degradation of output power for the worst case scenario. Even for the worst case scenario, we have 0.3 dB margin in order to achieve 40 dBm output power level which is good enough. Consequently, we decided to combine 16 cells of 8x150 μm (3 via) transistors at the output stage. In other words, the total periphery used in the output stage was selected as 16x8x150 μm = 19.2 mm.

3.3 Matching Networks Design

3.3.1 Output Matching Network Design

The output matching network design is the most critical part of the power amplifier design since it directly determines the output power level. In the design of output matching network, we paid special attention to design the matching network for optimum load and have low loss in order to achieve desired power level. As the other significant point, WIN foundry informed us that capacitances may vary in the interval of $\pm$%5 due to the process tolerance. Therefore, the loads shown the transistors and the loss of matching network should be as insensitive as possible to the process tolerance of the capacitors. Therefore, we optimized the matching network for not only optimum load but also insensitive response to the process tolerance. Simplified model of the output matching network is shown in Figure 3.9.

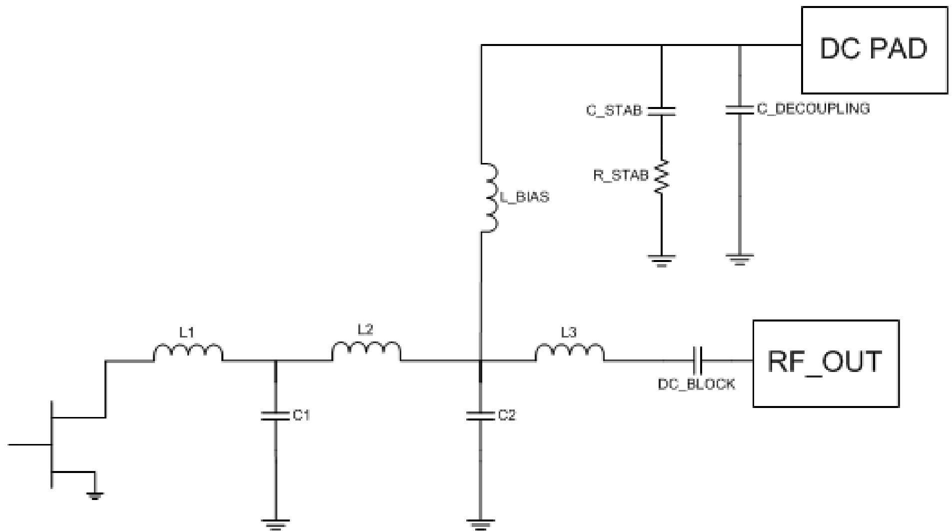


Figure 3.9: Simplified schematic model of the output matching network.

As it can be seen in Figure 3.9, we used low-pass matching networks that consist of series inductors and shunt capacitors. However, we used transmission lines in the design instead of using inductors. Shunt capacitors were realized by Metal-Insulator-Metal (MIM) capacitors (600 pF/mm^2) of PP25-21 process. Figure 3.10 shows the layout of a 40x40 μm^2 capacitor from top view. Bias line was tuned to show the circuit almost open not to change the impedance level in the output matching network. In addition to RF bypass capacitor, we added shunt network that consisted of series MIM capacitor and a thin-film-resistor against possible low-frequency oscillations. The sizes of MIM capacitor and thin-film resistor were optimized considering the stability analyses which will be discussed in the following chapters. Figure 3.11 shows the layout of a 50x50 μm^2 (50 ohm/sq) thin-film resistor of PP25-21 process.

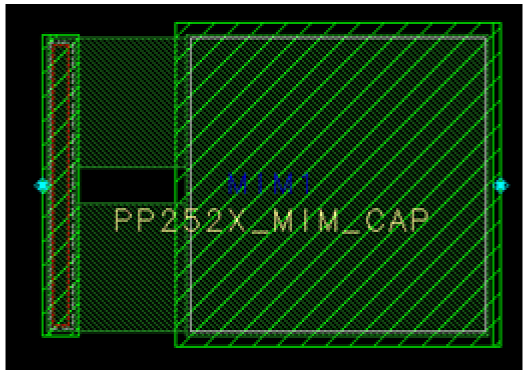


Figure 3.10: Layout of a 40x40 μm^2 capacitor corresponds to 960 fF.

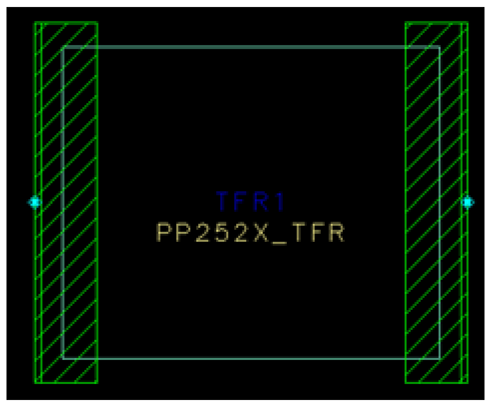


Figure 3.11: Layout of a 50x50 μm^2 thin-film resistor (TFR) corresponds to 50 ohm.

Figure 3.12 shows the layout of the output matching network. We used cluster matching technique as it is discussed before. In this technique, the output network provides both combining and matching to realize the optimum loading for output power with minimum loss. Bias was also supplied through an RF line which is decoupled in-band and with a lossy low frequency termination. In order to protect the symmetry of the matching network, the shunt capacitors were used at the combination junctions and the drain bias was supplied from both sides.

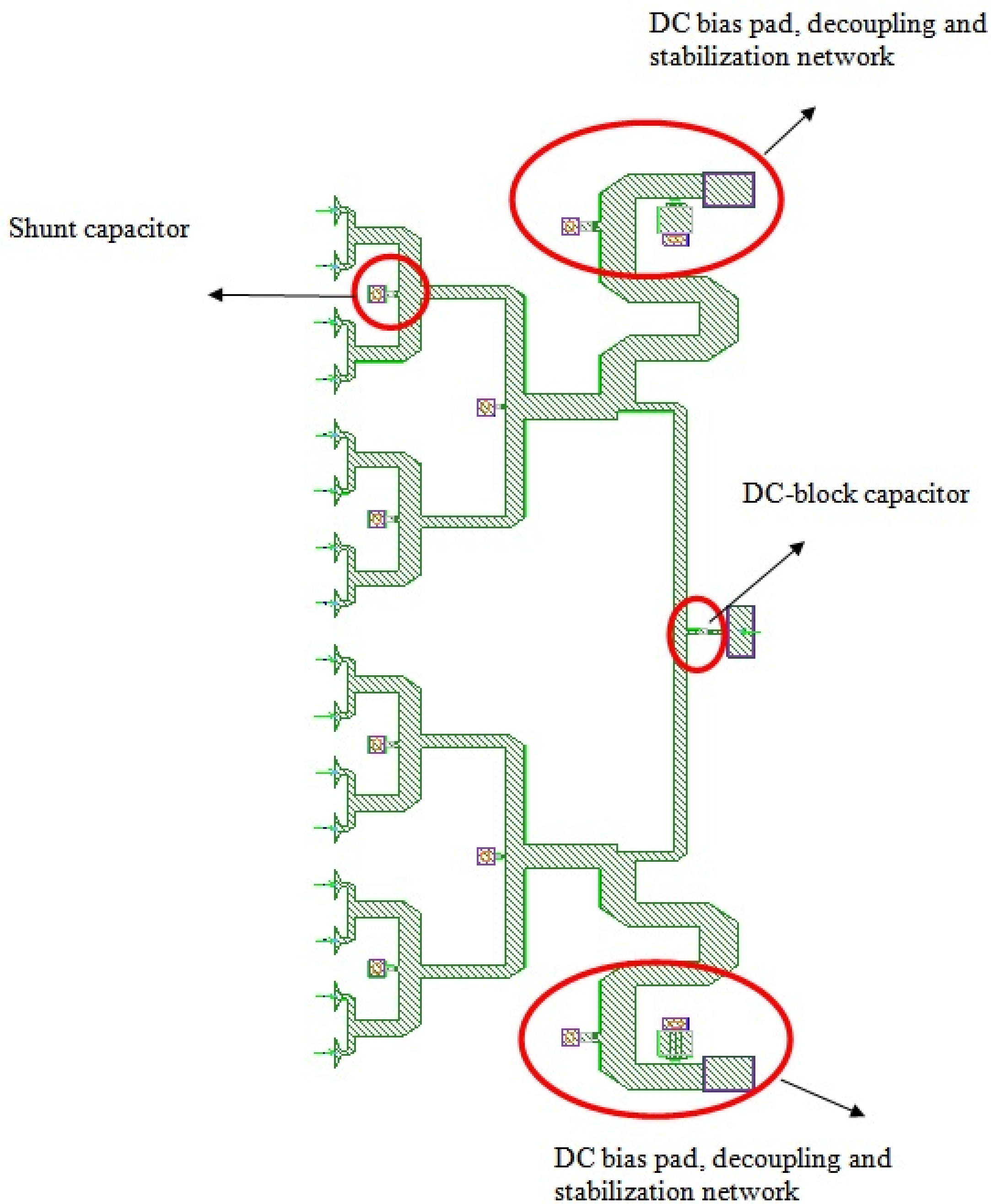


Figure 3.12: Layout of the output matching network.

The loading to the each of 16 cells in the band of operation is shown in Figure 3.13. We optimized the matching network components in order to keep the loss less than 0.85 dB in the band when ±%5 change in capacitance was considered. Figure 3.14(a)-(b) show how the loading and loss changed when the process tolerance was considered.

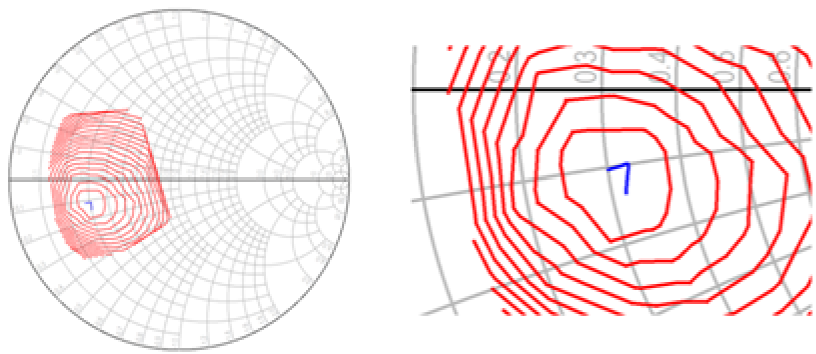
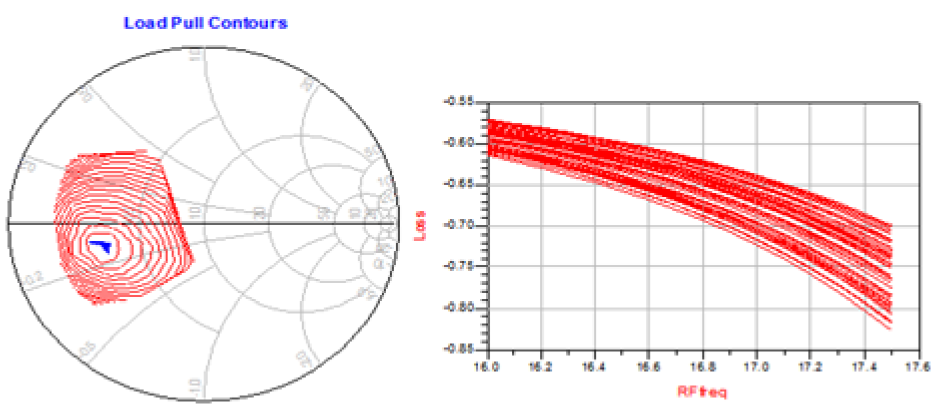


Figure 3.13: Loading shown to the output cells in the band of 16-17.5 GHz.



(a) (b)

Figure 3.14: When ±%5 capacitance tolerance considered (a) shows the loading spread on the Smith chart and (b) shows how the output matching loss changed with capacitance tolerance.

One of the most critical part of the design part was to show the same loading to each of 16 cells since in order to provide the desired power, 16 cells must operate in-phase. Despite the fact that output matching network seems symmetrical, EM-simulations showed that different loadings were shown to each of 16 cells due to the coupling issues. Figure 3.15 shows how the loadings spread over the Smith chart.

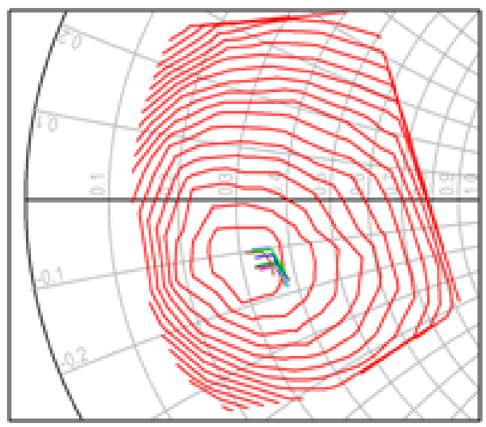


Figure 3.15: Impedance spread due to EM-coupling at the output matching network.

In order to prevent this situation, we implemented asymmetrical matching technique at the output stage. In order to show same loading to each cell, we created asymmetry on purpose by shifting the location of the first two combination junctions in the arrow directions. In Figure 3.16, encircled parts show where this asymmetry was created.

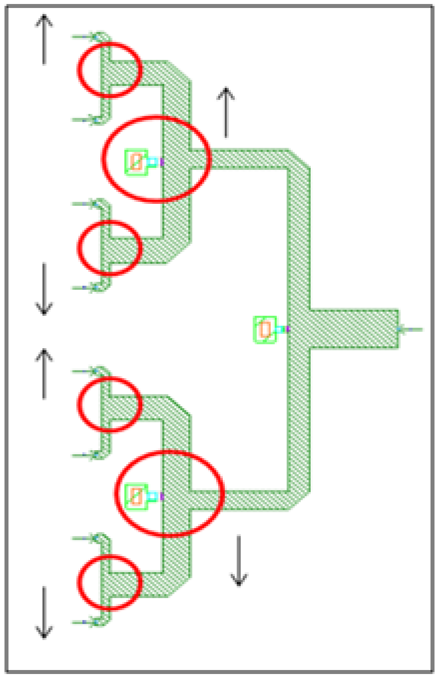


Figure 3.16: Asymmetry applied to the output matching network.

After we applied this asymmetry technique, we achieved to show almost same impedance to 16 cells. Figure 3.17 shows how this technique was successful to minimize EM-coupling effects at the output matching network. As it can be seen, the loadings were almost same for each of 16 cells which was necessary condition for efficient power combining at the output stage.

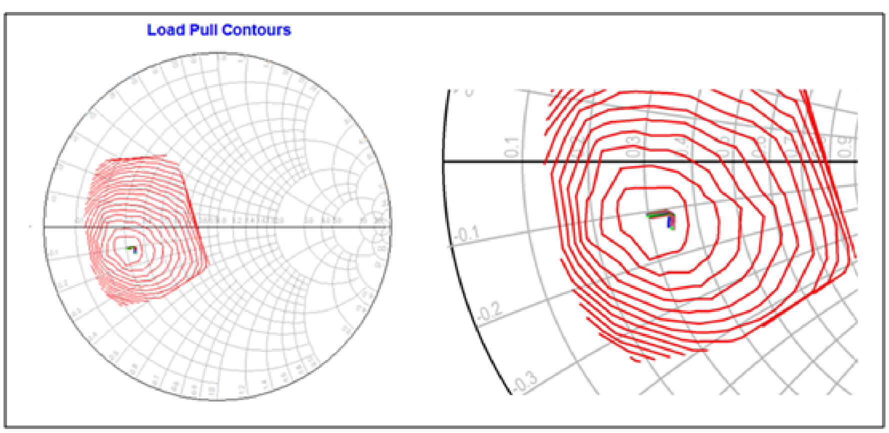


Figure 3.17: Loadings of 16 cells after asymmetry applied.

3.3.2 1st Interstage Matching Network

Selection of the required periphery of the driver stage is also significant in order to achieve necessary output power and efficiency performances. The main condition for the driver stage is to provide necessary power to the output stage to drive it into the saturation. Therefore, in order to achieve required output power, driver stage shouldn't go into saturation earlier than the output. Due to this reason, the periphery of the driver stage must be selected large enough to drive the output stage into saturation. However, choosing large periphery value for the driver stage degrades efficiency performance and results in less gain. Therefore, the driver stage periphery requires an optimum selection, as well. In this thesis work, we decided to use 8 cells of 8x150 μm (3 via) transistor which makes the power drive ratio 1:2 for this design.

After we decided the periphery of the driver stage, we designed the first interstage matching network. Since we aimed to maximize the power delivered from the driver stage, we designed the first interstage matching network to transfer the input impedance of the output stage to the $Z_{optpower}$ impedance of the driver stage transistors. We minimized the insertion loss of the matching network, as well. Figure 3.18 shows the simplified schematic version of the first interstage matching network.

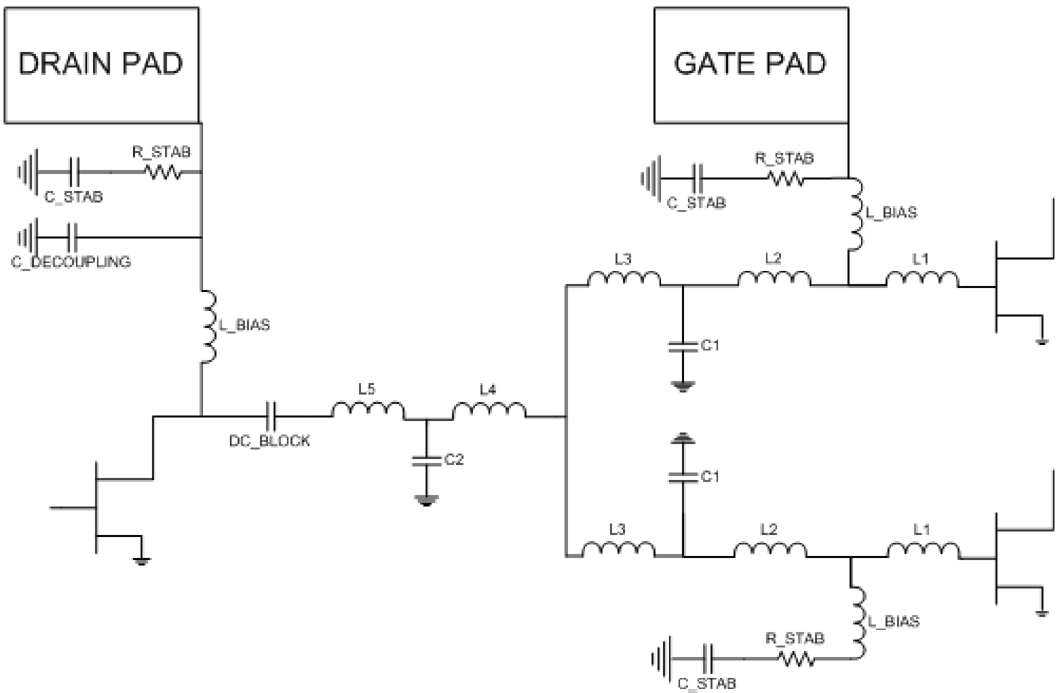


Figure 3.18: Simplified version of the first interstage network.

Figure 3.19 shows the layout of a part of the interstage network. Since there were 16 transistors at the output stage and 8 transistors at the driver stage, the first interstage network connected two of the output cells to the single cell of the driver stage. In the design of this matching network, we used low-pass matching networks consisting of series inductors and shunt capacitors. As we did in the output matching network, series inductors were realized by transmission lines. Gate bias of the transistors of the output stage was applied between a capacitor and resistor which were tuned for stabilization of the circuit. Drain bias of the driver stage was applied between bias line and decoupling capacitor. Additionally, we added a shunt stabilization network which consists of series capacitor and resistor. The component values of this network were optimized for low frequency stability. Considering the symmetry issue, we used double side biasing for both drains of the driver stage and gates of the output stage. Drains of the driver stage cells were connected to each other by bias bus bar which had no effect on

RF performance. Figure 3.20 shows the layout of the first interstage matching network. DC block capacitors, stabilization networks on the gate and drain bias lines are encircled in Figure 3.19. Bias pads are also named as VD2 (Drain bias pad of the driver stage) and VG3 (Gate bias pad of the output stage).

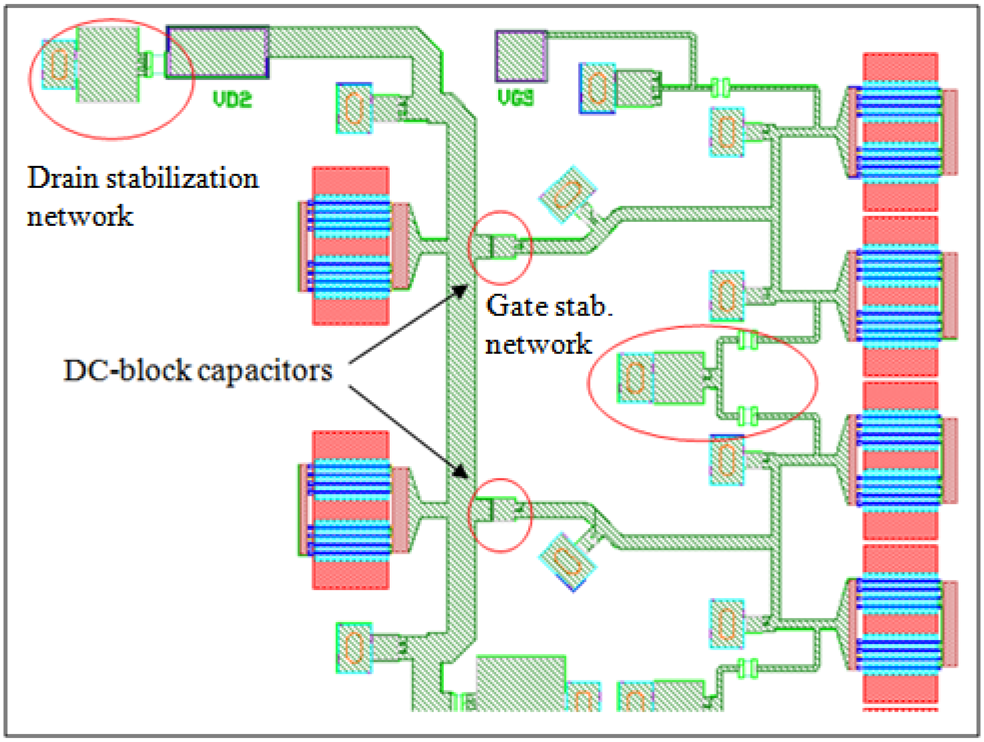


Figure 3.19: Layout of a part of the first interstage network.

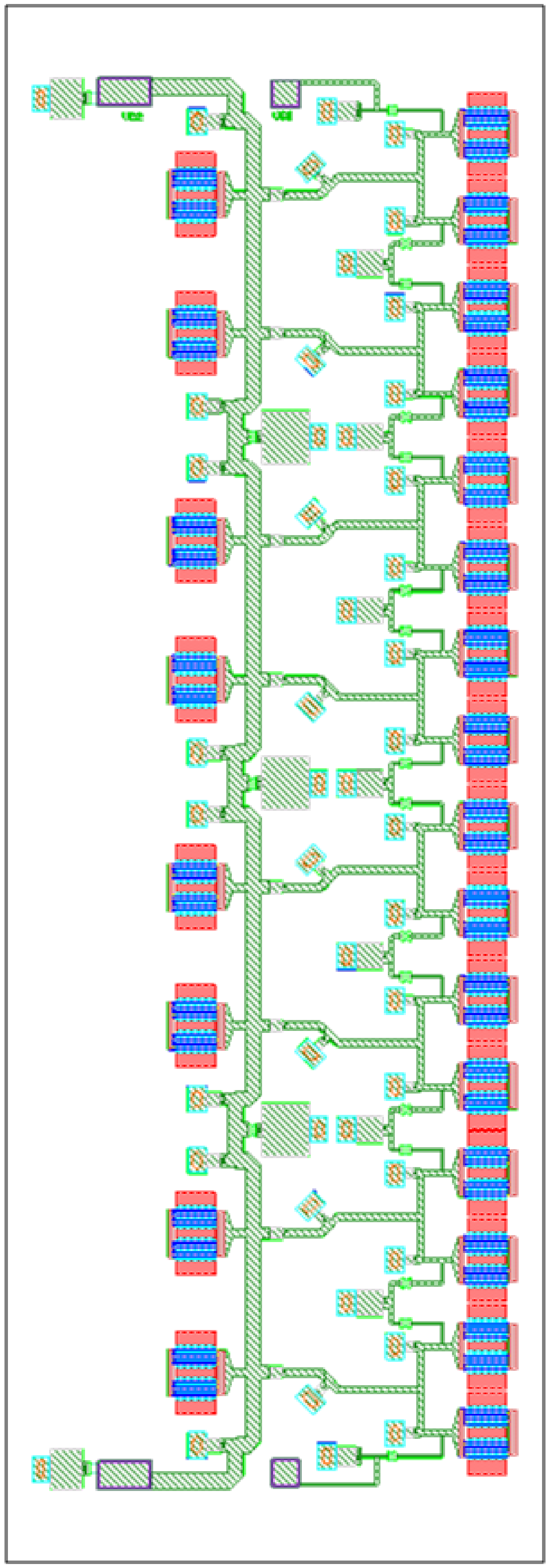


Figure 3.20: Layout of the 1st interstage network.

We designed the interstage matching network for maximum power. The loading shown each of 8 cells at the driver stage is given in Figure 3.21 (a). Figure 3.21 (b) shows the loading spread when ±%5 capacitance tolerance considered.

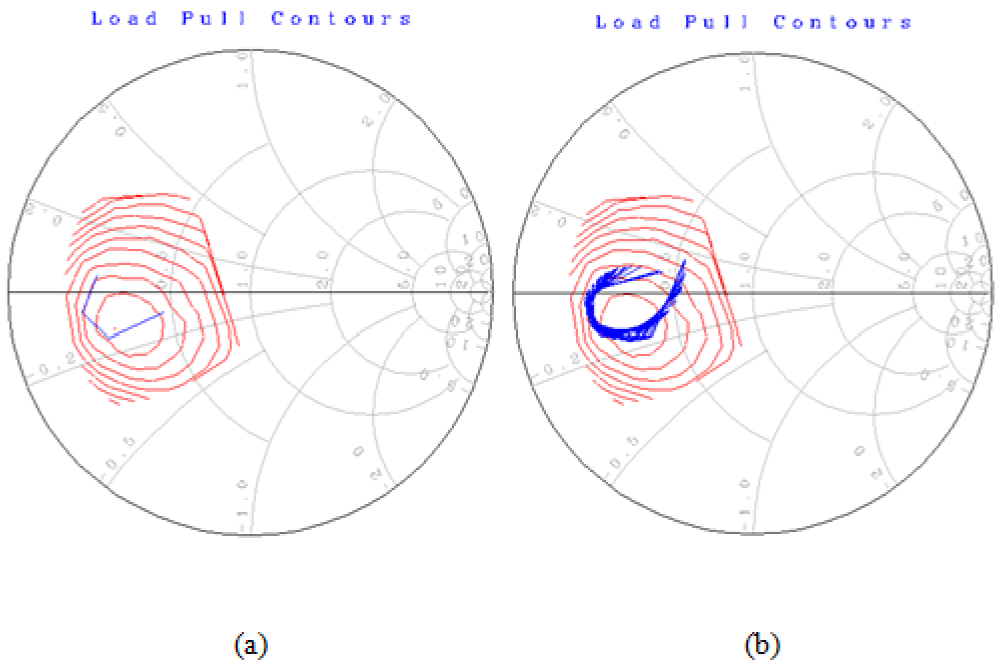


Figure 3.21: (a) shows the loading shown each cell and (b) the loading spread when capacitance tolerance is considered.

In the design of the 1st interstage matching network, we conducted an additional analysis to see the saturation level of the driver stage when the output stage reached 3 dB saturation level. In this analysis, we assumed that the output cells reached desired power at 3 dB saturation level and we checked the power level provided by the driver stage. We monitored the difference between 3 dB saturation power of the driver stage and the power provided by the driver stage when output cells reached 3 dB saturation. Figure 3.22 shows this headroom analysis result considering capacitance tolerance. The worst case condition was detected at 16 GHz because Figure 3.21 shows that a single cell provided 28.12 dBm (which was 2.2 dB less than maximum power) at 16 GHz for -%5 capacitance tolerance condition. For same condition, headroom was simulated as 4.8 dB which means that real headroom was $4.8 - 2.2 = 2.6$ dB. According to this analysis, when the output cells reached 3 dB saturation, the cells at the driver stage provided 2.6 dB less power than their own 3 dB saturation level which was safe enough for the worst case condition.

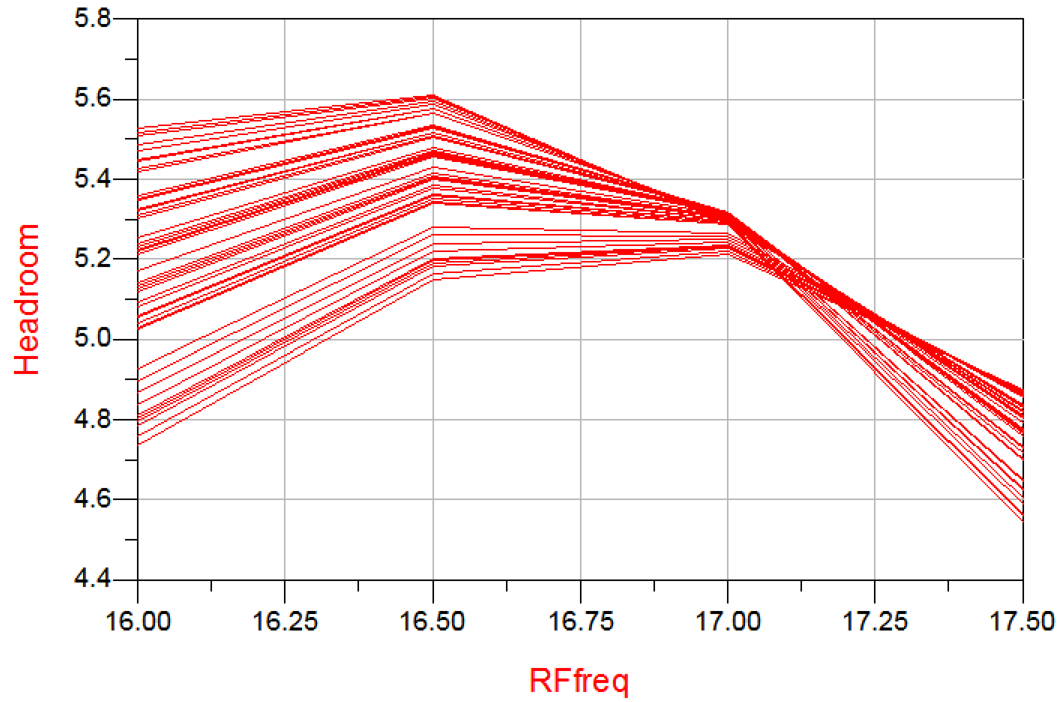


Figure 3.22: The headroom analysis of 1st interstage matching network.

3.3.3 2nd Interstage Matching Network

We added 3rd stage in order to satisfy the gain requirements. Therefore, the main function of this stage was to enhance the gain and adjust the gain flatness considering the design requirements. We used 4 cells of 8x150 μm (3 via) transistor at this stage. The second interstage matching network basically connected the 8 cells at the driver stage to the 4 cells at the first stage. As we did in the design of other matching networks, we used low-pass matching technique that consists of series inductor and shunt capacitors. We put stabilization networks and optimized their values for low-frequency stability. Figure 3.23 shows the layout of the second interstage network. DC block capacitors, stabilization networks of the drain and gate bias lines are shown in the circles in Figure 3.24.

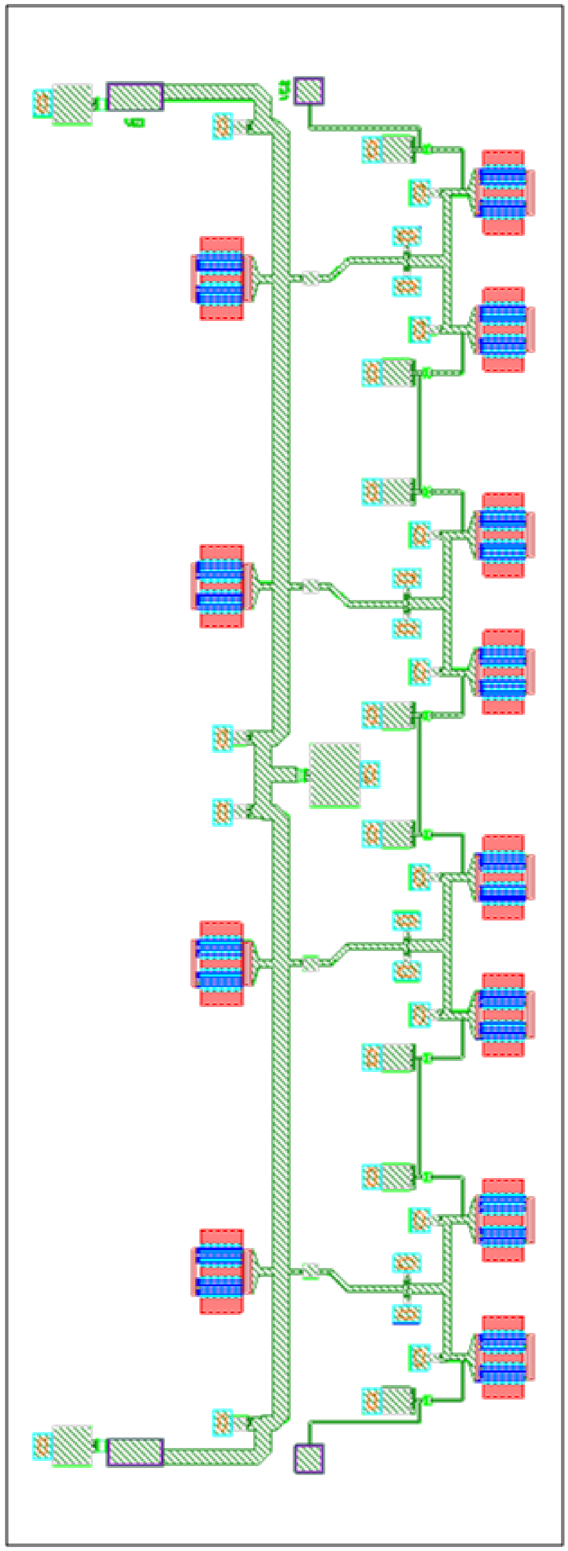


Figure 3.23: Layout of the 2nd interstage network.

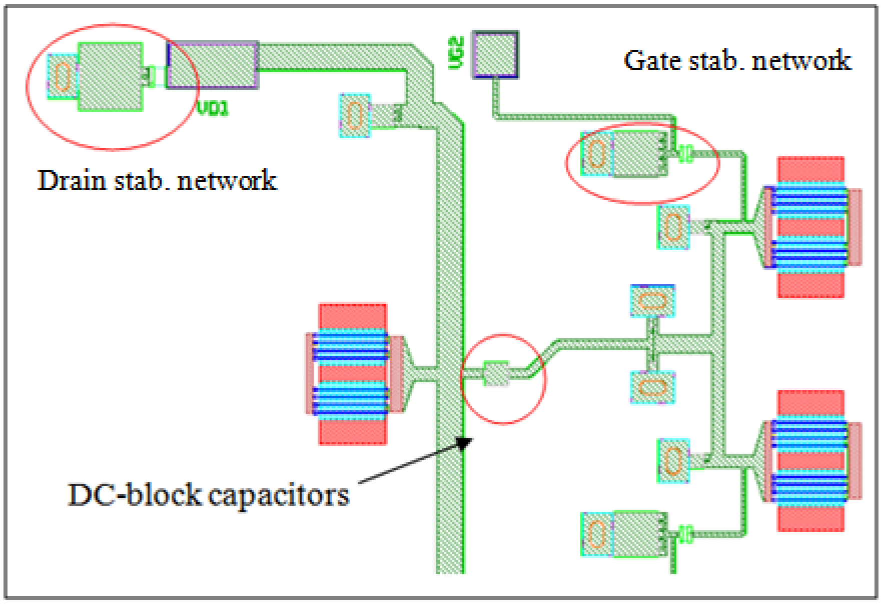


Figure 3.24: Layout of a part of the 2nd interstage matching network.

We designed this interstage matching network to increase the gain and optimize the gain flatness. The loading shown each of 4 cells at the first stage is given in Figure 3.25.

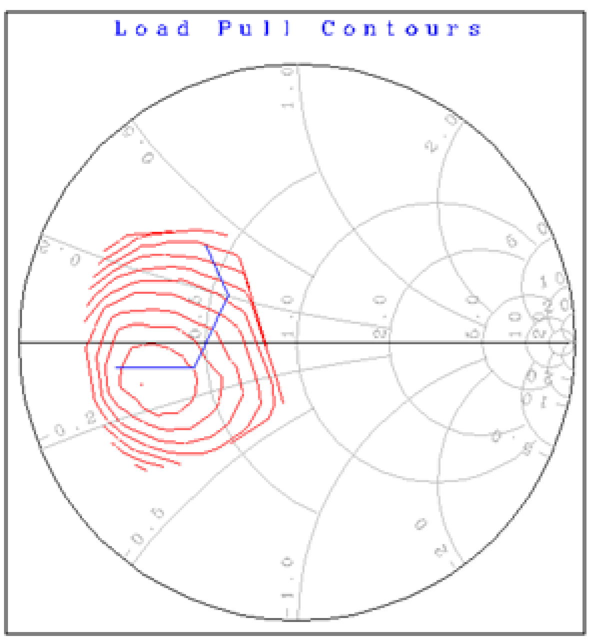


Figure 3.25: The loading shown each cell at the first stage.

3.3.4 Input Matching Network

Input matching network was designed to provide the splitting from the RF input to the 4 cells of 8x150 μm (3 via) transistor. RF matching and combining consisted of low-pass matching sections of series inductors and shunt capacitor. We added stabilization networks connected to the gate of each cell in order to provide low-frequency stability. Additionally, we used a series connection of a parallel RC which provided a further gain reduction at low frequency. Figure 3.26 and 3.27 shows the layout of the input matching network.

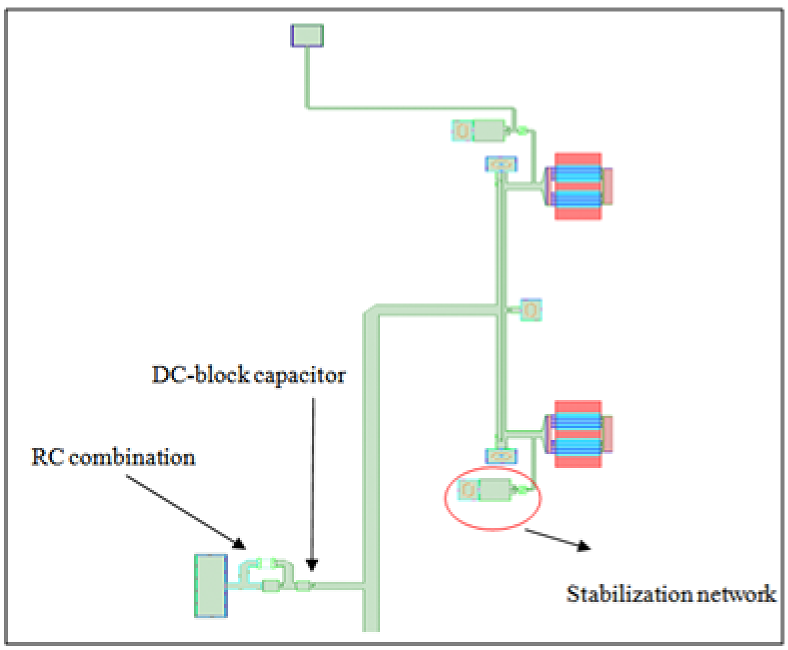


Figure 3.26: Layout of a section of the input matching network.

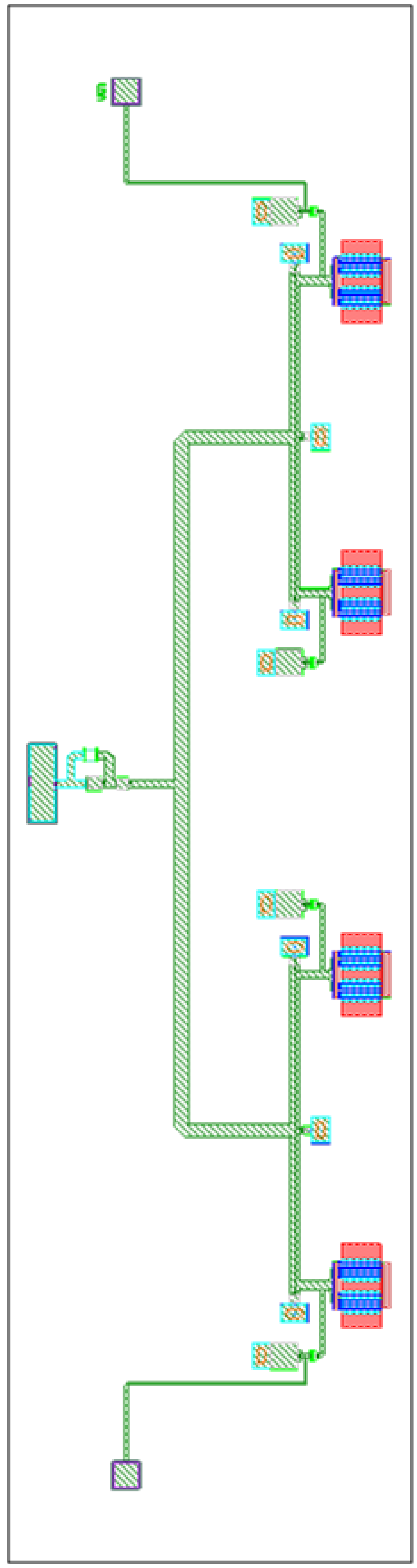


Figure 3.27: Layout of the input matching network.

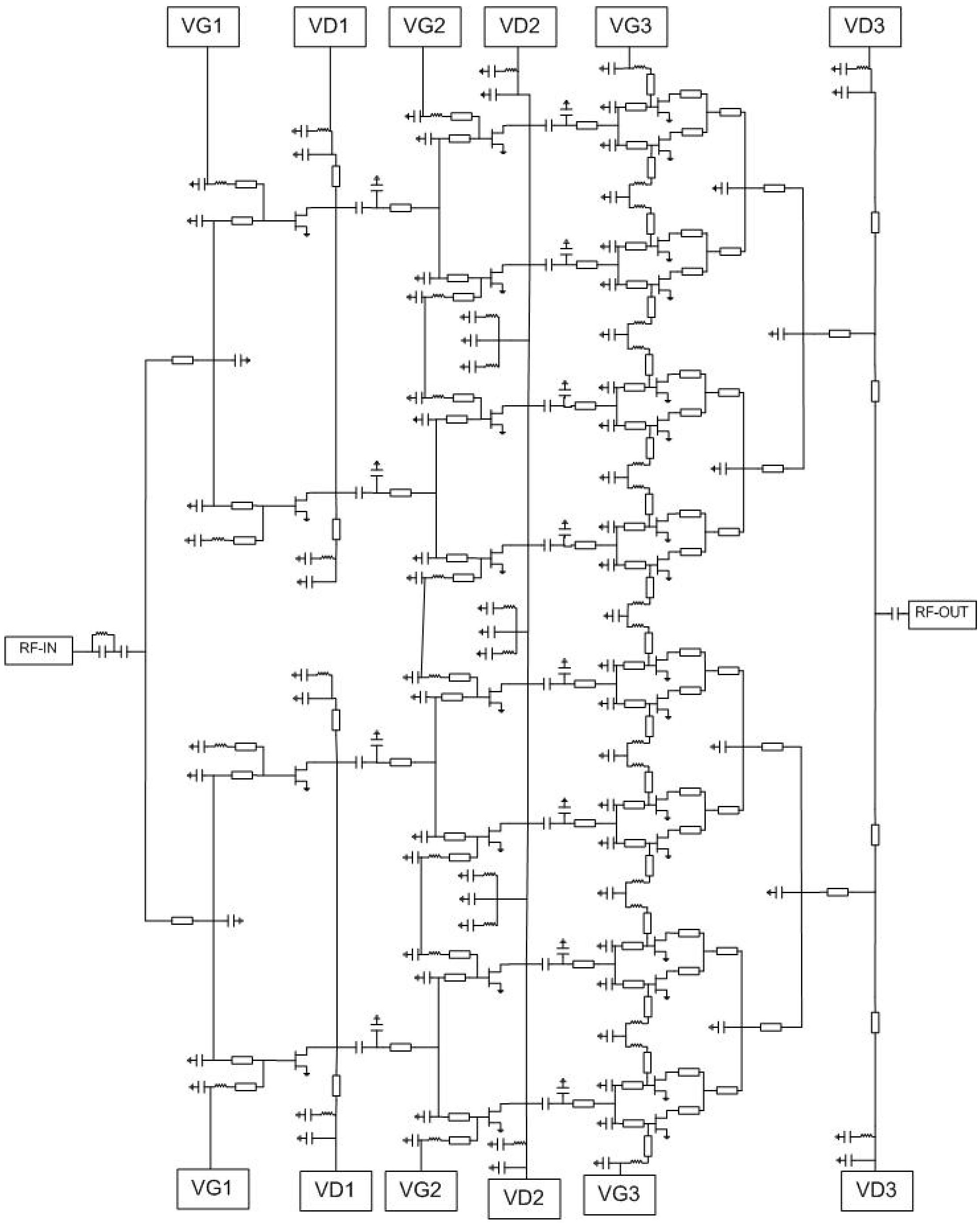


Figure 3.28: Schematic view of the final design.

The input matching network was designed to flatten the gain response and enhance the input return loss of the MMIC. Initially, the schematic design was completed using the passive components of the PP25-21 design kit as it is shown in Figure 3.28. Figure 3.29 shows the small-signal simulation results. We also checked and optimized the effect of the process tolerance on the small-signal simulation result of the MMIC. Figure 3.30 exhibits the process tolerance effect on the small signal performance of MMIC. Considering the process tolerance on the capacitors and the transistors, we designed s_{21} and s_{11} parameters as wide as possible. Although, the required small-signal gain was minimum 22 dB and optimum 24 dB, we designed to achieve higher gain due to possible drop in the gain of the transistors.

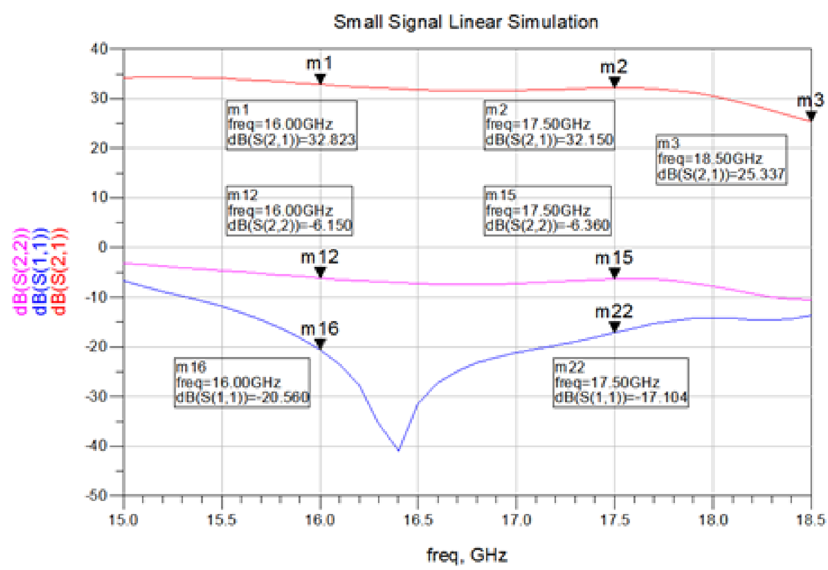


Figure 3.29: Small signal linear simulation results.

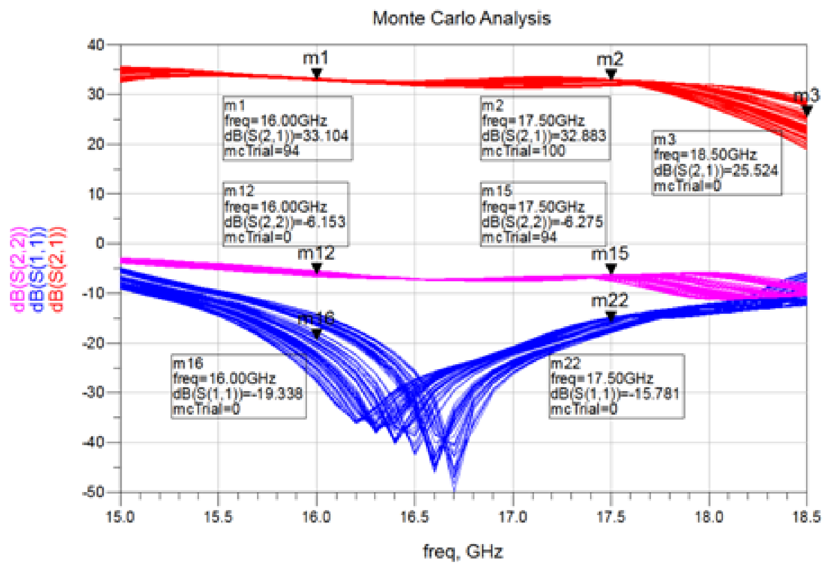


Figure 3.30: S-parameters simulations results considering ±%5 capacitance tolerance.

After the design of all matching networks were optimized and completed, EM simulations were then performed. Figure 3.31 shows the S-parameter performance of MMIC after EM simulations were completed. Figure 3.32 shows the final layout of this work. Final chip dimension is 5.5 x 5.7 mm^2.

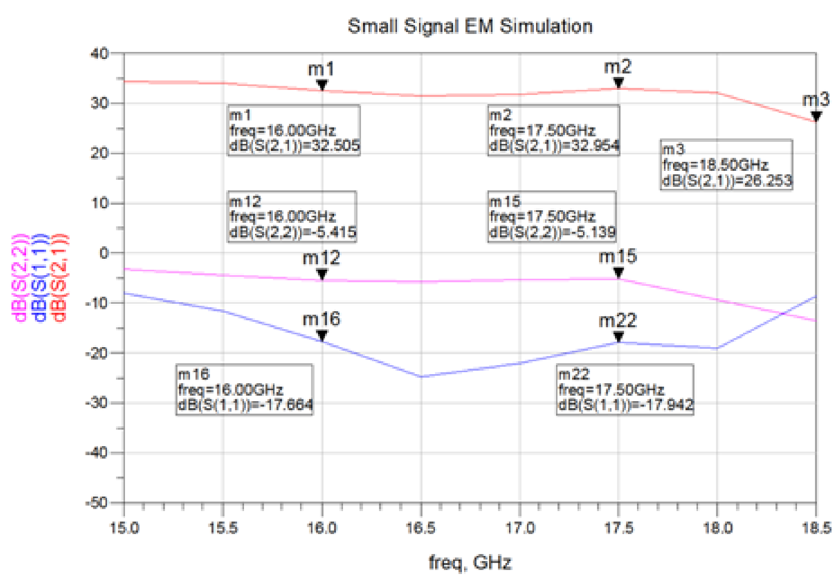


Figure 3.31: Small signal EM simulations.

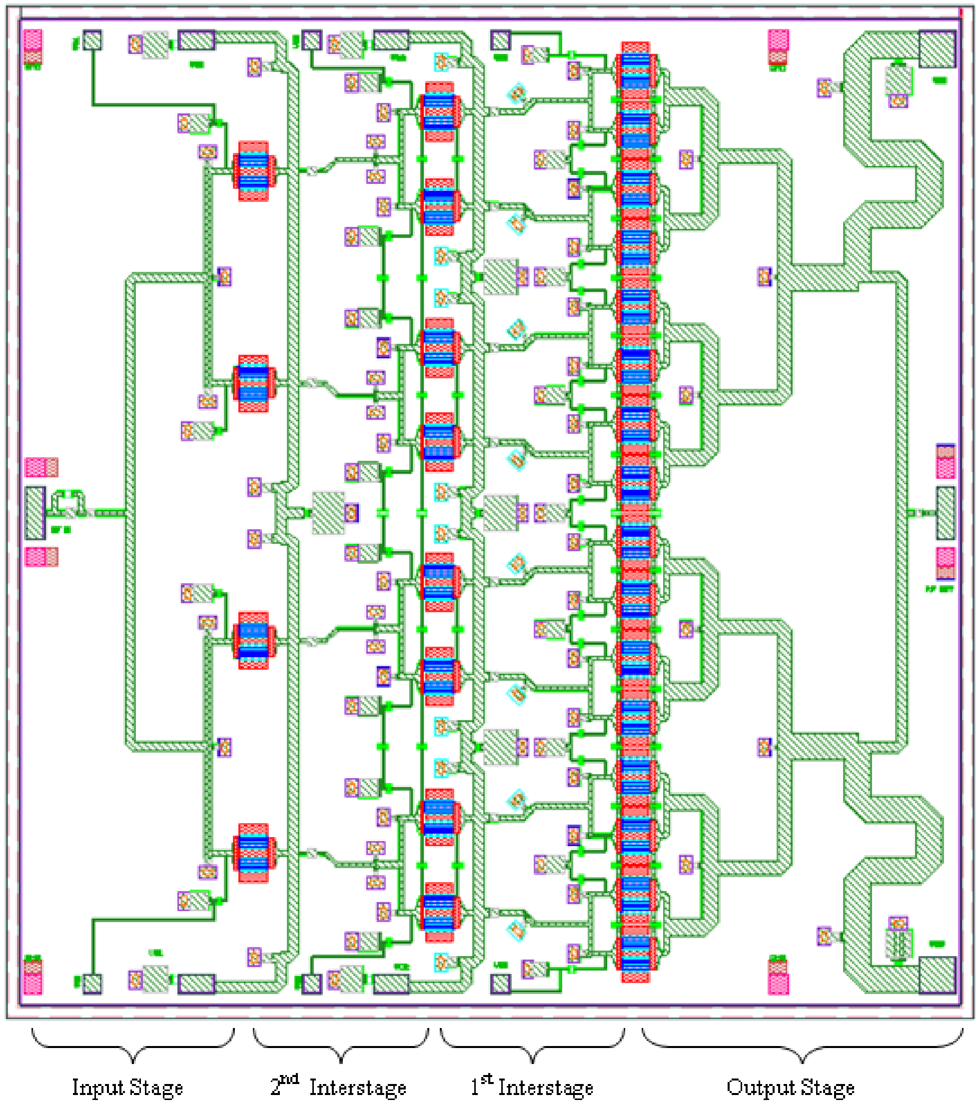


Figure 3.32: Final layout of the entire amplifier.

3.4 Stability

Stability analysis is also another significant part of the design which requires special precautions to avoid unwanted oscillations. From this point of view, we made analyses to ensure the unconditional stability of the design. We can divide these analyses into two major groups: Even-mode stability and odd-mode stability analyses.

3.4.1 Even-Mode Stability Analysis

As it is mentioned before, we put stabilization networks on the drain and gate bias lines to introduce out-of-band loss to the circuit in order to ensure the even-mode stability of the design. From this point of view, we checked not only Rollett stability factor (K) for the entire amplifier but also Nyquist stability criterion for individual stages because in such multistage amplifiers, checking K factor of the overall design is not enough. Therefore, we benefited from Nyquist stability criterion approach at each individual stage. According to Nyquist stability criterion, instabilities can occur if the magnitude (the product of the reflection coefficients at the input and output for each stage) is greater than 1 and encircles $(-1+0j)$ point in counter-clockwise direction [20]. We checked the Nyquist stability criterion at both the gates and drains of the transistors of each stage. Figure 3.33 and 3.34 shows the simulation results of even-mode stability analyses. The Nyquist plots show that the magnitudes of the contours are less than 1 which satisfies the Nyquist stability criterion. The K factor of the entire amplifier also indicates the unconditional stability of the design.

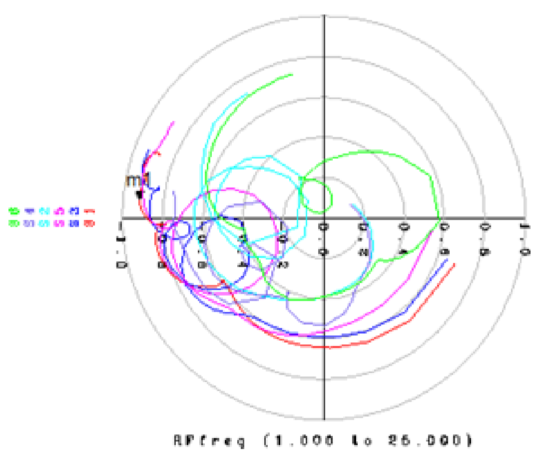


Figure 3.33: Nyquist stability criterion analyses of the design.

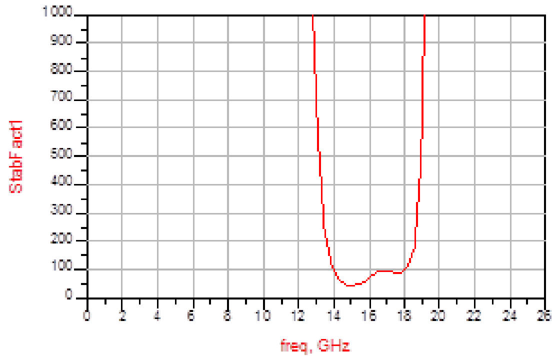


Figure 3.34: The Rollett Stability factor of the design.

3.4.2 Odd-Mode Stability Analysis

Odd-mode instabilities are more likely to occur in the multidevice amplifiers due to the different characteristics of the transistors and the matching technique. In the multidevice amplifiers, the parallel combination of the transistors usually is preferred to satisfy the required output power. However, there might be slight differences in the transistor parameters which result in different power and gain performances for each of these transistors [1]. In addition to that, due to the EM coupling in the matching networks, the symmetry is distorted and this may excite the odd-mode instabilities, as it is discussed in the output matching network chapter. Due to these two main reasons, odd-mode stability analysis requires a special attention for the multistage and multidevice amplifiers like our work.

In the odd-mode analysis of the design, we implemented the practical derivation of Nyquist stability criterion technique for MMIC design described by Ohtomo. This method looks at the open-loop transfer functions of from $G_1(jw)$ to $G_k(jw)$ at the circuit junctions between passive networks and active devices. A necessary and sufficient condition of the stability of the loop is that none of these functions shall encircle the critical point $(1 + 0j)$ clockwise direction [21]. In order to prevent the odd-mode stabilities, we put resistors between the gates and drains of the transistors and the values of these resistors were tuned considering the Nyquist criterion. Figure 3.35 shows the examples of circuit layouts for calculating $G_1(jw)$ and $G_3(jw)$.

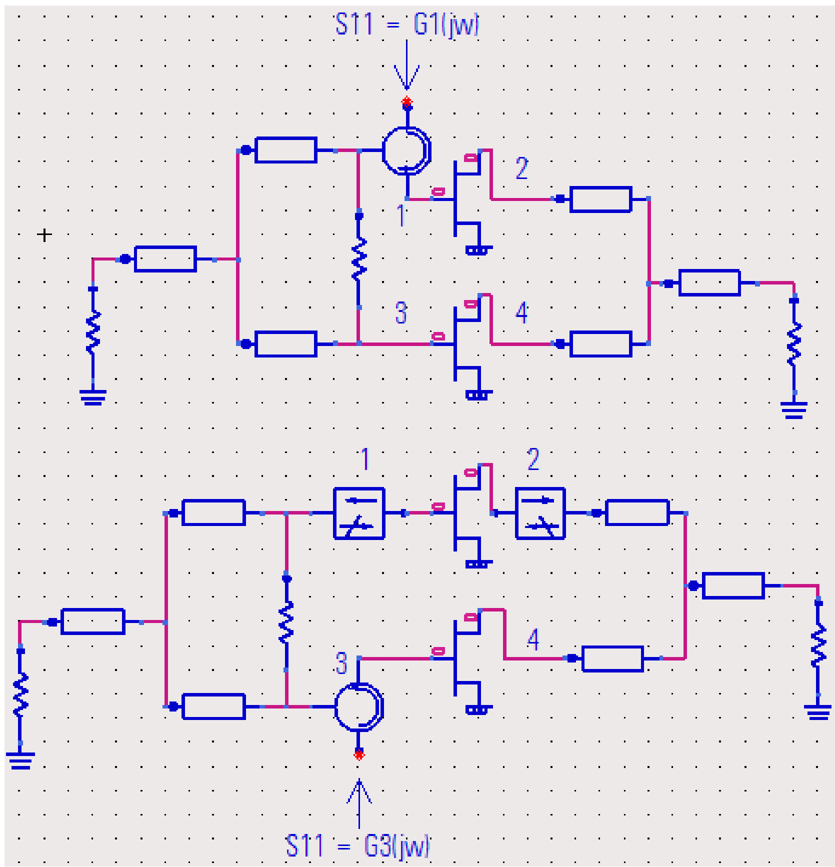


Figure 3.35: Examples of circuit layout of a simple loop [21].

As it is seen on the Figure 3.35, s_{11} looking from the port 1 gives the open loop transfer functions but for $G_k(jw)$ where $k > 1$, ideal isolators are inserted between active devices and passive networks at the port 1 to (k-1). We applied this technique to all the loops in the design and tuned the odd-mode resistors using these simulation results. Figure 3.36 shows the Nyquist plots of open-loop transfer functions of the loops. In the Figure 3.37, the odd-mode resistors between the output cells are shown as an example. As the simulation result shows, odd-mode resistors prevented the possible odd-mode oscillations since there was no encirclement to $(1 + 0j)$ point in the clockwise direction.

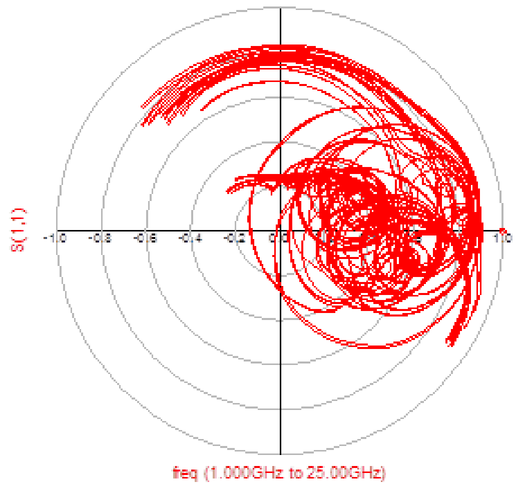


Figure 3.36: Nyquist plots of open-loop transfer functions of the loops.

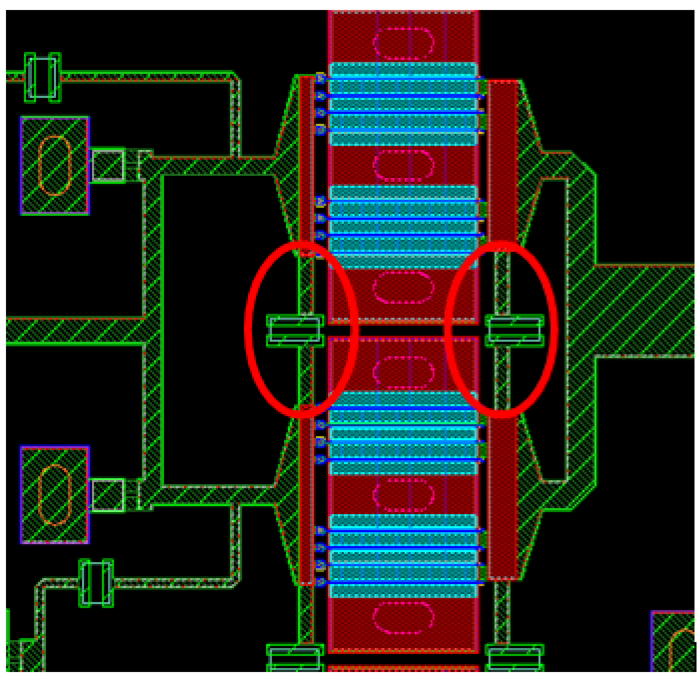


Figure 3.37: Layout of the transistors at the output stage with odd-mode resistors.

Chapter 4

Measurement Results

4.1 Small Signal Measurements

Small signal measurement setup includes DC power supplies, a network analyzer and a probe station. Measurements are performed using GSG (Ground-Signal-Ground) 250 μm probes. MMIC device is mounted on a copper carrier using thermal epoxy (SK70-J202 Diemat). Before the small-signal measurements are carried out, on-wafer calibration is performed in order to arrange the probe tips as the reference plane of the measurement setup. For off-chip decoupling, 100 pF single layer capacitors are used as close as possible to DC pads of the gates. In addition to that, 1 μF surface mount capacitors are added on every DC bias line. In the small-signal measurement, RF bondwires aren't used, although we include the bondwire effect in the design procedure. Therefore, the comparison between measurement and simulation results is made by embedding the RF bondwire effect to the measurement results. DC biasing is provided from double-side of the MMIC using the DC pads on the chip. Figure 4.1 and 4.2 shows the photographs of the fabricated MMIC and S-parameters measurement setup.

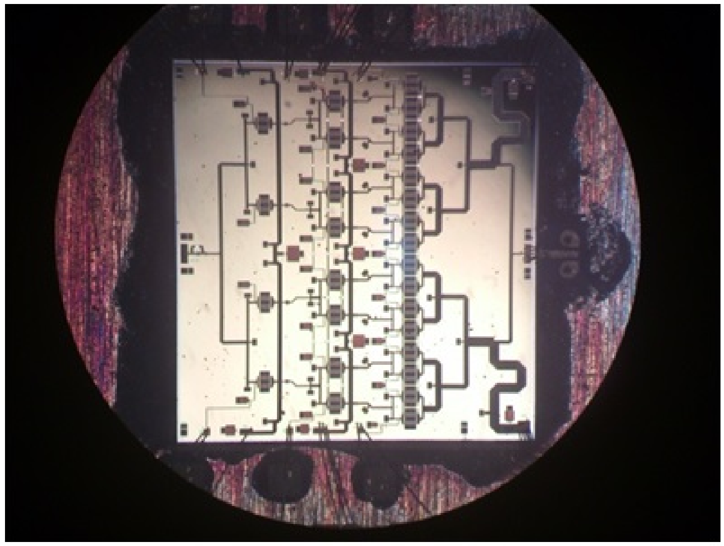


Figure 4.1: Photograph of the fabricated MMIC.

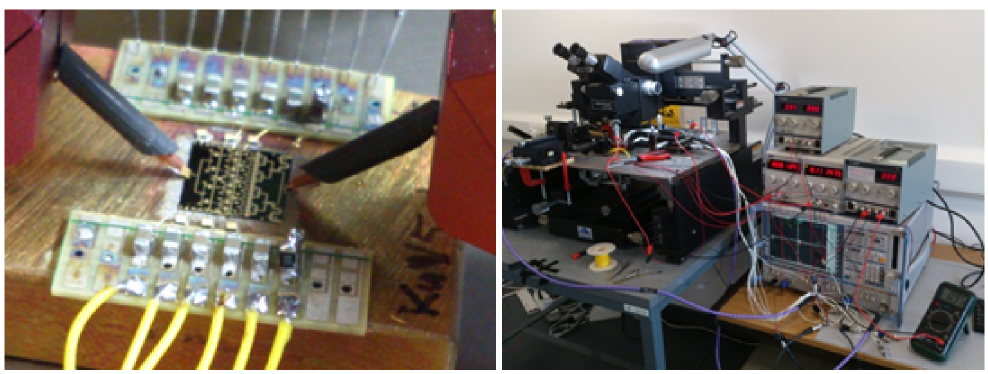


Figure 4.2: Photograph of the S-parameters measurement setup.

Small signal measurement and simulation results are shown in Figure 4.3. Dotted lines show the measurement results. The small signal gain of the amplifier is between 26.34 dB and 24.5 dB in the band of 16-17.5 GHz as required. Within the band, s_{11} is less than -10.5 dB which is worse than the simulation results at 16.5 GHz. s_{22} measurement result is almost same with the simulation and it is less than -7.5 dB in the band of operation.

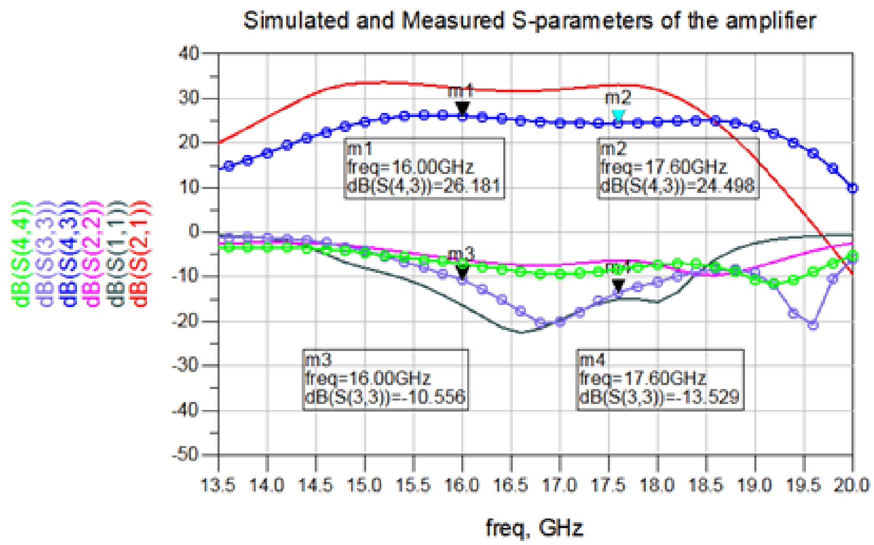


Figure 4.3: S-parameter comparisons between measurement and simulation. Dotted lines show the measurement results.

4.2 Large Signal Measurements

Photograph of our continuous-wave (CW) power measurement setup is given in Figure 4.4. This measurement setup contains 3 Agilent E3634A DC power supplies, E3631A Tripple output DC power supply, E8257D PSG Signal Generator (250 KHz-40 GHz), E4418B EPM Series Powermeter, N8487A Power Sensor (50 MHz-50 GHz), 6-18 GHz Driver amplifier, 20 dB attenuator and Sigma System's Temperature Controller which use nitrogen to control the temperature. We measure MMICs in the connectorized modules instead of using probe stations because we need to arrange the base temperature using the temperature controller. Temperature of the device is monitored using Texas Instrument's LM20 temperature sensor which is placed very close to the chip on the carrier. Figure 4.5 shows the photograph of the chip mounted on the module.

Figure 4.4: Large Signal measurement setup.

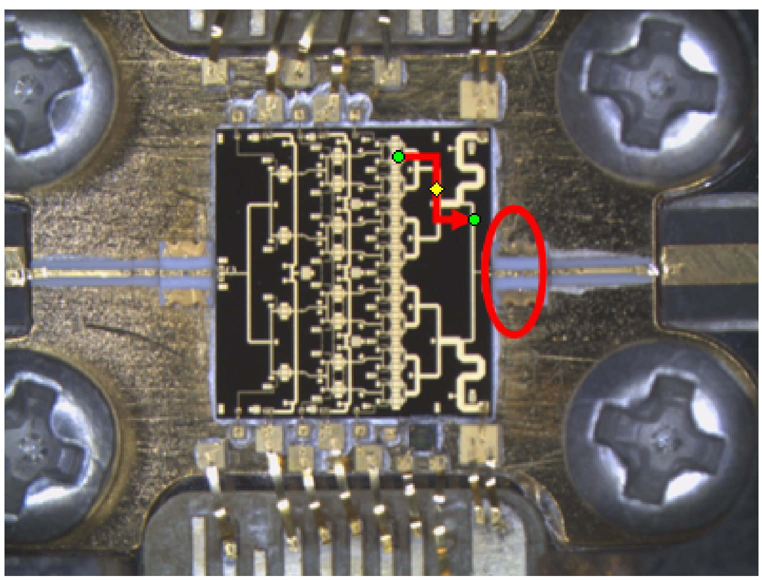
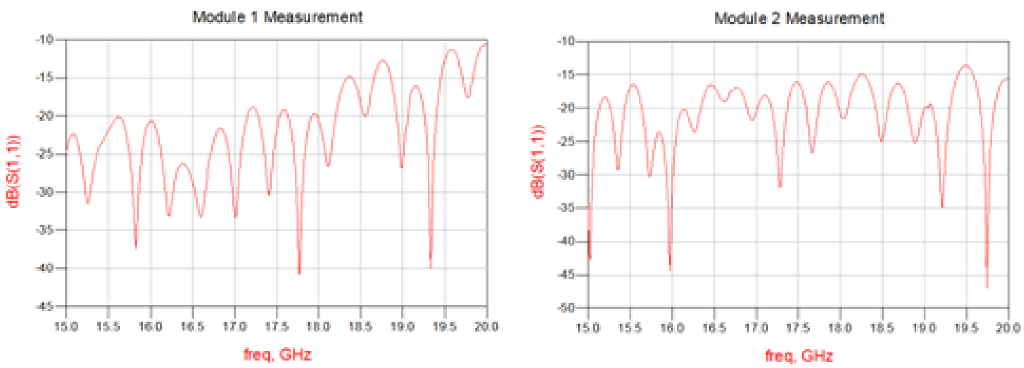


Figure 4.5: Photograph of the MMIC mounted on the carrier. Red circle shows the test point at the RF output. s_{11} measurement is performed looking from this test point in the arrow direction.

In order to make sure that we can show 50 ohm to RF output pad of the MMIC, we put a test point very close to the chip and check the s_{11} performance looking from the test point using 450 μm Cascade probe. Figure 4.6 shows the photograph of the setup where we perform the s_{11} measurement of the module. After 1-port calibration is done, s_{11} measurement is performed from the test point shown in Figure 4.5.

Figure 4.6: Photograph of the setup we perform the s_{11}measurement of the module. Manual tuner is shown in the red circle.

We check s_{11} performance of each module looking from the test point at the output. Figure 4.7 shows the s_{11} measurement results of the module 1 and module 2. As the measurement results indicate that we manage to show 50 ohm better than -20 dB in the module 1 but s_{11} performance of the module 2 is not as good as module 1. Therefore, s_{11} of the module 2 is tuned in order to have better 50 ohm performance using a manual tuner at the output. Tuning process is repeated at 0.25 GHz steps between 15 GHz and 18.5 GHz.



(a) (b)

Figure 4.7: s_{11} measurement of (a) module 1 and (b) module 2 looking from the test point at the output.

Considering 50-ohm arrangements, two modules are measured when the gate bias is -0.9V and drain voltage is 8V. Under this bias condition, we measure the output power level at 3 dB compression, the drain efficiency and the gain when the base temperature is 85°C which is the worst case condition. Figure 4.8, 4.9 and 4.10 show the gain, saturated output power and drain efficiency measurement results, respectively.

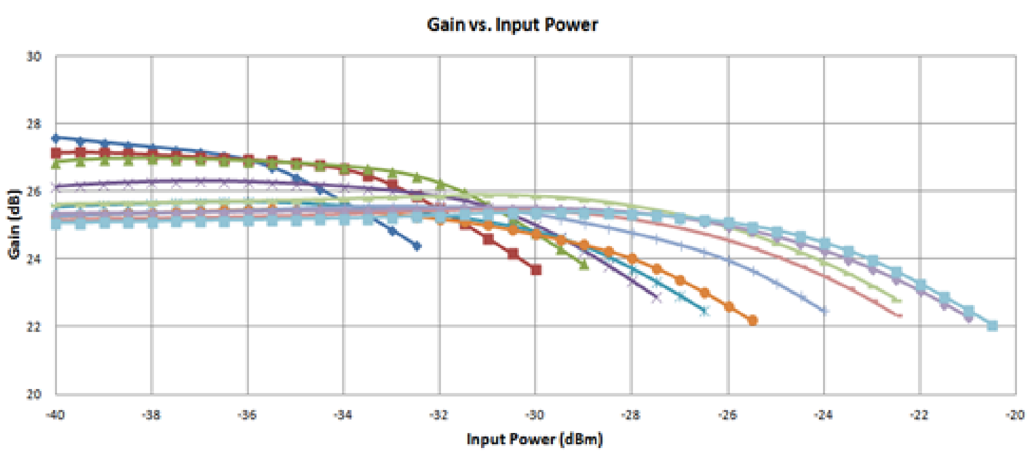


Figure 4.8: Gain vs. input power between 15.5 GHz and 18 GHz.

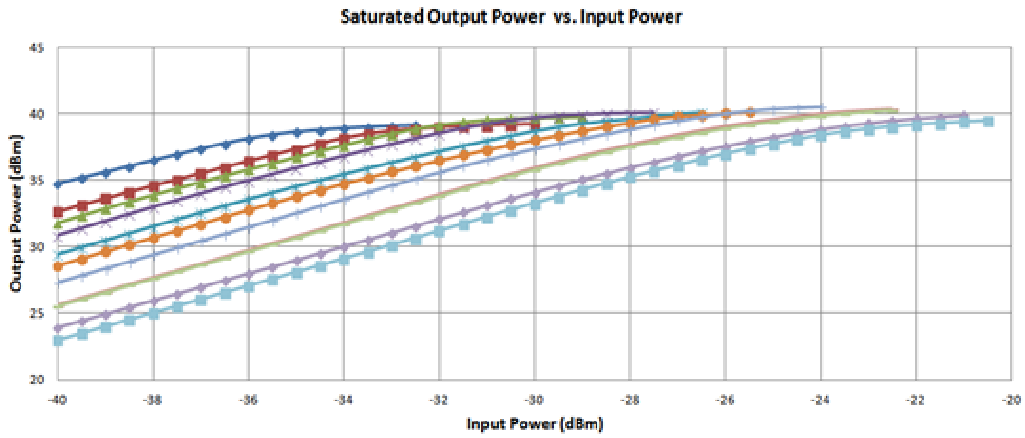


Figure 4.9: Saturated output power vs. input power between 15.5 GHz and 18 GHz.

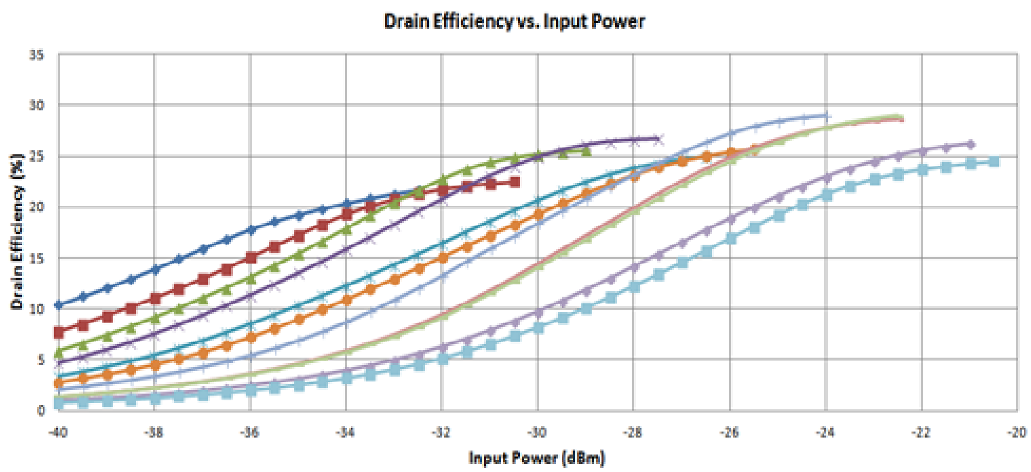


Figure 4.10: Drain efficiency vs. input power between 15.5 GHz and 18 GHz.

Figure 4.11 and 4.12 show the output power and drain efficiency graphs of the module 1 at 3 dB compression when the base temperature is 85°C. Large-signal measurements show that we obtain minimum 40 dBm output power at 3 dB compression when the base temperature is 85°C. The drain efficiency is also measured between %25-30 at the frequency of operation 16-17.5 GHz.

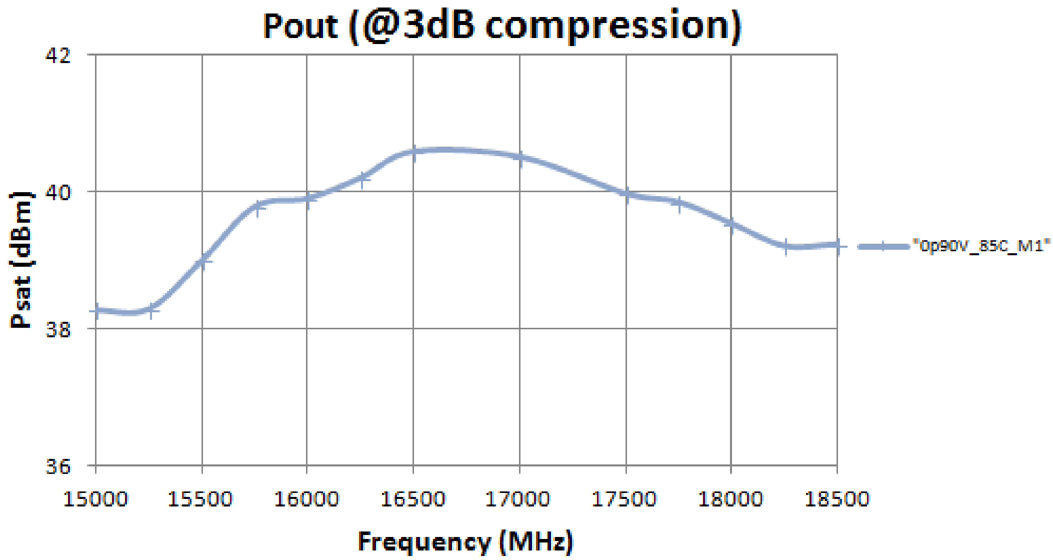


Figure 4.11: Output power at 3 dB compression vs. frequency.

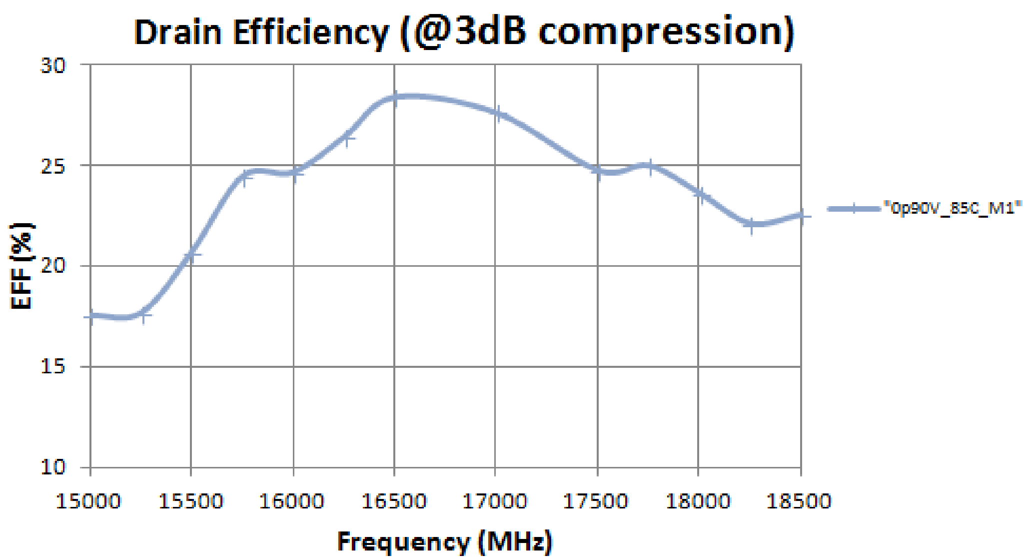


Figure 4.12: Drain efficiency at 3 dB compression vs. frequency.

We also repeat the large signal measurements for Vg=-0.9V and base temperature is 65°C in order to see the improvement in the output power and efficiency. Also, we measure the MMIC for Vg=-1.0V when the base temperature is 85°C. Figure 4.13 and 4.14 show the output power and the drain efficiency performance of the module 1. Highest output power is expected when Vg=-0.9V and the base temperature is 65°C due the increased thermal performance. The worst case result is expected when the gate voltage is -1.0V and the base temperature is 85°C due to both worse thermal performance and lower gate voltage. To sum up, the measurement results are expected for Module 1 MMIC measurement.

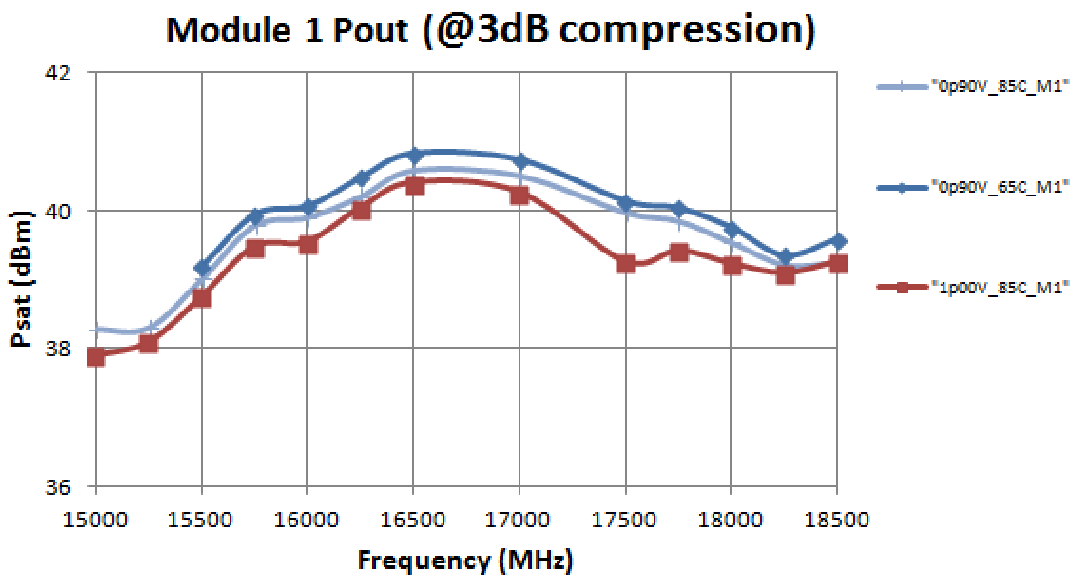


Figure 4.13: Output power at different gate bias and temperature conditions.

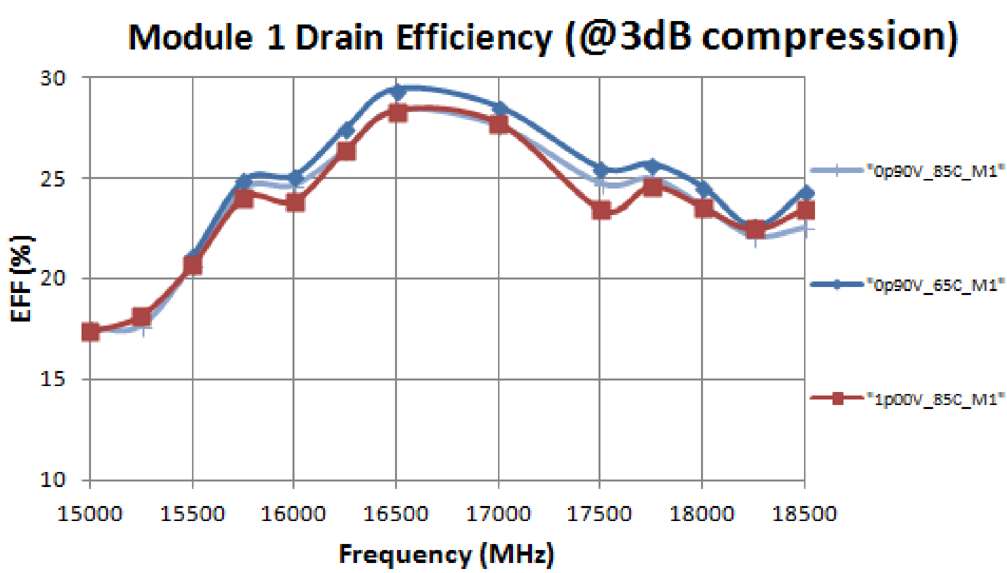


Figure 4.14: Drain efficiency at different gate bias and temperature conditions.

Same measurements are repeated for the second chip to see the process variation effect on the performance of the MMIC which is very important especially for commercial purposes. Figure 4.15 and 4.16 show the measurement results of the module 2 in comparison with module 1 when Vg=-0.9V and the base temperature is 85°C.

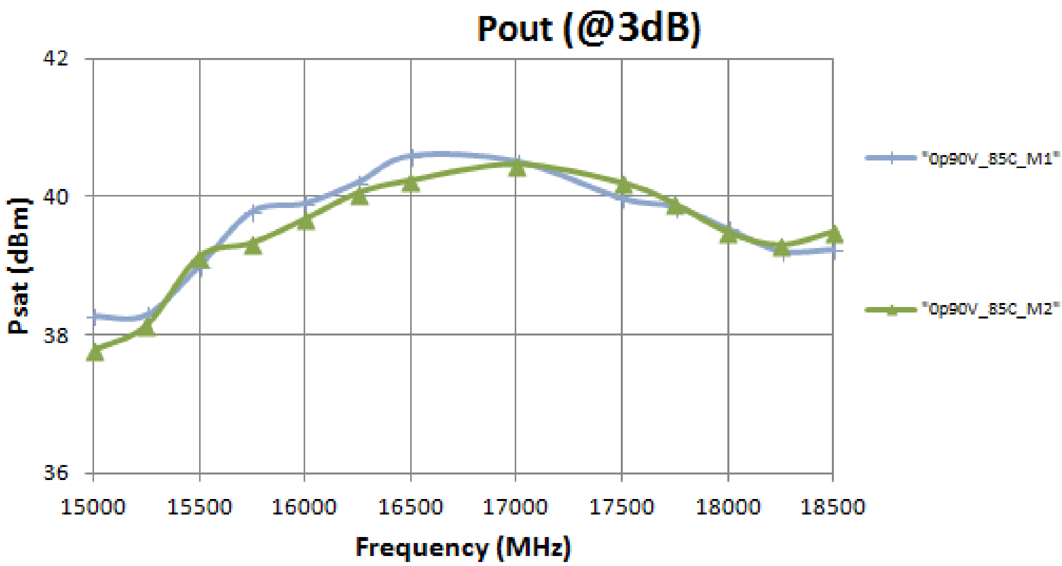


Figure 4.15: Output power vs. frequency graph of Module 1-2.

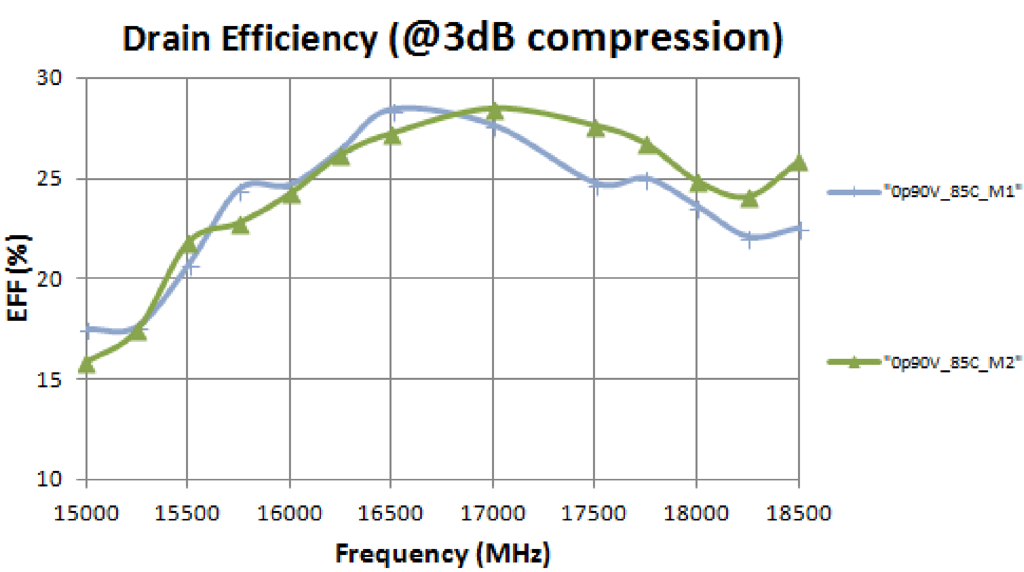


Figure 4.16: Drain efficiency vs. frequency graph of Module.

As it can be seen on the graphs above, both MMICs exhibits similar output power and efficiency performances. The only minor difference between them is that 2nd MMIC provides less output power at the beginning of the band which may be caused by the process tolerance effect on the output matching network. However, considering the results of these 2 MMICs it can be said that design requirements are satisfied. When Vg=-0.9V and the base temperature is 85°C which is the worst case condition, we achieve 10-W output power at 3 dB compression for continous-wave (CW) operation and the drain efficiency varies between %25-30. We also have 26.5-24 dB small signal gain within the band which is higher than the design requirement. Figure 4.17 and 4.18 summarize the output power and the drain efficiency measurements of both MMICs.

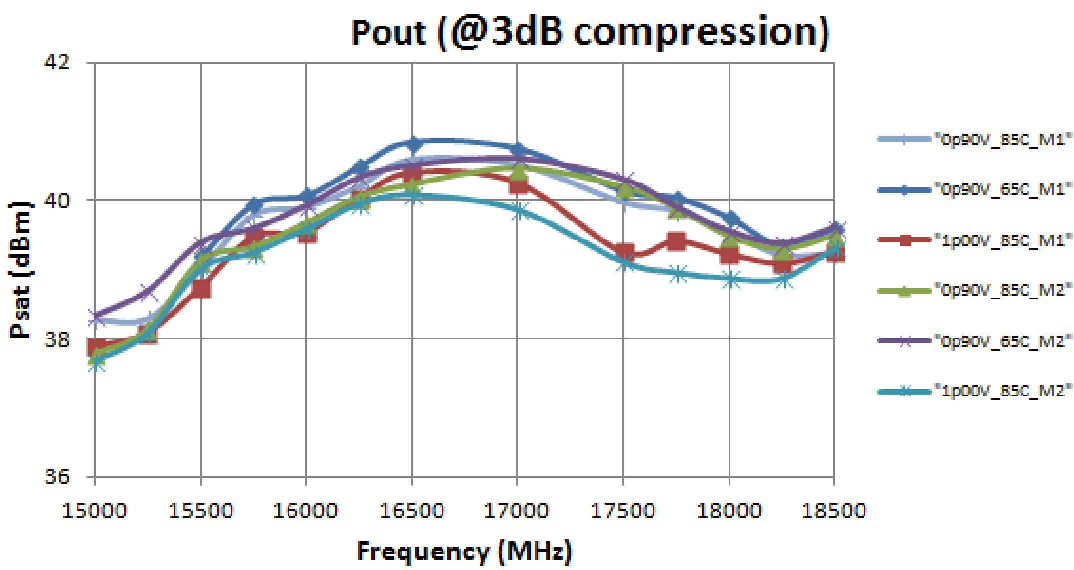


Figure 4.17: Output power vs. frequency graph of Module 1-2 for 3 different bias and base temperature conditions.

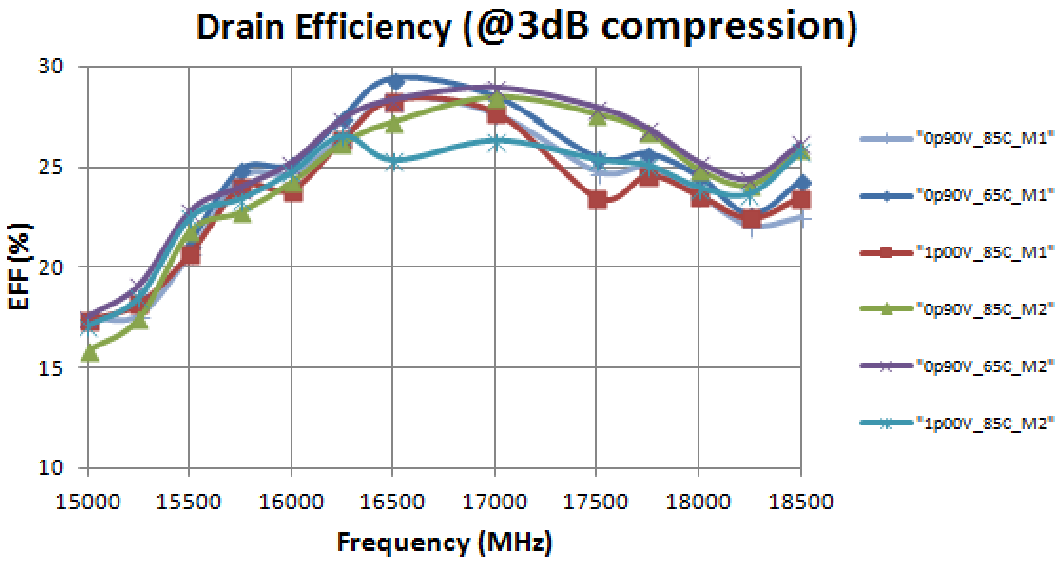


Figure 4.18: Drain efficiency vs. frequency graph of Module 1-2 for 3 different bias and base temperature conditions.

If these results are compared with one of the most common used Ku-band HPA GaAs MMICs in the market, the importance of the output power performance of our design can be realized. MA-COM's MMIC XP5024 that is designed for 14.5-17 GHz provides 17 dB small signal gain at ambient temperature and when the duty cycle is %1 with 1 msec period, it can provide 40 dBm (10-Watt) output power [22]. However, the measurements under continuous-wave mode operation show that it can only provide 37.8 dBm (6-Watt) when the base temperature is 85°C. It means that when the base temperature is 85°C under CW-mode operation, two XP5024 MMICs must be combined in order to obtain 10-Watt output power. Consequently, XP5024 offers less power and gain at 16-17.5 GHz in comparison with our design.

As the other significant comparison between our design and XP5024, we compared the continuous wave mode output power over the chip area value of MMICs with each other. Since it is a power-based comparison, we normalized the x-dimension of our chip because we provided 26 dB small-signal gain whereas XP5024 offers 17 dB. Therefore, we obtained an approximate x-dimension size for our design in order to achieve 17 dB small-signal gain instead of 26 dB for a reasonable comparison of power densities of MMICs. Considering this fact, our MMIC dimensions would be approximately 3.67x5.7 mm^2 whereas the dimensions of XP5024 are 4x4.2 mm^2. Considering these areas, at 85°C base temperature and under continuous-wave operation, our MMIC offers 10W/20.919 mm^2 = 0.478 W/mm^2. On the other hand, MA-COM offers 6W/16.8mm^2 = 0.357 W/mm^2. As it can be seen in this comparison, our design offers higher output power density at 85°C base temperature under continuous-wave mode.

Considering both output power and output power density comparisons, our design provides considerable advantages to a module designer. First of all, in order to achieve 10-W continuous-wave output power, two XP5024 MMICs must be combined. However, a single our MMIC design can provide 10-W power which implies less cost. Especially, for high volume productions it provides an important saving. In addition to that, combining two MMICs increases the design complexity. From this point of view, our design is also more preferable than XP5024.

Chapter 5

Conclusion and Future Work

In this work, we aim to design and fabricate a three-stage 16-17.5 GHz MMIC high power amplifier using WIN Semiconductor's (Taiwan) 0.25 μm gate-length AlGaAs/InGaAs/GaAs pHEMT process (PP-2521). In the design, load-pull and small signal measurements are used instead of the model of the design kit due to the reliability concerns. After the determination of the process, the size of the transistor at the output stage is decided according to the gain, output power and the chip size specifications. The challenging part of the design is to achieve 10-W under continuous-wave operation when the base temperature is 85°C in the band of 16-17.5 GHz. Considering the load-pull measurements of the individual transistors, we decide to combine 16 cells of 8x150 μm (3 via) transistor at the output stage in the common-source configuration in order to achieve 10-W output power at 3 dB compression. Combining the transistors at the output stage makes the output matching harder due to the lower optimum impedance. Therefore, we use the cluster matching technique. In this technique, it is possible to match the device over wide bandwidth due to the intermediate impedance levels and this technique also offers efficient power combining due to in-phase feeding the device. After completing the output matching network, we decide the transistor size of the cells at the driver stage. The total gate periphery of the driver stage is also critical since the driver stage must provide enough power to the output stage to drive it into the 3 dB compression. Considering the gain and efficiency specifications, optimum selection is required for selection of the transistor size of the driver stage. In this design, we decide to use 8 cells of 8x150 μm transistor which makes the driver ratio 1:2. Third stage is added to satisfy the gain requirements which is minimum 22 dB in small-signal. We optimize the third stage for the gain flatness specifications. After the finalization of the MMIC design, the overall MMIC size is 5.5 x 5.7 mm^2.

The designed power amplifier is fabricated at WIN Semiconductor's foundry and both small-signal and large signal measurements are performed on the fabricated MMIC. In small-signal measurements, we obtain 26-24.5 dB within the band. In large-signal measurements, we achieve minimum 40 dBm (10-W) at 3 dB compression for continuous-wave operation when the base temperature is 85°C. The drain efficiency is measured between %25-30 within the band. We repeat the measurements for 2nd MMIC in order to see the process variation effect and we obtain similar output power and efficiency results which show that the extra effort in the design phase worked. We also perform the load-pull measurements for the MMIC circuit using a manual tuner at the output and try to enhance the power within the band. The maximum power that can be obtained changing the manual tuner is 40.5 dBm and %30 drain efficiency. When the manual tuner arrangements are used in the simulation in order to see the optimum load that should be shown to the transistors, it is realized that output matching must be slightly shifted to the maximum efficiency contours from the maximum power load. The reason behind this shift is to enhance the thermal performance by increasing the efficiency because enhanced thermal performance also helps to increase the output power performance.

For future work, we can change the output matching network considering the load-pull measurement of the fabricated MMIC at the 2nd iteration. By using this new optimum load, output power can be easily enhanced at 16 GHz. In addition to that, for 2nd iteration, we can use 8x175 μm transistors at the output stage by sacrificing the gain because the small-signal measurements show that we have enough margin for the gain specifications which is minimum 22 dB.

Bibliography

[1] I. J. Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers*, 1st ed. Wiley Inc, 2009.

[2] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kennington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. Sokal, "RF and Microwave Power Amplifiers and Transmitter Technologies Part 1," *High Frequency Electronics*, pp. 24 – 26, 2003.

[3] T. Mimura, "The Early History of the High Electron Mobility Transistor (HEMT)," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, no. 3, 2002.

[4] L. Aucoin, "HEMTs and pHEMTs," 1991.

[5] D. Hadziabdic and V. Krozer, "Power Amplifier Technology at Microwave and Milimeter-Wave Frequencies Overview," in *Microwave Conference (GeMIC)*, 2008.

[6] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, 1st ed. Wiley Inc, 2009.

[7] D. Pavlidis, "HBT vs. PHEMT vs. MESFET: What's best and why," *Compound Semicond.*, vol. 5, no. 5, pp. 56 – 59, 1999.

[8] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN-GaN HFET with a field modulating plate," *IEEE Electron Device Letter*, vol. 24, no. 5, pp. 289 – 291, 2003.

[9] K. Joshin, T. Kikkawa, H. Hayashi, S. Yokogawa, M. Yokoyama, N. Adachi, and M. Takikawa, “A 174 W high-efficiency GaN HEMT power amplifier for W-CDMA base station applications ,” *IEDM Tech. Dig.*, pp. 983 – 985, 2003.

[10] W. Johnson, L. Piner, A. Vescan, R. Therrien, P. Rajagopal, J. C. Roberts, J. D. Brown, S. Singhal, and K. Linthicum, “12 W/mm AlGaN-GaN HFETs on silicon substrates,” *IEEE Electron Device Letter*, vol. 25, no. 7, pp. 459 – 461, 2004.

[11] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Charvakar, T. Wisleder, U. K. Mishra, and P. Parikh, “12 W/mm AlGaN-GaN HFETs on silicon substrates,” *IEEE Electron Device Letter*, vol. 25, no. 3, pp. 117 – 119, 2004.

[12] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, “12 W/mm AlGaN-GaN HFETs on silicon substrates,” *IEEE Trans. on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1764 – 1783, 2012.

[13] U. K. Mishra, P. Parikh, and Y. F. Wu, “AlGaN/GaN HEMTs: An overview of device operation and applications.”

[14] T. Edwards, “MMICs: state of the industry in 2013 and future prospects,” *Semiconductor Today*, pp. 94–95, 2013.

[15] F. Wang, “Design and analysis of high-efficiency l-band power amplifiers,” Ph.D. dissertation, California Institute of Technology, 2006.

[16] J. L. B. Walker, *Handbook of RF and Microwave Power Amplifiers*, 1st ed. Cambridge University Press, 2012.

[17] D. M. Pozar, *Microwave Engineering*, 3rd ed. Wiley Inc., 2005.

[18] S. Mons, J. C. Nallatamby, R. Quere, P. Savary, and J. Obregon, “A Unified Approach for the Linear and Nonlinear Stability Analysis of Microwave Circuits Using Commercially Available Tools,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2403 – 2409, 1999.

[19] D. Teeter, A. Platzker, and R. Bourque, "A Compact Network for Eliminating Parametric Oscillations in High Power Amplifiers," *Microwave Symposium Digest*, vol. 3, pp. 967 – 970, 1999.

[20] J. Truxal, *Introductory Systems Engineering*. McGraw Hill, 1972.

[21] M. Ohtomo, "Stability Analysis and Numerical Simulation of Multidevice Amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 41, no. 6/7, pp. 983 – 991, 1993.

[22] *14.5-17 GHz GaAs MMIC Power Amplifier*, MA-COM, Nov. 2010.