ANALOG INTEGRATED CIRCUIT OF A LOW LEVEL HIGH VOLTAGE CURRENT SOURCE WITH CAPACITIVE LOAD COMPENSATION

A THESIS
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
AND THE INSTITUTE OF ENGINEERING AND SCIENCES
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

By
Mustafa Ertuğrul ÖNER
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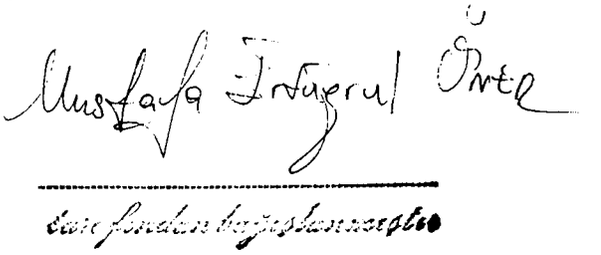

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah Atalar(Supervisor)

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Director of Institute of Engineering and Sciences

ABSTRACT

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Mustafa Ertuğrul Öner
M.S. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Abdullah Atalar
October 1997

Atomic Force Microscopes(AFM) are used to sense the deflections on the crystalline surfaces and convert the information gathered to an image of surface map. In a newly proposed interferometric sensor, cantilevers are micromachined into the shape of interdigitated fingers to form a diffraction grating and the tip displacement is determined by measuring the intensity of diffracted modes. Detection of modes is achieved by means of a photodetector(PD) array mounted just above the cantilevers. For this purpose , a PD array of 2×8 composed of MSM-PDs is designed and manufactured. A p^+/n PD is also designed for testing. In addition, a high voltage low level current source is required to drive the tips of the cantilevers for the purpose of lithography. The current source designed for this purpose can supply 10nA current through the resistive cantilever in spite of an existing capacitance at load. Current source includes an internal capacitive current compensation circuit to fix the current of resistive load at $10nA$. Test of designed circuit is done and prototypes of chip are fabricated using Alcatel Mietec I2T CMOS process. PD array and current source are supposed to be prototypes of the related blocks in AFM.

ÖZET

YÜKTEKÍ KONDANSATÖR AKIMINI TELAFÍ EDEBÍLEN DÜŞÜK SEVÍYE YÜKSEK GERÍLÍM AKIM KAYNAĞI TASARIMI

Mustafa Ertuğrul Öner
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
Tez Yöneticisi: Prof. Dr. Abdullah Atalar
Ekim 1997

Atomik mikroskop, kristallerin yüzey haritalarını elde etmekte kullanılır. Kristallerin yüzey sapmaları mekanik ve optik bir takım düzenekler vasıtasıyla elde edilir ve bu bilgi daha sonra görüntüye dönüştürülür. Yüzey sapmalarını ölçmek için kullanilan ızgaralar lazer ile aydınlatıldığında sapmanın büyüklüğü ile orantılı yoğunlukta ışık modları elde edilir. Bu modları ölçmek için MSM fotodiyot dizgisi içeren bir çip tasarlandı. MSM fotodiyotlar CMOS teknolojisine gösterdikleri uyumdan dolayı seçildi.

Buna ek olarak, ızgaraları sürmek için gereken 10nA'lik akim kaynağı hazırlandı. Akım kaynağı birbirine parallel direnç ve kondansatörden oluşan bir yükü sürebilecek ve direnci içeren koldan 10nA'lik akım geçirebilecek şekilde tasarlandi. Kondansatör içeren kolda yük gerilimindeki değişiklerden dolayı oluşan akım, akım kaynağı içerisinde yapılan düzenlemeler ile telafi edildi. Yüksek gerilim akım kaynağının çipi yapıldı.

ACKNOWLEDGEMENT

I would like to express my gratefulness to Prof. Dr. Abdullah Atalar for his suggestions and guidance throughout the development of this thesis.

I wish to thank A.Suat Ekinci for his invaluable help.

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Special thanks to Suzan and my parents for their encouragement and patience.

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Chapter 1

Introduction

Atomic Force Microscopes (AFM) are devices used commonly to get an image of crystalline surfaces on the atomic level. AFM's are able to measure deflections that are much less than 1 Å. The cantilever with an integrated tip is the main element of those microscopes. Design of cantilevers is an important topic because it determines the sensitivity of the system.

The measure of deflections on atomic level is achieved by means of techniques such as tunneling [1], the optical lever [2], interferometer [3] and piezoresistor [4]. Optical techniques become more and more popular because of their high sensitivity. Schonenberger and Alvarado [5] developed a scheme in which a birefringent prism is used to divide a laser into sensing and reference beam. The prism is placed so that the reference beam is reflected off the cantilever and sensing beam is reflected near the tip. Reflected beams are detected and analyzed by a split photodiode. Rugar et al. [3] developed a deflection sensor based on the interference of light between cleaved end of an optical fiber and the backside of cantilever.

A new interferometric sensor for the AFM where a cantilever is micromachined into the shape of interdigitated fingers to form a diffraction grating is proposed by A.Atalar [6]. This technique requires an illumination source and a standard photodetector. A resolution comparable to other interferometric

sensors can be achieved. In that method, intensity rather than the position of the reflected beam is measured and therefore the problem of aligning an array of photodiodes is eliminated.

When the cantilever is illuminated by a Gaussian beam with diameter of 20μ and a wavelength of $\lambda = 670$nm, the fingers form a phase sensitive diffraction grating and the tip displacement is determined by measuring the intensity of diffracted modes. As deflection increases, the intensity of the reflected beam at 0^{th} mode diminishes and at 1^{st} mode rises. For a deflection of a quarter wavelength , reflected beam at 0^{th} mode is minimum and it is maximum at 1^{st} mode. The cantilever deflection can be determined by either measuring the intensity of the 0^{th} mode, 1^{st} mode or difference between the modes. To detect

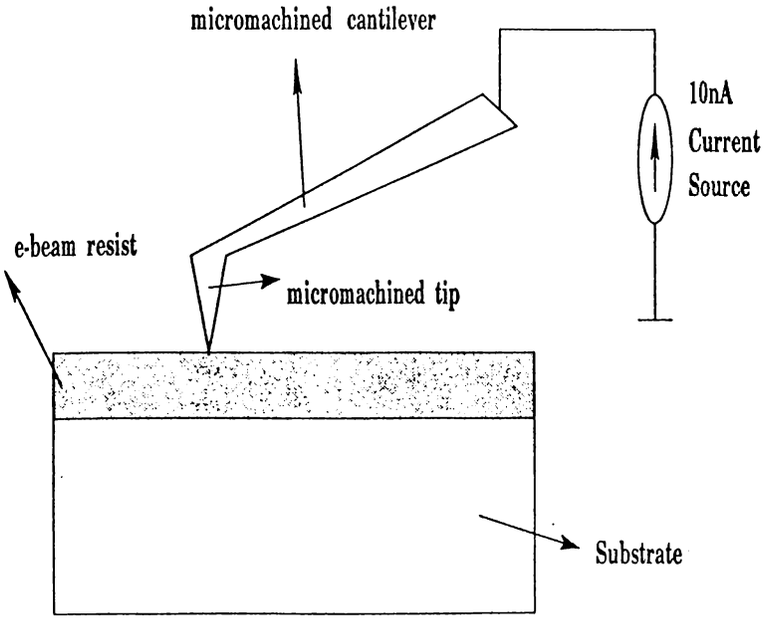

Figure 1.1: Cantilever on Crystal Surface

the intensity of deflected modes, an array of photodetectors placed just above the cantilever tips is required. Metal-Semiconductor-Metal photodetectors are used for this purpose. MSM-PD's have attracted significant interest recently for device applications due to their wide bandwidth, low capacitance, low cost of fabrication, high sensitivity, low dark current and monolithic integrability with high speed electronic and microwave devices [7]. An MSM photodetector array is prepared to measure the intensity of diffracted modes.

The cantilever tips must be driven by an high voltage low level current source for the purpose of lithography [8]. In order to get surface map of crystalls, the substrate surface is first covered by e-beam resist. The scanning tip of the micromachined cantilever expose the e-beam resist by supplying a curent of 10nA as shown in Figure 1.1.

The exposed regions of e-beam resist are developed afterwards by some chemical processes and image information is obtained. The exposure of the e-beam resist could also be achieved by means of a fixed voltage supply. But it is observed that the change in substrate voltage from 40V to 80V make the constant exposure impossible. Figure in 1.2 shows the current of e-beam resist

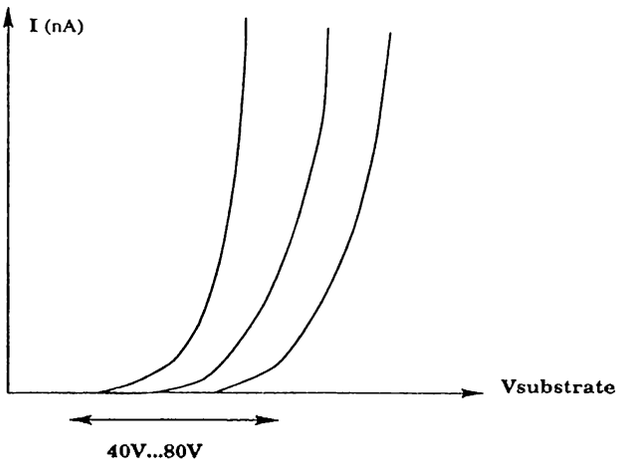

Figure 1.2: Current of e-beam resist vs. substrate voltage

vs. substrate voltage. It is evident from above plot that if cantilever tips are driven by a fixed voltage source then the amount of current through the e-beam resist will change drastically due to varying ON time and constant exposure could not be achieved. The proposed constant current source overcomes this problem and provide constant exposure [9]. The typical level of current is 10nA and required voltage is -100V.

In actual scan of cantilever tips over crystalline surfaces, an inherent capacitance of order $1 - 2$pF will also be present. The current source must have the ability of supplying 10nA current through the resistive cantilever load in spite of the existing capacitance. The resistive load is time varying and is

around $3 - 8G\Omega$ which cause the load capacitance to supply or withdraw current through the resistive branch. 10nA current source must include an internal load capacitive current compensation circuit to fix the current of resistive cantilever load at 10nA.

This thesis includes the design of Load Capacitive Current Compansating Current Source and a Metal-Semiconductor-Metal Photodetector Array, two of the building blocks of AFM.

In Chapter 2, the elements of CMOS High Voltage 10nA Current Source Without Capacitive Current Compensation is presented. A brief discussion on current mirror stages, current amplification and de-amplification , cascode output stages and voltage divider bias circuits is given. The transistor dimensions are calculated for 10nA current source.

In Chapter 3, the performance of the fixed 10nA current source is analyzed. Its output current stability against the changes in output voltage is observed. Simulations for both cases: resistive load only and resistive & capacitive loads are presented.

In Chapter 4, the capacitive current compensating circuit is introduced. The building blocks of that circuit, namely differentiator, buffer, voltage controlled current source and non-inverting amplifier are discussed. Their performance tests are presented. The overall circuit of Low-Level High-Voltage Current Source with Capacitive Load Compensation is given.

In Chapter 5, the operational amplifier which is used in the current source is introduced. Its performance tests on open-loop gain, phase margin, output impedance, CMRR etc. are presented. Transistor values used in design of op amp is given.

In Chapter 6, MSM photodetector structures and their capabilities are discussed.Test results of p^+/n photodiode are given.

In Appendix A, layout of current source building blocks are presented. Overall circuit layout is also added. In Appendix B, photodetector layouts are given. Appendix C inludes the process parameters of transistors. Appendix D shows pin configuration of current source chip.

Chapter 2

Current Supply Building Blocks

2.1 Current Mirror

2.1.1 Introduction

One of the main blocks of the current compensated 10nA current source is the current mirror. There exists many realizations of current mirrors serving for various needs. They might be used to copy a current from any circuit branch. Parallel connection provide the opportunity of generating many exact copies simultaneously. In addition to that, successive connection of complementary current sources allows changing the direction of current.

Figure 2.1 shows simple n-type and p-type current mirror blocks. The n-type block is used for withdrawing current from output node while p-type is used for supplying current.

I_{bias} represent the current to be mirrored with a certain gain. By connecting drain and gate of the M_1 we guarantee that transistor to be in saturation. Then,

governing equation of transistor current in saturation region is:

$$I_{bias} = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_1(V_{GS1} - V_{Tn})^2(1 + \lambda V_{DS1}) \tag{2.1}$$

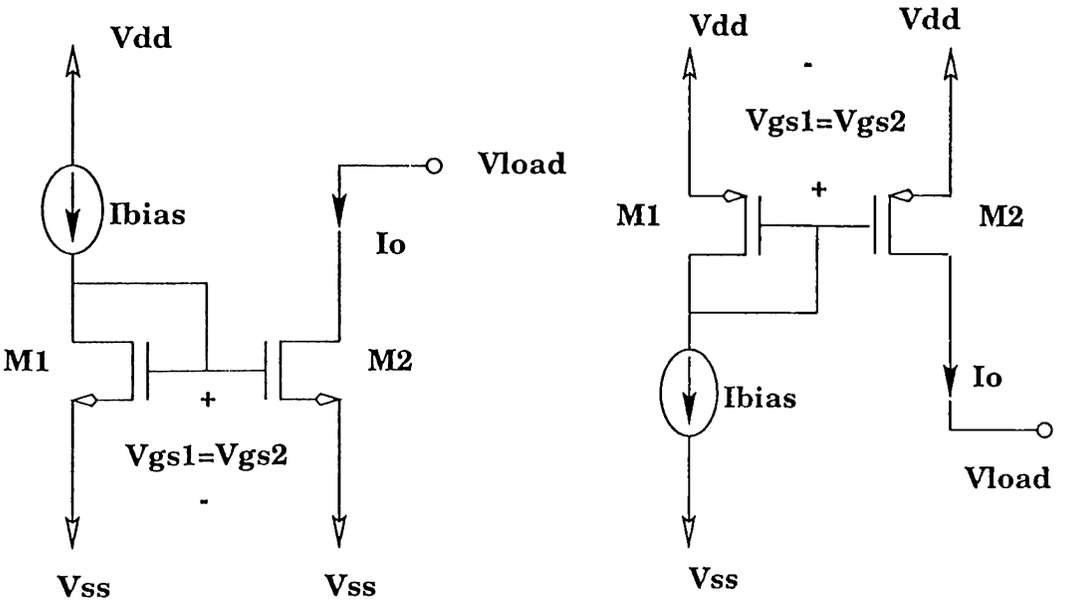

Figure 2.1: N-type and P-type current mirror blocks

Bias current enforces gate-to-source voltage of M_1 and M_2 to reach a certain value. Assuming M_2 also in saturation, the same bias current will flow through the drain of M_2, provided M_1 and M_2 are same size transistors. If the size of the transistors are different, drain current of M_2 will change in proportion to (W/L) ratios of M_1 and M_2. The value of V_{GS1} is determined by (W/L) ratio of first transistor. If the output voltage of current source is a low value, then it would be better to set gate-to-source voltage as low as possible to make M_2 enter saturation more easily.

Output current I_0 set by M_2 is given to be:

$$I_0 = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_2(V_{GS2} - V_{Tn})^2(1 + \lambda V_{DS2}) \tag{2.2}$$

Equations 2.1 and 2.2 yield:

$$\frac{I_0}{I_{bias}} = \frac{(W/L)_2}{(W/L)_1}\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \tag{2.3}$$

If there exist no loading effect on output transistor M_2, drain to source voltages V_{DS1} and V_{DS2} would become equal. Even if this is not true, very small values of channel-length-modulation parameter λ guarantees that:

$$\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \approx 1 \tag{2.4}$$

Then we can safely use current mirror gain equation:

$$I_0 = I_{bias}\frac{(W/L)_2}{(W/L)_1} \tag{2.5}$$

If we call current gain factor to be β, then:

$$\beta = \frac{(W/L)_2}{(W/L)_1} \tag{2.6}$$

and

$$I_0 = \beta I_{bias} \tag{2.7}$$

2.1.2 Current Amplification/Attenuation

Appropriately choosing the gain factor β, current amplification and attenuation can be achieved. Successive use of mirror blocks for this purpose are shown in Figure 2.2.

Let's call:

$$\beta_1 = \frac{(W/L)_{1b}}{(W/L)_{1a}}, \beta_2 = \frac{(W/L)_{2b}}{(W/L)_{2a}}, ..., \beta_n = \frac{(W/L)_{nb}}{(W/L)_{na}}. \tag{2.8}$$

The bias current mirrored through each current mirror block with a certain gain. When current reach to the last stage:

$$I_0 = \beta_3\beta_2\beta_1 I_{bias} \tag{2.9}$$

If n of those mirror blocks are cascaded:

$$I_0 = \beta_n\beta_{n-1}....\beta_3\beta_2\beta_1 I_{bias} \tag{2.10}$$

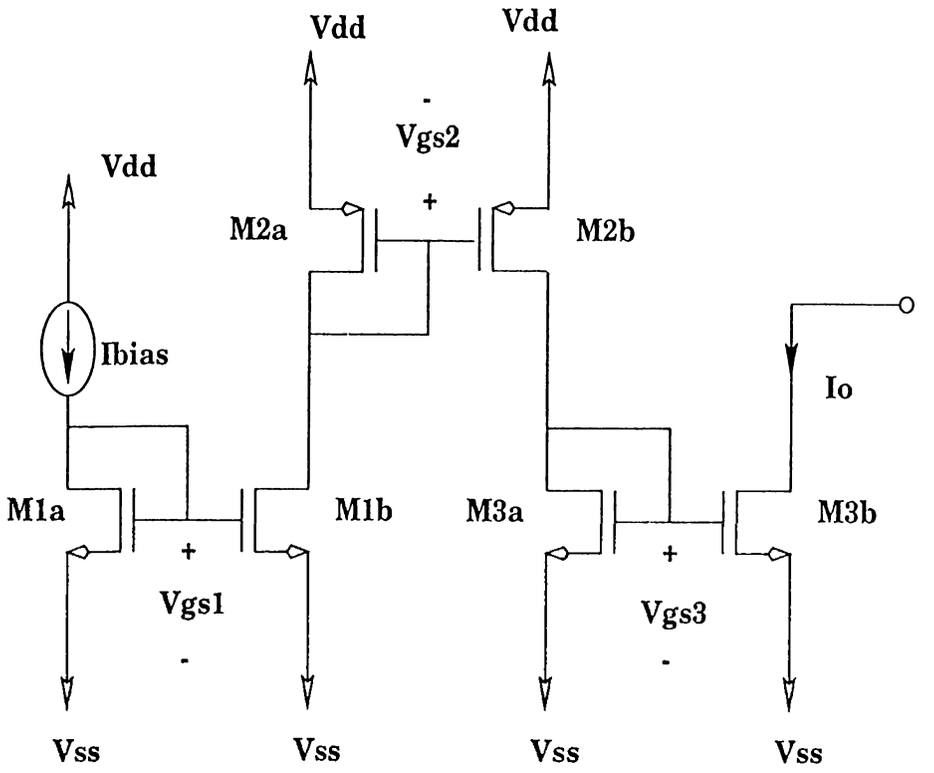

Figure 2.2: Cascaded current mirrors for current amplification and attenuation

If multiplication of β_i's is greater than one, cascaded mirror stage functions as a current amplifier and vice versa.

2.1.3 Saturation Condition

In cascaded use of current mirrors, one must be careful in keeping the transistors M_{ib} in saturation. Actually, if the current gain of each mirror block is grater than one, then there exist an upper bound for the bias current in terms of supply voltages and mirror gains. This upper bound constraint weakens in current attenuation but still exist.

For the sake of convinience, let:

$$K_i = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_i \tag{2.11}$$

Then

$$\beta_i = \frac{K_{ib}}{K_{ia}} \tag{2.12}$$

From Equation 2.1

$$V_{GS1} = \sqrt{\frac{I_{bias}}{K_{1a}}} + V_{Tn} \tag{2.13}$$

The drain current of M_{1b} becomes

$$I_2 = \frac{K_{1b}}{K_{1a}} I_{bias} \tag{2.14}$$

and enforce V_{GS2} to be

$$V_{GS2} = \sqrt{\frac{K_{1b}/K_{1a} I_{bias}}{K_{2a}}} + V_{Tp} \tag{2.15}$$

To get M_{1b} in saturation we must have

$$V_{DS1b} \geq V_{GS1} - V_{Tn} \tag{2.16}$$

but also

$$V_{DS1b} = V_{DD} - V_{SS} - |V_{GS2}|. \tag{2.17}$$

Combining equations 2.15, 2.16 and 2.17

$$V_{DD} - V_{SS} - |V_{Tp}| - \sqrt{\frac{(K_{1b}/K_{2a}) I_{bias}}{K_{1a}}} \geq \sqrt{\frac{I_{bias}}{K_{1a}}} \tag{2.18}$$

or

$$I_{bias} \leq K_{1a} [\frac{V_{DD} - V_{SS} - V_{Tp}}{1 + \sqrt{(K_{1b}/K_{2a})}}]^2 \tag{2.19}$$

Above statement gives the condition of keeping M_{1b} in saturation. We will follow a similar procedure to find the saturation condition of M_{ib}'s. To make M_{2b} enter into saturation

$$|V_{DS2b}| \geq |V_{GS2}| - |V_{Tp}| \tag{2.20}$$

If we assume $|V_{Tp}| = V_{Tn} = V_T$ referring to process parameters given in Appendix C then

$$|V_{GS3}| = \sqrt{\frac{K_{1b}K_{2b}}{K_{1a}K_{2a}K_{3a}} I_{bias}} + V_T \tag{2.21}$$

Substituting Equation 2.21 into 2.20 and using $|V_{DS2b}| = V_{DD} - V_{SS} - V_{GS3}$

$$V_{DD} - V_{SS} - |V_{GS3}| \geq |V_{GS2}| - V_T \tag{2.22}$$

or

$$V_{DD} - V_{SS} - V_T - \sqrt{\frac{K_{1b}K_{2b}}{K_{1a}K_{2a}K_{3a}} I_{bias}} \geq \sqrt{\frac{K_{1b}K_{2b}}{K_{1a}} I_{bias}} \tag{2.23}$$

Then the upper bound on I_{bias} is found to be:

$$I_{bias} \leq \frac{K_{1a}K_{2a}}{K_{1b}} [\frac{V_{DD} - V_{SS} - V_T}{1 + \sqrt{(K_{2b}/K_{3a})}}]^2 \tag{2.24}$$

We may generalize this result to n-mirror blocks. To keep M_{nb} in saturation, upper bound on I_{bias} is as follows:

$$I_{bias} \leq \frac{K_{1a}K_{2a}K_{3a} \cdots K_{na}}{K_{1b}K_{2b}K_{3b} \cdots K_{(n-1)b}} [\frac{V_{DD} - V_{SS} - V_T}{1 + \sqrt{(K_{na}/K_{(n+1)a})}}]^2 \tag{2.25}$$

Using Equations 2.12 and 2.25

$$I_{bias} \leq \frac{K_{na}}{\prod_{i=1}^{n-1} \beta_i} [\frac{V_{DD} - V_{SS} - V_T}{1 + \sqrt{(K_{na}/K_{(n+1)a})}}]^2 \tag{2.26}$$

The saturation condition of the last transistor of cascaded stages depends mainly on the output node voltage. If this voltage is high in magnitude compared to the available supply voltages, it would be difficult to keep output transistor in saturation.

Saturation of M_{ib}'s will not be a direct problem because we will use cascaded current mirror stages for current de-amplification by setting $\beta < 1$. However the saturation condition have to be kept in mind for a proper design.

2.2 10nA Current Source

The main difficulty of the design of the 10nA current source is the 100V supply range. Actually, we are required to design the current source using +5V and −95V as supply voltages. This current source will drive the cantilevers in AFM and the supply voltages are chosen for this requirement.

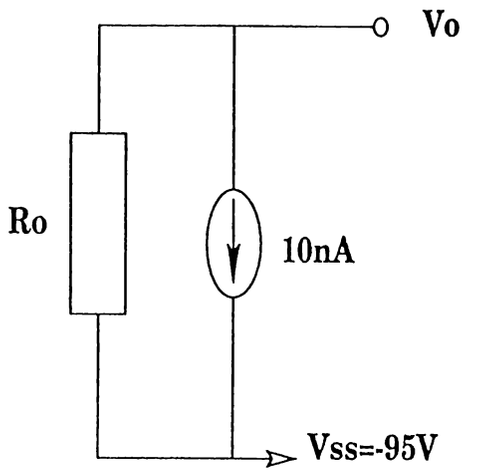

Figure 2.3: Simple Model for Current Source

The operation of the current source is limited by supply voltages. Voltage swing at output node V_o cannot exceed available supply range, otherwise some of the transistors in current source cuts off and operation fails. Also the output impedance R_o of the current source must be chosen as high as possible in order to get rid of changes in supply current of 10nA when output voltage sweeps a certain voltage range.

A 100V voltage drop accross the current source with $10nA$ requires

$$\frac{100V}{10nA} = 10^9\Omega \tag{2.27}$$

resistance which is impractical in chip fabrication process. This much of resistance cannot be obtained directly and therefore we must propose another method. We will first start from a relatively higher current level around a few micro ampers and use cascade current mirror stage for current attenuation down to 10nA. One must be careful in choosing starting current level. At high levels of currents, power consumption comes into play. If overall 10nA

current source withdraws a current of 10mA, this will correspond to $1W$ power consumption. Keeping this fact in mind, we will try to use currents as low as possible.

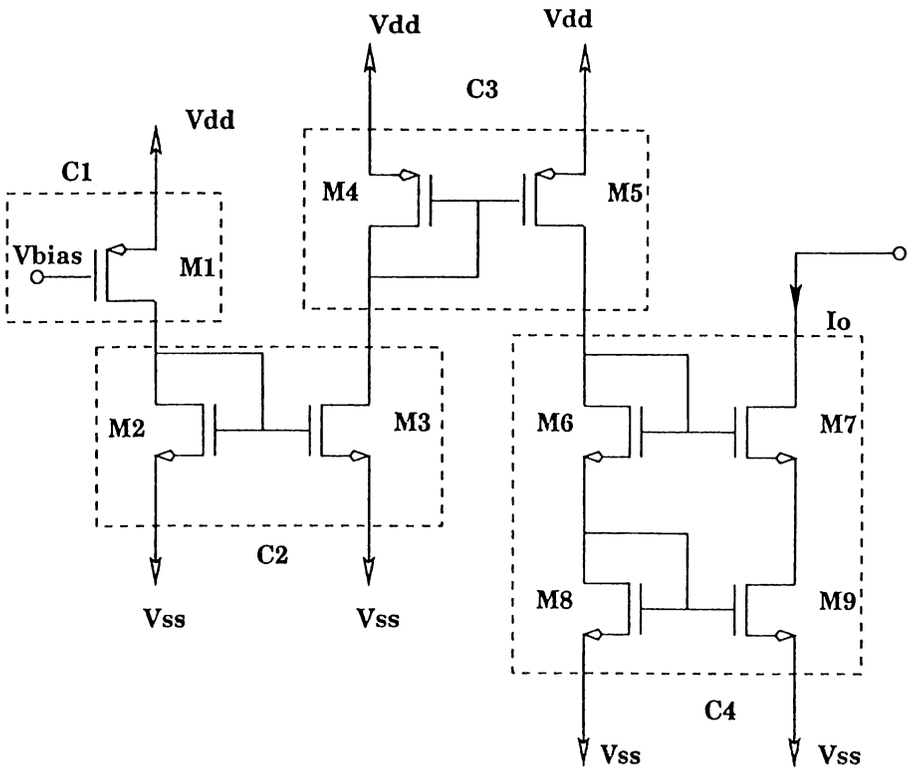

Figure 2.4: 10nA Current Source with no load capacitive current compensation

Circuit in Figure 2.4 shows the general topology of the 10nA current source. Supply voltages used are $V_{DD} = 5V$ and $V_{SS} = -95V$. The transistor M_1 in subcircuit C_1 supplies the current I_{bias}, which make all the transistors ON. V_{bias} is the bias voltage which is supplied by another voltage divider circuit discussed next. The gate of the M_1 is at almost infinite impedance and will have no loading effect at bias circuit.

Subcircuits C_2 and C_3 are cascaded current mirror stages and achieve a current division. They also isolate current biasing transistor M_1 from voltage variations at the output node.

Figure 2.5 shows the modified form of uncompensated current source. During capacitive current compensation in Chapter 4, we will design a load capacitive current compensating circuit and generate a copy of load capacitive

current. This current will be fed back through non-inverting pin of an operational amplifier. Non-inverting pin will be connected to the drain of M_4 as shown in Figure 4.12. In order not to saturate the operational amplifier, this voltage must be somewhat lower than V_{DD}. Actually, to achieve a current division, the (W/L) ratio of transistor M_4 cannot be chosen so low, which leads us to gate-to-source voltage of around $1V$. Therefore, the voltage at the node to which operational amplifier will be connected become around $4V$. This voltage is very close to V_{DD} and saturate the operati0nal amplifier. To draw that voltage down to around $0V$ and give a proper operation range to operational amplifier, two more p-type current mirror stages will be connected in parallel to C_3. To achieve output stability, Cascode (or Improved Wilson) current

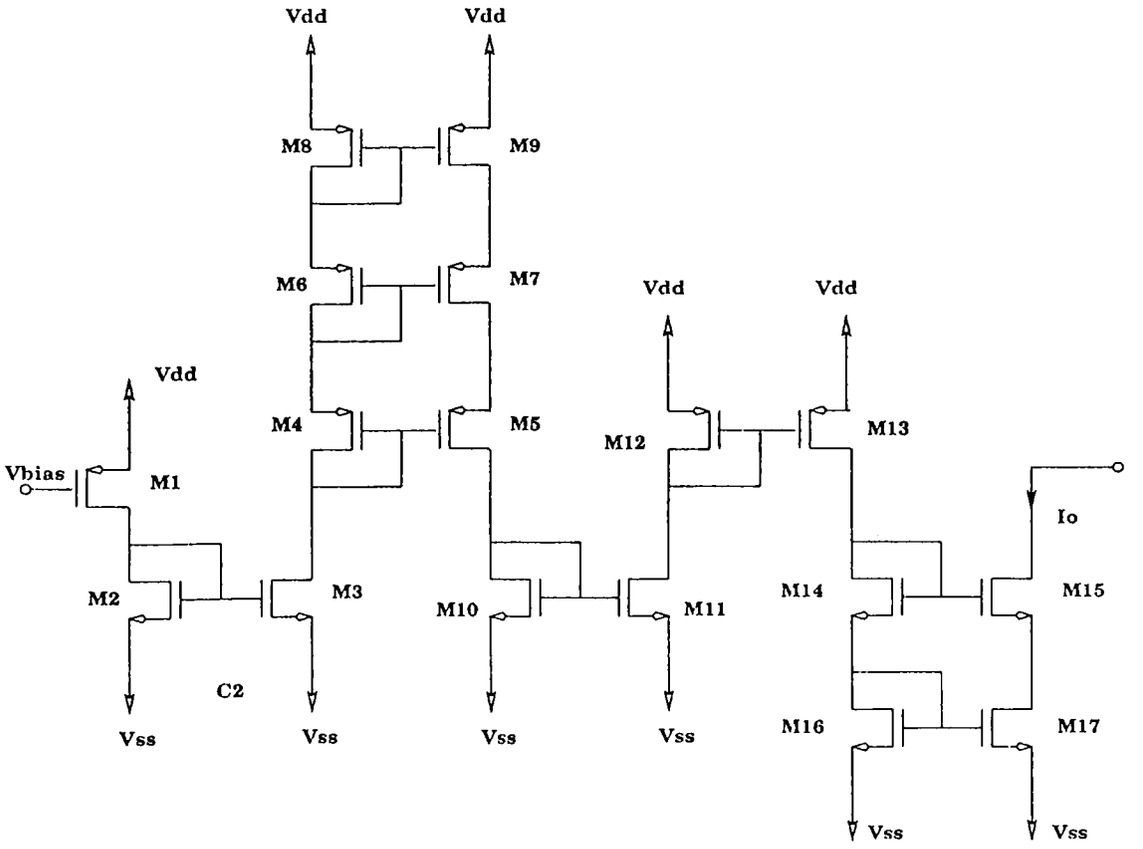

Figure 2.5: Final 10nA Current Source with no load capacitive current compensation

source is placed at the last stage, labeled as subcircuit C_4. (W/L) ratios of transistors in current source are given in Table 5.1.

Transistor	(W/L)
M_1	40 μ /221 μ
M_2	20 μ /20 μ
M_3	20 μ /20 μ
M_4	22 μ /20 μ
M_5	22 μ /20 μ
M_6	22 μ /20 μ
M_7	22 μ /20 μ
M_8	21 μ /20 μ
M_9	21 μ /20 μ
M_{10}	40 μ /24 μ
M_{11}	20 μ /80 μ
M_{12}	40 μ /24 μ
M_{13}	20 μ /80 μ
M_{14}	50 μ /10 μ
M_{15}	20 μ /50 μ
M_{16}	50 μ /10 μ
M_{17}	20 μ /50 μ

Table 2.1: Transistor sizes of 10nA Current Source.

2.2.1 Output Current Stability

The Cascode Current Source C_4 serves as the output stage and prevents the output current from changing in response to load voltage variations. Cascode Current Source is composed of two current mirror blocks connected in parallel. The small signal output resistance is given to be

$$R_o = r_{o7}[1 + (g_{m7} + g_{mb7})r_{o9}] + r_{o9} \tag{2.28}$$

where

$$r_o = \frac{1}{g_d} \tag{2.29}$$

and

$$g_d = \frac{\lambda}{1 + \lambda V_{DS}} I_D. \tag{2.30}$$

Also the transconductance g_{mb} is given to be

$$g_{mb} = -\frac{\gamma g_m/2}{\sqrt{2\phi_p + V_{SB}}}. \tag{2.31}$$

The low channel-length modulation characteristics of the process causes' R_o to reach even $10^9\Omega$ by which we achieve good output current stability. Actually

$$R_o = \frac{\Delta V_o}{\Delta I_o} \Longrightarrow \Delta I_o = \frac{\Delta V_o}{R_o} \tag{2.32}$$

and the relation in Equation 2.32 tells us that to get a few pico ampers change in output current in response to possible 30V to 80V change in load voltage we require an output impedance of order many giga ohms. Cascading more and more current mirror blocks will continuously raise output impedance and output current stability, but this time it will have a negative effect on possible range of output voltage swing to keep output transistors in saturation. In other words, maximum load impedance that current source can drive fall below the maximum possible value of $10G\Omega$ for supply range of 100V and current of 10nA.

2.3 Voltage Divider Bias Circuit

Amplifier stages and current sources need various dc bias voltages and currents for their operations. Usually the circuits have only two dc voltage supplies , $V_{DD} > 0$ and $V_{SS} \leq 0$, and all other bias voltages must be obtained externally. To obtain the dc bias voltages $V_{b1}, V_{b2}, \cdots, V_{bn}$ where $V_{SS} < V_{b1} < V_{b2} < \cdots < V_{bn} < V_{DD}$, I have used voltage division. It is not suitable to use resistive dividers in MOS technology because of their large silicon area consumption. Instead, MOSFETs are used in a totem-pole configuration [14] .

Figure 2.6 shows the PMOS Voltage Divider. For all transistors in the chain $V_{GS} = V_{DS}$ and hence the saturation condition $|V_{DS}| > |V_{GS}| - |V_T|$ is satisfied. The same current I_{bias} flows through the transistors and given to be

$$I_{bias} = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_1(V_{b1} - V_{T1})^2 \tag{2.33}$$

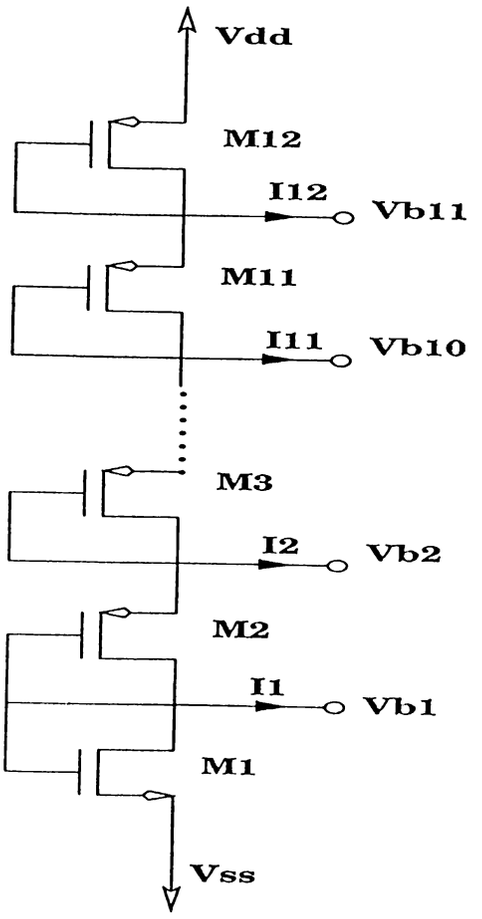

Figure 2.6: Voltage Divider Bias Chain

$$= \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_2(V_{b2} - V_{b1} - |V_{T2}|)^2 \tag{2.34}$$

$$= \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_{12}(V_{DD} - V_{b12} - |V_{T12}|)^2 \tag{2.35}$$

But all the equations above valid only if the current drawn or supplied by the node to which bias voltage will be applied is much smaller than the bias current I_{bias}, i.e, $I_i < I_{bias}$ is assumed. In our design, we will use this bias voltages to drive the gate of MOS transistors and hence we may use all those equations safely.Notice that only transistors M_1 and M_{12} have no body effect but for the others threshold voltages are different for different devices.

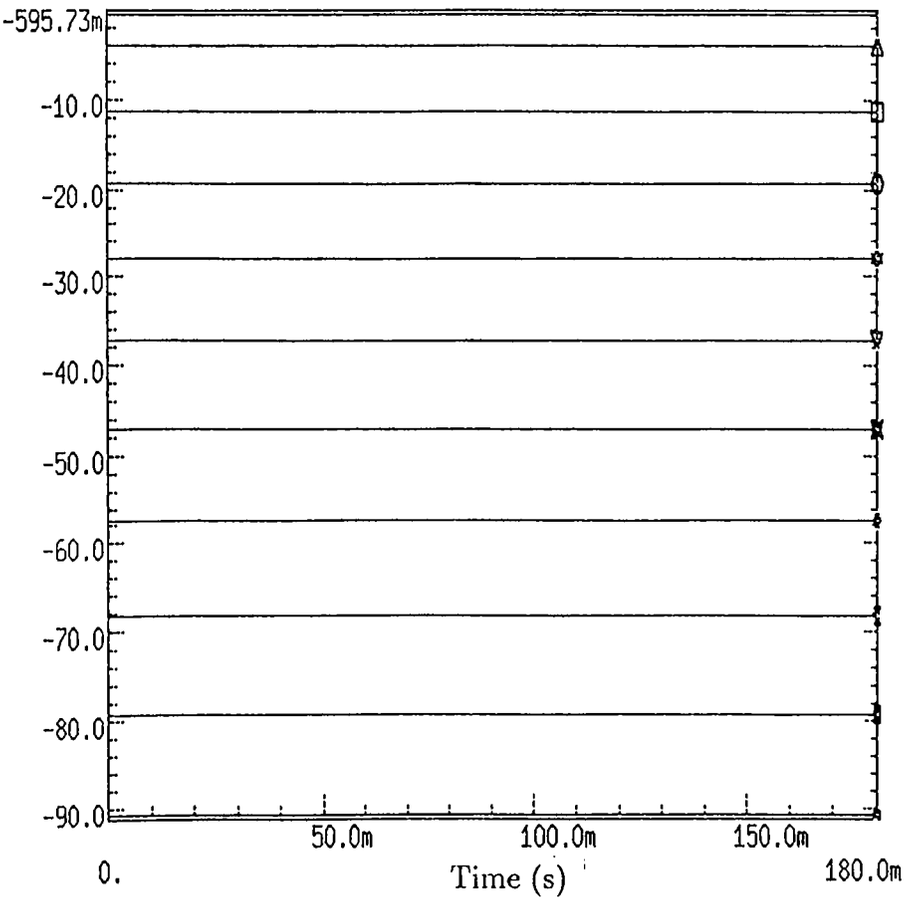

Figure 2.7: Available Bias Voltages

Threshold voltages are given by

$$V_{T1} = V_{Tn} \tag{2.36}$$

$$|V_{T2}| = |V_{Tp}| + \gamma(\sqrt{2|\phi_p| + V_{DD} - V_{b2}} - \sqrt{2|\phi_p|}) \tag{2.37}$$

$$|V_{T11}| = |V_{Tp}| + \gamma(\sqrt{2|\phi_p| + V_{DD} - V_{b11}} - \sqrt{2|\phi_p|}) \tag{2.38}$$

$$|V_{T12}| = |V_{Tp}| \tag{2.39}$$

where V_{Tn} and V_{Tp} are the threshold voltages of NMOS and PMOS transistors for $V_{SB} = 0$ respectively. γ is a device constant given by

$$\gamma = \frac{\sqrt{2\varepsilon q N_{imp}}}{C_{OX}} \tag{2.40}$$

where ϵ is the permittivity of silicon and N_{imp} is the density of impurity ions in the bulk.

The available bias voltages in the actual voltage divider chain of current source shown in Figure 2.7. From top of the plot, bias voltages correspond to $V_{b11}, \cdots, V_{b1}$ respectively. $V_{b10} = -3.99V$ and $V_{b1} = -90.99V$ has been used to generate bias currents of current source and operational amplifier. If we used a PMOS transistor instead of M_1 in bias chain, it would become impossible to generate the bias voltage of $-90.99V$ since the threshold voltage of PMOS M_1 would reach to about $10V$ and limits the value of V_{b1} at minimum $-85V$. NMOS transistor at M_1 completely overcome that problem.

Calculated values of (W/L) ratios for the transistors in voltage divider bias chain of Figure 2.6 are shown in Table 2.2

Transistor	(W/L)
M_1	200 μ /20 μ
M_2	15 μ /20 μ
M_3	200 μ /20 μ
M_4	200 μ /20 μ
M_5	200 μ /20 μ
M_6	200 μ /20 μ
M_7	200 μ /20 μ
M_8	200 μ /20 μ
M_9	200 μ /20 μ
M_{10}	200 μ /20 μ
M_{11}	200 μ /20 μ
M_{12}	201 μ /20 μ

Table 2.2: Transistor sizes of Voltage Divider Bias Chain.

Chapter 3

Test of Current Source

3.1 Output Current Stability

The output impedance of current source simply modeled as in Figure 3.1 is very important since it determines the output current stability.

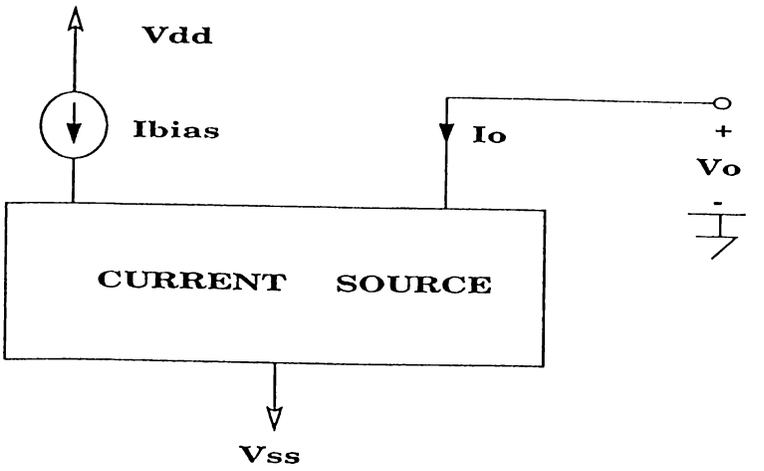

Figure 3.1: A simple model of current source

Output impedance of the current source is calculated by connecting an AC voltage source in place of V_o. Then R_o is calculated using

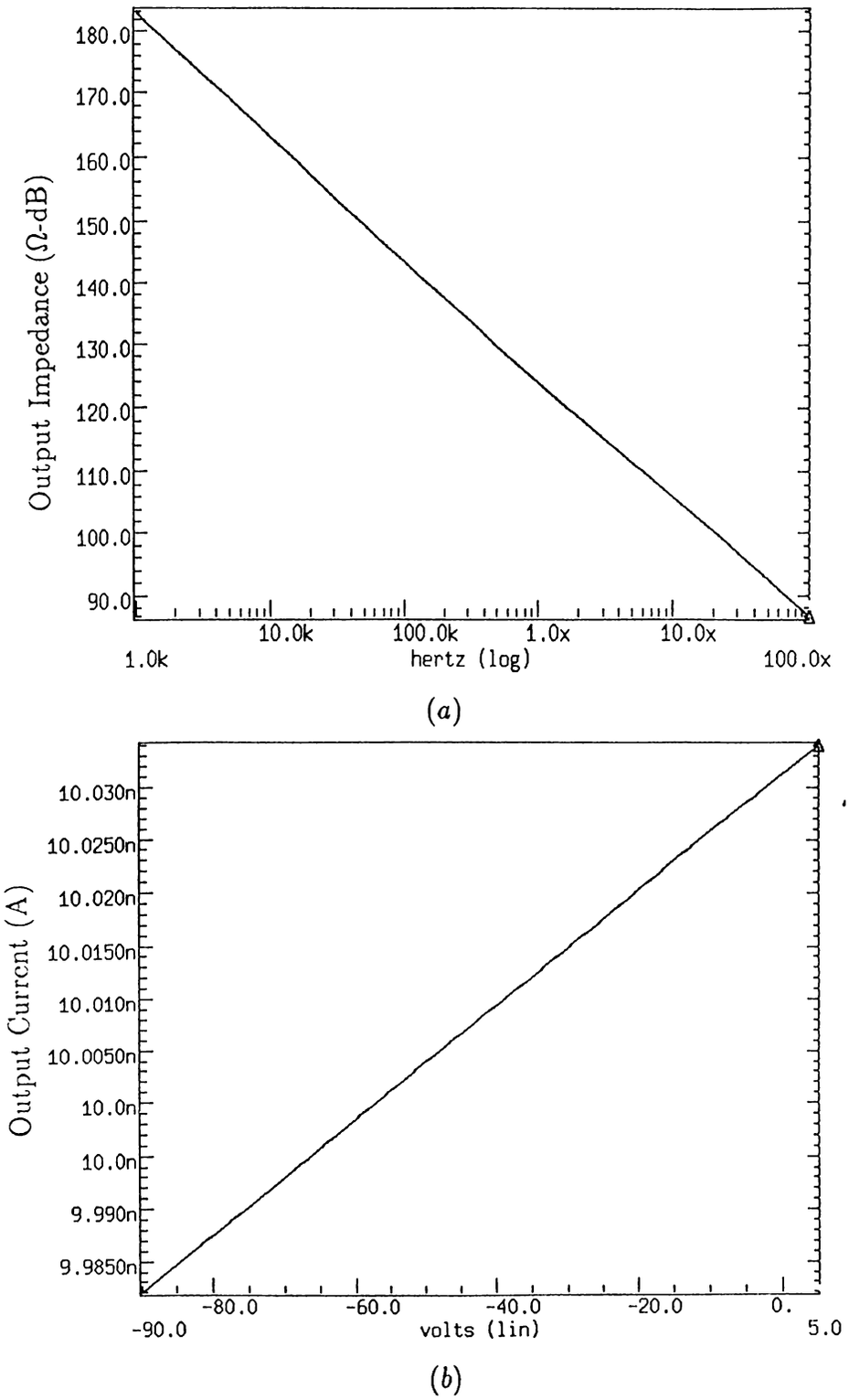

Figure 3.2: (a) Plot of Output Impedance (dB) vs. Frequency (Hz-log) and (b) Plot of Output Current (A) vs. Vo (V)

$$R_o = \frac{V_o}{I_o} \tag{3.1}$$

Frequency response of output impedance is plotted in Figure 3.2-a. It shows that at the expected operation range of a few kHz, the output impedance of current source is around giga ohms which is sufficient for required output stability. In fact, plot in Figure 3.2-b confirms our expectations. Output voltage V_o is swept from $-90V$ to $+5V$ and change in current sunk is observed. Since output voltage is changed dc-wise, current stability is controlled by output impedance of around $1 - 2G\Omega$ which, in turn, will result in a deflection of 10.0350nA−9.9820nA= 53pA. $\Delta V_o = 95V$ and $\Delta I_o = 53$pA lead us to sensitivity of

$$\frac{\Delta I_o}{\Delta V_o} = 0.56pA/V \tag{3.2}$$

In other words, $1V$ change in output voltage will cause a deflection of 0.56pA in output current which is negligible compared to the current level of 10nA. But we must be careful in trusting this performance. This plot is a result of DC analysis and therfore output impedance assumed is at its peak. In a normal operation , depending upon the frequency component of output voltage performance of current source will degrade.

3.2 Resistive Load

In order to show the effects of AC components at output voltage, configuration in Figure 3.3 is used. The variable load resistance as a function of time is first plotted in Figure 3.4. The rate of change in load resistance determine the AC component of output voltage. The faster R_L change , the lower is the output impedance encountered and the more deflection from 10nA is observed. Second plot in Figure 3.4 shows this phenomena. Third plot is the zoomed out repetition of the second plot, in which current stability can be observed more appropriately.

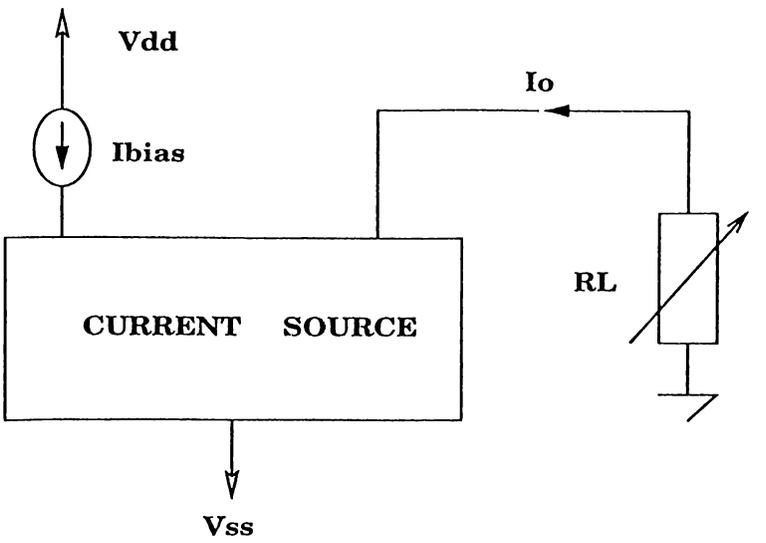

Figure 3.3: Current Source Driving Variable Resistive Load

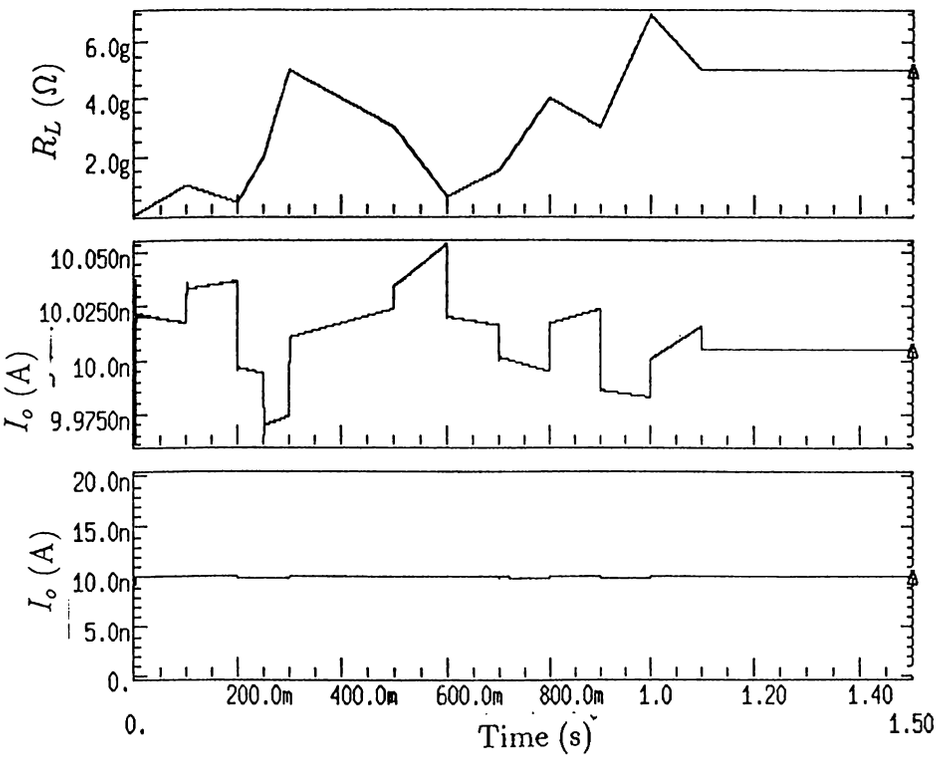

Figure 3.4: (a): Rl vs. Time (s) (b): Output Current vs. Time (s), (c): Output Current vs. Time (s)-zoomed out

3.3 Resistive and Capacitive Loads

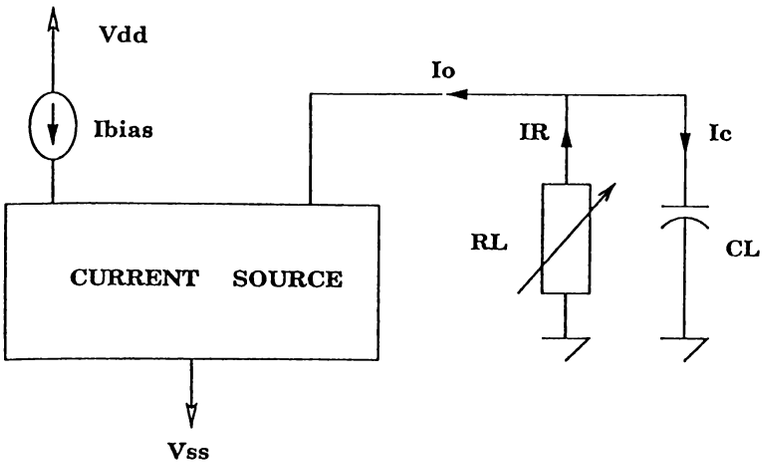

Figure 3.5: Current Source Driving Variable Resistive Load and a Parallel Capacitance

In actual use of this current source , the load will be not only a resistance but also a capacitance of order $1 - 2$pF parallel to resistance as shown in Figure 3.5 . This capacitance causes problem in operation. The current source must have the ability of supplying 10nA current through the resistive branch. It is evident from the Figure 3.5 that the change in load resistance will cause an alternating voltage accross the load capacitance and the capacitance will withdraw or supply current proportional to the derivative of that voltage. The current through the capacitive branch is given to be

$$I_c = C_L \frac{dV_o}{dt} \tag{3.3}$$

and

$$I_R = I_o + I_C \tag{3.4}$$

Noting that the capacitive branch can supply or withdraw a current of many nano ampers, the current through the resistive branch may divert drastically from 10nA.

Figure 3.6 shows the simulation results of circuit in Figure 3.5. First plot of Figure 3.6 is the current through the resistive branch which is equal to the

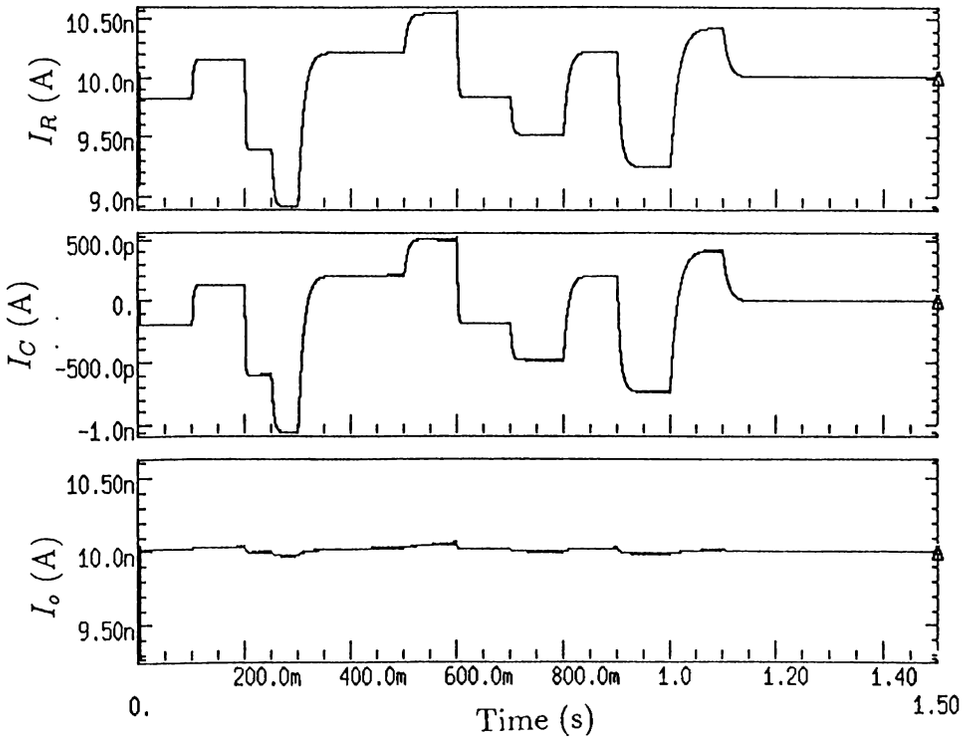

Figure 3.6: (a): Current through resistive branch vs. Time (s) (b): Current through capacitive branch vs. Time (s) (c): Total current of source vs. Time (s)

sum of the capacitive current in second plot and total current supplied in third plot. It is obvious that if load resistance change more rapidly, larger capactive currents will be generated and more deflection from 10nA will occur.

Our next job in Chapter 4 is to add a capacitive current compensating branch to our original current source so that the current through the resistive branch is equal to 10nA no matter what the load voltage variation is.

Chapter 4

Capacitive Current Compensation

In order to compensate the current through the capacitive branch, we must first create a copy of that current. The only way of generating the capacitive current is to follow the mathematical relation that it obeys. We know that capacitive current is given by

$$I_C = C_L \frac{dV_o}{dt}, \tag{4.1}$$

that is, we need a differentiator to get the derivative of output voltage.

4.1 Differentiator

Figure 4.1 is a simple differentiator. A straight-forward analysis show that

$$V_o = -R_d C_d \frac{dV_{in}}{dt}. \tag{4.2}$$

The block elements R_d and C_d are used to obtain a certain multiple of input voltage derivative.

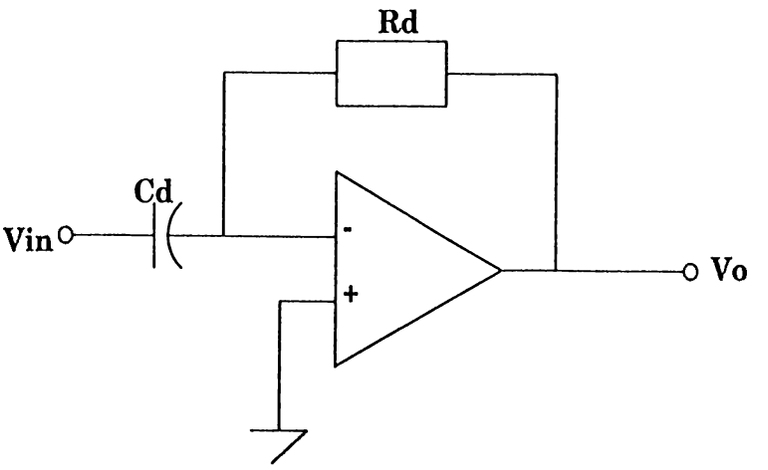

Figure 4.1: Differentiator

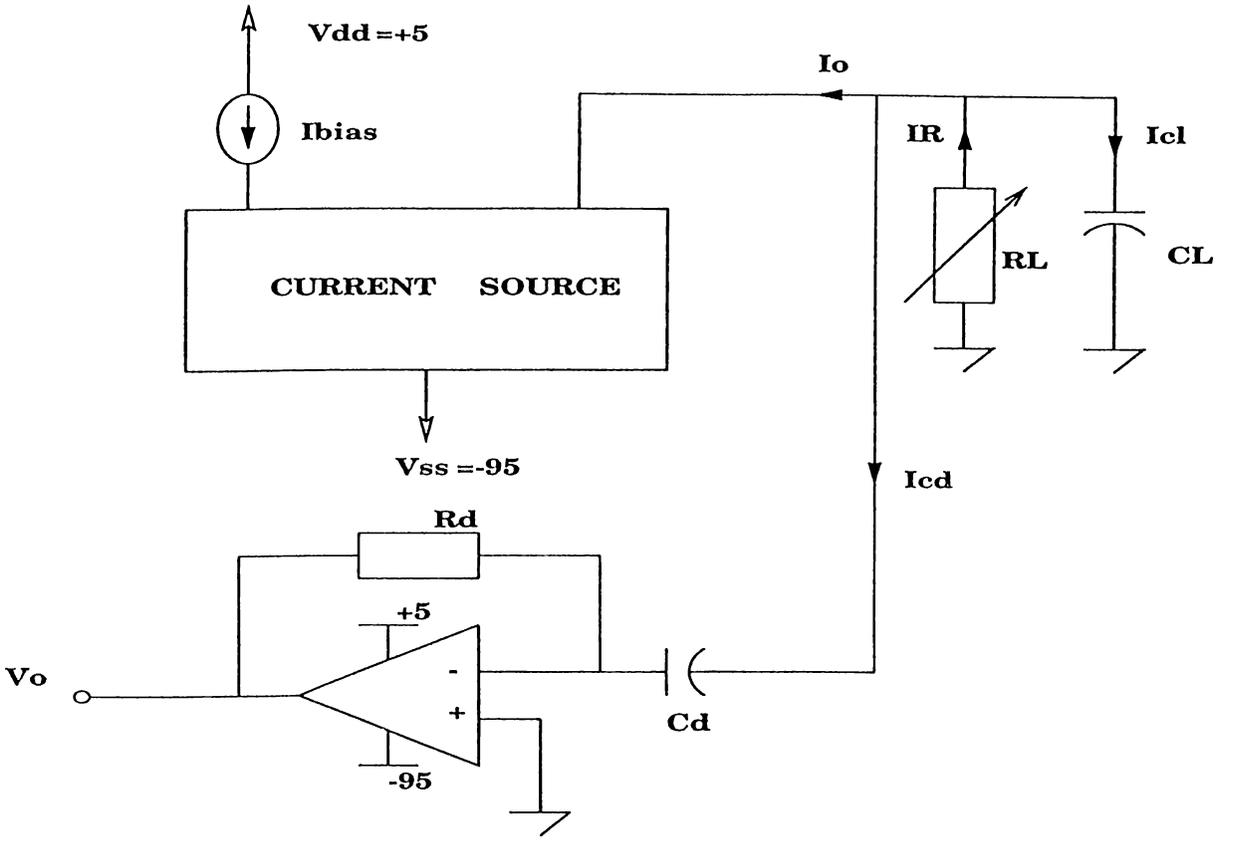

Figure 4.2: Differentiator connected to the current source

Their values cannot be used arbitrarily in the case of a realistic opamp and one must be careful on the characteristics of the amplifier. If differentiator is connected directly to the output of the current source as in Figure 4.2 the differentiator capacitor C_d will become parallel to load capacitance C_L since it is connected in between output node of current source and virtual ground. In other words, the current we try to compensate increases. Since

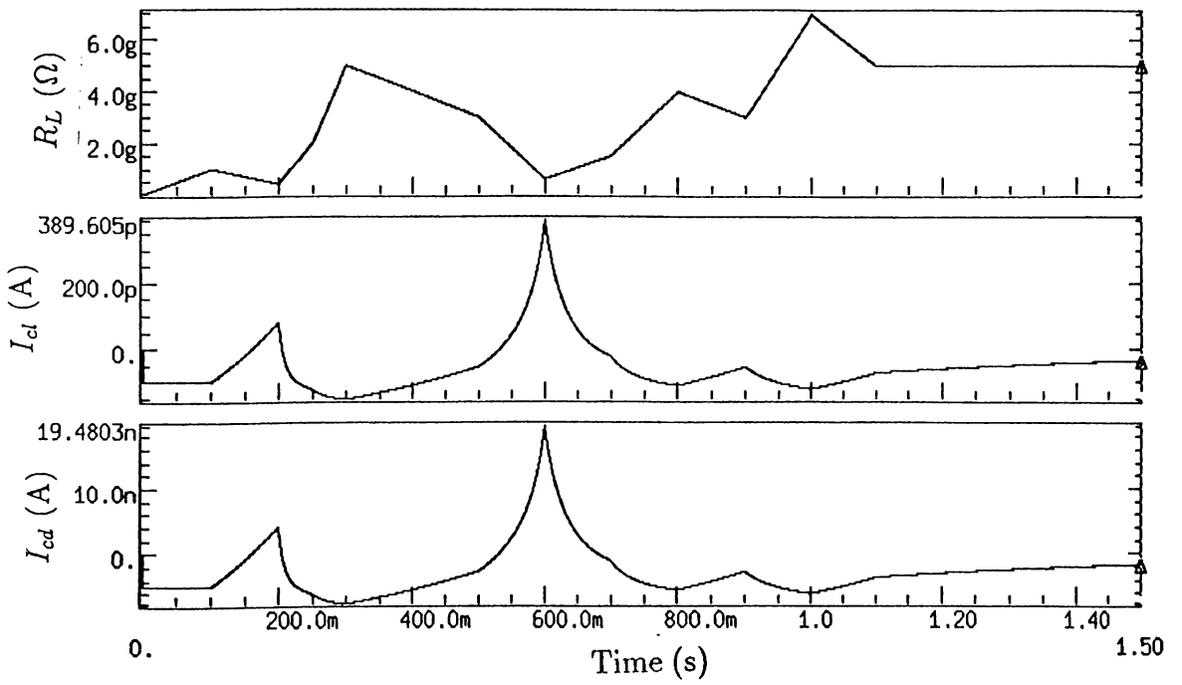

Figure 4.3: Capacitive currents when differentiator connected. (a): Load resistance vs. Time (s), (b): Load capacitive current vs. Time (s), (c): Capacitive current due to differentiator vs. Time (s)

the differentiator capacitance is 50 times the load capacitance, it supplies or withdraws 50 times more current. In fact, the capacitive currents in (b) and (c) of Figure 4.3 are the same in shape but (c) is almost 50 times (b).

To overcome this problem, a buffer will be embedded between current source and differentiator, which is discussed in the next section. Opamp used is a realistic one and discussed in detail in Chapter 5. In simulation, the element values are chosen to be $R_d = 100\text{k}$, $C_d = 100\text{p}$ and $C_L = 2\text{pF}$.

4.2 Buffer

An output stage must be able to deliver a considerable amount of power into a low-impedance load with acceptably low levels of signal distortion. Therefore, in general, it is required to have one or more of the following desirable properties [15] :

- Low output impedance
- Large output voltage swing
- Large output current swing
- Almost unity gain
- Large input impedance

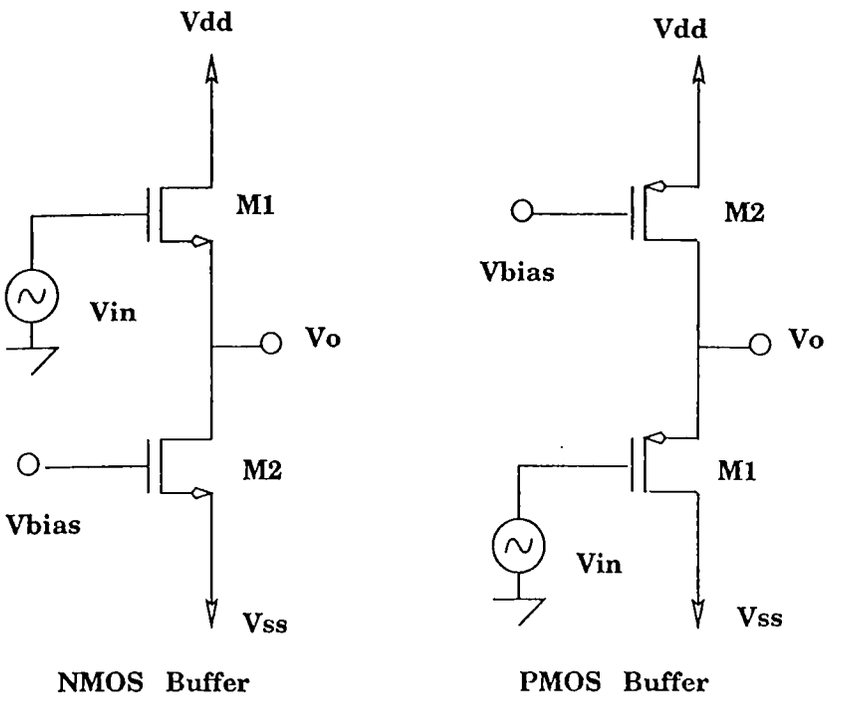

Figure 4.4: NMOS and PMOS Output Buffers

Figure 4.4 shows NMOS and PMOS output stages which can provide the above requirements.

4.2.1 DC Voltage Shift

A close look to the circuit of buffers reveals that they also function as a DC Level Shifter. The (W/L) ratios of transistors M_1 and currents supplied by transistors M_2 determine the gate-to-source voltage of transistors M_1 which eventually leads to DC shift between output and input nodes. It is evident from the above two circuit that for NMOS Buffer

$$V_o = V_{in} - V_{gs1} \tag{4.3}$$

and for PMOS Buffer

$$V_o = V_{in} + |V_{gs1}|. \tag{4.4}$$

Then NMOS buffer fulfills a downward DC-shift while PMOS Buffer operate as an upward DC-level shifter. Available voltage in negative side is -95V and gives wider operation range, therefore it is better to use downward DC-level shifter , i.e NMOS buffer in order not to deal with degradation of the input signal. In Figure 4.5 the downward DC voltage shift characteristics of NMOS

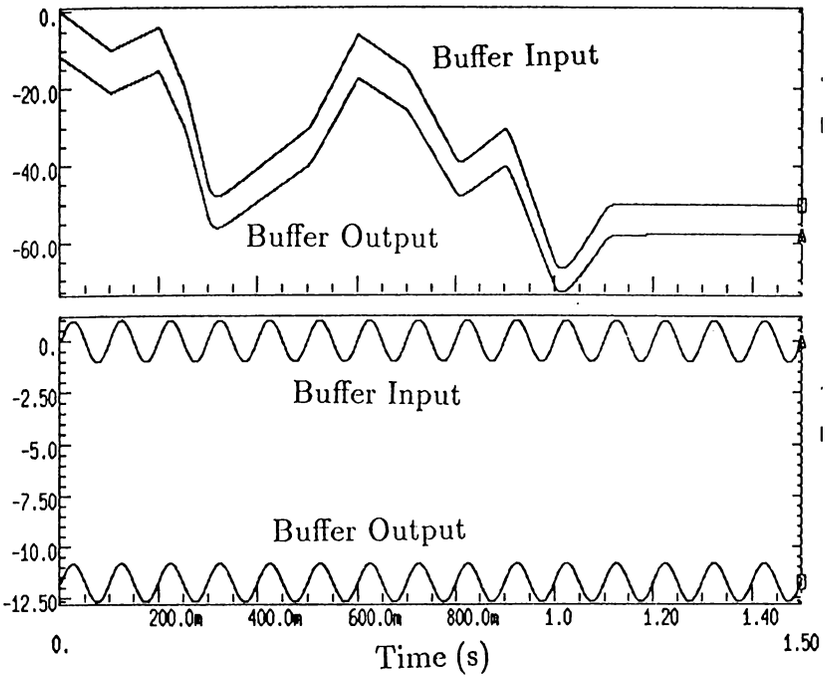

Figure 4.5: NMOS Buffer DC-Level Shift Operation

buffer is clearly observed. In both plots, upper wavefoms are the inputs and lower DC-wise shifted waveforms are outputs. The amount of shift is around 11V. Actually, the lower amounts of shift cannot be obtained using available supply voltages. That is because, V_{SB} of transistor M_1 is much greater then zero and cause a large body effect. If there were no body effect

$$V_{in} - V_{out} = V_{T0} + (V_{bias} - V_{ss} - V_{T0})\sqrt{\frac{(W/L)_2}{(W/L)_1}} \tag{4.5}$$

and one can fully control DC voltage shift. But the large body effect cause

$$V_{in} - V_{out} = V_T + (V_{bias} - V_{ss} - V_{T0})\sqrt{\frac{(W/L)_2}{(W/L)_1}} \tag{4.6}$$

where

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_F + V_{out}} - \sqrt{2\phi_F}). \tag{4.7}$$

We cannot reduce the DC shift below the threshold voltage which gets larger

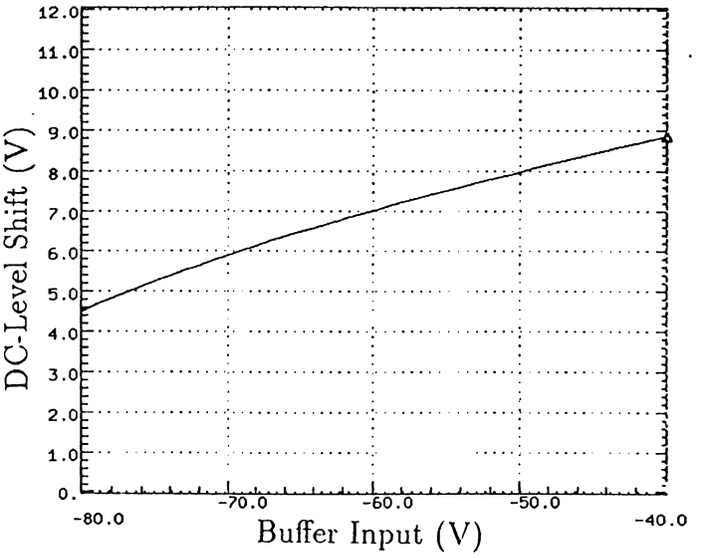

Figure 4.6: NMOS Buffer DC-Level Shift vs Vin (V)

including the body-effect. The linearity of DC shift is examined in Figure 4.6. It is evident that as input signal gets larger and larger, amount of DC shift also rise. The large signal behaviour of the buffer will cause the amount of DC shift to change.

4.2.2 Small-Signal Gain

By small-signal analysis on NMOS buffer, it can be confirmed that

$$A_v = \frac{1}{1 + (|g_{mb1}| + g_{d1} + g_{d2})/g_{m1}}. \tag{4.8}$$

Since $g_{m1} \gg |g_{mb1}|, g_{d1}$ and g_{d2} , voltage gain of buffer is approximated by

$$A_v \approx 1. \tag{4.9}$$

(a) of the Figure 4.7 shows that the voltage gain is very close to unity. (b) is the corresponding phase shift. In fact, gain of the buffer is not so much important in our circuit, because the gain lost at buffer stage can be compensated by changing the gains of subsequent stages.

4.2.3 Output Impedance

Using small-signal equivalent circuit of NMOS Buffer, expression of output impedance is calculated to be

$$R_{out} = \frac{1}{|g_{mb1}| + g_{d1} + g_{d2} + g_{m1}}. \tag{4.10}$$

There is a trade-off between the current through the buffer and output impedance. Higher levels of buffer current accompanies with the lower output impedance but this time we must be careful on power limitation. Fortunately, buffer in our circuit will drive a differentiator which has a high input impedance hence output impedance will not create a problem.

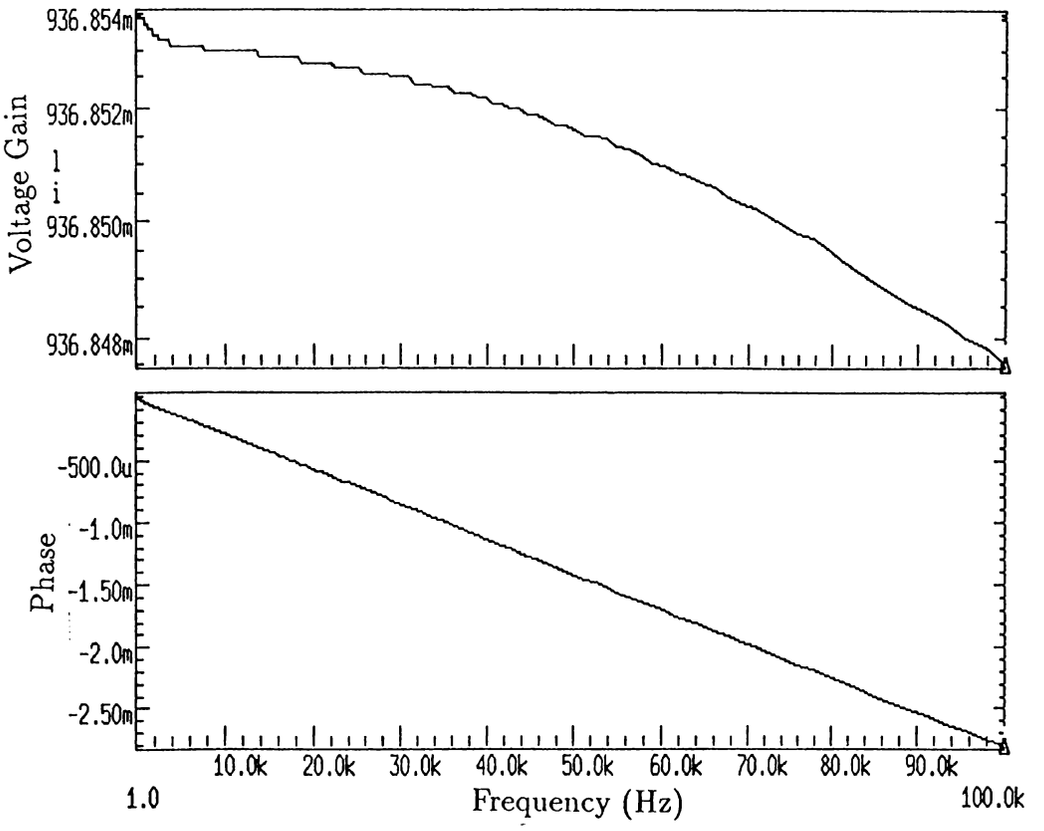

Figure 4.7: (a): Small Signal Voltage Gain and (b): Phase Shift

4.3 Buffer and Differentiator

Remember that our aim in design of a buffer was to eliminate the effect of differentiator capacitance C_d on the current of resisistive load. After the insertion of NMOS buffer, circuit in Figure 4.2 turns into the circuit in Figure 4.8.

Referring to the Figure 4.8, differentiator capacitance C_d and the current source output are completely isolated by means of buffer stage. But one must be careful in choosing the buffer stage because total gate capacitance of transistor M_1 will cause a problem similar to that of C_d. Therfore, in design of buffer , the size of transistor M_1 is kept as small as possible to keep its gate capacitance much lower than C_L. A proper design revealed that this gate capacitance could be reduced to $0.23pF$. This value is smaller than C_L but still its contribution to current through resistive load is important and must taken

into account in setting compensation parameters.

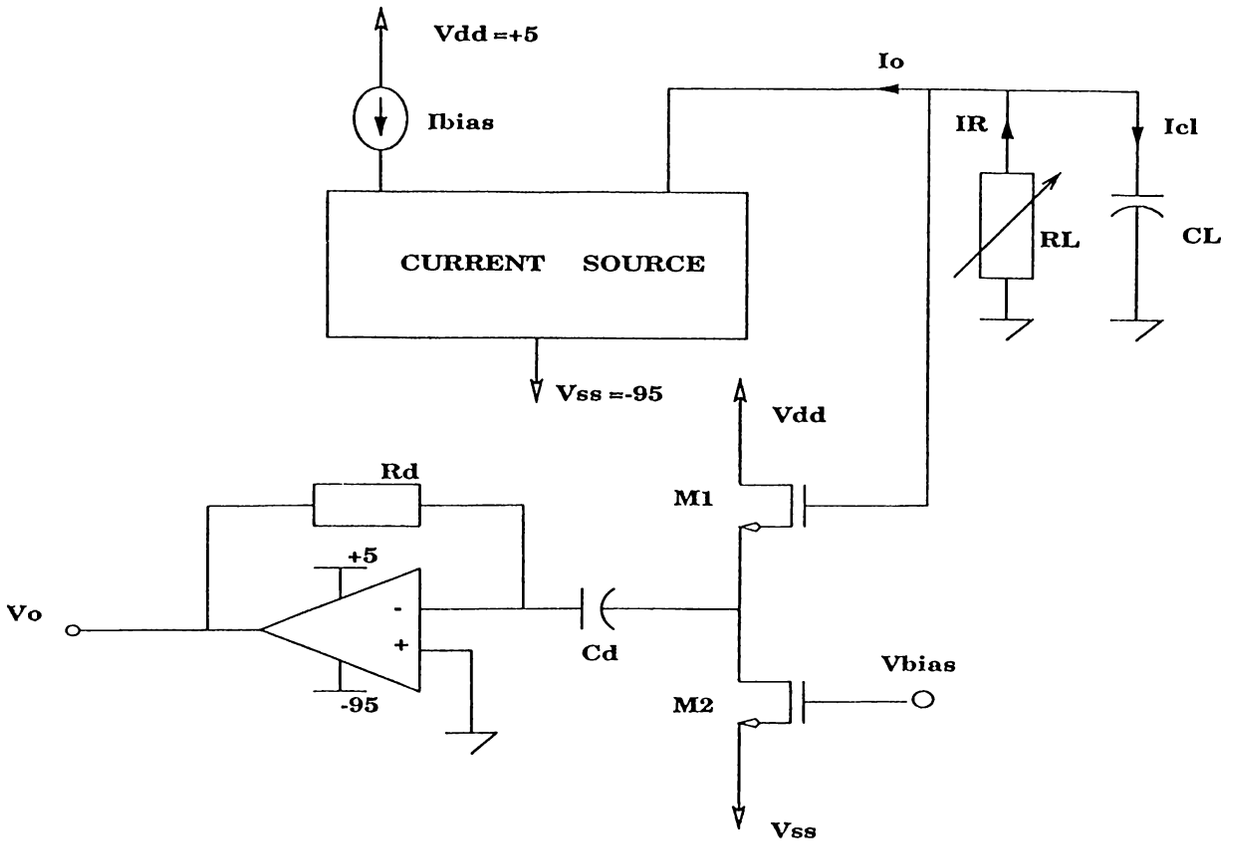

Figure 4.8: Differentiator and Buffer connected to the current source

Compared to Figure 4.3, the improvement of circuit performance after adding buffer stage is evident from Figure 4.9. First plot of that figure is the change in load impedance. It is redrawn here to get a feeling of relation between capacitive currents and load impedance change. In fact, assuming total current supplied by the current source fixed, derivative of the output voltage is proportional to the derivative of load impedance. The shape of capacitive current in (b) hence coincides with the waveform in (a) and is more reasonable than that in Figure 4.3.

Third plot of the Figure 4.9 is the differentiator output. Using pre-defined parameters and an ideal opamp, the output voltage of differentiator must be equal to

$$V_o = -5 \times 10^6 I_c \tag{4.11}$$

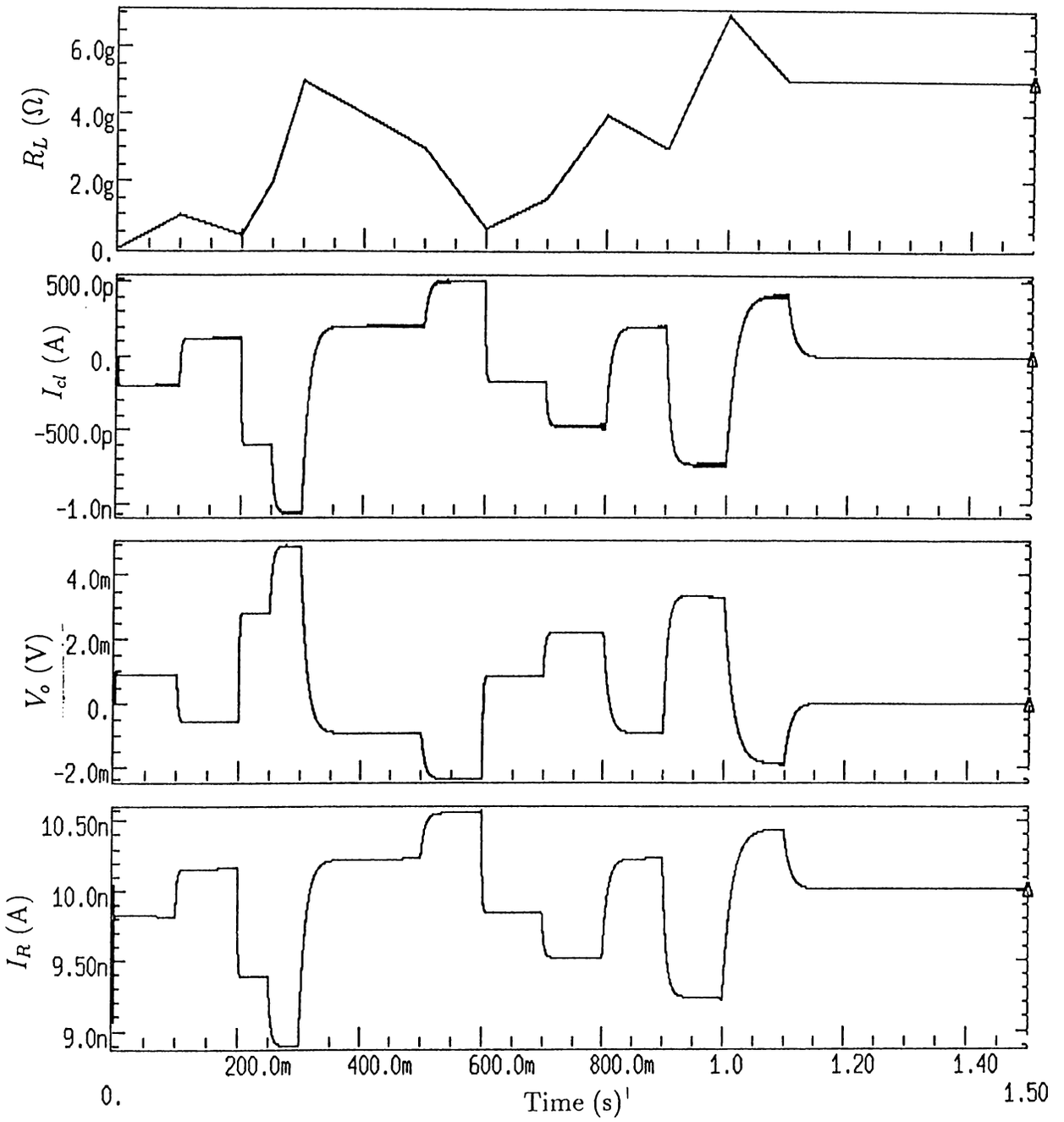

Figure 4.9: (a): Load Impedance vs. Time (s), (b): Current Through Load Capacitance, (c): Differentiator Output , (d): Current Through Load Resistance

But simulation using the realistic op-amp which will be discussed next gives $V_o = -4.55 \times 10^6 I_c$. In setting of compensating branch parameters this value should be taken into account.

Finally, (d) is the current of resistive load, which is equal to the sum of fixed current of 10nA and capacitive load current.

As a final remark, note that, DC shift of the current source output voltage after use of buffer cause no problem since it is directly input to a differentiator and completely eliminated.

4.4 Voltage Controlled Current Source

The next job is to convert that voltage into a current linearly and apply to the output node of original current source. There exist many types of VCCS's but not many of them satisfy our desires. The required specifications of VCCS are as follows:

- Voltage to current conversion must be linear
- Governing equation must be independent of input voltage
- Depending upon the polarity of input signal, it must have the ability of supplying and withdrawing current

Circuit in Figure 4.10 satisfies all the requirements. Using Kirchoff's Voltage and Current Laws, equations below can be written.

$$V_{in} = I_1 R_1 + I_3 R_3, \tag{4.12}$$

$$I_2 R_2 + I_4 R_4 = 0, \tag{4.13}$$

$$I_4 = I_3 + I_0 \tag{4.14}$$

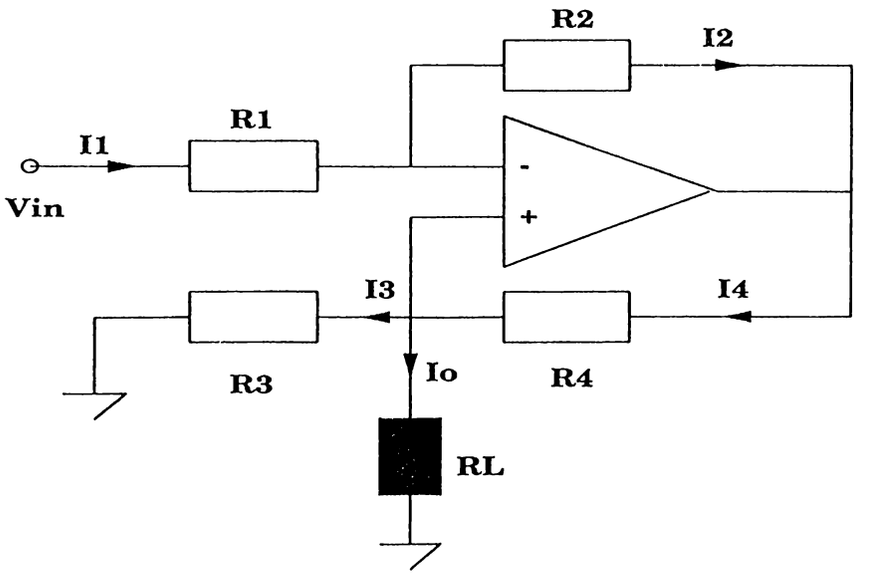

Figure 4.10: Voltage Controlled Current Source

and

$$I_1 = I_2. \tag{4.15}$$

Additionally, if

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} = k \tag{4.16}$$

then

$$R_2 = kR_1 \tag{4.17}$$

and

$$R_4 = kR_3. \tag{4.18}$$

Substituting Equations 4.17 and 4.18 into Equation 4.13

$$I_2R_1 + I_4R_3 = 0. \tag{4.19}$$

Using Equations 4.14, 4.15 and 4.19

$$\underbrace{I_1R_1 + I_3R_3}_{V_{in}} + I_0R_3 = 0 \tag{4.20}$$

and hence

$$V_{in} + I_0 R_3 = 0. \tag{4.21}$$

Then we conclude that the governing equation of the VCCS is

$$I_0 = -\frac{V_{in}}{R_3}. \tag{4.22}$$

The VCCS discussed carries all the nice properties desired but the only inherent disadvantage is that it requires exact matching of resistors. Otherwise the relation in Equation 4.22 will no longer be valid. Circuit in Figure 4.10 is also capable of supplying or withdrawing current independent of load impedance. But note that, the value of load resistance determines the voltage at non-inverting pin of the operational amplifier. In addition to that, this voltage is transferred to the output pin of opamp depending upon the ratio of resistors,k and hence there is always a danger of opamp being saturated. To overcome that, the resistor values and the voltage at non-inverting pin must be specified carefully.

4.4.1 Input Impedance

The input impedance of VCCS is an important parameter because it loads the differentiator. A simple analysis assuming output and input impedances of opamp to be zero and infinity respectively reveals that

$$R_{in} = \frac{R_3 R_1}{R_3 + R_L} \tag{4.23}$$

- By using Equation 4.23 we conclude that input impedance of VCCS may be very low depending upon the value of load impedance and hence load the differentiator. The proper operation of differentiator is very important, hence an additional gain controlling stage with high input impedance will be embedded between differentiator and VCCS.

4.5 Voltage Gain Stage

Circuit in Figure 4.11 is a Non-inverting Amplifier with high input impedance. It can be shown that

$$A_v = 1 + \frac{R_2}{R_1}. \tag{4.24}$$

By choosing the values of resistors appropriately, any gain can be specified.

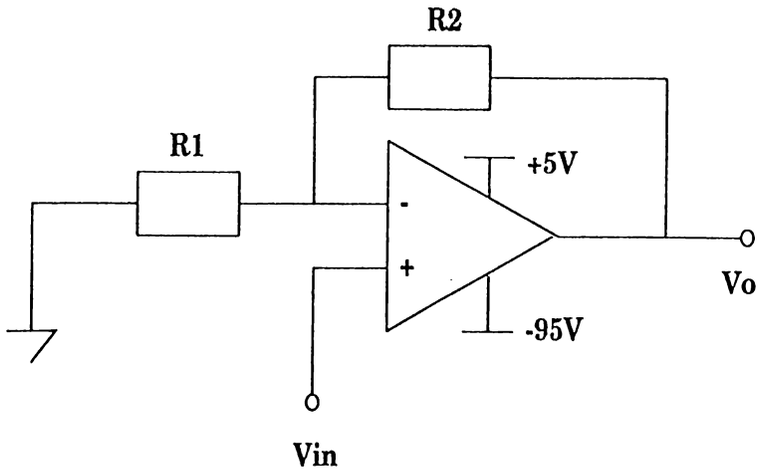

Figure 4.11: Non-inverting Amplifier with High Input Impedance

The input impedance is found to be

$$R_{in} = \frac{AR_i}{1 + R_2/R_1} \tag{4.25}$$

where A is the open-loop gain and R_i is the input impedance of the OpAmp. Since both have very high values , resultant input impedance is even larger than R_i.

4.6 Current Compensating Circuit

Circuit shown in Figure 4.12 is the final topology including all the circuit elements described. Note that fixed $10nA$ current source has been modified to help the operation of VCCS. In fact, additional current mirror stages in

the 10nA fixed current source provide a DC voltage of a few mV at node A to which feedback path from VCCS is connected. Element parameters are so chosen that current through the 2pF load capacitance is completely eliminated.

The overall circuit is designed for 2pF load capacitance but it can be adjusted for other values. For example, by changing only the parameters of non-inverting amplifier exact current compensation can be achieved.

For a proper operation of the circuit, the current generated by compenastion branch must exactly match the load capacitive current when it arrives output node. It is observed that higher values of compensation current may cause a positive feedback and hence instability may occur. Therefore, in adustment of feedback parameters one must start from a compensating current less than actual load capacitive current and slowly increase the current gain. To be specific , lets define some current gain parameters:

G1 Current Gain from node A to output. It is set to 1/545

G2 Voltage Gain of Buffer. It is set to 0.937

G3 Gain of Differentiator

G4 Gain of Non-inverting Amplifier

G5 Current Gain of VCCS

Then, to avoid positive feedback and achieve exact compensation the necessary and sufficient condition is

$$G_1 G_2 G_3 G_4 G_5 = 1. \tag{4.26}$$

Since G_1 and G_2 are fixed

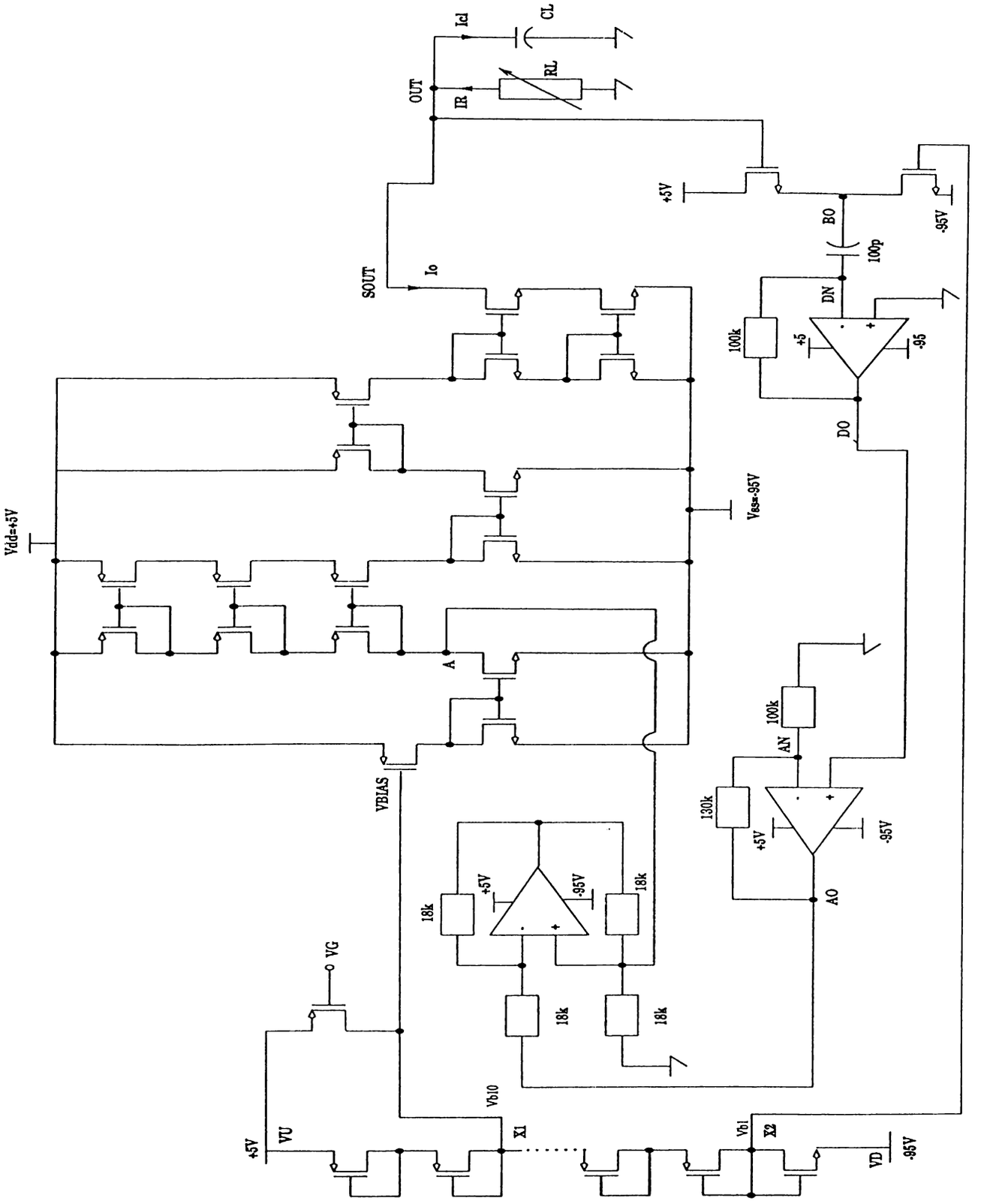

Figure 4.12: Overall Circuit with Capacitive Current Compensation

$$G_3 G_4 G_5 = 582 \tag{4.27}$$

In fact, from circuit in Figure 4.12 it is found that $G_3 = 4550k$, $G_4 = 2.3$ and $G_5 = 1/18k$. These values of gains confirms Equation 4.27.

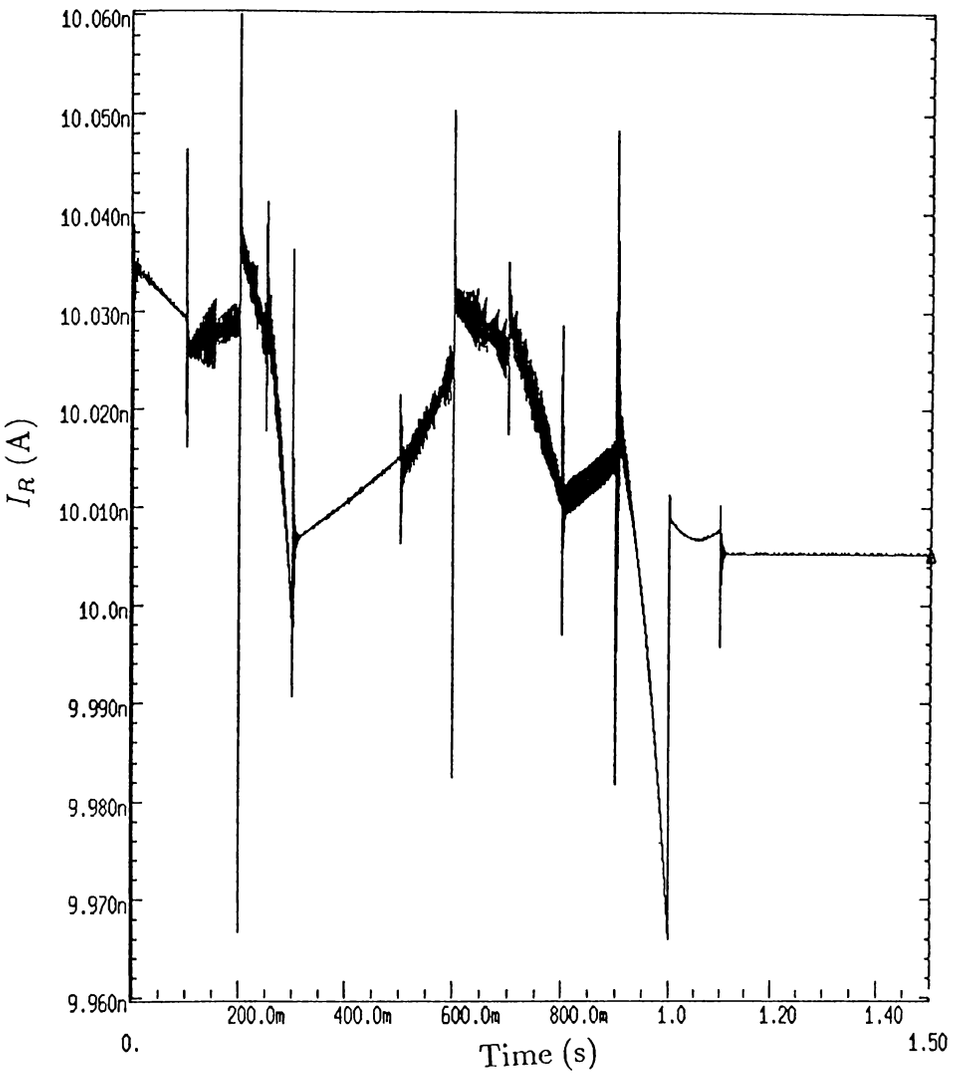

Figure 4.13: Current through resistive load after current compensation

Plot in Figure 4.13 is the result of overall circuit. This result must be compared to (a) of Figure 3.6 in which current through resistive load without compensation is shown.

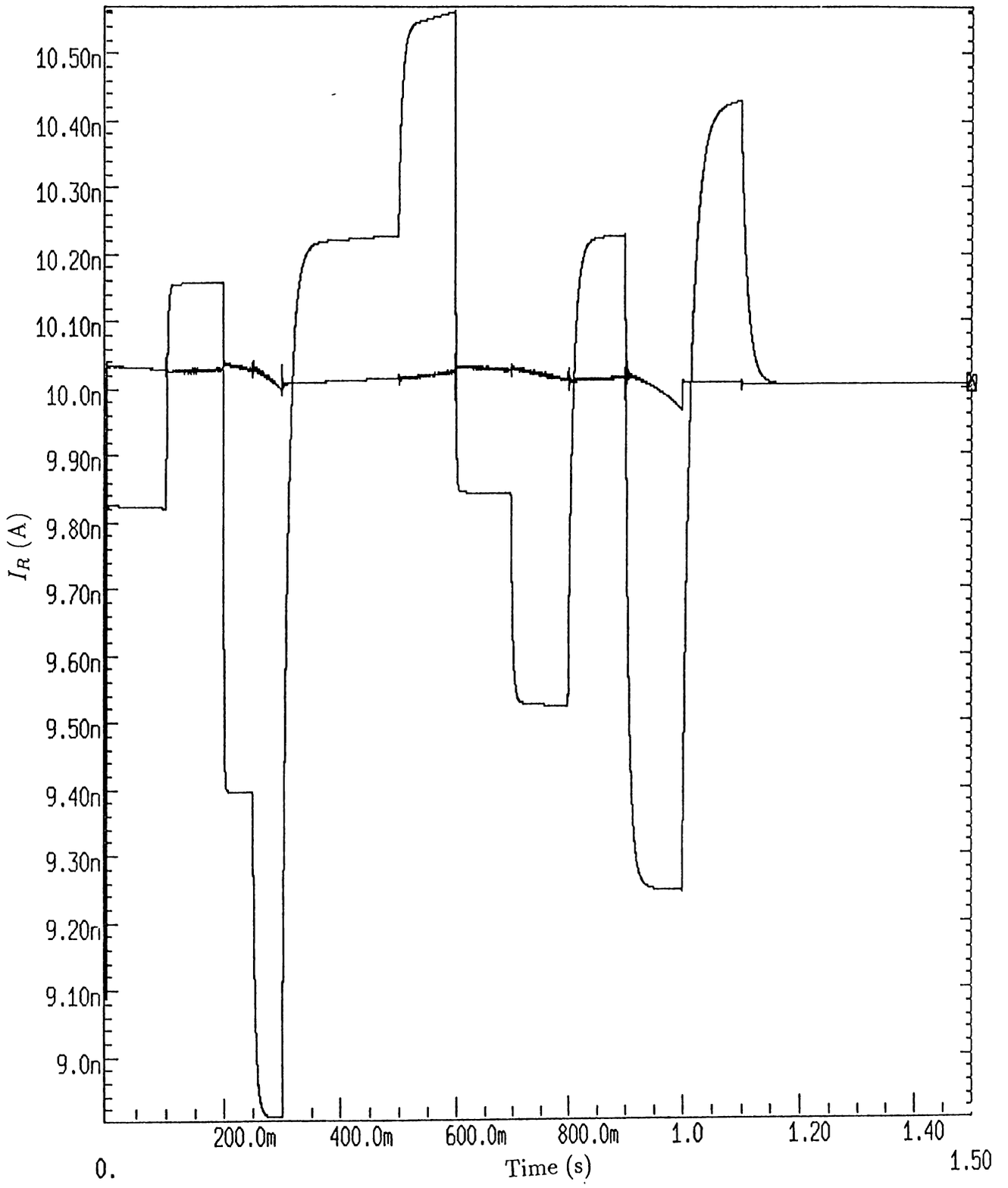

Figure 4.14: Resistive load currents with and without compensation

For convinience, the currents through the load resistance are drawn for both cases: With current compensation and without current compensation. Plot in Figure 4.14 gives the chance of comparing these currents. Circuit performance is quite satisfactory.

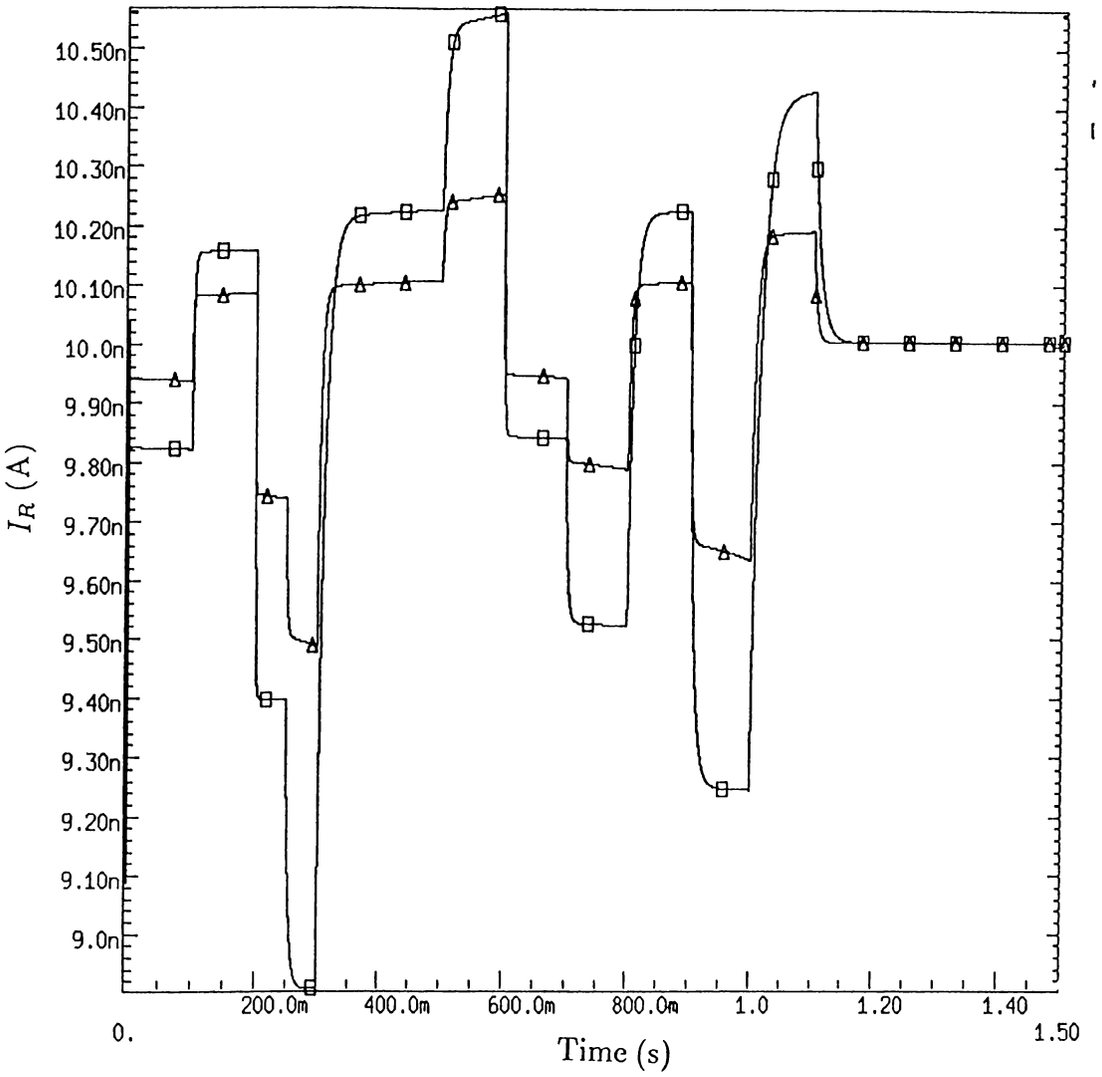

Figure 4.15: Resistive load currents with and without compensation-Effect of feedback gain

If current compensation job is not successfully achieved it is better to change the value of resistors of non-inverting amplifier slightly. To show the effect of feedback gain let's reduce it by reducing the gain of non-inverting amplifier. The feedback resistor in the amplifier is changed from $130k$ to $30k$ which means G_4 is no longer equal to 2.3 but 1.3. With this value of G_4, Equation 4.27 cannot

be satisfied and not a full capacitive current compensation can be achieved. Referring to Figure 4.15, the current generated by feedback path does not match the capacitive current exactly and hence, even if current through resistive load shrinks toward 10nA it does not have the desired shape. In order to provide a fixed 10nA current through resistive load , one must play with feedback gain.

In Figure 4.15 , the waveform with larger swing stands for the resistive load current without compensation and the other is that after compensation.

4.6.1 Feedback Model

At that step, we are ready to introduce the linear model of load capacitive current compensated current source. Main blocks of the current source are buffer, differentiator, non-inverting amplifier and voltage controlled current source. As a result of small signal analysis, it is found that all of these blocks have poles at many mega hertz. Corresponding gains of these blocks have been presented in Section 4.6. Referring to all of those information and circuit topology given in Figure 4.12 we derive the linear model shown in Figure 4.16.

For convinience some of the information given earlier will be repeated here. G_1 is the attenuation of current mirror stages from feedback connection point A in circuit of Figure 4.12 to load and is equal to 1/545. R and C are load impedance and capacitance respectively. They are both assumed to be constant throughout the analysis.

G_2 and p_2 are the gain and pole of NMOS buffer. They are equal to 0.937 and 68MHz respectively. $G_3 = 4.55 \times 10^6$ and $p_3 = 15$MHz are the gain and pole of differentiator stage. For non-inverting amplifier stage $G_4 = 2.3$ and $p_4 = 22$MHz. Finally, VCCS has the pole of $p_5 = 2$MHz and gain of $G_5 = 1/18000$.Gain stage K does not really exist but it serves for controlling the feedback gain during the stability analysis. Root-locus analysis is implemented by MATLAB using K as the gain parameter. Loop gain at which system become unstable is determined.

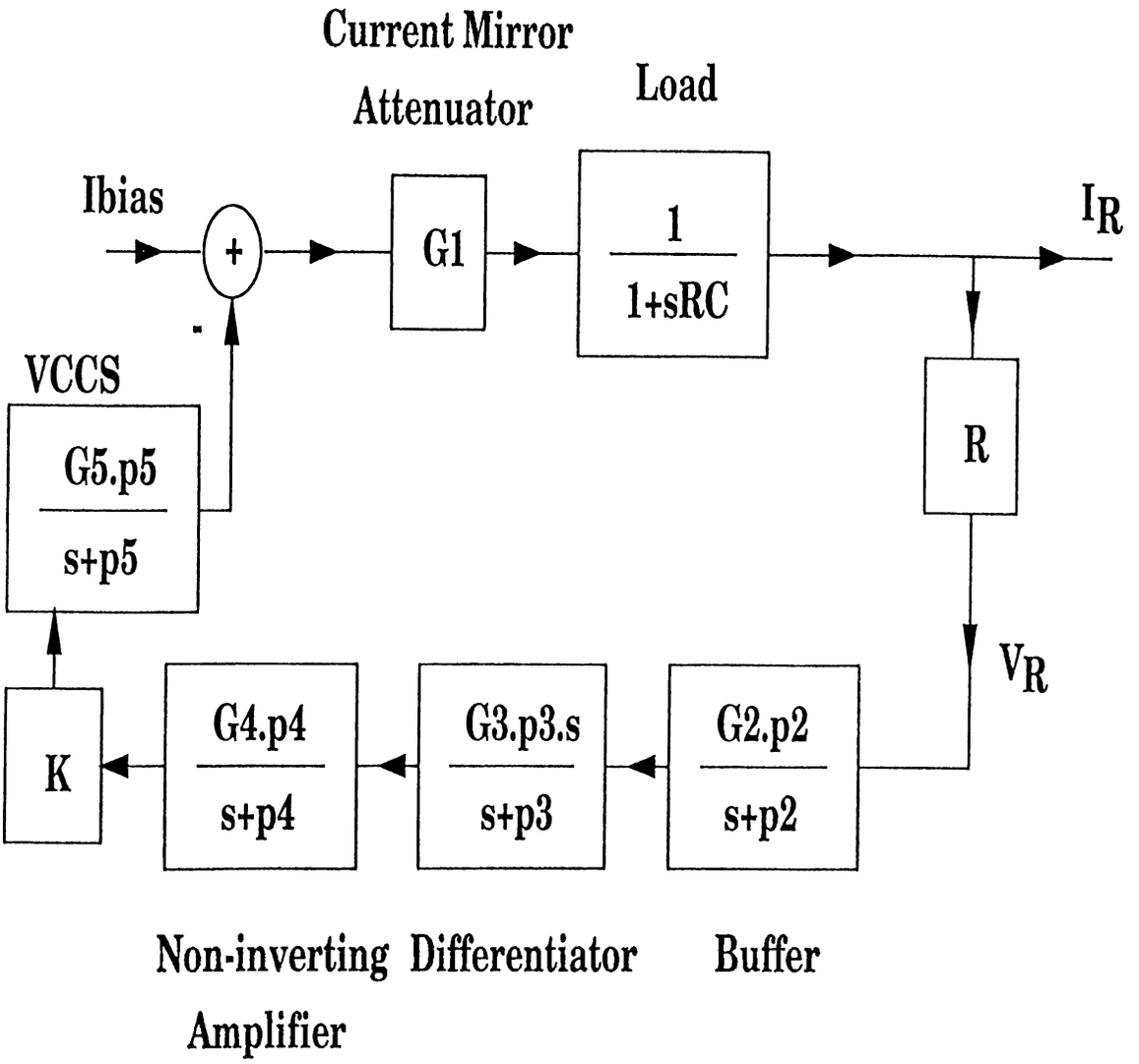

Figure 4.16: Feedback Control Model of Compensated Current Source

Figure 4.17 shows the locations of poles of overall system as K being the parameter. It is observed that the poles of final system are very close to those stated above. Dominant pole which is very close to origin, is generated by RC of the load and gets a minimum value of 50Hz when load impedance is 10M and load capacitance 2pF. Possible range of load impedance is from 4G to 8G and hence the dominant pole can move from 62.5Hz to 125Hz.

The gain K at which the real parts of the poles become positive is measured to be 7.827. Therefore, further increase in feedback gain makes the circuit unstable.

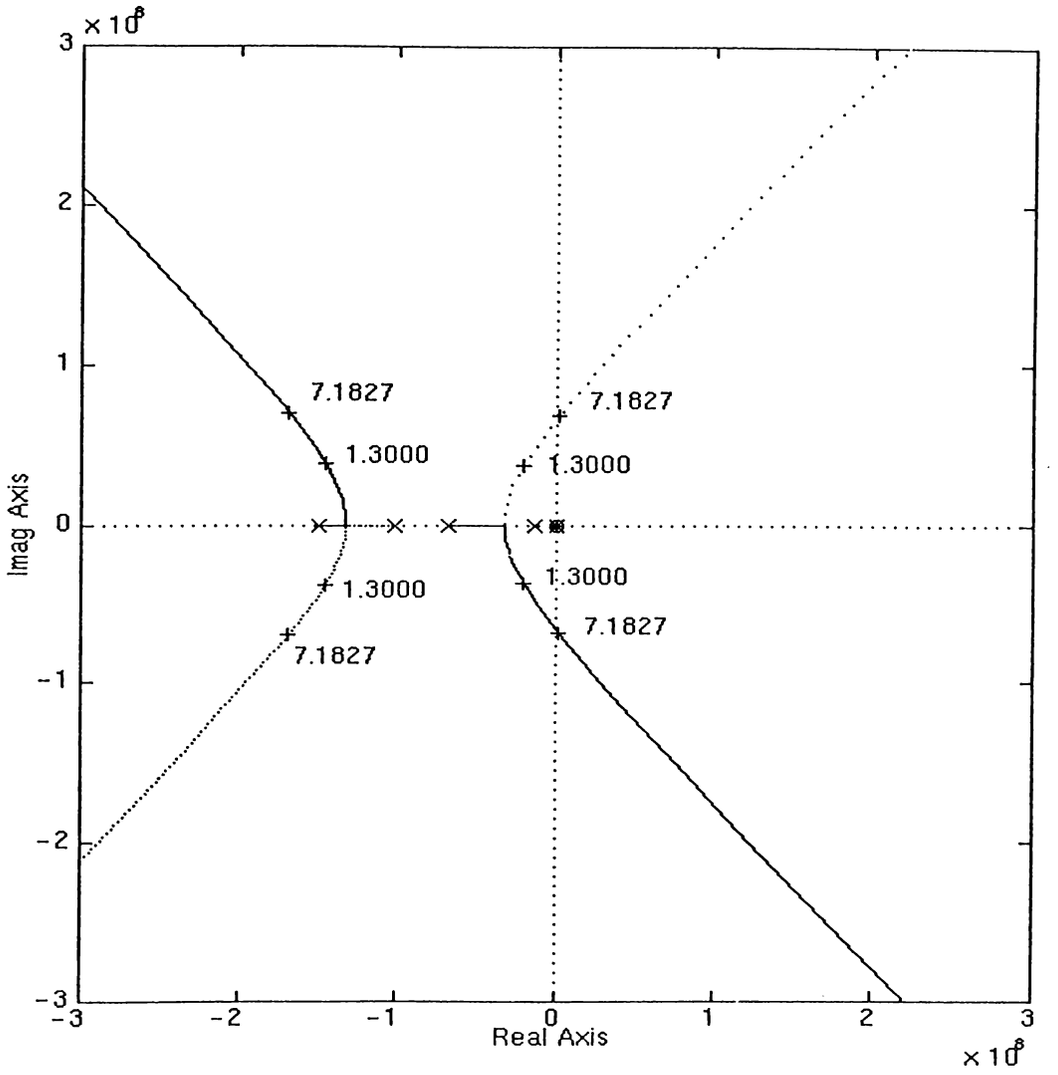

Figure 4.17: Root-Locus Analysis

In order to decide how much this result fits the original circuit, open loop gain of original current source circuit is determined by means of HSPICE simulations for different feedback gains. Phase margins will provide the necessary information for stability.

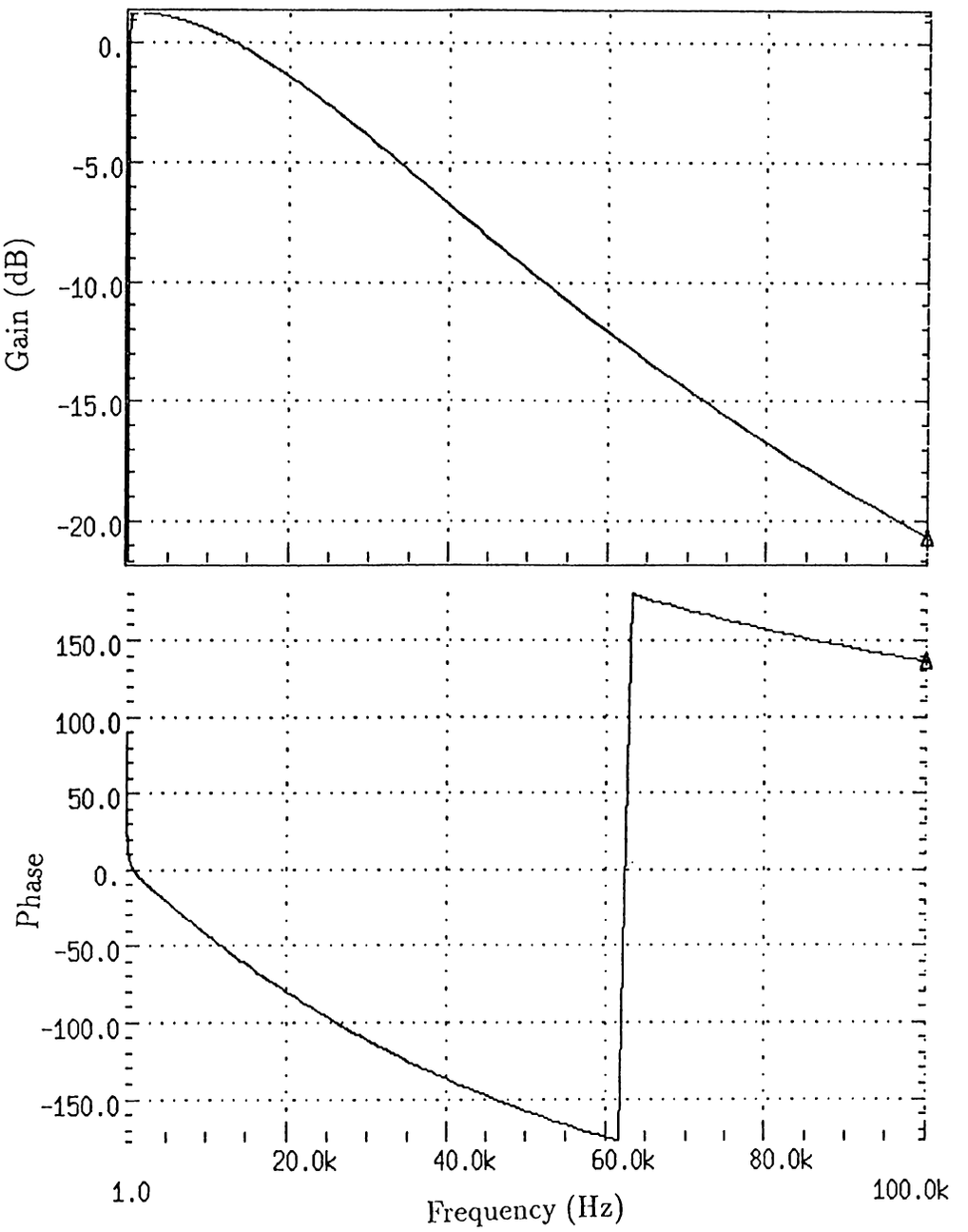

Figure 4.18: Open-loop gain of current source. (a) Gain (dB) vs. Freq (b) Phase vs. Freq - Feedback Gain(K)=1.3

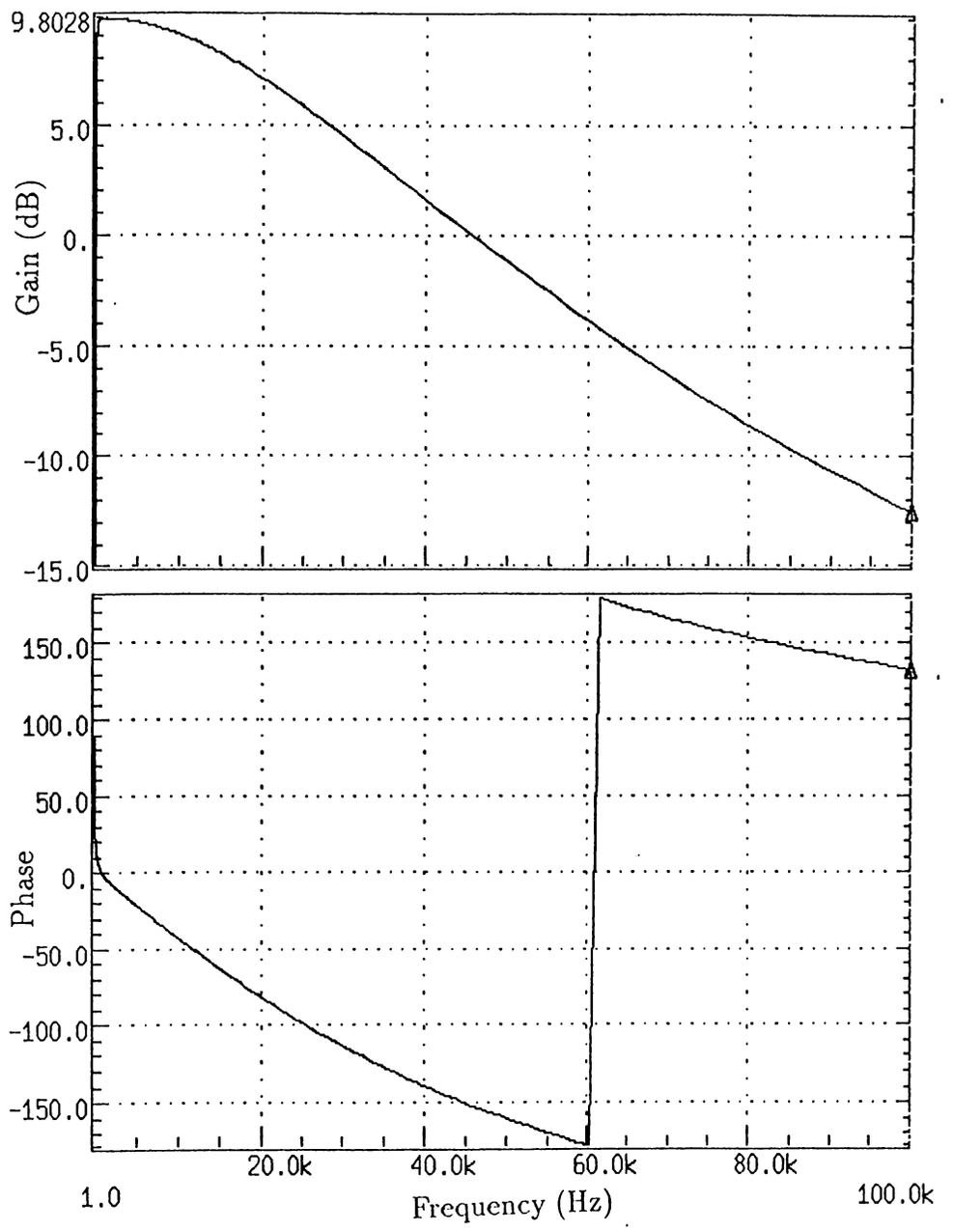

Figure 4.19: Open-loop gain of current source. (a) Gain (dB) vs. Freq (b) Phase vs. Freq - Feedback Gain(K)=3.47

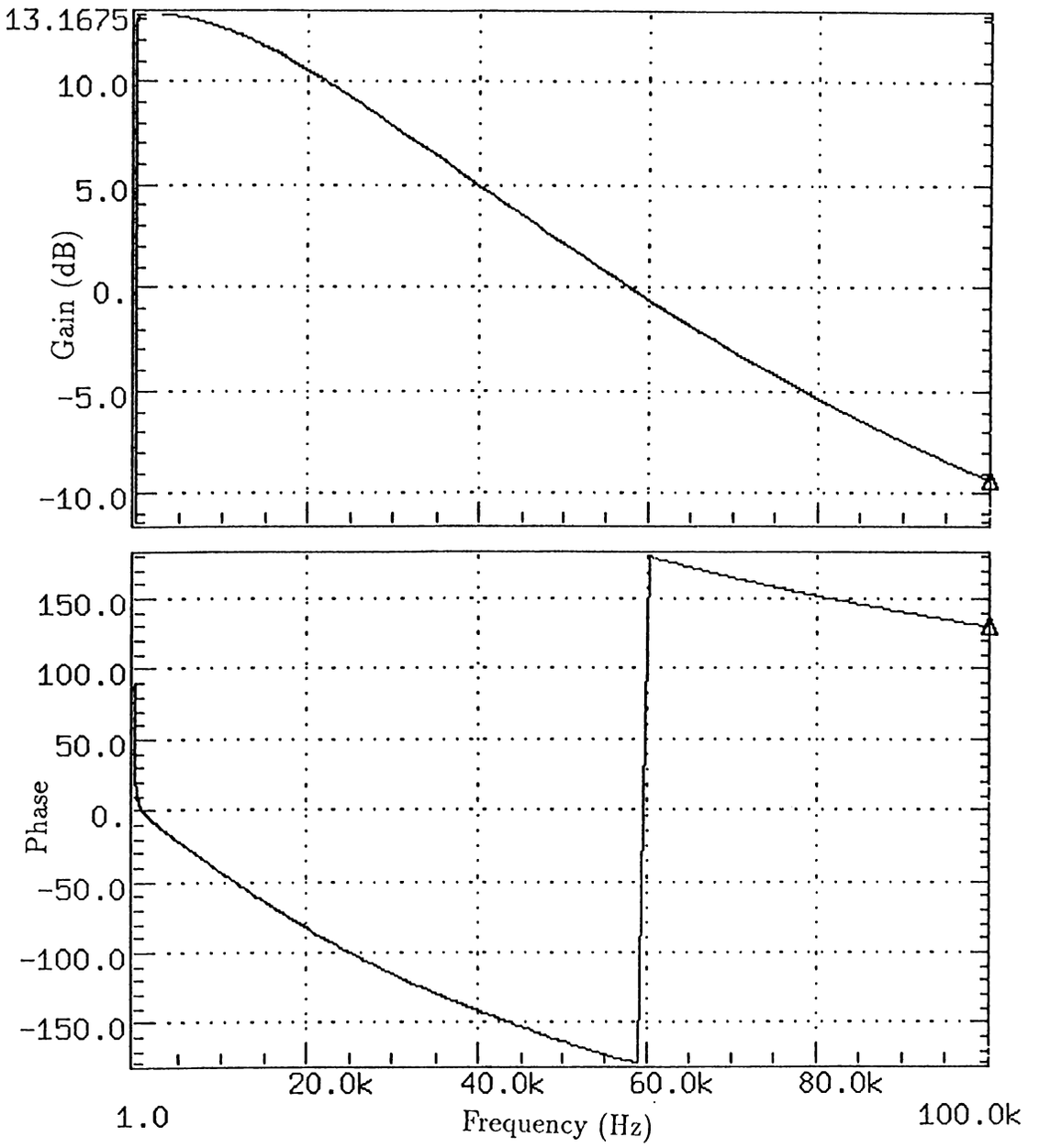

Figure 4.20: Open-loop gain of current source. (a) Gain (dB) vs. Freq (b) Phase vs. Freq - Feedback Gain(K)=5.20

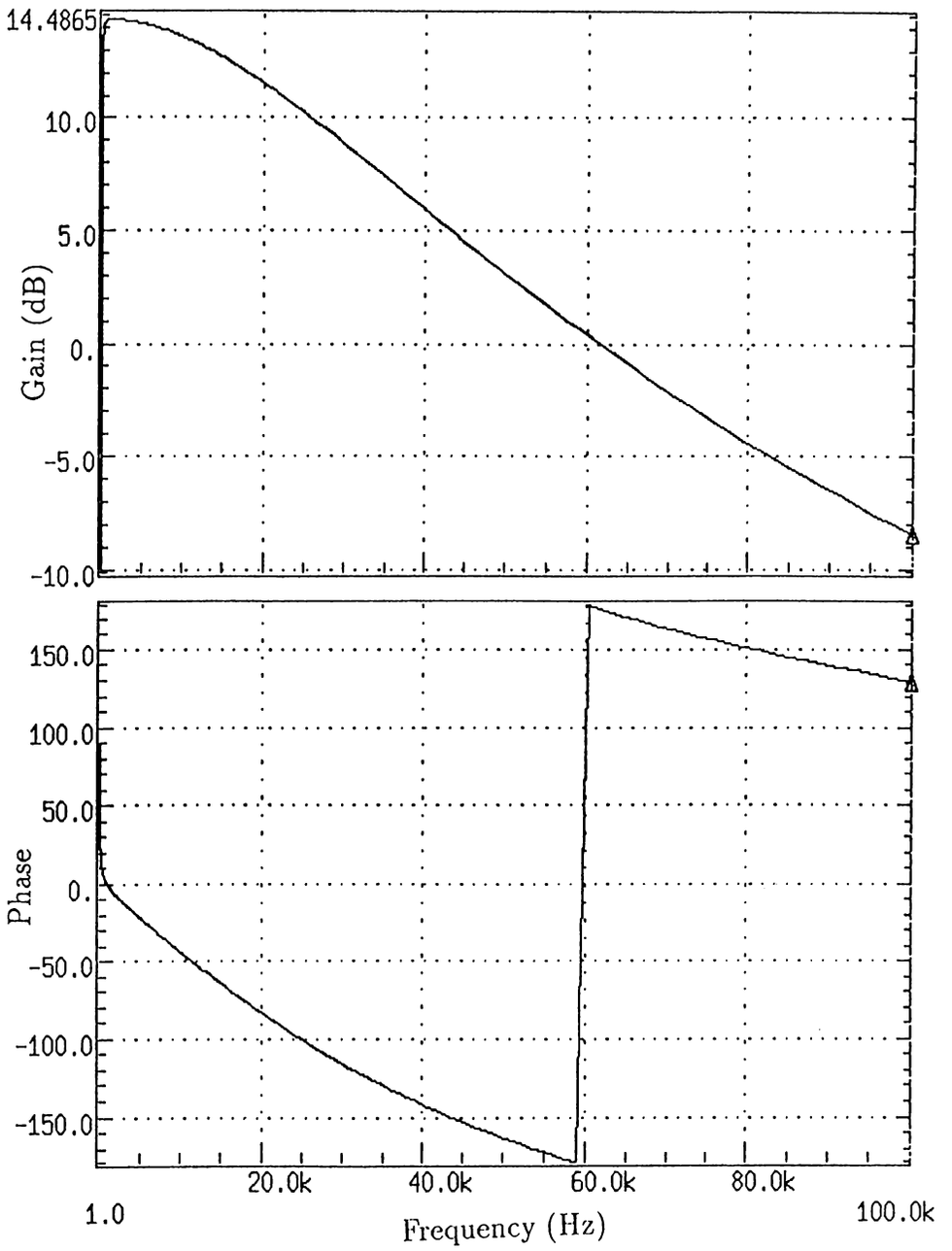

Figure 4.21: Open-loop gain of current source. (a) Gain (dB) vs. Freq (b) Phase vs. Freq - Feedback Gain(K)=5.86

Figure	Open-Loop Gain (K)	Phase Margin
4.18	1.30	125°
4.19	3.47	30°
4.20	5.20	4°
4.21	5.86	UNSTABLE

Table 4.1: Open Loop Gains and Phase Margins.

Open-loop gains and corresponding phase margins are shown in Table 4.1. Circuit become unstable whenever open-loop gain reaches the value of 5.86 for fixed value of load impedance. In fact, this result is very similar to that obtained from root-locus analysis. Comparing the gains 5.86 and 7.827, the first one is more reliable since it is obtained from the original circuit.

Chapter 5

Operational Amplifier

5.1 Introduction

An operational amplifier is one of the most versatile and widely used building blocks in linear circuit applications. Basically, operational amplifiers are direct coupled differential amplifiers with extermely high voltage gain, extremely high input impedance and very low output impedance. They are usually used with external feedback to achieve precision, gain and bandwidth control.

CMOS opamps contains NMOS and PMOS transistors all of which are operated in their saturation region. A practical opamp has a finite gain of order $60 - 120$dB at low frequencies. There is always a DC offset voltage at the output and it is in the order of μV at the input. The common mode signal amplification may not be equal to zero. This property is described by the parameter CMRR and it is a measure of opamp ability to suppress noise. The open-loop gain decreases with increasing frequency due to stray capacitances. The frequency at which open-loop gain reaches 1 is called unity-gain frequency and denoted by ω_o. Then, if the phase at ω_o is greater than $-180°$, the system will be stable. Phase margin is defined as the phase at ω_o plus 180°. Phase margin is a measure of opamp stability and must be set larger than 30°.

5.2 Circuit Topology

Circuit in Figure 5.1 is the operational amplifier used in previous chapters. The input transistors M_1 and M_2 have symmetrical structures. M_3 and M_4 are active loads and have also identical structures. They are also the governing transistors of current mirrors composed of M_3-M_5 and M_4-M_6.

M_9 , M_{10} and M_{15} operate as a current source and supply the current that makes operational amplifier work. M_7 and M_8 are also current mirrors and provide a symmetrical operation. M_3 and M_{14} creates a current mirror structure and biases the output gain stage. M_{16}-M_{17} and M_{18}-M_{19} pairs set two different source followers. They function as an output stage and a DC level shifter. These level shifters are used to obtain a zero offset at operational amplifier output.

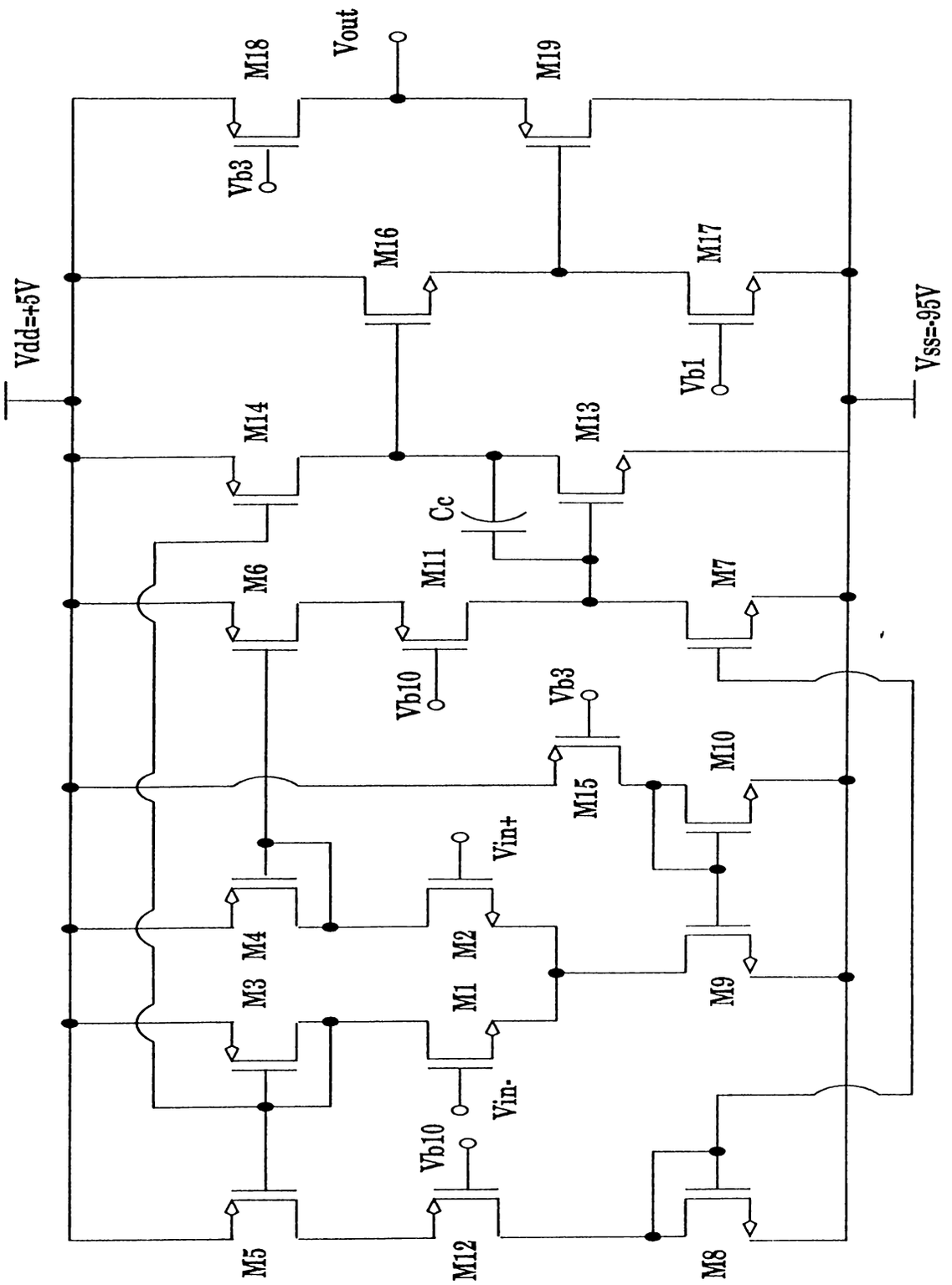

Figure 5.1: Operational Amplifier

5.3 Test of Operational Amplifier

In order use an op amp properly, it must satisfy certain specifications. The values of open-loop gain, CMRR, output impedance, phase margin, available DC range and offset voltage are important parameters and must be set appropriately.

5.3.1 Open-Loop Gain

To find the open-loop gain of operational amplifier which is given by

$$A_v = \frac{V_o}{V_{in}} \tag{5.1}$$

configuration in Figure 5.2 is used. Plot in Figure 5.3 shows open-loop gain

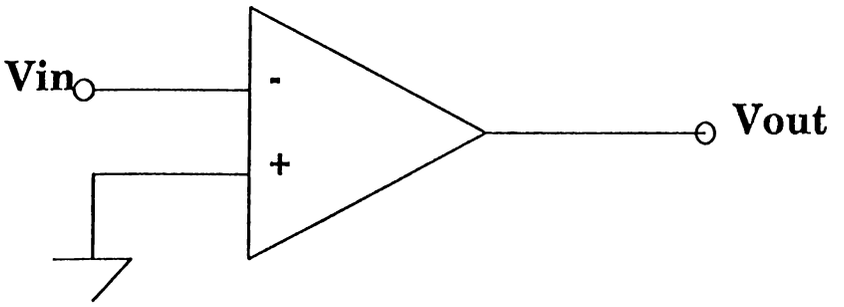

Figure 5.2: Determination of Open-Loop Gain

in dB vs. frequency. From that plot it is measured that opamp open-loop 3 dB bandwidth is

$$BW = 3.64Hz \tag{5.2}$$

Low bandwidth is due to a pole close to jw axis and that pole is generated by very high impedance nodes in the circuit. Impedances mostly determined by g_d which is given by

$$g_d = \frac{\lambda I_D}{1 + \lambda V_{DS}} \approx \lambda I_D. \tag{5.3}$$

The channel-length modulation parameter λ is set to be 1μ by founders and therefore g_d is at the level of picos. Inverse of g_d gives impedance which become a considerably high value.

Advantage of low channel-length modulation factor is that very high gains can be easily obtained. It is therefore open-loop gain is in the orders of 130dB while 3-dB bandwidth is a few hertz. But the thing which is important is GBW, gain-bandwidth product. It is given by

$$GBW = A_v(0)BW \tag{5.4}$$

and hence it is equal to almost 11.5MHz.

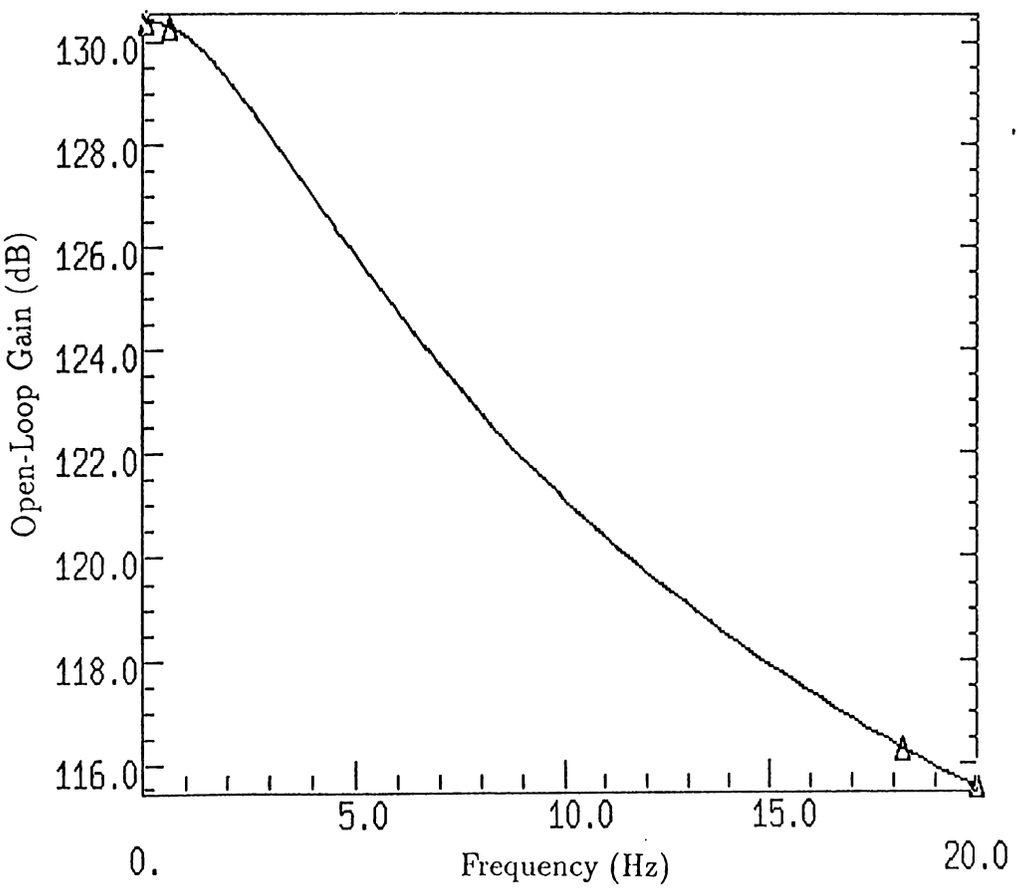

Figure 5.3: Open-Loop Gain (dB) vs. Frequency (Hz)

5.3.2 Phase Margin

(a) and (b) in Figure 5.4 shows open-loop gain and phase respectively. It is measured that the phase at unity gain is around $-150°$ and hence corresponds to a phase margin of 30°.

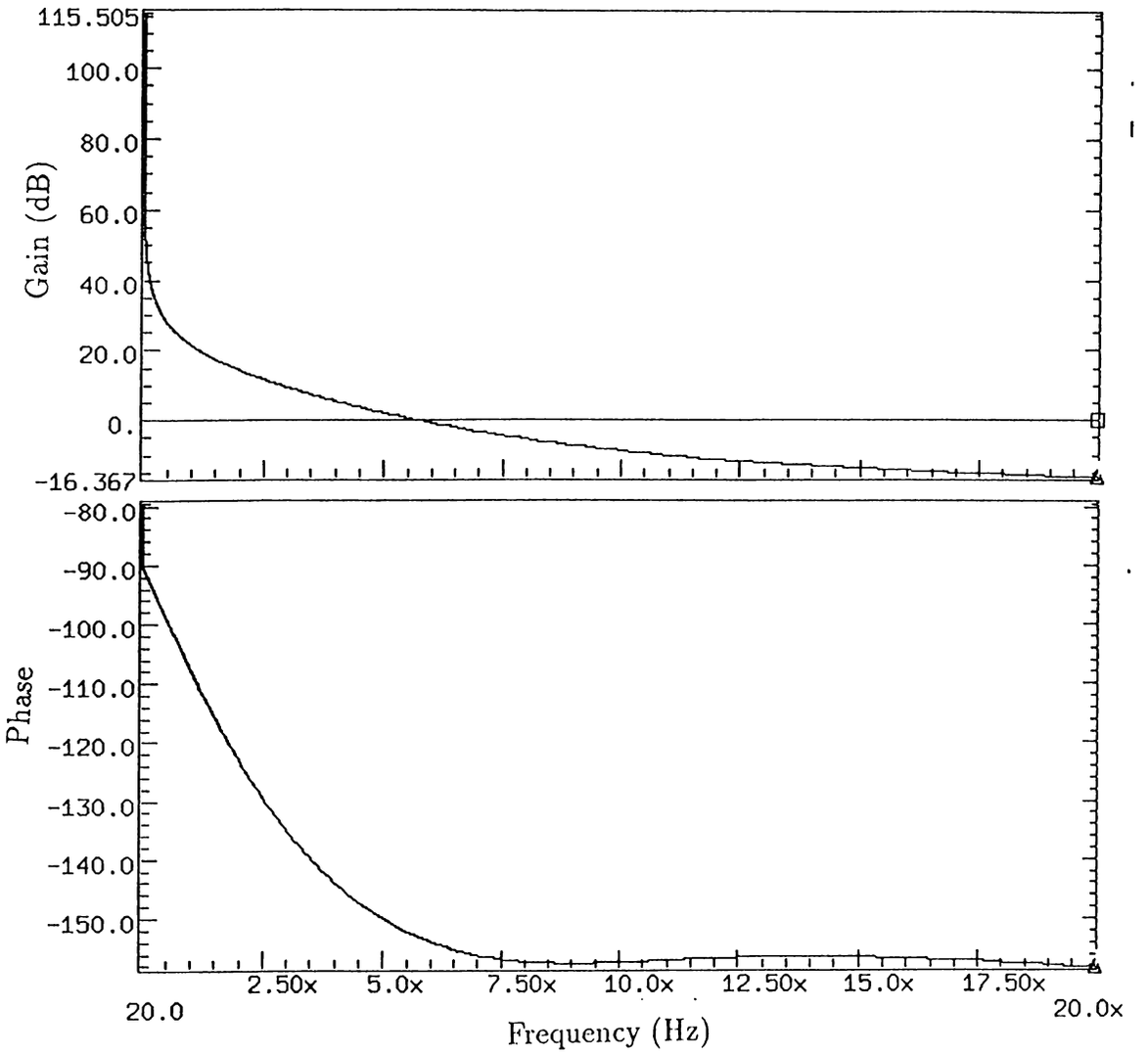

Figure 5.4: Determination of Phase Margin ; (a): Open-loop gain (dB) vs. Freq.(MHz), (b): Phase vs. Freq. (MHz)

5.3.3 Offset Voltage

To find the offset voltage, configuration in Figure 5.5 has been used. The

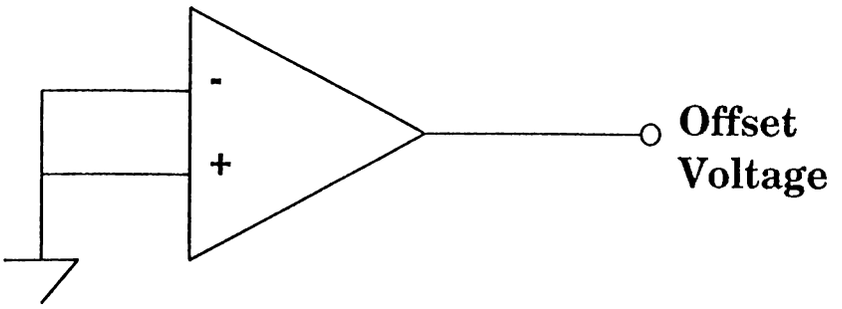

Figure 5.5: Determination of Offset Voltage

offset voltage at output is found to be $-457.81\mu V$. This corresponds to input offset voltage of $144.7pV$.

5.3.4 Output Impedance

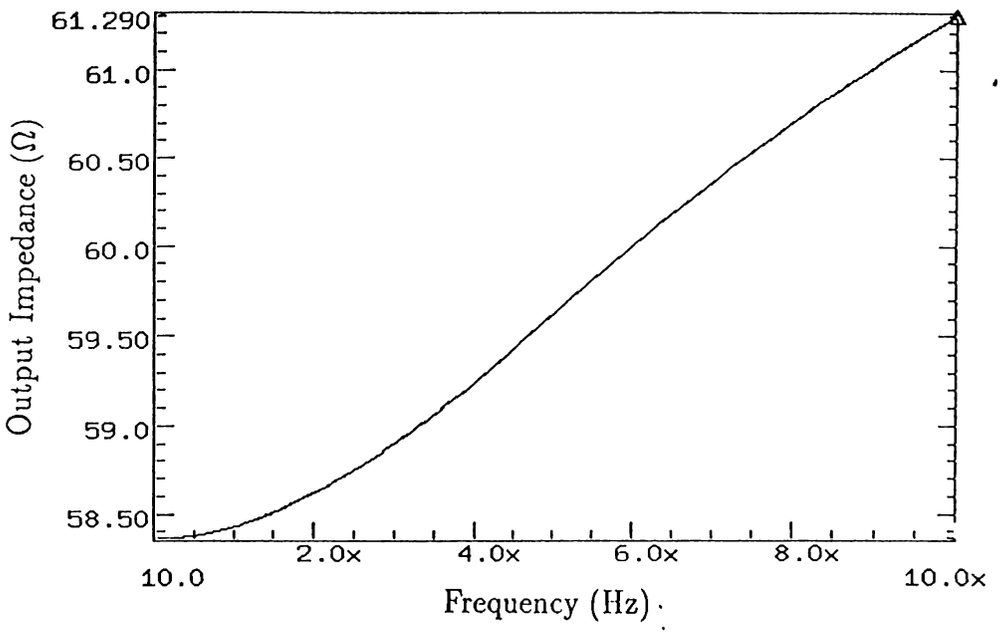

Figure 5.6: Output Impedance vs. Frequency[10Hz-10MHz]

As mentioned, the output impedance of an op amp must be low for proper operation. Plot in Figure 5.6 shows that the output impedance is around 58Ω at low frequencies.

5.3.5 CMRR

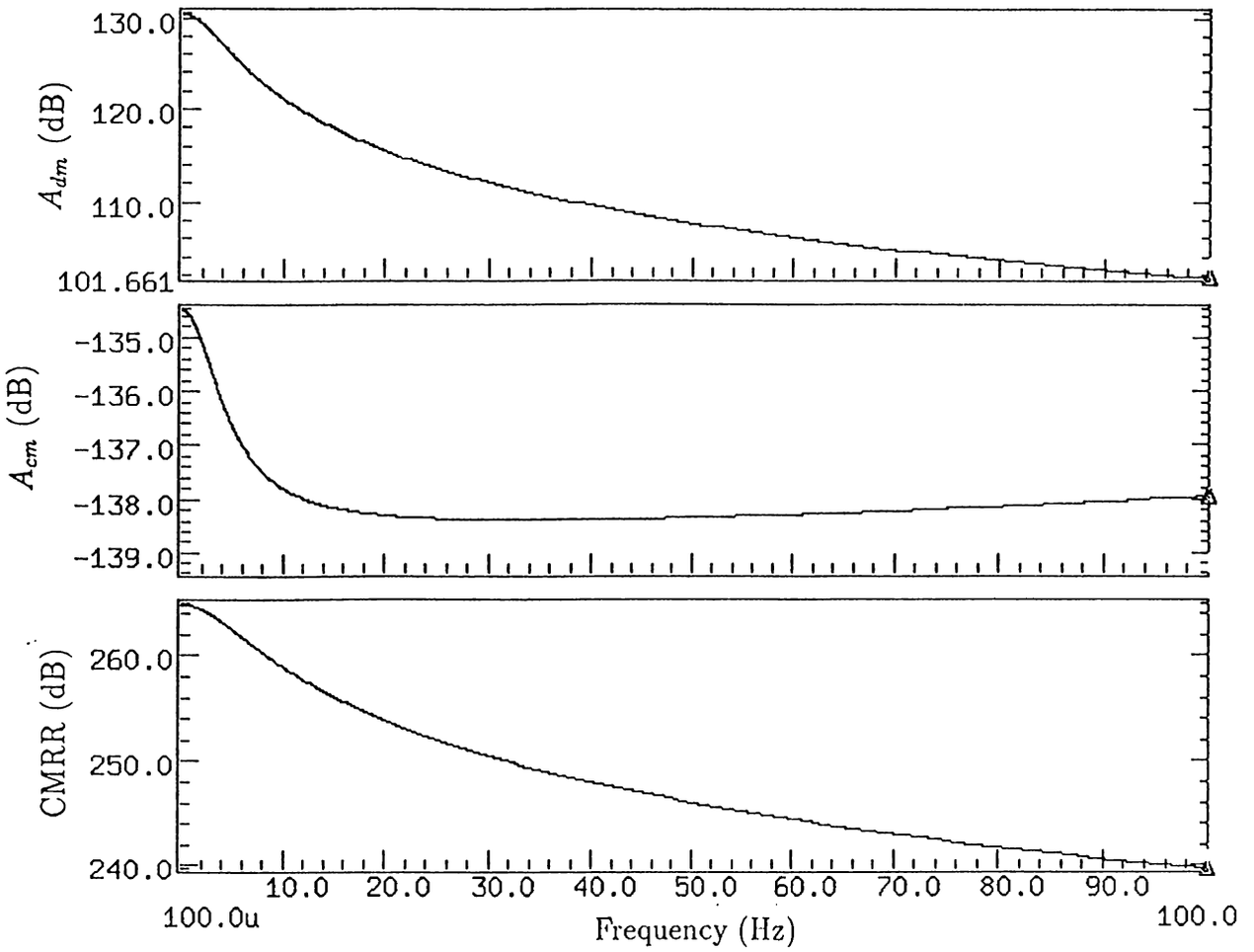

Figure 5.7: (a):Differential Mode Gain (dB), (b): Common Mode Gain (dB), (c):CMRR (dB)

CMRR of an op amp is defined to be

$$CMRR = \frac{A_{dm}}{A_{cm}} \tag{5.5}$$

where A_{dm} and A_{cm} are differential and common mode gains respectively. (a) in the Figure 5.7 shows the differential mode gain in dB. It is similar to first plot of Figure 5.4. Common mode gain in (b) is obtained by connecting the same input signal to both of inverting and non-inverting pins. Then CMRR in (c) is equal to

$$CMRR(dB) = A_{dm}(dB) - A_{cm}(dB). \tag{5.6}$$

5.4 Transistor Values

Transistor	(W/L)
M_1	200 μ /1 μ
M_2	200 μ /1 μ
M_3	21 μ /29 μ
M_4	21 μ /29 μ
M_5	21 μ /29 μ
M_6	21 μ /29 μ
M_7	20 μ /50 μ
M_8	20 μ /50 μ
M_9	20 μ /40 μ
M_{10}	20 μ /40 μ
M_{11}	100 μ /28 μ
M_{12}	100 μ /28 μ
M_{13}	50 μ /22 μ
M_{14}	184 μ /10 μ
M_{15}	131 μ /87 μ
M_{16}	220 μ /10 μ
M_{17}	20 μ /220 μ
M_{18}	209 μ /10 μ
M_{19}	250 μ /20 μ

Table 5.1: Transistor sizes of Operational Amplifier.

Transistor sizes of operational amplifier in Figure 5.1 are listed below in Table 5.1.

Chapter 6

Photodetector Design

6.1 Introduction

A photodetector is a device that measures photon flux or optical power by converting the energy of photons into another measurable form. The absorption of a photon by an intrinsic photoconductor results in the generation of an electron-hole pair. The application of an electric field to the material results in the transport of both electrons and holes through the material and hence an electric current in the circuit of detector is produced.

The semiconductor photodiode detector is a p-n junction structure. Photons absorbed in the depletion layer generate electrons and holes which are subjected to an electric field. Two carriers drift in opposite directions and induces an electric current in the external circuit. The photo-generated current is always opposite to forward diode current. Since the electric field outside the depletion region is very small, electrons and holes generated far away from the depletion region wander randomly until they recombine. Electron and hole pairs generated in the vicinity of depletion region may contribute to the current by diffusion process. Outside the depletion region, only the electrons and holes generated within a diffusion-length distance might be effective on

photo-current.

Another photodetector of interest is the Metal-Semiconductor-Metal photodetectors (MSM-PD) which have shown a great promise over the past few years in design of optoelectronic receivers. Their cruical feature is the compatibility with the field-effect transistor process technology. Due to low parasitic capacitances, an MSM-PD is advantagous for high speed and low noise operations. Even though the quantum efficiency is lower than that of a vertical p-i-n diode because of shadowing of interdigitated fingers, MSM-PD's still lead to larger bandwidth product. The quantum efficiency can be increased in expense of bandwidth. MSM-PD structures allow the designer to control detector characteristics. It is as much easy as changing finger spacing or finger widths. An observed property of MSM-PD's is that their sensistivity increases with an increase in applied bias before breakdown occurs. Note that increased sensitivity is advantegous for better signal detection.

The performance of a photedetector is characterized by quantum efficiency, responsivity and response time. The PDs designed will be tested in terms of these parameters.

6.2 Photodetector Structure

One important parameter to be considered for a photo-detector is quantum efficiency, η. It is defined as the probability that a single photon incident on the device generates a photocarrier pair that contributes to the detector current. Not all incident photons can produce electron-hole pairs because some might be reflected from the semiconductor surface. Also some electron-hole pairs generated may recombine prior to their collection by electrodes. Finally, if the light is not properly focused on active area, some photons will be lost. The quantum efficiency, therefore strictly depends on device parameters, structure and light. Also, the quantum efficiency, η, is a function of wavelength because the absorption coefficient depends on wavelength.

Specifically, the quantum efficiency of a PD is given by:

$$\eta = (1 - r)(1 - \exp(-\alpha d)) \tag{6.1}$$

where

r Fresnel Reflectivity

α Absorption Coefficient

d Thickness of the Absorption Layer.

Therefore, the efficiency of PDs can be inreased by using anti-reflective coating by which more of the photons can be absorbed. Fresnel reflectivity r shows this fact.

Another way of describing quantum efficiency is the following:

$$\eta = \frac{I_{ph}/q}{P_{inc}/h\vartheta} \tag{6.2}$$

where

I_{ph} Photo-current

I_{ph}/q Number of carriers collected to produce photo-current

P_{inc} Incident optical power

$h\vartheta$ Photon energy

$P_{inc}/h\vartheta$ Number of incident photons.

Hence η means the number of carriers generated by a single photon. Another important parameter that characterize a PD is responsivity. The responsivity is the relation between the incident optical power and the electrical current generated. If every photon generates η electrons and photon flux per second is given by Φ then the electron flux becomes $\eta\Phi$. Then

$$I_{ph} = q\eta\Phi \tag{6.3}$$

Also the incident power can be written as

$$P_{inc} = h\vartheta\Phi. \tag{6.4}$$

Combining equations 6.3 and 6.4

$$I_{ph} = \eta\frac{qP_{inc}}{h\vartheta} = \mathcal{R}P_{inc} \tag{6.5}$$

where

$$\mathcal{R} = \eta\frac{q}{h\vartheta}(A/W). \tag{6.6}$$

Therefore, responsivity is described to be the current produced by unit incident optical power. In free space, this is equivalent to

$$\mathcal{R} = \eta\frac{\lambda_0}{1.24}(A/W). \tag{6.7}$$

λ_0 is the wavelength of incident light in μm. Referring to Equation 6.7, responsivity increases with wavelength λ_0 because detectors give response to photon flux rather than to the optical power. For higher values of λ_0, optical power of

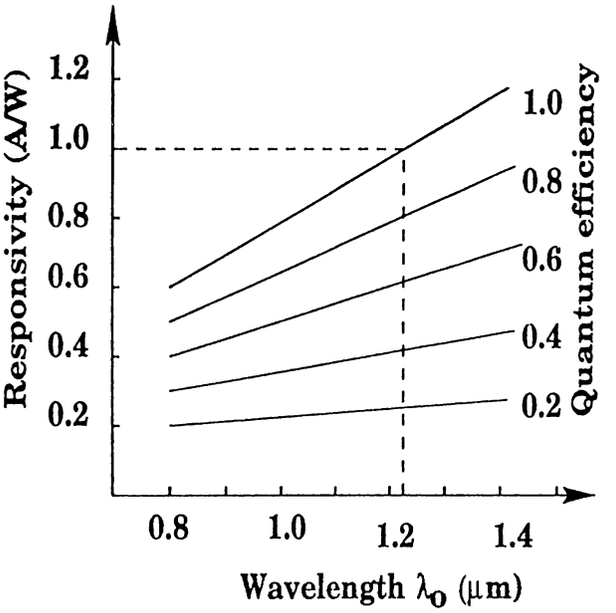

Figure 6.1: Responsivity (A/W) versus Wavelength (μm)

a single photon is lower. Hence, the same amount of optical power is carried by more photons, which in turn produce more electron-hole pairs. But it must be

noticed that the region over which $\mathcal{R}$ rises with λ_0 is limited by the wavelength dependence of quantum efficiency. At wavelengths above a certain value, $\mathcal{R}$ falls drastically.

Responsivity versus wavelength λ_0 with quantum efficiency η as a parameter is drawn in Figure 6.1. It is evident that responsivity corresponding to wavelength 1.24μm and $\eta = 1$ is unity. However, for sufficiently large λ_0, quantum efficiency gets smaller because absorption cannot occur when $\lambda_0 \geq \lambda_g = hc_0/E_g$. The wavelength λ_g is the long-wavelength limit of the semiconductor. $E_g = 1.11eV$ is the bandgap energy of silicon and the value of $\lambda_g = 1.15\mu$m.

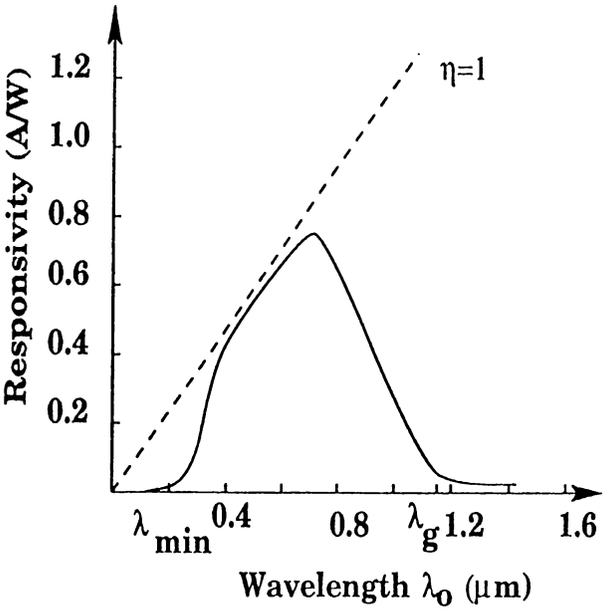

Figure 6.2: Responsivity (A/W) versus Wavelength (μm). Effect of higher and lower wavelengths.

For sufficiently small values of λ_0, quantum efficiency also decreases because most of the photons are absorbed near the surface. The absorption coefficient α is inversely proportional to wavelength and gets very high values for low wavelengths. Due to very high densities of photo-generated carriers near the surface, recombination lifetime becomes quite short and the photocarriers recombine before they are collected. Figure 6.2 describes this wavelength dependence of responsivity.

The photodetector structure used is shown in Figure 6.3. The PD shown is called p^+/n photodiode. It is advantageous to use this PD in CMOS process

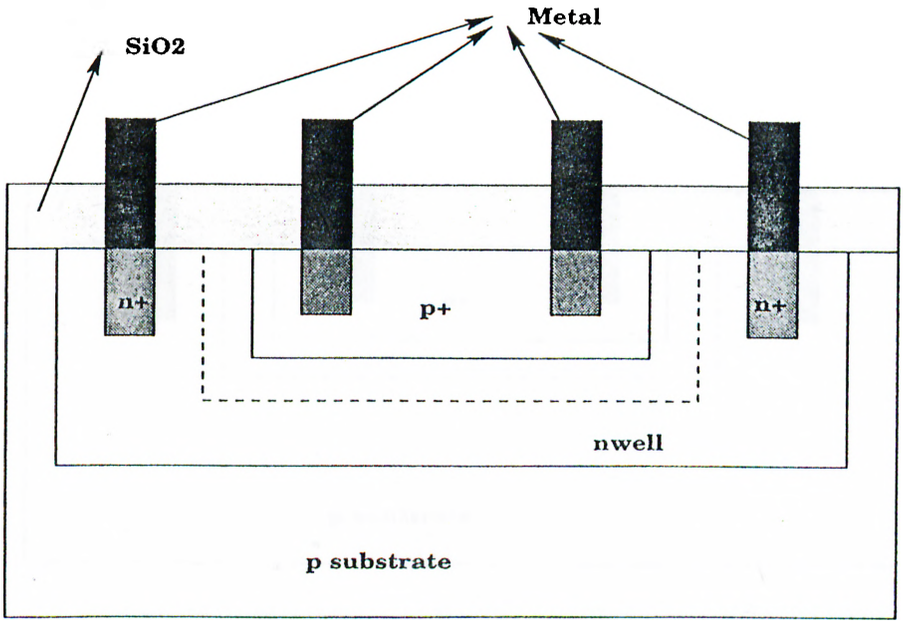

Figure 6.3: p+/n Photodetector

because it is isolated from common p-substrate by n-well by which no noise contribution to the MOS transistors in the same chip is provided.

In p^+/n photodiode, a depletion region is formed between p^+ region and n-well. Since the density of acceptor atoms are much larger than the density of donor atoms, depletion region expands more into n-well. When the detector is illuminated, photons are absorbed mainly in the depletion region. In addition, one must take care of the generation of electron and hole pairs at a diffusion length distance from the depletion region. The depth of the p^+ region is given to be 0.3μm by the Orbit SCNA20 Mosis process, which is used to fabricate the detector chip. Diffusion lengths are $L_n = 0.35\mu$m and $L_p = 21\mu$m. Since diffusion length of p-type region is much larger than the depth of p^+ region, electron-hole generation in p^+ region is fully taken into account. In n-well, L_p must also be added to the depletion region width.

Under same conditions, p^+/p photodiode in Figure 6.3 is expected to be more efficient than n^+/p photodiode since it can use more of the incident power to generate electron-hole pairs. This is because, $L_p = 21\mu$m directly

adds to depletion region width in the p-substrate and enlarges the effective area considerably. This additional expansion is only $L_n = 0.35\mu$m for p^+/p photodiode.

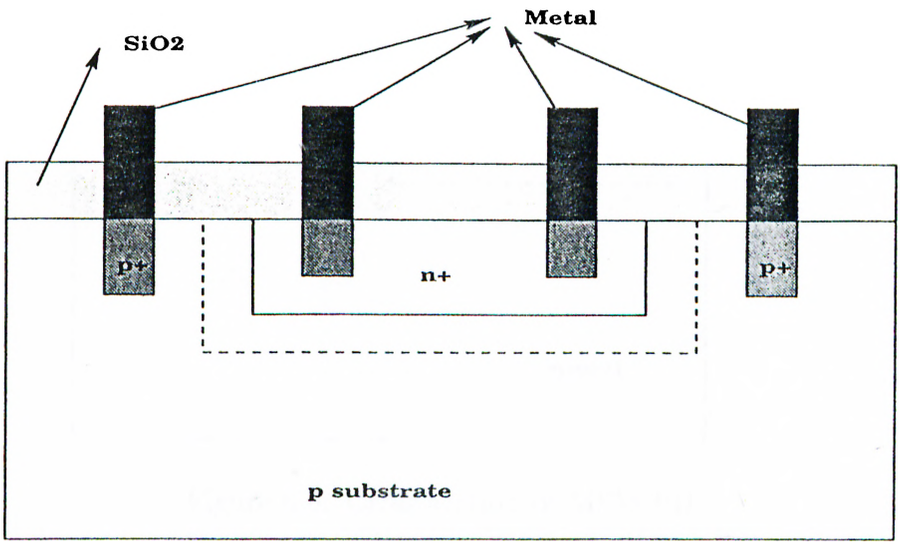

Figure 6.4: n+/p Photodetector

Figure 6.5 shows basic MSM-PD structure. Referring to that figure, a bias is applied between the contacts and an electric field is generated. Note that the contacts between the silicon substrate and the metal electrodes are Schottky contacts. When photons are absorbed by the semiconductor surface ,

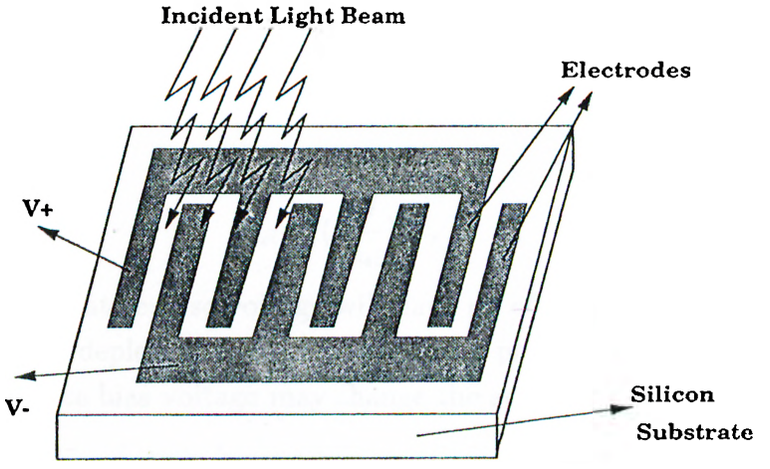

Figure 6.5: Structure of Basic MSM-PD

mobile charge carriers are generated. The electrical conductivity of the material

increases in proportion to photon flux. The available electric field between the fingers transports electron and hole pairs and they are collected at electrodes.

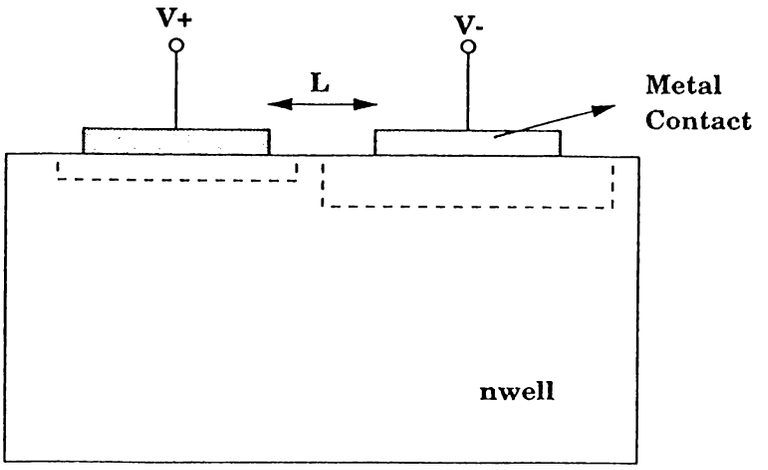

Figure 6.6: Cross-section of MSM-PD

Actually, MSM-PD shown in Figure 6.6 is two Schottky barriers connected back-to-back. When a potential difference is created between the metals, Schottky diode at positive supply side is forward biased while the other is reverse biased. Depletion regions are formed under both metals but that under reverse biased side is larger. The widths of the depletion regions depends on the reverse bias applied. When the detector is illuminated, electron-hole pairs generated in the depletion region is collected by the electrodes. As reverse bias rises, the width of depletion region enlarges and the amount of photo-current generated increases. At a specific reverse voltage, depletion widths consume the whole length L and punch-through occur. The value of that reverse voltage is given by:

$$V_R = (\frac{qN}{2\epsilon_{si}})L^2. \tag{6.8}$$

Further increases at reverse voltage will have no effect on the amount photo-current since the depletion regions cover all the photo-sensitive area. But the increase at reverse bias voltage may change the speed of carrier collection.

I-V characteristic in Figure 6.7 shows how an MSM-PD gives response to an incident optical power as applied reverse bias is changed. The amount of reverse bias voltage to reach the punch-through depends mainly on the displacement of metal contacts and the doping density of substrate.

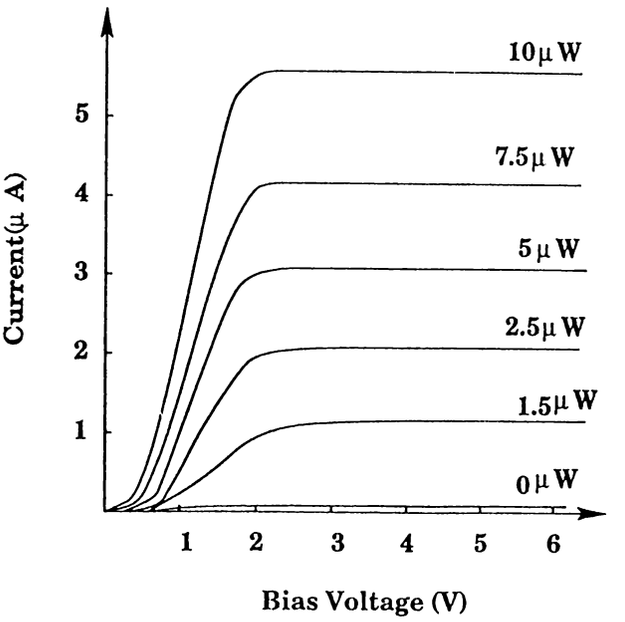

Figure 6.7: I-V characteristics of an MSM-PD under different light powers.

Specifically, the quantum efficiency of an MSM-PD is given by:

$$\eta = (1-r)\frac{s}{s+w}[(1-\exp(-\alpha d)] \tag{6.9}$$

where

r Fresnel Reflectivity

w Finger Width

s Finger Spacing

α Absorption Coefficient

d Thickness of the Absorption Layer.

By means of anti-reflective coating, the number of photons reflected can be decreased. Fall in r will cause the quantum efficiency increase. Finger spacing is one of the dominant parameters. Increase in finger spacing will generate more photo-sensitive area and hence will increase η. But now, it takes relatively more time to collect photo-generated electron and hole pairs. In other words

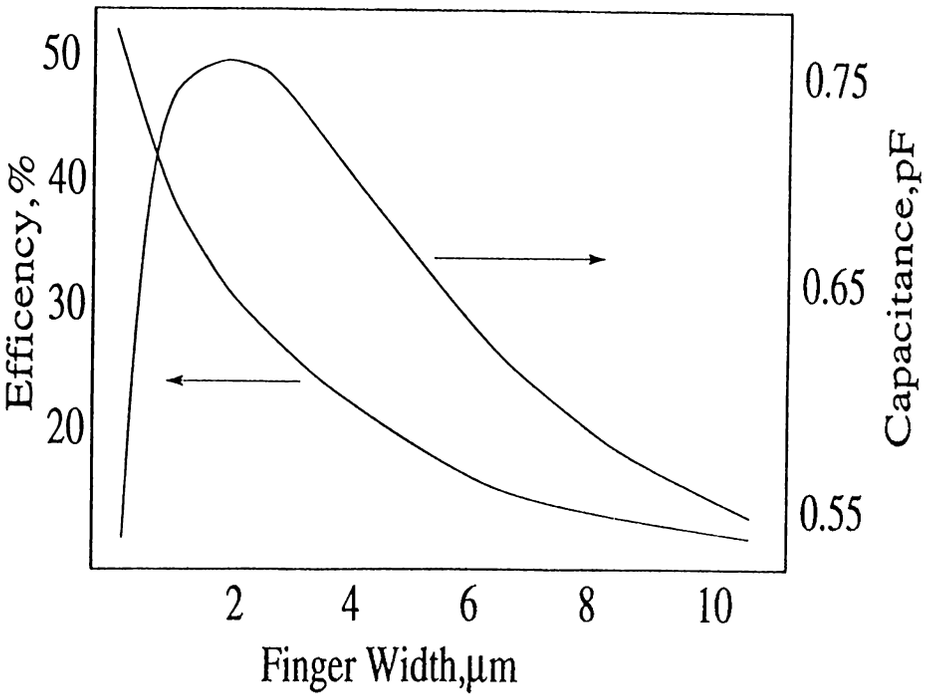

Figure 6.8: Finger Width dependece of Quantum Efficiency and Capacitance

bandwidth will decrease. One needs to optimize finger spacing using the trade-off between bandwith and the η. Similarly, decrease in finger width w also increases η since more active area become available.

The capacitance between the finger widths affect the response time. For a detector area of $300\mu m \times 300\mu m$ and finger spacing of $s = 4\mu m$, quantum efficiency and total capacitance against the finger width is plotted in Figure 6.8 [10]. The total capacitance is directly proportional to the number of fingers and finger width. As finger width increases, total capcitance first increases but afterwards it start to fall because of fall in number of fingers associated with large finger width. Also, less and less photsensitive area remains with increasing finger width and therefore quantum efficiency falls accordingly.

6.3 Test of PD

In order to test the performance of photodetector, an experiment set-up as shown in Figure 6.9 is prepared. The photodetector under test is fabricated using the Orbit SCNA20 Mosis process. Laser beam generated by the source is $50mW$ and directly incident onto neutral density filter which reduces the level of power. Reduced power is then focused onto the chip including the PD under test. The radius of the incident light beam is almost $800\mu m$. The incident

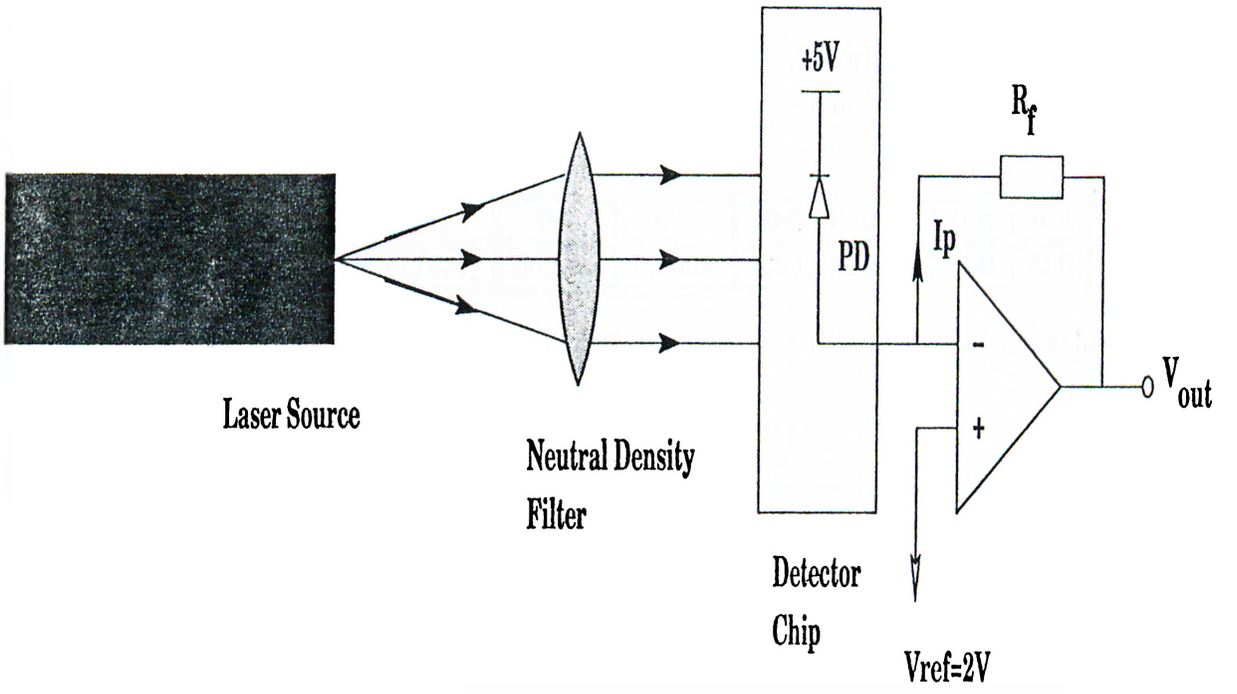

Figure 6.9: Experiment Setup for Performance Measurement of PD

power is absorbed by depletion regions under the p^+ region and at side-walls of it. Diffusion lengths must be added to depletion region widths. Taking the detector surface to be $x = 0$ reference and the direction inside the detector to be positive direction, fraction of photon power absorbed under p^+ region and at its side walls is given by:

$$\xi = \frac{\int_0^{x_{p+}+x_n+L_p} \exp(-\alpha x)dx}{\int_0^{\infty} \exp(-\alpha x)dx} = 0.401 \qquad (6.10)$$

where $x_{p+} = 0.3\mu$m is the depth of p^+ region. $L_n = 0.35\mu$m is the diffusion length at n-side. x_n is the depletion region width at n-side and given by:

$$x_n = \frac{N_A}{N_A + N_D}[\frac{2\epsilon_{si}}{q}(\frac{1}{N_A} + \frac{1}{N_D})(V_{bi} + V_r)]^{1/2} = 30\mu m \tag{6.11}$$

$N_A = 2 \times 10^{18}/cm^3$ and $N_D = 5.5 \times 10^{16}/cm^3$ is set by foundry. $\epsilon_{si} = 11.7\epsilon_0$ where $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm. $V_r = 3V$ is the applied reverse bias. Built-in voltage V_{bi} is found from

$$V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2}) = 0.882V \tag{6.12}$$

where $V_T = 26mV$ and $n_i^2 = 2 \times 10^{20}/cm^6$. Absorption coefficient $\alpha = 100(1/cm)$ is used. It is actually wavelength dependent and given by

Wavelength, λ (μm)	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Absorp. Coeff., α (1/cm)	50,000	10,000	4,500	2,000	950	350	110

Table 6.1: Absorption Coefficient of Silicon for Different Wavelengths.

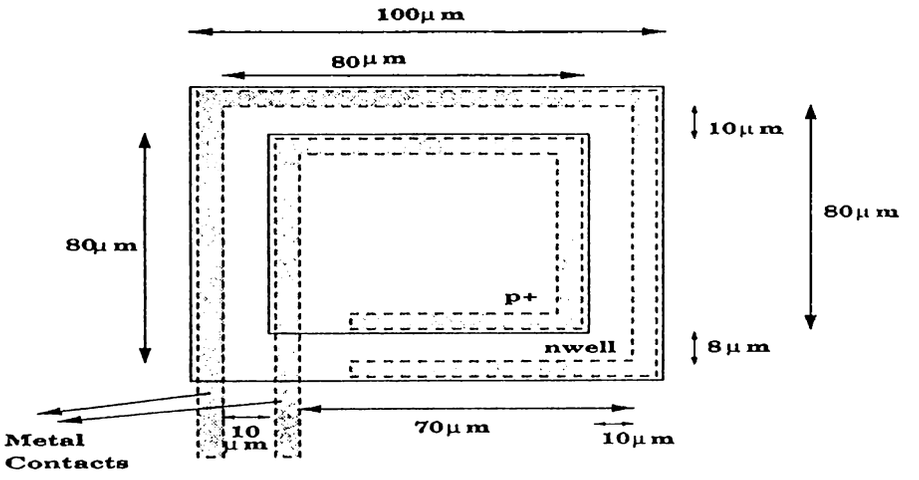

Figure 6.10: Layout dimensions of p^+/n photodetector

One of the effective areas of photodetector is p^+ region which has an area of 60×60. In addition to that, the area at sides which has a value of $80 \times 12 + 80 \times 10 \times 2 + 70 \times 8 = 3120$. Amount of power focused onto the chip after

density filter is varied and quantum efficiency is calculated. The diameter of the power beam is measured to be 80μm and it is directly focused onto the phodetector. The wavelength of the incident light beam is 633nm. The output voltage of transimpedance amplifier in Figure 6.9 is measured with feedback gain resistance of $R_f = 4.7k\Omega$. Responsivity is calculated using

$$\mathcal{R} = \frac{I_{ph}}{P_{inc}} = \frac{V_o/R_f}{P_{inc}}. \tag{6.13}$$

The results of responsivity and quantum efficiency calculations are presented below in Table 6.2. To find the impulse response of the photodetector chip,

$P_{inc}(\mu W)$	Output Voltage (mV)	$I_{ph}(\mu A)$	R	η
331	380	80.85	0.2443	0.4782
215	250	53.19	0.2474	0.4844
120	140	29.78	0.2482	0.4861

Table 6.2: Responsivity and Quantum Efficiency calculations for R_f = 4.7k and λ_0 = 633nm

a laser impulse train of 20Hz is made incident on the chip. The response of PD to a single impulse is shown in Figures 6.11 and Figure 6.12 for incident power of $465nW$ and $397nW$ respectively. Transimpedance amplifier gain is chosen to be 10^7.

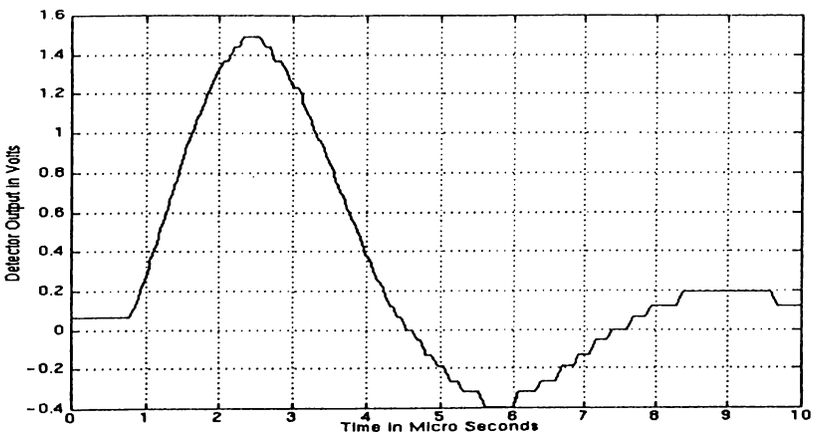

Figure 6.11: Impulse Response for Incident Power of $465nW$ and $R_f = 10M\Omega$

(n+/p) Photo-detector

Pinc	Output(mV)	Ip(e-6)	Resp.	Quan. Eff.
100	45	6.60	0.066	0.1296
369	135	19.85	0.054	0.1066
496	208	30.58	0.062	0.1210
695	301	44.26	0.064	0.1247

(p+/n) Photo-detector

Pinc	Output(mV)	Ip(e-6)	Resp.	Quan. Eff.
98	167	24.55	0.2506	0.4909
279	465	68.38	0.2451	0.4801
525	904	132.96	0.2526	0.4948
620	1128	165.21	0.2669	0.5228

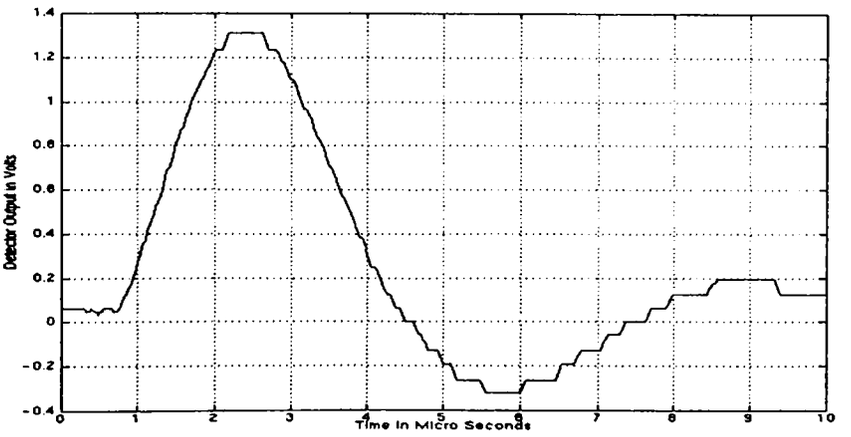

Figure 6.12: Impulse Response for Incident Power of $397nW$ and $R_f = 10M\Omega$

From those figures it is observed that pulse width is around $3\mu s$ and hence this detector can be used upto 300kHz.

We couldn't test MSM photo-detectors. Metal fingers in a MSM-PD must be placed below the SiO_2 layer but in our chip containing MSM-PDs metal fingers are placed above the SiO_2 layer mistakenly. Only test results of p^+/n PD has been presented.

Chapter 7

CONCLUSION

In this thesis, an integrated circuit of low-level high-voltage current source has been presented. The current source is designed to drive the cantilever tips of Atomic Force Microscope. In fact, cantilever tips commonly encounter a load impedance of $4 - 8G\Omega$ and must be driven by a current source of 10nA. That is to say, the current source must supply the currrent of fixed 10nA no matter what the load voltage is in the range $40 - 80$V.

The output current stability against the load voltage changes is achieved by placing Cascode Current Source as a last stage of cascaded current mirrors. Current mirror stages are used for current division. They also give the opportunity of adjusting output current linearly.

During the scan of cantilever tips over the crystalline surfaces there exist an inherent capacitance of a few pF between the cantilever tip and the surface. Rapid changes in load impedance creates a non-zero derivative of load voltage which in turn creates capacitive currents of many nano ampers. This capacitive current directly adds onto the current of the resistive branch. Since the requirement is to fix the current through the resistive load at $10nA$, current source must contain an internal adjustable current compensation mechanism to eliminate the effect of load capacitance.

Current compensation is achieved by using circuit elements like buffers, differentiators, operational amplifiers and voltage controlled current sources. The copy of capacitive current is generated by using those building blocks and it is used to eliminate the effect of capacitive current on resistive load.

In compensation circuitry, the feedback gain must be adjusted by the user depending upon the value of expected load capacitance. The gain of voltage controlled current source, buffer and cascaded current mirror stages are fixed internally but the gain of differentiator and non-inverting amplifier stage must be set by user. The only requirement is that the closed loop gain must equal to 1. Gain of one means that the capacitive current is copied exactly. For higher gains, stability analysis is done using both linear model and original of the circuit.

Noting that the overall gain larger than unity may cause instability, one must first set the gain less than unity and increase it gradually by changing the gain of non-inverting amplifier or differentiator. But the feedback resistance and the capacitance of differentiator block is not advised to be changed drastically from their original values because they affect the opeartion of operational amplifier. Gain can be adjusted more safely by changing the parameters of non-inverting amplifier. The result is then **the closer is the loop gain to unity, the better compensation is achieved.**

By this thesis, it is shown that load capacitive current compensated current source of $10nA$ can be implemented using high voltage Alcatel Mietec I2T CMOS technology. Compensation can be designed to be adjustable.

A p^+/n PD has been designed and tested. Quantum efficiency, responsivity and speed of detector have been found. It is concluded that this PD is sufficient for our needs.

As a future work, this current source might be designed to be electronically adjustable by replacing resistors of non-inverting amplifier with voltage controlled mosfet resistors. Hence, instead of changing the resistors manually it would be enough just to change the value of voltage controlling resistors.

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APPENDIX A

Layouts of Current Mirror Building Blocks

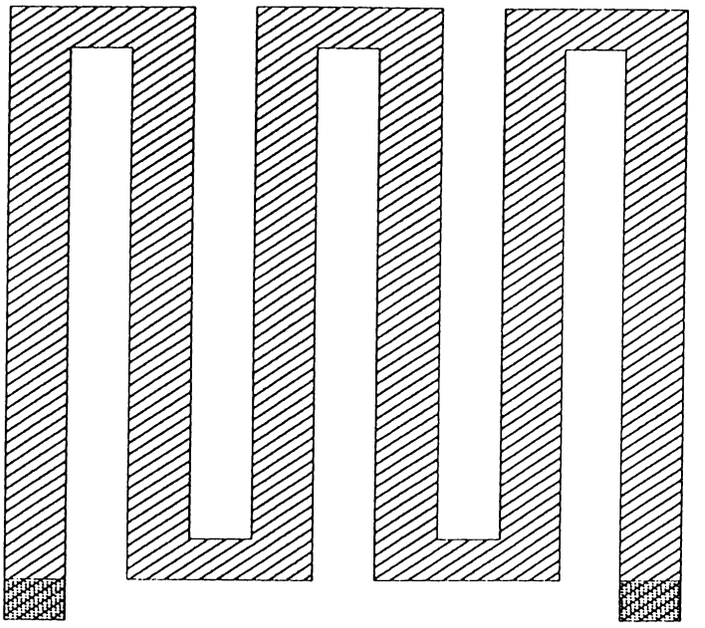

Figure A.1: Layout of 18kΩ Resistor

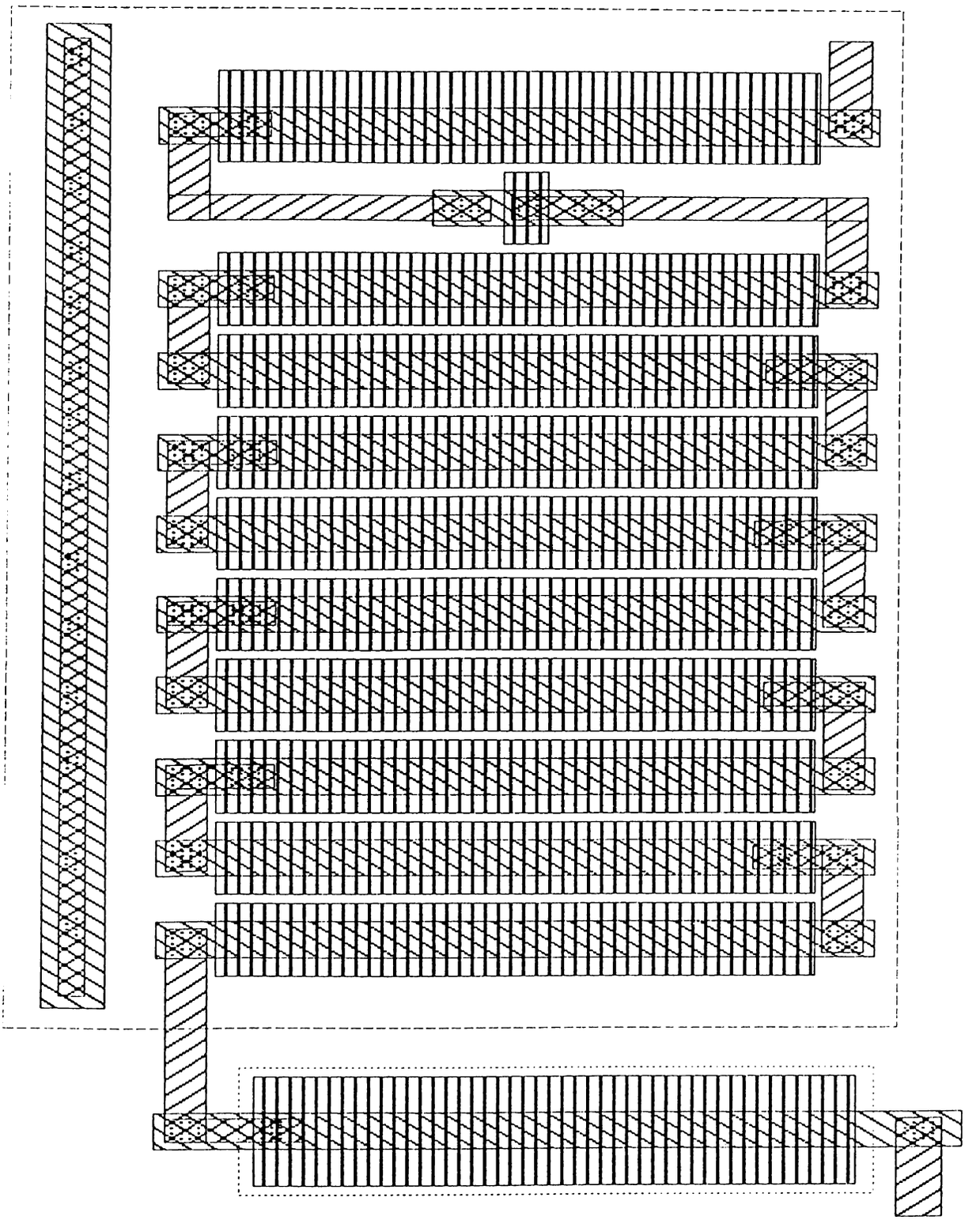

Figure A.2: Layout of Voltage Divider Bias Chain

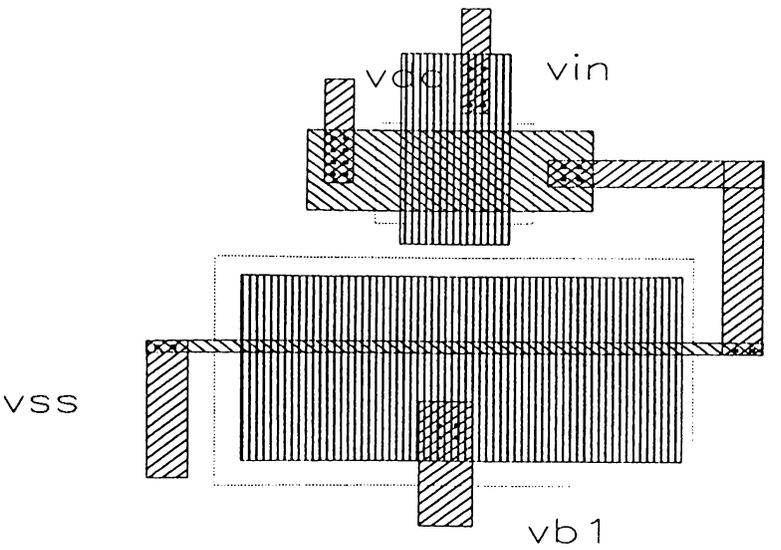

Figure A.3: Layout of NMOS Buffer

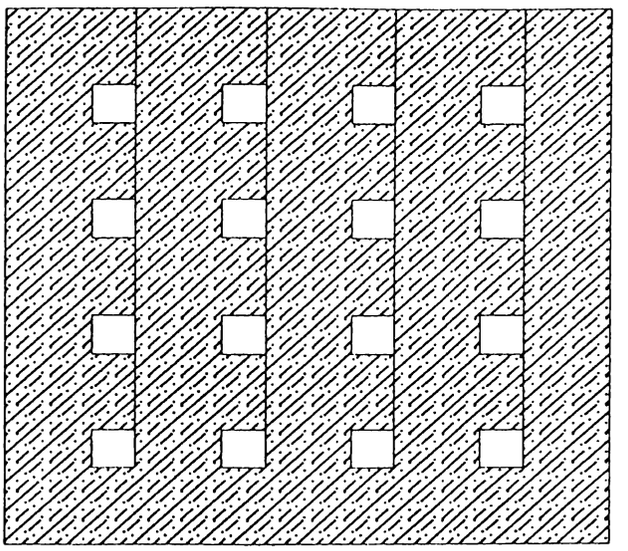

Figure A.4: Layout of a Single Bonding Pad

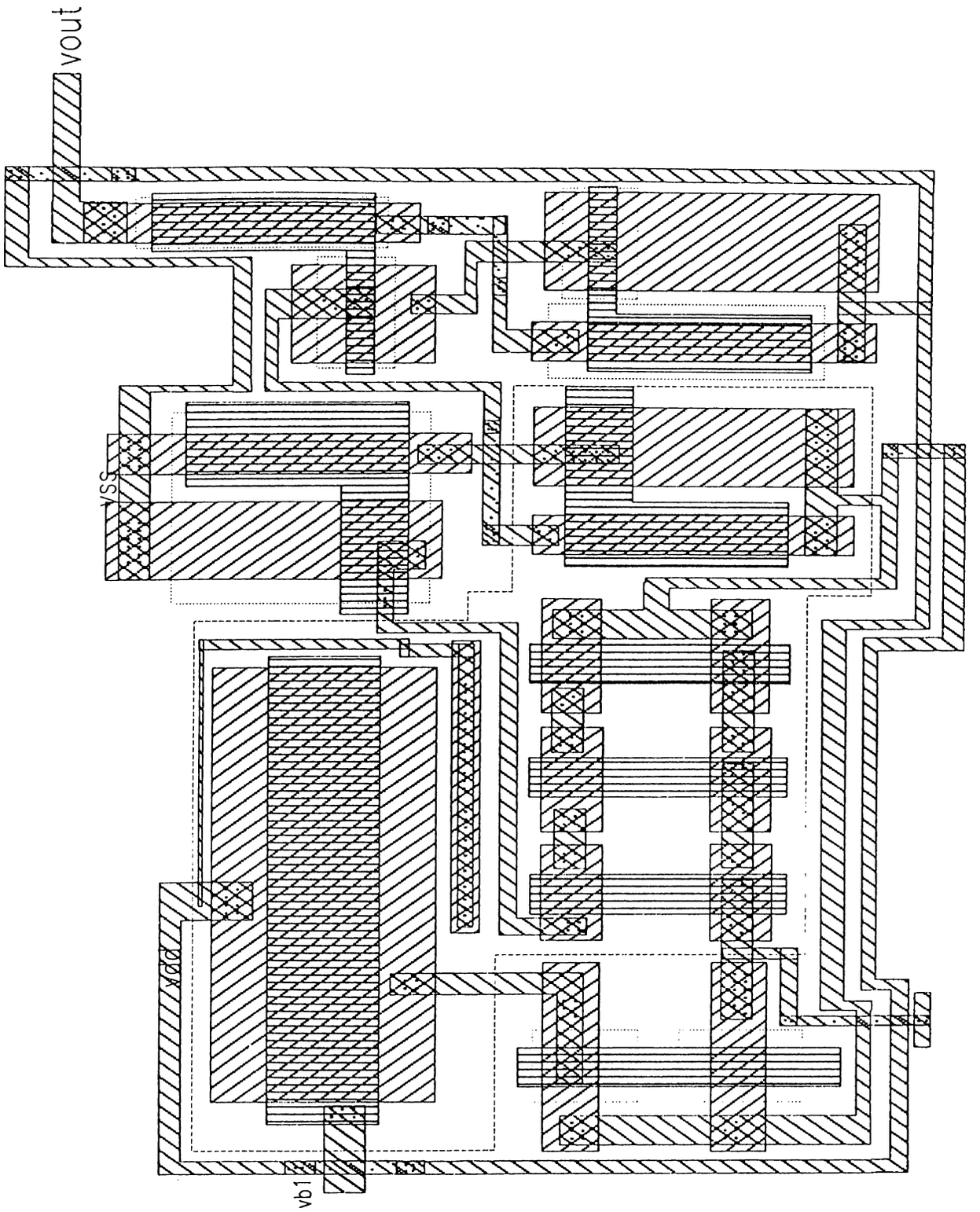

Figure A.5: Layout of Uncompensated Current Source

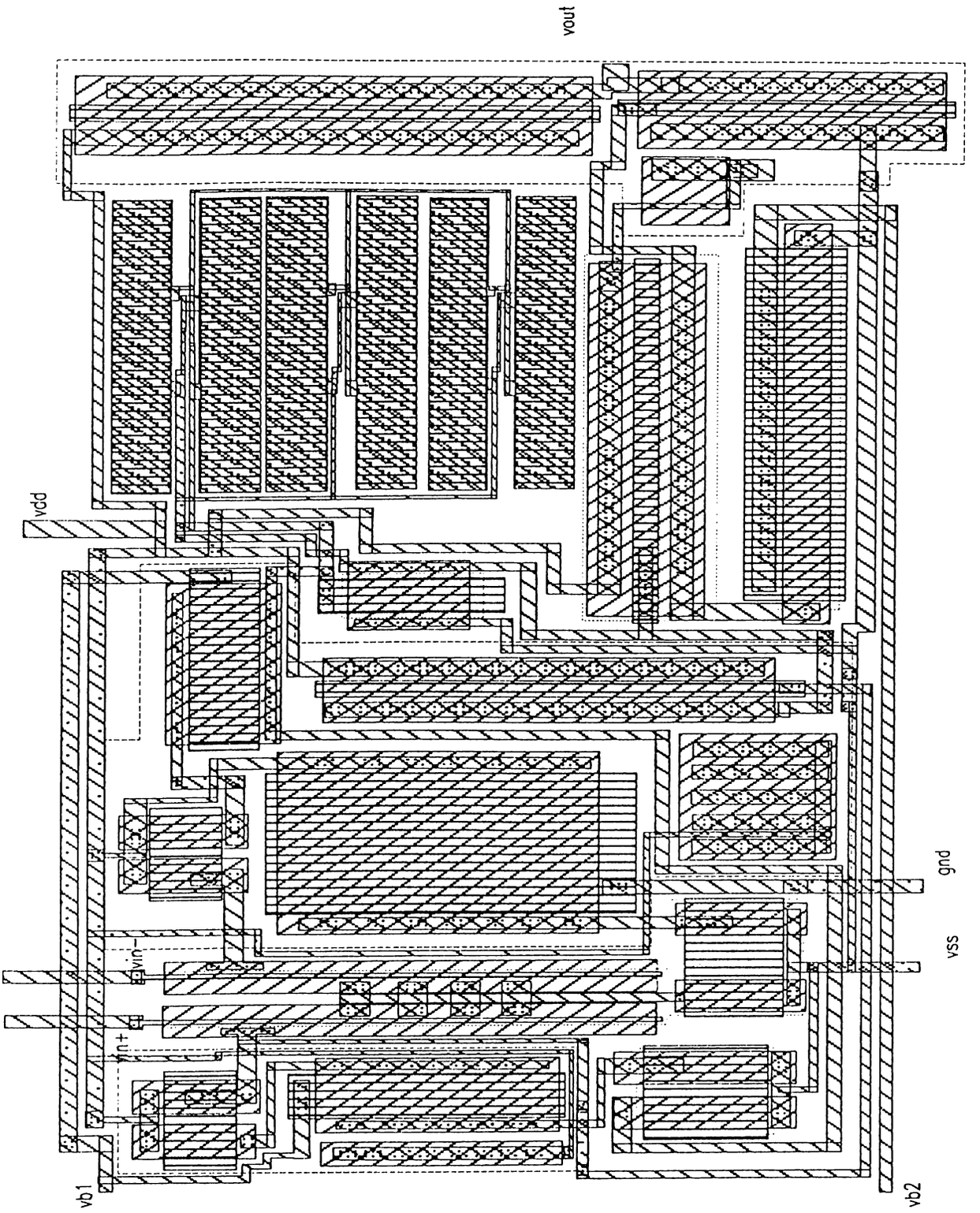

Figure A.6: Layout of High Voltage Operational Amplifier

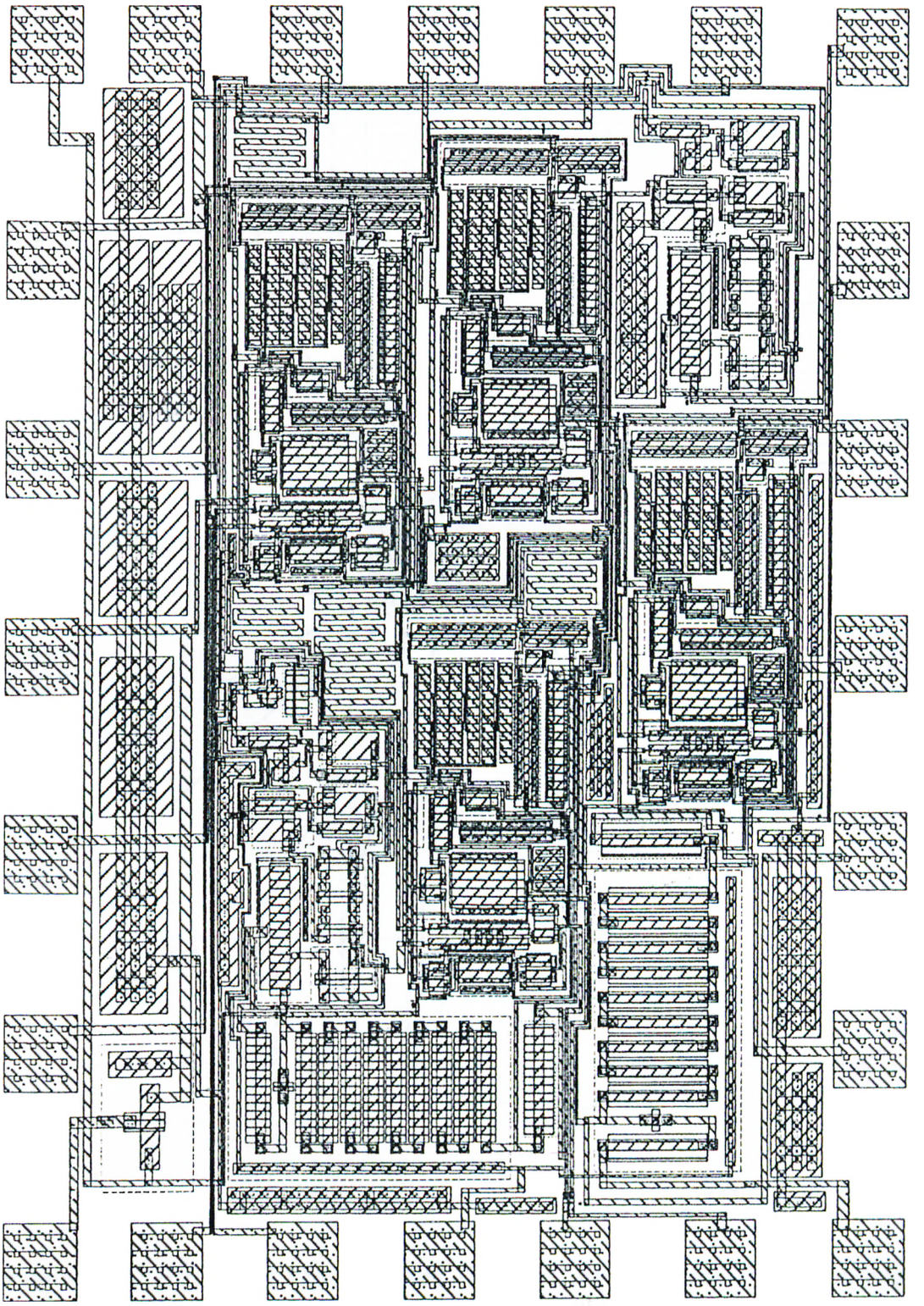

Figure A.7: Layout of Compensated Overall Current Source

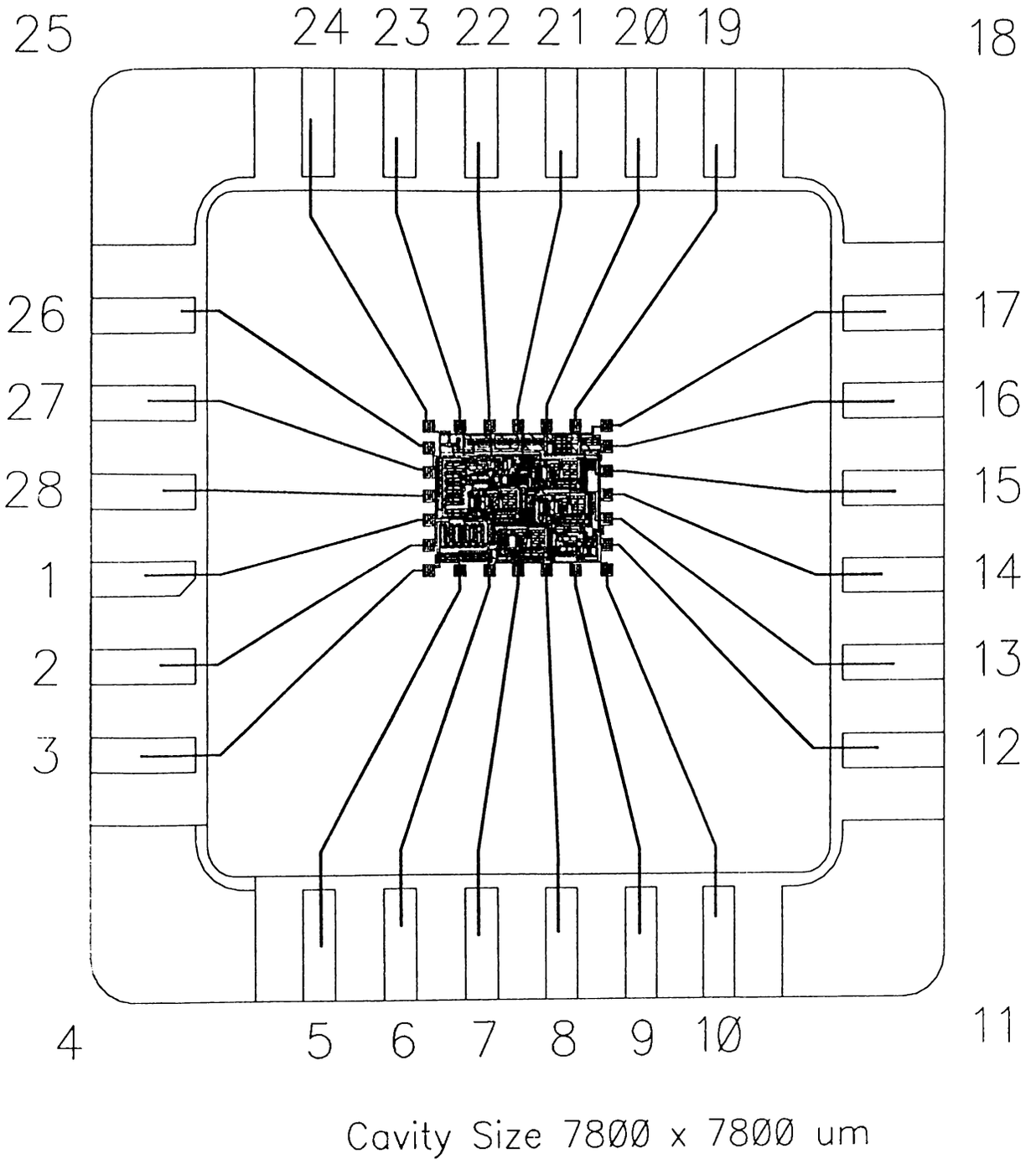

Figure A.8: Layout of Compensated Overall Current Source With Bonding Pads

APPENDIX B

Photodetector

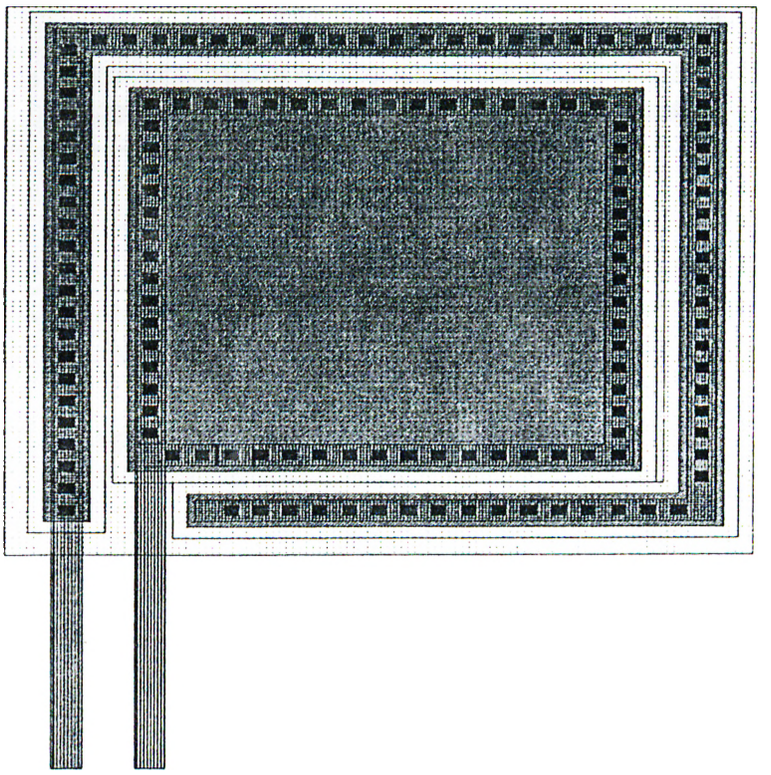

Figure B.1: Layout of a Single p+/n PD

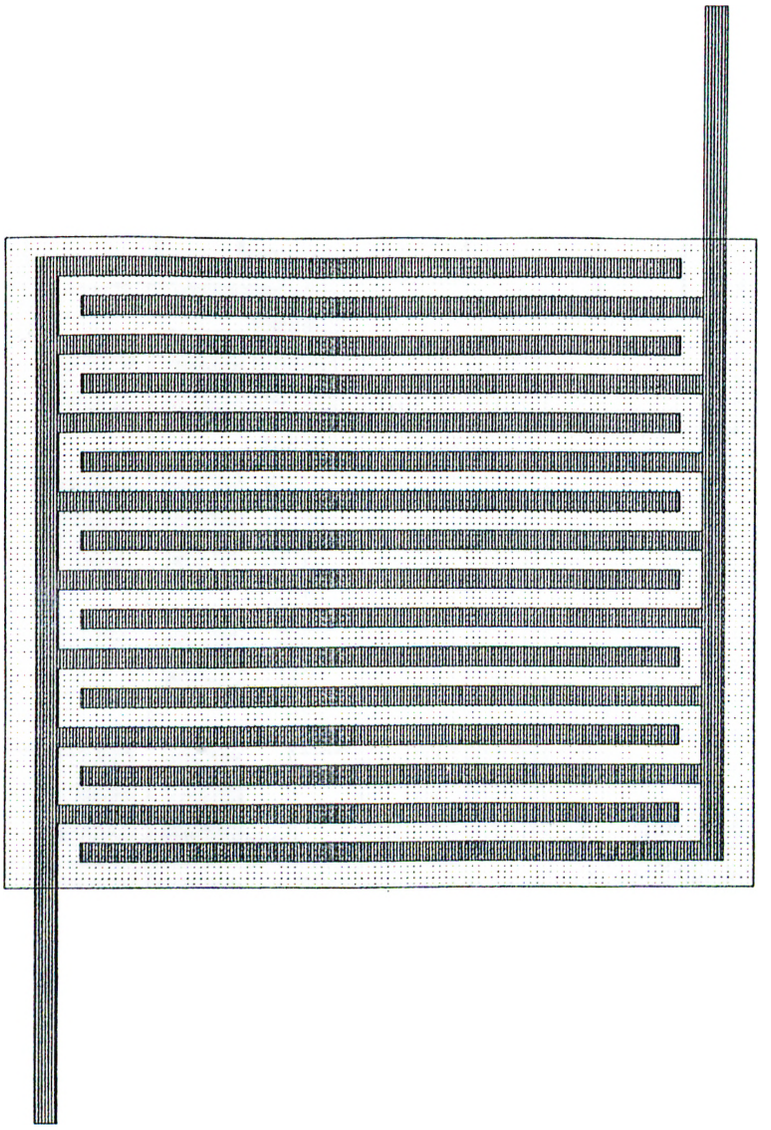

Figure B.2: Layout of a Single MSM-PD

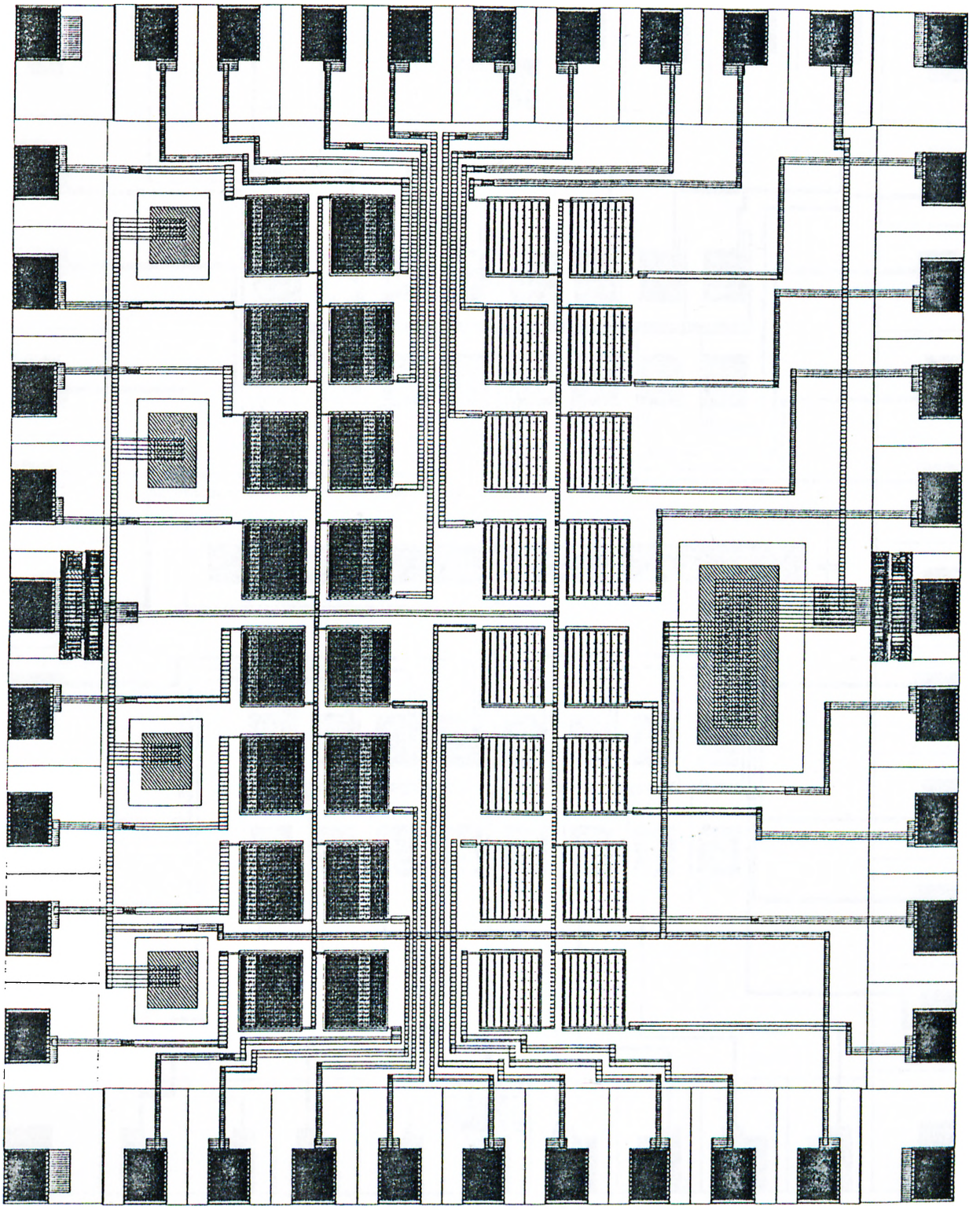

Figure B.3: Layout of MSM-PD array

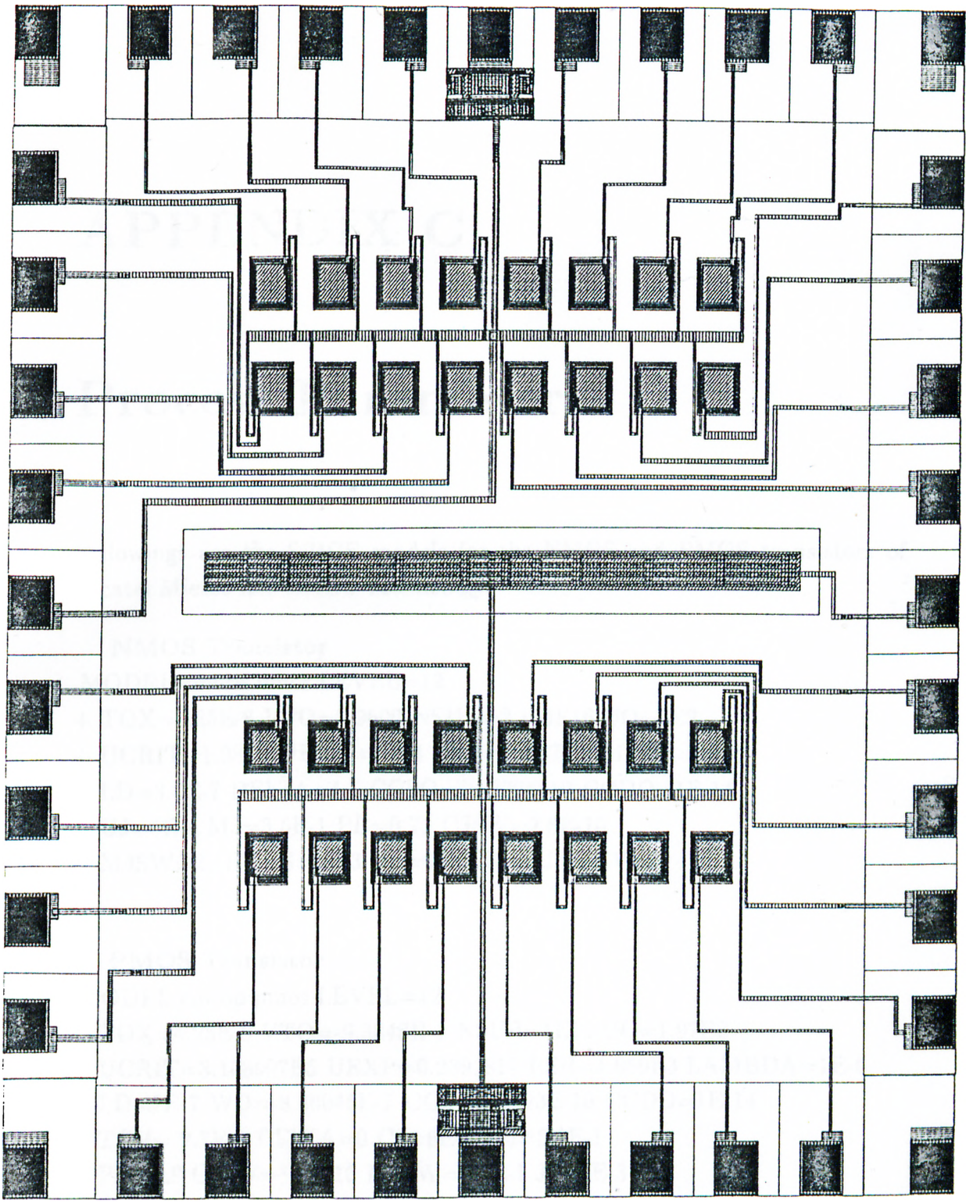

Figure B.4: Layout of p^+/n and n^+/p photodetector arrays

APPENDIX C

Process Parameters

Followings are the SPICE models for the NMOS and PMOS transistors of Alcatel Mietec I2T CMOS Technology.

NMOS Transistor

```
.MODEL cmosn nmos LEVEL=12
+ TOX=4.25E-8 VTO=0.9600 NSUB=3.100E16 UO=6E2
+ UCRIT=1.08E5 UEXP=0.124 RSH=5.2E2 LAMBDA=1E-6
+ LD=3.6E-7 DELTA=4.1 CGSO=1.6270E-10 CGDO=1E-14
+ CJ=5E-4 MJ=3.5E-1 PB=0.73 CJSW=2.8E-10
+ MJSW=2.1E-1 JS=1E-3 XL=0U XW=0U NLEV=0
```

PMOS Transistor

```
.MODEL cmosp pmos LEVEL=12
+ TOX=4.25E-8 VTO=-9.3848E-1 NSUB=1E16 UO=1.97E2
+ UCRIT=3.108907E5 UEXP=0.2392812 RSH=1.059E3 LAMBDA=1E-6
+ LD=7E-7 WD=-8.36046E-7 CGSO=0.423E-10 CGDO=1E-14
+ TCV=-2.7E-3 DELTA=0 CJ=6E-4 MJ=5.1E-1
+ PB=0.9 CJSW=3.6E-10 MJSW=3.5E-1 JS=1E-3
+ XL=0U XW=0U NLEV=0 TLEV=1
```

APPENDIX D

Chip Topology

D.1 Chip Overview

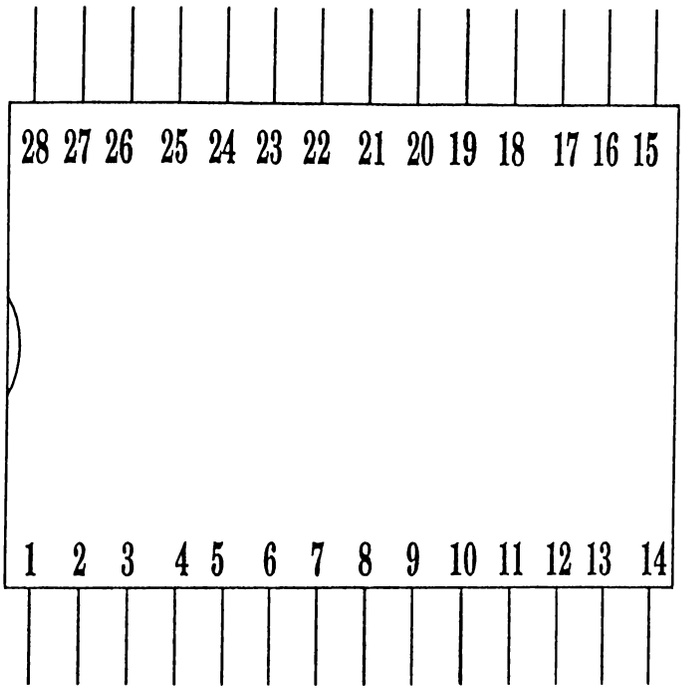

Figure D.1: Current Source Chip, General Overview

D.2 Pin Configurations

Pin Number	Node	Function
1	VSS	Negative Supply
2	VB3	0V
3	VU	Voltage Divider Upper Node
4	Corner	Dummy
5	VD	Voltage Divider Lower Node
6	X1	Vb_{10}
7	X2	Vb_1
8	SON	Single Opamp Vin-
9	SOP	Single Opamp Vin+
10	SOO	Single Opamp Vout
11	Corner	Dummy
12	BO	Buffer Output
13	OUT	Current Source Output
14	RI	18k Test Resistor Pin1
15	RO	18k Test Resistor Pin2
16	A	Feedback Point
17	VBIAS	Voltage bias of compensated current source
18	Corner	Dummy
19	SOUT	Single Current Source Output
20	VB	Voltage bias of Single Current Source
21	VDD	Positive Supply
22	DO	Differentiator Output
23	DN	Differentiator Vin-
24	VG	ON-OFF Control
25	Corner	Dummy
26	AO	Non-Inverting Amplifier Output
27	AN	Non-Inverting Amplifier Vin-
28	VDD	Positive Supply

D.3 Pin Connection

The current source chip contains the following blocks:

- A 10nA capacitive current compensated current source containing three opamps, one current source and one voltage divider bias chain
- A single current source without current compansation
- A single voltage divider bias chain
- A single test resistance

For proper test of the chip, supply voltages are chosen to be $V_{DD} = +5V$ and $V_{SS} = -95V$.

VU and VD are to test the performance of bias circuit, therefore VU=+5V and VD=-95V can be used. This bias chain also generate the bias voltages of single opamp. X1 and X2 are the two bias voltages available as output.

SON is single opamp inverting input and SOP is single opamp non-inverting input.SOO is the output pin of this single opamp. It may be used for testing purposes. BO is buffer output and differentiator capacitance of 100pF must be connected between BO and DN. Differentiator resistance of 100k must be connected between DN and DO.

Non-inverting amplifier gain is set by connecting a 100k resistance between AN and GND, 130k resistance between AN and AO. Load resistance and capacitance must be connected to output pin of OUT.

SOUT is the output pin of single current source. It is current is adjusted by means of VB. To get 10nA current at load it must be set to $-4V$. VB is not allowed to fall below $-6V$.

RI and RO are two pins of a test resistance.

VG is for ON/OFF control. VG=5V and VG=0V makes compensated current source ON and OFF respectively. VBIAS is the bias voltage of capacitive current compensated current source.