

ATOMIC SCALE INVESTIGATION OF CLEAN AND
EPI-GROWN Si(001) SURFACES USING SCANNING
TUNNELING MICROSCOPY

A THESIS
SUBMITTED TO THE DEPARTMENT OF PHYSICS
AND THE INSTITUTE OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

By

H. Özgür Özer
January 1996

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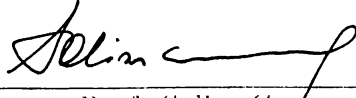
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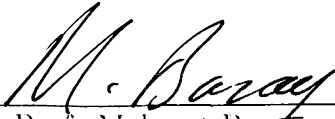
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Abstract

ATOMIC SCALE INVESTIGATION OF CLEAN AND EPI-GROWN SI(001) SURFACES USING SCANNING TUNNELING MICROSCOPY

H. Özgür Özer

M. S. in Physics

Supervisor: Assoc. Prof. Recai Ellialtıođlu

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In this thesis, clean and epi-grown Si(001)(2×1) surfaces are analysed by Scanning Tunneling Microscopy (STM). The STM and Ultra High Vacuum System (UHV) in which the microscope is installed, are described. A brief history of the studies on the reconstruction and fundamental features of the Si(001) surface is also given. First, the sample and tip preparation techniques were optimized. Sample preparation method, which includes both *ex situ* chemical and *in situ* heating cleaning procedures, was found not to give routinely the clean and atomically flat surfaces, because of the criticality of the temperature values used during heat treatments. The monoatomic steps, dimer rows, defects such as missing dimer and dimer groups, were observed on clean Si(001) surfaces. Double height step formation due to contamination was also detected on a few samples. Buckling of dimers which is believed to be due mainly to either the high defect density or tip-surface interaction, was observed on one sample. Si and Ge were grown epitaxially on the silicon substrate, with 0.11 ML and 3.2 ML coverages, respectively. The Si growth on Si(001) was found to occur as island

formation because of the low substrate temperature (~ 300 °C). Strong shape anisotropy and diffusional anisotropy in the growth have been observed. On the other hand, the large coverage of Ge on Si(001) at a relatively high substrate temperature (~ 500 °C), are resulted in step flow growth rather than individual island formation on the terraces.

Keywords: Scanning Tunneling Microscope, Ultra High Vacuum, Si(001)(2×1) reconstruction, Epitaxial growth.

Özet

TEMİZ VE ÜZERİNE EŞÖRGÜSEL TABAKA BÜYÜTÜLMÜŞ SI(001) YÜZEYLERİNİN TARAMALI TÜNELLEME MİKROSKOBU KULLANILARAK ATOMİK DÜZEYDE İNCELENMESİ

H. Özgür Özer

Fizik Yüksek Lisans

Tez Yöneticisi: Assoc. Prof. Recai Ellialtıođlu

Ocak 1996

Bu tezde, temiz ve üzerine eşörgüsel tabaka büyütülmüş Si(001)(2×1) yüzeyleri Taramalı Tünelleme Mikroskobu (TMM) kullanılarak incelenmiştir. TMM ve onun içine yerleştirildiđi Ultra Yüksek Vakum Sistemi açıklanmaktadır. Ayrıca, Si(001) yüzeyinin yeniden yapılanması ve temel özellikleriyle ilgili çalışmaların kısa bir tarihçesi de verilmektedir. İlk olarak, örnek ve iğne hazırlama teknikleri optimize edildi. Hem sistem dışı kimyasal hem de sistem içi ısıtarak temizleme prosedürleri içeren örnek hazırlama yönteminin, özellikle ısıtmada kullanılan sıcaklık değerlerinin kritikliđi yüzünden, düzenli bir şekilde temiz ve atomik seviyede düz yüzeyler vermediđi görülmüştür. Temiz Si(001) yüzeylerinde bir atom yüksekliđindeki basamaklar, çiftli sıralar, eksik çiftli ve çiftli grupları gibi kusurlar gözlenmiştir. Kirliliđe bađlı çift atom yüksekliđindeki basamak oluşumu da birkaç örnekte ortaya çıkarılmıştır. Başlıca sebebinin yüksek kusur yoğunluđu, ya da TMM iğnesinin etkisi olduđuna inanılan çiftillerin asimetrikleşmesi olayı da bir örnekte görülmüştür. Si ve Ge silisyum ana yüzeyi üzerine, sırasıyla 0.11 ve

3.2 mono-tabakalarla, eřörgüsel olarak büyütülmüřtür. Si'ın büyümesi, düşük ana yüzey sıcaklıđından (~ 300 °C) dolayı, ada oluřumu řeklinde gerekleřmiřtir. Büyümede yön bađımlı yapılanma ve yayılma tespit edilmiřtir. Diđer yandan, görece yüksek sıcaklıkta (~ 500 °C) ok miktarda Ge kaplanması, teraslar üzerinde kendi başına adaların oluřumundan ok basamak akıřı řeklinde bir büyümeyle sonuçlanmıřtır.

Anahtar

sözcükler: Taramalı Tünelleme Mikroskobu, Ultra Yüksek Vakum Sistemi, Si(001)(2×1) yeniden yapılanma, eřörgüsel büyüme.

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Chapter 1

Introduction

The phenomenon of tunneling has been known for more than sixty years-ever since the formulation of quantum mechanics. As one of the main consequences of quantum mechanics, a particle such as an electron, which can be described by a wave function, has a finite probability of entering a classically forbidden region. Consequently, the particle may tunnel through a potential barrier which separates two classically allowed regions.

Tunneling phenomena has been first proposed by Oppenheimer¹ in 1928 as a result of his theoretical studies on the ionization of hydrogen atoms in a constant electric field. Esaki² and Giaver³ were the first two scientists who observed electron tunneling experimentally, in p-n junctions and in planar metal-oxide-metal junctions, respectively. Tunneling of Cooper pairs between two superconductors was predicted by Josephson.⁴ These three scientists received the Nobel Prize in Physics for 1973, for their contributions to the investigation of tunneling phenomena.

Devices such as Metal-Insulator-Metal (MIM) diodes, hot electron transistors, superconducting quantum interference devices, which use tunneling through an insulating barrier like oxides, were developed in 1970s. However, barriers such as oxides, do not permit either to change the width of the barrier or to reach the surface of each electrodes for surface investigations. In that respect vacuum tunneling, the most important feature of scanning tunneling microscope, has

certain advantages.

The predecessor of STM is the Topographiner developed by Young et al.,⁵ the basic principle of which is field emission. It is very similar to the scanning tunneling microscope as far as its operation is concerned, i.e. it uses a sharp tip and the scanning is achieved by piezoelectric translators. The field emission current is kept constant by adjusting the relative position of the tip to the surface. However the lateral and vertical resolutions were limited to 1000 Å and 30 Å respectively, due to relatively large distance between tip and surface of several hundred Å in the field emission regime.

Teague⁶ and Poppe⁷ have observed vacuum tunneling in 1978 and 1981 respectively. However Binnig and Rohrer were the first to use vacuum tunneling as a microscope. In 1982 Binnig, Rohrer and coworkers^{8,9} have constructed the scanning tunneling microscope by observing vacuum tunneling on platinum samples with tungsten tip. For this construction Binnig and Rohrer received the Nobel Prize in Physics in 1986.

1.1 Brief Theory of Scanning Tunneling Microscopy

Scanning tunneling microscopy is a powerful and a unique tool for the investigation of structural and electronic properties of surfaces. In order to understand what is measured by STM and interpret the images, several theories are developed by scientists. Before trying to understand the theory of STM, good understanding of the basic principles of vacuum tunneling is necessary.

1.1.1 Vacuum Tunneling

In vacuum tunneling the potential in the vacuum region acts as a barrier to electrons between the two metal electrodes. In the case of STM, these electrons correspond to the surface and the tip. Fig.1.1 shows this barrier schematically. The transmission probability for a wave incident on a one-dimensional barrier can

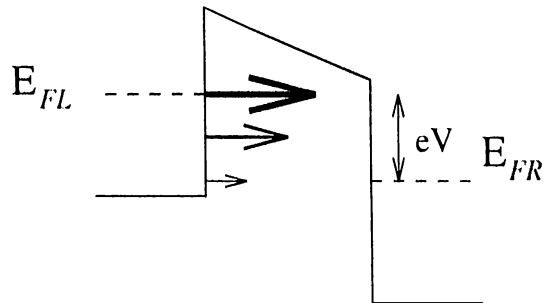


Figure 1.1: Schematic of potential barrier between electrodes for vacuum tunneling

The dashed lines correspond to the Fermi levels of the electrodes. There is voltage difference V across the gap.

easily be calculated. The solutions of Schrödinger's equation inside a rectangular barrier in one dimension have the form

$$\psi = e^{i\kappa x}. \quad (1.1)$$

Thus the crucial parameter is κ , where

$$\kappa^2 = \frac{2m(V_B - E)}{\hbar^2} \quad (1.2)$$

where E is the energy of the state, and V_B is the potential in the barrier. In general V_B may not be constant across the gap, but for the sake of simplicity let us assume rectangular barrier. In the simplest case V_B is the vacuum level, so for states at the Fermi level, $V_B - E$ is just the work function.

The transmission probability, and hence the tunneling current, decays exponentially with barrier width d as

$$I \propto e^{-2\kappa d}. \quad (1.3)$$

For tunneling between two metals with a voltage difference V across the gap, only the states within eV above or below the Fermi level can contribute to tunneling. The electrons in states within eV below the Fermi level on the negative side tunnels into the empty states within eV above the Fermi level on

the positive side. Other states cannot contribute either because there are no electrons to tunnel at higher energy, or because there is not any empty state to tunnel into at lower energy.

1.1.2 STM Imaging

The basic idea underlying STM is quite simple. As illustrated in Fig. 1.2 a sharp tip is brought close enough to the surface that at a convenient operating voltage, typically 2 mV to 2 V, a measurable tunneling current, typically between 0.1 nA and 10 nA, is obtained. There are basically two modes of operation of STM. The first and the most used one is the constant current mode in which the tip is scanned over the surface, while the tunneling current is kept constant by changing the vertical position of the tip with a control circuit. The control circuit achieves this by applying suitable voltages to the z Piezo. The applied voltage to the piezoelectric drives simply gives the path of the tip. If a line scan in x direction is extended to many lines in y direction, an image which consists of a map $z(x, y)$ of the tip position versus lateral position (x, y) is obtained.

In the second mode, namely the constant height mode, as the name suggests the tip is kept nearly at a constant height during the scan and the tunneling current is monitored. The control circuit only keeps the average current constant. Then a weighted sum of I and y plotted versus x forms the image.

Each mode has its own advantages. Constant current mode can be used to scan surfaces which are not atomically flat. On the other hand, the constant height mode allows for much faster scanning of atomically flat surfaces since only the electronics, not the z Piezo, must respond to the structure passing under the tip. Fast imaging is important in the sense that it enables researchers to study processes in real time, minimizing image distortion due to piezoelectric creep and thermal drift.

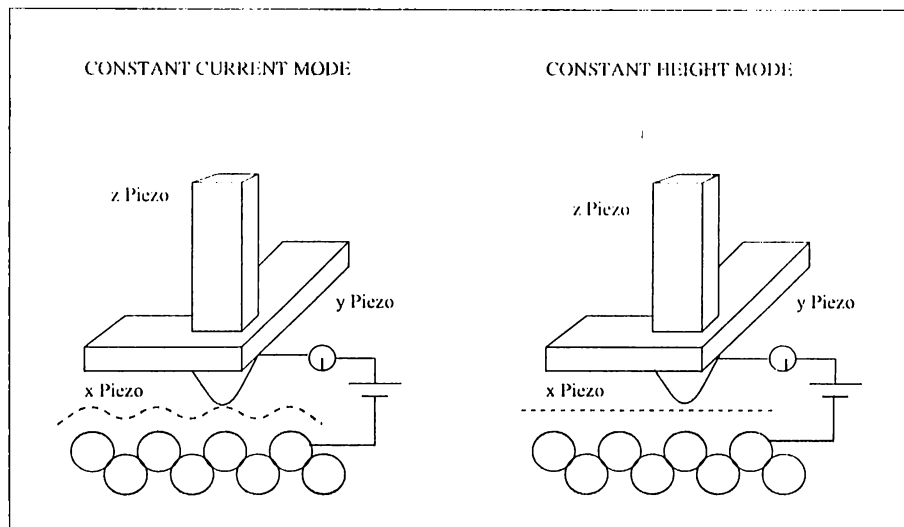


Figure 1.2: Basic STM

Two modes of operation of STM. The dashed lines are the contours followed by the tip

1.1.3 Theory of STM

As long as the resolution of STM is of the order of a nanometer or larger, it is adequate to interpret the image as a surface topograph. However, if the concern is on atomic resolution images, it is not even clear what is meant by a topograph. The most reasonable definition is that a topograph is a contour of constant charge density. This contradicts the principle of vacuum tunneling which says only the electrons near the Fermi level contribute to tunneling, even though all electrons below the Fermi level contribute to the charge density. The following theory developed by Tersoff and Hamann¹⁰ is explanatory even in case of atomic resolution.

In first order perturbation theory, the tunneling current is

$$I = \frac{2\pi e}{h} \sum_{\mu,\nu} \{f(E_\mu)[1 - f(E_\nu)] - f(E_\nu)[1 - f(E_\mu)]\} |M_{\mu\nu}|^2 \delta(E_\nu + V - E_\mu), \quad (1.4)$$

where $f(E)$ is the Fermi function, V is the applied voltage, $M_{\mu\nu}$ is the tunneling matrix element between states ψ_μ and ψ_ν of the respective electrodes, and E_μ is the energy of the state ψ_μ . For most purposes, the Fermi functions can be

replaced by their zero-temperature values which are unit step functions. In this case the above equation, in the limit of small voltage, reduces to

$$I = \frac{2\pi}{h} e^2 V \sum_{\mu, \nu} |M_{\mu\nu}|^2 \delta(E_\mu - E_F) \delta(E_\nu - E_F). \quad (1.5)$$

These equations are quite simple. The problem is to evaluate the tunneling matrix elements. Bardeen¹¹ showed that, under certain assumptions, the tunneling matrix elements can be expressed as

$$M_{\mu\nu} = \frac{\hbar^2}{2m} \int d\mathbf{S} \cdot (\psi_\mu^* \nabla \psi_\nu - \psi_\nu \nabla \psi_\mu^*), \quad (1.6)$$

where the integral is over any surface lying entirely within the barrier region. If we choose a plane for the surface of integration, and neglect the variation of the potential in the region of integration, then the surface wave function at this plane can be conveniently expanded in the generalized plane-wave form

$$\psi = \int d\mathbf{q} a_{\mathbf{q}} e^{-\kappa_q z} e^{i\mathbf{q} \cdot \mathbf{x}}, \quad (1.7)$$

where z is height measured from a suitable origin at the surface, and

$$\kappa_q^2 = \kappa^2 + |\mathbf{q}|^2. \quad (1.8)$$

A similar expansion applies for the other electrode, replacing $a_{\mathbf{q}}$ with $b_{\mathbf{q}}$, z with $z_t - z$, and \mathbf{x} with $\mathbf{x} - \mathbf{x}_t$. Here \mathbf{x}_t and z_t are the lateral and vertical components of the position of the tip, respectively. Then, substituting these wave functions into Eq.1.6, the matrix elements can be obtained as

$$M_{\mu\nu} = -\frac{4\pi^2 \hbar^2}{m} \int d\mathbf{q} a_{\mathbf{q}} b_{\mathbf{q}}^* \kappa_q e^{-\kappa_q z_t} e^{i\mathbf{q} \cdot \mathbf{x}_t}. \quad (1.9)$$

Thus given the wave functions of the surface and tip, a simple expression for the tunneling matrix element and tunneling current can be found.

However the atomic structure of the tip is generally not known. What would be the criteria in the estimation of the atomic structure of the tip? There are two important points to be considered in this respect. First, the aim is maximum possible resolution, hence the smallest possible tip. The thing wanted to be

measured is the properties of the bare surface, not the complex interacting system of tip and surface. Therefore, the ideal STM tip would consist of a mathematical point source of current, whose position is denoted \mathbf{r}_t . In that case, Eq.1.5 for the tunneling current reduces to¹⁰

$$I \propto \sum_{\nu} |\psi_{\nu}(\mathbf{r}_t)|^2 \delta(E_{\nu} - E_F) \equiv \rho(\mathbf{r}_t, E_F). \quad (1.10)$$

Thus the ideal STM would simply measure $\rho(\mathbf{r}_t, E_F)$, namely the local density of states at E_F (LDOS). LDOS explicitly means the charge density from states at the Fermi level. The LDOS is evaluated for the bare surface. It doesn't depend on the complex tip-sample system. The only dependence related to the tip is its position. Therefore according to this model STM has a simple interpretation as measuring a property of the bare surface.

However, Tersoff Hamann Theory is valid only for large tip sample separations. For small separations, in order to interpret the images, a detailed analysis of the tip sample interaction is necessary, since the interaction is strong enough to affect the measurements. Various studies on this subject¹²⁻¹⁴ have shown that the complex interacting system of the tip and the sample affects the corrugation amplitude.

1.2 Scanning Tunneling Spectroscopy

Scanning tunneling spectroscopy provides information complementary to the information obtained in conventional topographic imaging. By measuring the detailed dependence of the tunneling current on the applied voltage at specific locations of the sample, it is possible to obtain a measure of the electronic density of states of the sample on an atomic scale. If both the energies and the spatial locations of the electronic states are known, direct comparisons with the theory can be made. However, a general theory for the use of STM for the spectroscopy of electronic surface states has not yet been developed. Since the electronic states of the tip and their interaction with the sample surface have to be considered for each sample-tip combination, the evaluation of a general theory is quite difficult.

Tunneling spectroscopy in planar junctions was studied long before STM.¹⁵ However, the development of spatially-resolved spectroscopy with STM stimulated the interest in this area. Because of the difficulty of calculating $I(\mathbf{r}_t, V)$ in general, the studies mostly focused on $I(V)$, without considering the dependence to the position of the tip.

Selloni et al.¹⁶ suggested that the results of Tersoff and Hamann¹⁰ could be qualitatively generalized for modest voltages as

$$I(V) \propto \int_{E_F}^{E_F+V} \rho(E) T(E, V) dE, \quad (1.11)$$

where $T(E, V)$ is the barrier transmission coefficient, and $\rho(E)$ is the local density of states given by Eq. 1.10 at or very near the surface, and assuming a constant density of states for the tip. However, this simple model does not come up with a straightforward interpretation for the tunneling spectrum.¹⁸ In particular, the derivative dI/dV has no simple dependence on the density of states $\rho(E_F + V)$. It can be said that a sharp feature in the density of states of the sample (or tip), at an energy $E_F + V$, will lead to a feature in $I(V)$ or its derivatives at voltage V .

However, there is a problem with the above statements. The problem is the strong V -dependence of the transmission coefficient, $T(E, V)$, which results in a distortion of features in the spectrum.¹⁹ Stroscio, Feenstra, and coworkers¹⁹ proposed a simple solution to this problem. To eliminate the exponential dependence of $T(E, V)$ on V they normalize dI/dV by dividing it by I/V . Therefore the quantity $d \ln I / d \ln V$ is mostly used for identification of density of states in the STM results.

There is an important problem in tunneling spectroscopy studies. The electronic density of states of the tip is usually unknown, so it is not so simple to extract the knowledge of the electronic structure of the surface from the spectroscopy measurements. This problem can be overcome by using the same tip, consequently having a constant background during all measurements.

In accordance with the modes of STM imaging there are various types of scanning tunneling spectroscopy. These are constant current, constant

separation, and variable separation spectroscopy, to name a few. Since in constant current spectroscopy, in tracing the bias voltage in the specified interval, typically between two values symmetric with respect to zero, the zero value of the voltage causes the tip to crash into the sample, this mode is experimentally difficult to perform. Constant separation spectroscopy is the experimentally most preferred one. It is rather simple, if no spatial resolution is wanted. At a constant separation, the applied voltage is varied over the specified interval while simultaneously measuring the tunneling current. However, in order to correlate the tunneling spectra with the topograph of the surface, the spectroscopy must be carried out simultaneously with the topographic imaging. This was first achieved experimentally by Hamers et al.,²⁰ and called spatially resolved spectroscopy. It can be done periodically at many points on the sample as well as at a few points. Spatially resolved spectroscopy is more complex and experimentally more difficult to achieve, not only because of the necessity of a more complicated control circuit, but due to the need for very stable STM tips, which are very difficult to prepare.

1.3 STM on Semiconductors

Scanning Tunneling Microscope can be used to image only metals and doped semiconductors, since its working principle is the tunneling of electrons. This seems to be a limitation on the applications. However, with the use of the techniques developed for scanning tunneling microscopy, many other surface sensitive instruments have been developed since the invention of STM. Atomic Force Microscope,²¹ Near-Field Optical Scanning Microscope,²² Scanning Tunneling Optical Microscope,²³ Ballistic Electron Emission Microscope²⁴ are some of these instruments in which various interactions are used for microscopy to analyze different physical properties.

Since its invention, STM has become a widely used instrument to investigate semiconductor surfaces. This is not just because of the power of STM or the necessity to investigate the topographic and electronic properties of these surfaces on an atomic scale, but due to a property of these surfaces that makes them

very suitable samples for STM measurements, as well. This property is the reconstruction of bulk terminated semiconductor surfaces, which will be discussed in detail in Chapter 3. Reconstruction of the surface results in large corrugation on the surface, as large as a few Å. These large corrugation amplitudes are very easy to detect with STM and can easily be converted into an illustrative gray level image. There are other features of semiconductor surfaces, such as dimers and steps, that have relatively larger lateral separations, which also makes the surface properties to be easily resolved. On the other hand the reconstructed semiconductor surface may exhibit considerable local differences in electronic structure. Because of the reasons stated above, semiconductor surfaces are used as model systems for the development of scanning tunneling microscopy techniques. Besides, surface science has also gained much about semiconductors with the usage of STM. Hence it can be said that STM and semiconductor surfaces had a mutual scientific life.

In the last 20 years, semiconductor technology has also gained an acceleration. Silicon based integrated circuits, especially, have been developed with very high yield. However, the technological thirst for faster and smaller devices enforces scientific research on semiconductors. SiGe and GaAs heterostructures have begun to form the basis of high-speed semiconductor technology. It is well understood that, to increase the quality and speed of heterostructure based devices, very thin layers, sometimes only a few monolayers of structures are necessary. This can be achieved with Molecular Beam Epitaxy and related techniques. However, almost all semiconductor surfaces contain single atom high steps separated by few hundreds of Å. Thus without processing of the surface, it is impossible to obtain atomically flat layers having homogenous thicknesses. This problem brings the necessity to investigate the semiconductor surfaces and epitaxial growth at an atomic level. The aim is to decrease the number of steps, which will allow homogenous growth of layers on substrates. By using STM it is possible to observe the mechanisms of growth, and to understand the growth conditions giving the best surfaces. By association of MBE and STM systems, even real time images of epitaxial growth can be acquired.

In this thesis, we attempted to investigate the clean and Si/Ge grown Si(001) surfaces using STM. Sample/tip preparation methods, STM analysis of Si(001)(2×1) reconstructed surface and the first results of Si/Ge growth on Si(001) are presented. The instruments, mainly the UHV-STM system, are also described. The history of the theoretical and experimental studies on the reconstruction of the Si(001) surface is briefly reviewed, as well.

Chapter 2

UHV STM System

2.1 Ultra High Vacuum System

The experiments were performed with a scanning tunneling microscope which is installed in an ultra high vacuum (UHV) system, which has been designed and constructed by Oral and Ellialtioglu.²⁵ The schematic diagram of the UHV system is given in Fig.2.1. The UHV system is composed of two chambers one for preparation, and the other for STM measurements. The analysis chamber contains a Low Energy Electron Diffraction (LEED) instrument, which is used to determine the cleanliness of the sample surface, as well. There is a carousel on which four tips and/or samples can be stored in the analysis chamber. The carousel also serves as the sample holder for LEED instrument.

The Fast Entry Lock (FEL), which is isolated from the UHV chamber with a gate valve, is used to transfer the tips and samples into UHV without breaking the vacuum. FEL is attached to a linear-rotary magnetic transfer arm (MTA), on which the samples and tips are loaded to be transferred into the main chamber.

The main chamber is evacuated with a 60 l/s triode pump and a Titanium Sublimation Pump (TSP). The FEL is pumped with 60 l/s Varian Turbomolecular Pump backed by a double stage rotary pump. A nude ion gauge and a pirani gauge are used to measure the pressures of the main chamber and the backing line of turbo, respectively. All these gauges together with the

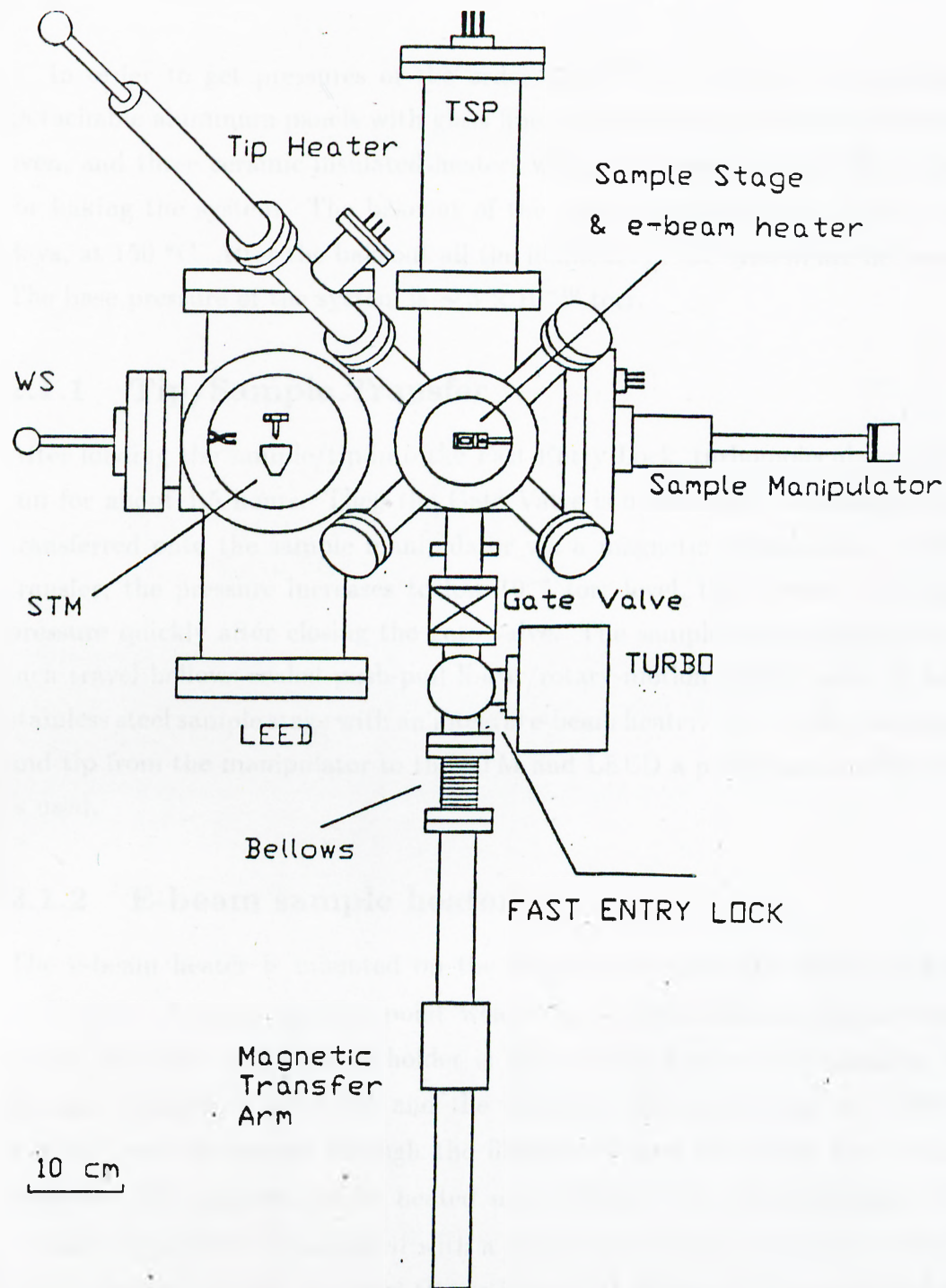


Figure 2.1: Schematic diagram of the UHV system. Taken from Ref. 26.

bakeout heaters, TSP, leak detection unit are controlled by an intelligent ion gauge controller.

In order to get pressures of the order of 10^{-10} torr bakeout is inevitable. Detachable aluminum panels with glass fiber insulation are used for the bakeout oven, and three ceramic insulated heaters with total power of 2.2 KW are used for baking the system. The bakeout of the system typically lasts 2 and a half days, at 150 °C. After the bakeout all the filaments in the system are de-gassed. The base pressure of the system is $\sim 3 \times 10^{-10}$ torr.

2.1.1 Tip/Sample Transfer

After loading the sample/tip into the Fast Entry Lock, turbomolecular pump is run for about 1.5 hours. Then the Gate Valve is opened and the sample/tip is transferred onto the sample manipulator via a magnetic transfer arm. During transfer, the pressure increases to low 10^{-8} torr level, then drops to the base pressure quickly after closing the gate valve. The sample manipulator is an 8-inch travel bellows sealed push-pull linear/rotary-motion feedthrough. It has a stainless steel sample stage with an integral e-beam heater. To transfer the sample and tip from the manipulator to the STM and LEED a pincer-grip wobble stick is used.

2.1.2 E-beam sample heater

The e-beam heater is mounted on the manipulator from the back, as shown in Fig.2.2. A tantalum wire point welded on an SEM filament holder serves as the filament. The sample holder is held on the heater with tantalum leaf springs. Sample is grounded and the tantalum filament is kept at -1200 V. The DC current passing through the filament is used to control the emission current. The samples can be heated up to 1450 °C by this technique. The sample temperature is measured with a simple home made pyrometer, which is placed on the viewport, such that the position of its pinhole is to coincide with the center of the sample. Since the intensity of the blackbody radiation reaching the pyrometer is dependent on the distance between the pyrometer and the sample, and there is a viewport between them, the pyrometer must be calibrated *in situ*.

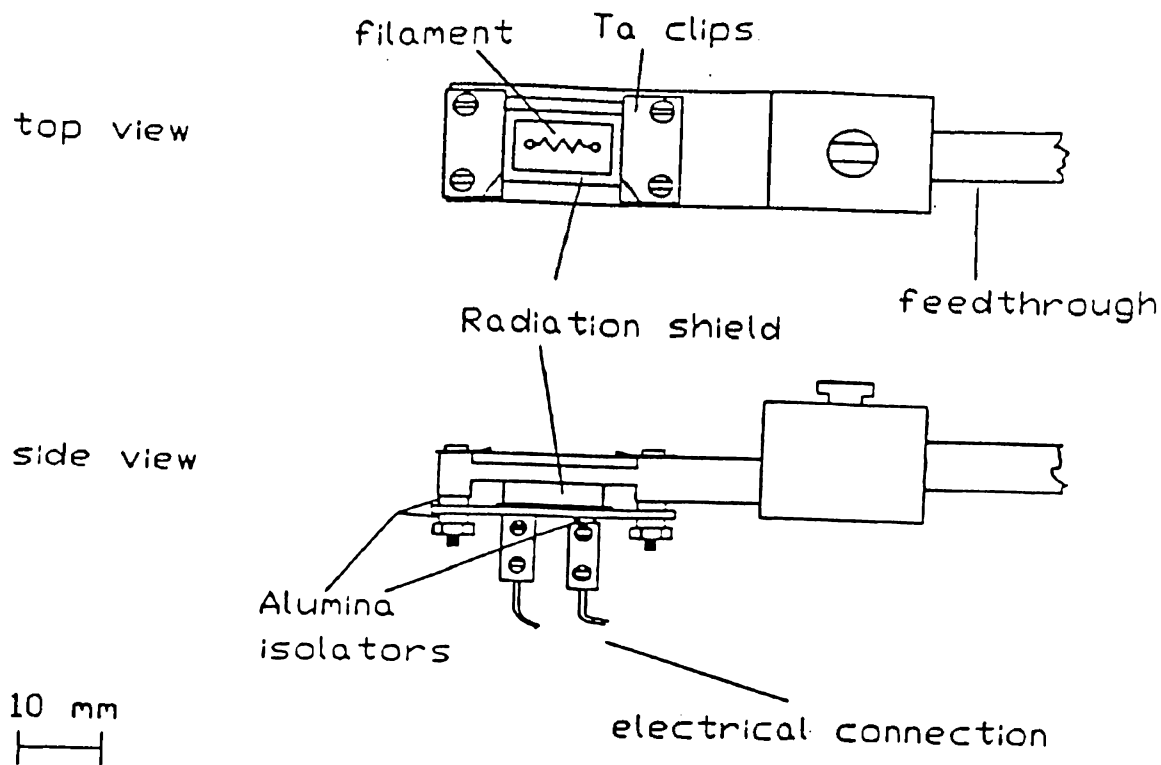


Figure 2.2: e-beam sample heater. Taken from Ref. 26.

The calibration is done with respect to the melting point of silicon.

2.1.3 Si and Ge Evaporators

There are two evaporators for silicon and germanium in the preparation chamber. They are mounted to 4-pin power feedthroughs on 2.75 inch O.D. flanges.

The germanium source is made up of 0.5 mm diameter tungsten wire in the form of a basket. Germanium granules are put into the basket and the basket is attached to the power feedthrough pins by inline barrel connectors.

On the other hand, a rectangular silicon wafer piece clamped by tantalum clips serves as the silicon source. The silicon wafer piece is heated by passing AC current through the wafer. Since in growth processes of a few monolayers the exposure time is very important there are shutters for both sources to start or end the growth.

2.2 STM

The STM is mounted on a UHV multi-seal flange in the analysis chamber. The schematic of the STM is given in Fig.2.3 and the parts are explained in detail below.

2.2.1 Vibration Isolation

External vibrations affect the distance between the tip and the sample, and hence the tunneling current. Therefore, if the microscope is not isolated from external vibrations, such as the vibrations of laboratory floor which has an amplitude of the order of a micrometer, it would be impossible to obtain reliable images. In our STM, vibration isolation is provided by a single stage spring suspension together with eddy current damping. Base of the microscope is suspended with four stainless steel springs as shown in Fig. 2.3. In addition, there are four Sm-Co magnets clamped to a stainless steel ring which rests on collars. These magnets together with the copper plates mounted on the STM base provide eddy current damping.

2.2.2 Coarse Approach

There are several coarse approach methods used for STM, namely, electrostatic louse, magnetically driven slider, inchworm motor etc. In our STM a piezo driven stick-slip type slider is used for coarse approach. In this way the sample can be positioned in two orthogonal directions. As it is seen in Fig.2.4, the slider is composed of three pieces. The central piece on which the piezos are mounted, is sandwiched between the two pieces containing the rails.

Operation of the slider is as follows²⁶: If the piezo voltage is slowly increased, then the upper and lower electrodes of the piezo plate are moved laterally with respect to each other under the shear stress. Since the piezo motion is slow, upper slider piece moves with the piezo. If the piezo voltage is now suddenly switched to zero volts, then the balls glued to the piezo will suddenly come back

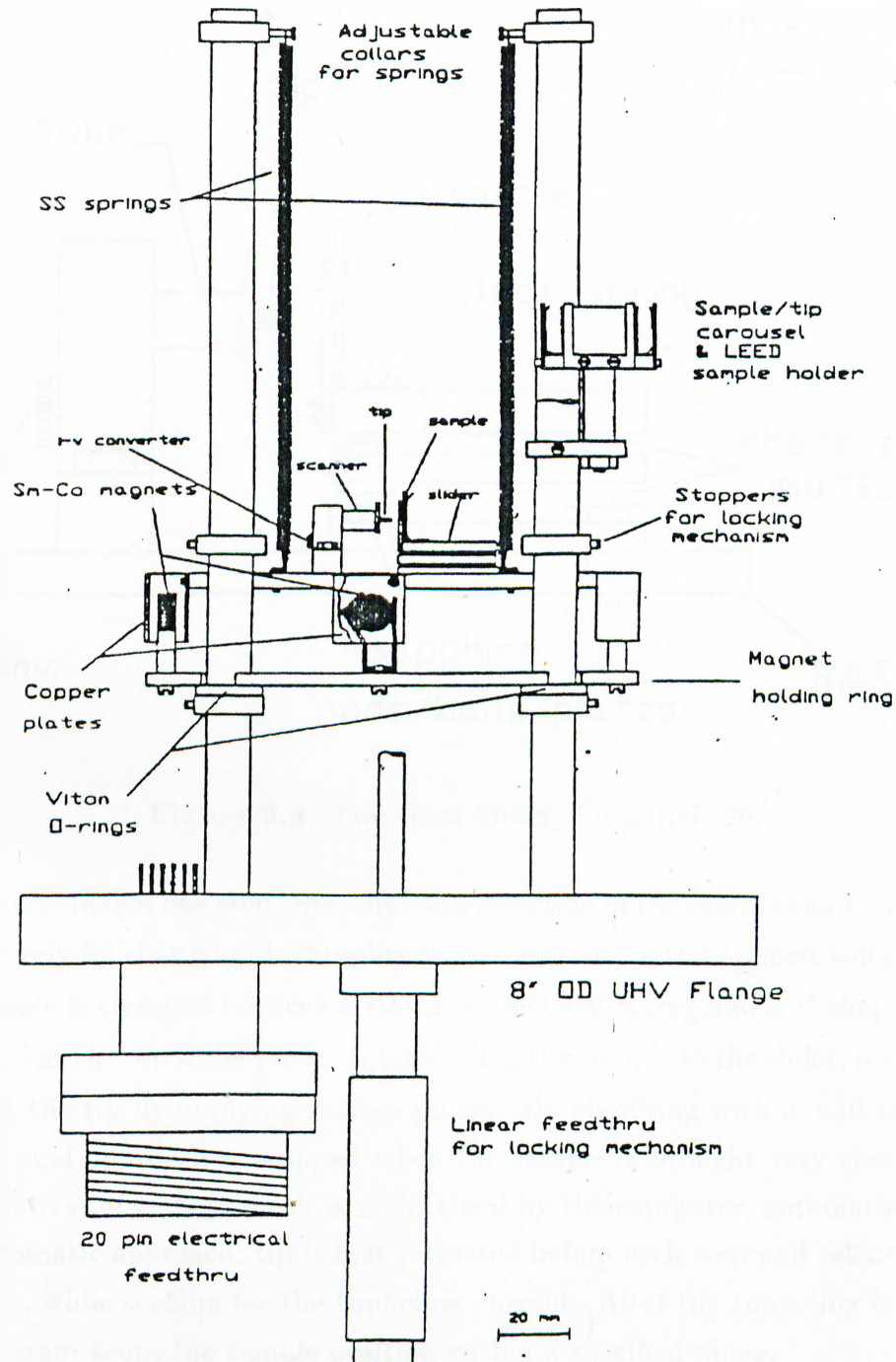


Figure 2.3: Scanning Tunneling Microscope. From Ref. 26.

to their original positions. However, the upper block will not follow piezo motion because of its relatively higher inertia and slides with respect to the balls. This

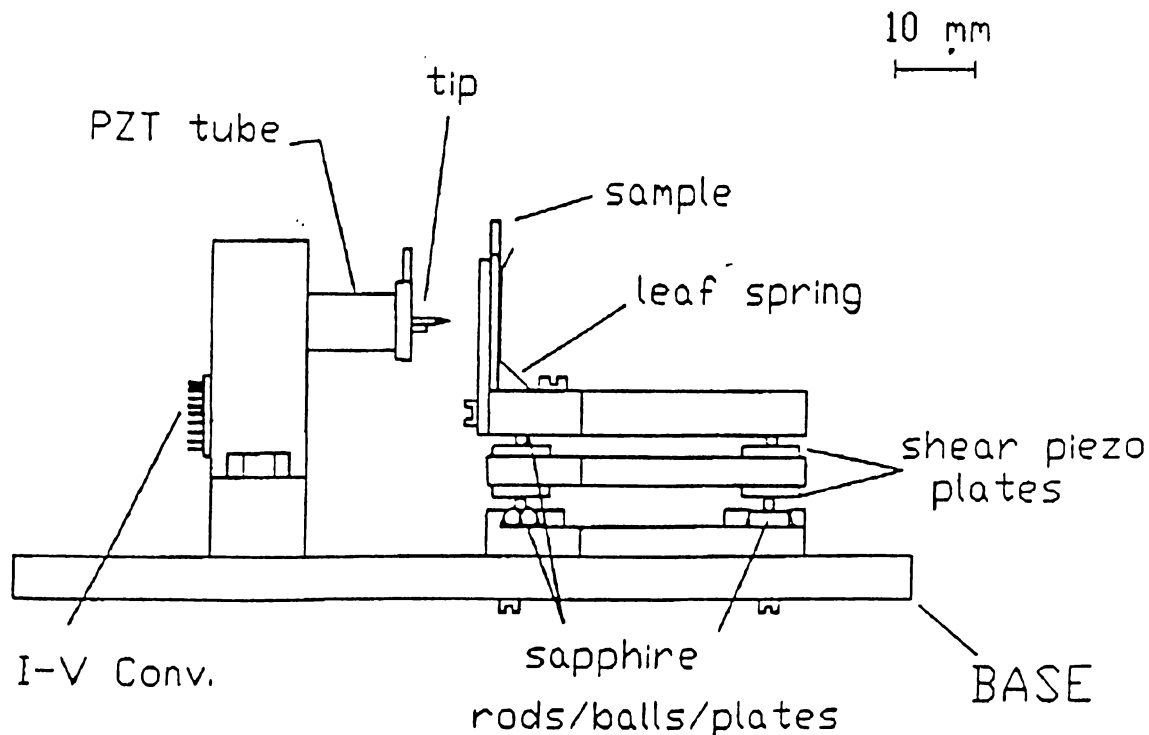


Figure 2.4: Two-Axes Slider. From Ref. 26.

whole cycle makes one step. Step size and direction of the motion can be adjusted respectively by changing the amplitude and polarity of the applied voltage.

Sample is clamped between a stainless steel leaf spring and a U-shaped plate mounted at the top slider piece. After loading the sample to the slider, it is moved towards the tip by applying voltage pulses. By observing with a $\times 10$ telescope this manual approach is stopped when the sample is brought very close to the tip. The rest of the approach is maintained by the computer, automatically. In the automatic approach, tip is first retracted before each step and released after the step, while seeking for the tunneling current. After the tunneling is sensed, the program keeps the sample position within a specified range.

2.2.3 Scanner

Our STM has a single tube piezo scanner. A stainless steel tip-holding station with tiny point-welded leaf springs is glued to the front end of the tube. The tip holder is inserted in that station by using the wobble stick. The outer electrode of the piezo tube is separated into four quadrants in order to achieve scanning in x and y directions. The whole tube is responsible for the motion in z direction, i.e. the z voltage is applied to all four quadrants while inner electrode is kept grounded. The scanner has a range of 6000 Å in each direction. This means, one can adjust the step size of the sample holder as large as 6000 Å during rough approach.

2.2.4 Tip

'Tip preparation is one of the most important problems of STM users'. In order to obtain atomic resolution, an atomically sharp tip containing at most a few atoms at the apex- is necessary. Even if you buy a commercial STM, you are not given prepared tips. All STM users in the world prepare tips themselves. There are several tens of methods of tip preparation. Although fifteen years have passed since the invention of STM, articles on new tip preparation techniques are still being published.^{27,28}

Tungsten, gold, platinum are typical metals used as STM tips. We use 0.2 mm diameter tungsten wire to prepare tips. Our method is electrochemical etching.²⁶ As illustrated in Fig.2.5, a straight tungsten wire is inserted in the beaker containing 10 % KOH solution floated on CCl_4 . A carbon electrode is immersed in the solution. When a DC bias, typically 6.5 to 7.5 Volts, is applied between the carbon electrode and the tungsten wire, the KOH solution etches the the wire. After a few minutes the wire is broken at the interface of the two liquids. The falling piece is a candidate for being a tip. To avoid damaging of the sharpness, the etching process is stopped as soon as the pieces break off from the tungsten wire. The shape and sharpness of the tip depends on the applied voltage, the position of the carbon electrode, the cleanliness of the solution, and

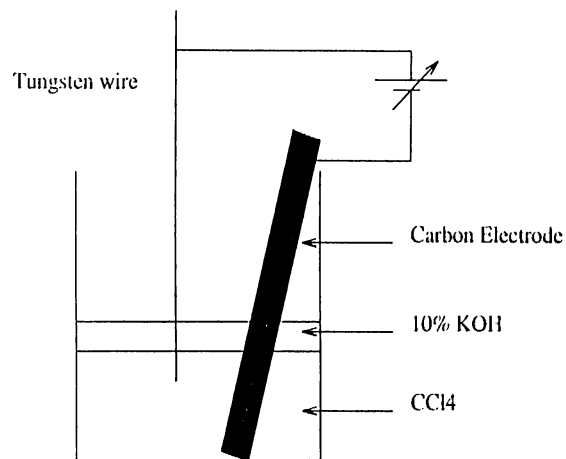


Figure 2.5: Tip Etching

how straight the wire is. Therefore, each time the tips were prepared, we have to come up with a new recipe.

The tips prepared with this method are point welded onto the stainless steel tip holders, then degreased from hydrocarbons by cleaning with trichloroethane, acetone, methanol and deionized water, successively. After being inserted to the tip transfer plates, the tips are ready to be transferred into the UHV chamber. SEM image of a typical tip prepared in this way is given in Fig.2.6.

Since the only way to understand whether a tip will work or not is to use it in an STM, it is necessary to prepare more than one tip to obtain a reasonable yield. Another important problem in tip preparation is the oxidation of the tips during etching and point welding. With an oxidized tip, it is impossible to obtain reliable STM results. Although there is an e-beam tip heater in the UHV system, since it hasn't been optimized yet the tips can't be annealed or cleaned from oxides. Therefore ultimate care should be taken to avoid oxidation of the tips during *ex situ* preparation.

Once the tunneling is obtained, the quality of the tip is understood by means of taking I-V curves. Besides the *ex situ* preparation of the tip, there are other processes that can be applied, by which one can make the tip operational. For example, applying short pulses to sample bias voltage stimulates tip switching,

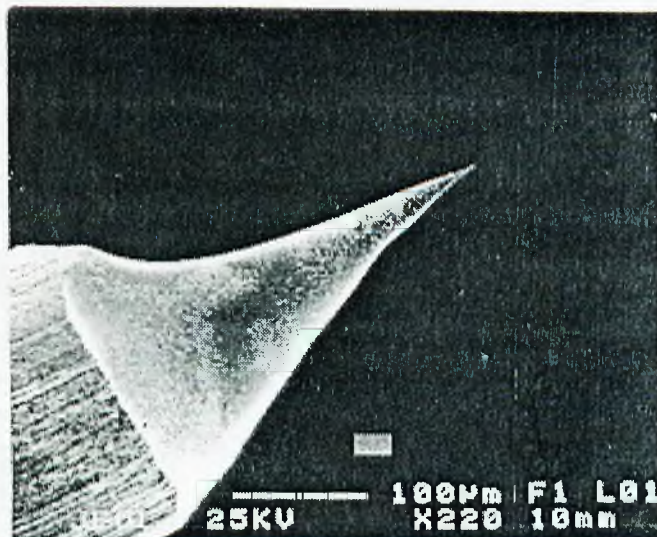


Figure 2.6: SEM picture of an STM tip.

i.e. capturing or leaving atoms from the apex, is an effective method. Taking dummy scans is another way to make the tips more stable. Even dipping into the sample can be used in case of emergency. Sometimes a clean tip may become unstable or a dirty tip may become atomically sharp during the operation of the microscope. An example of an initially sharp tip getting blunt while imaging the Si(001)(2×1) surface is given in Fig.2.8. On the other hand, Fig.2.7 shows a Si(001) surface imaged by a multi atom tip.

Another interesting example of an artifact caused by the tip is shown in Fig.2.9. A large area scan of a Si(001) sample is displayed. If the step at the right of the image is carefully observed, a contrast difference between the upper terrace of the step and the band near the step will be noticed. This is believed to be caused by a double tip.* The situation can be schematically described as in Fig.2.10. Initially, tip 1, which is closest to the surface, scans the upper terrace of the step. Later, when tip one extends downward to reach the lower terrace, tip 2 interrupts by tunneling from the upper terrace. The result is an image which is a repetition of the same region scanned first by tip 1 and later by tip 2.

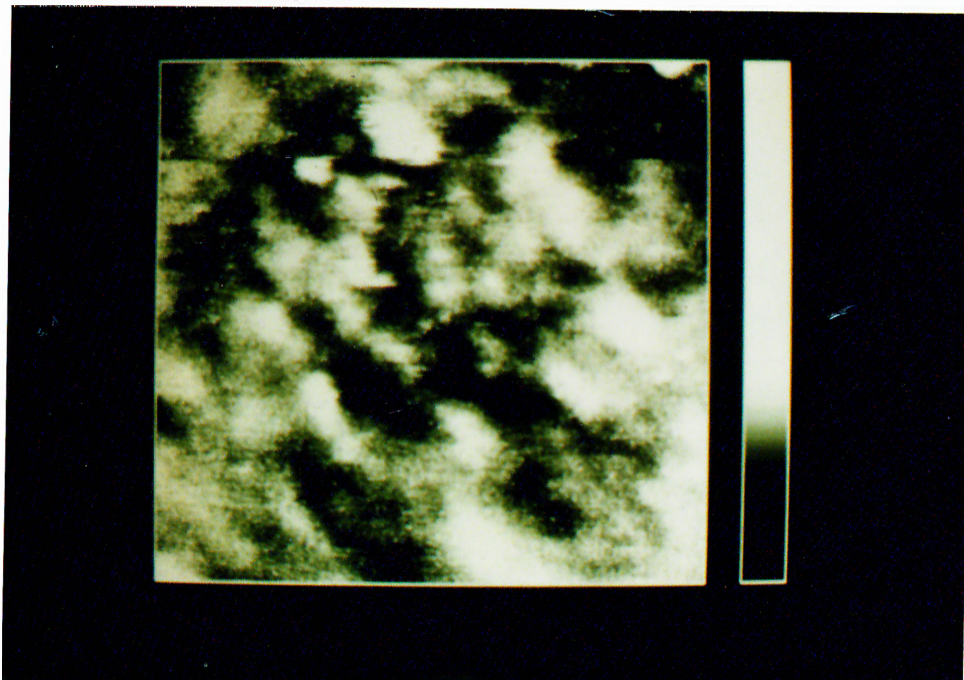


Figure 2.7: Si(001)(2×1) surface imaged with a multi atom tip.

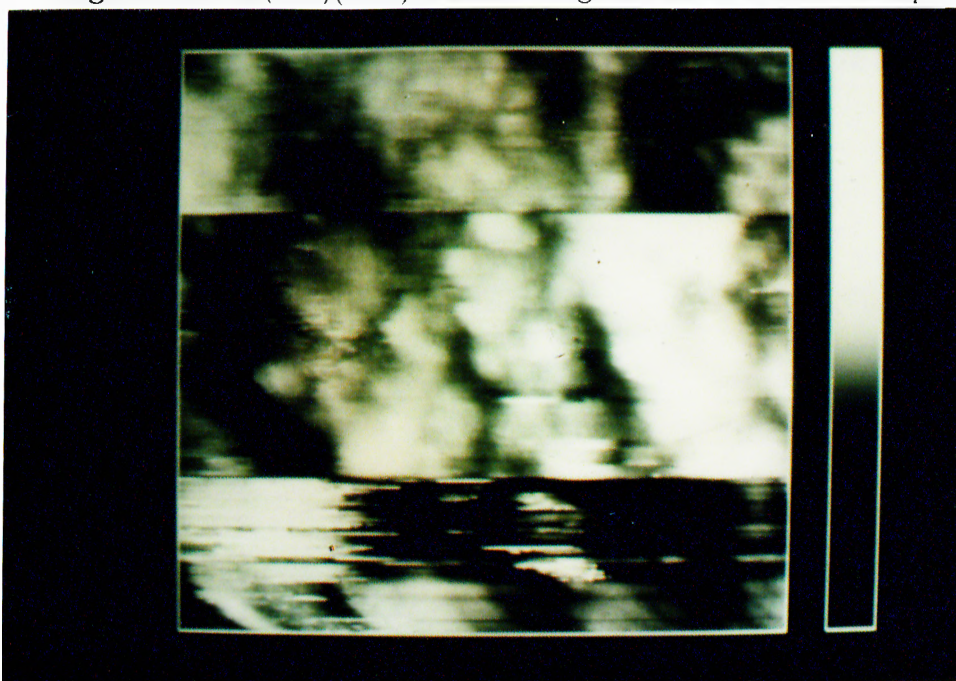


Figure 2.8: Initially sharp tip becoming blunt while imaging the Si(001)(2×1) surface.

2.3 Electronics and the Computer Interface

The STM electronics used in this thesis has been constructed, and the data acquisition and image processing softwares have been written by Oral.²⁶ A certain

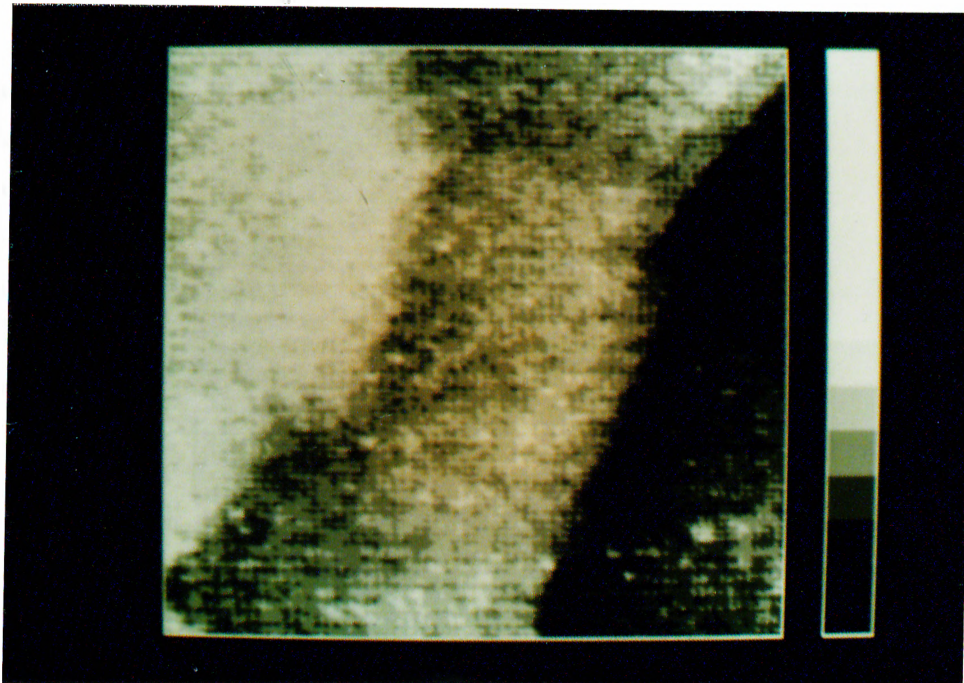


Figure 2.9: A step on a Si(001) surface imaged by a double tip.

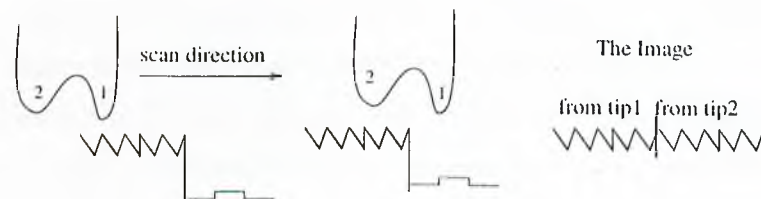


Figure 2.10: A possible schematic description of a double tip artifact.

bias voltage is applied to the sample and the tunneling current is measured with the preamplifier mounted at the back of the scanner. This preamplifier is the front-end of the i-v converter. The gain of the amplifier is 100 mV/nA. The control circuit, with the tunneling current and output voltage information, keeps the tip-sample separation within a specified range. The specification of the tip-sample separation is accomplished by setting the tunneling current to a certain value, and this is adjusted by the user.

A DT2821F data acquisition card is used for the computer interface. The control of the STM is performed by an i486 based personal computer having 80 MB HDD and a VGA color monitor. Data acquisition and image processing

software is able to record STM images at constant current and constant height mode. In the constant current mode, the tip is slowly scanned over the surface, while it is made to follow the vertical corrugations on the sample surface, the tip position, z , is recorded. The scan speed and the gain of the reading can be selected by the user. At each point, four voltage measurements are averaged to eliminate the noise. In the constant height mode, the tip is scanned over the surface very fast while the tunneling current is recorded. I-V curves can be acquired at any point, and it is possible to store the i-v curves for future reference.

The image data is stored in a 128×128 or 256×256 matrix. Top or 3-D view of the image is displayed just after the scan has been made. It is possible to store the images in data files for further processing. Previous images can also be read from the mass storage to make comparison between surfaces. Various displaying modes are available like top view, 3-D view and 3-D view with shading.

Generally, the results of the scans are not easy to interpret without image processing. The stored images are displayed and processed by another software. The finite slope that the images usually have, can be corrected by a slope correction subroutine. Thermal drift can be eliminated by another subroutine. Noisy images can be filtered by low pass convolution or median type filters. There are zooming, and cross sectioning options. The contrast of the image can be increased by histogram equalization.

Chapter 3

Si (001)(2×1)

Because of its electronic properties silicon has an important role in semiconductor technology. Although there are materials having relatively superior electronic properties, like GaAs, its abundance in the earth's crust, and hence its inexpensiveness has made Si one of the most widely used elements in advanced technology, from semiconductor microelectronics to solar cells. Silicon is a Group IV element with an indirect band gap energy of 1.17eV. It forms tetrahedral sp³ bonds, exhibiting a diamond crystal structure. The tetragonal bond structure plays an important role on the reconstruction of the Si(001) surface.

As mentioned earlier, STM and semiconductors have been in a cooperative relation since the invention of STM. Especially Si was the most widely used semiconductor in the development of scanning tunneling microscopy techniques and theories. Further, the controversies on the structure of Si surfaces, which are going to be discussed later, lasted with the first STM investigations. The first semiconductor surface imaged with STM was the 7 × 7 reconstruction of Si(111).²⁹ What does "7 × 7 reconstruction" mean? Due to the covalent nature of their bonds, clean semiconductor surfaces undergo a process called reconstruction. The periodicity of the surface atoms is different than that of the bulk atoms. The reason is quite clear. A simple bulk termination at the surface leaves a large number of unsatisfied (dangling) bonds. This results in a large free energy. As in every event in nature, the trend is to lower this free energy. This is achieved by the

rearrangement of the surface atoms to decrease the number of the dangling bonds, generally at some cost in increasing the fraction of the free energy derived from surface stress.³⁰ The terminology "m × n" refers to the two dimensional Miller-indices needed to describe the surface unit cell in terms of bulk lattice vectors. On an "m × n" reconstructed surface, the lattice constant in one direction is m times the bulk lattice constant, and n times that in the other direction. In the following sections, the reconstruction of the Si(001) surface will be discussed beginning from the first models proposed on its structure after the first LEED observations.

3.1 Dimerization on Si(001)

Si(001) surface displays a reconstruction that is a relatively simple modification of the bulk terminated structure. Initially, just after termination, each surface atom has two dangling bonds and is bonded to two subsurface atoms. A small displacement, without bond breaking, results in pairing of the surface atoms to form "dimers". Thus the number of dangling bonds is reduced from 2 to 1. This structure is a stable configuration and called 2×1 reconstruction of Si(001).

In their Low Energy Electron Diffraction (LEED) studies on Si(001) surface, Schlier and Farnsworth³¹ detected half-integral beams which they understood, could not arise from surface atoms in a bulk configuration. They proposed that the observed 2×1 surface mesh was consistent with a structure created when adjacent rows of surface atoms moved together in a bonding interaction. A schematic diagram of the Si(001) surface is shown in Fig. 3.1. This proposition of surface atom pairs (dimers) was not easily accepted for many years, because LEED investigations after those of Schlier and Farnsworth yielded higher order diffraction spots.³² The intensity and sharpness of the spots were strongly dependent on sample treatment. It was clear that only a symmetric dimer structure could not be the reason for all the observations.

Various other models, such as vacancy^{33,34} and conjugated chain models,³⁵ were proposed. This debate ended when electronic structure calculations by

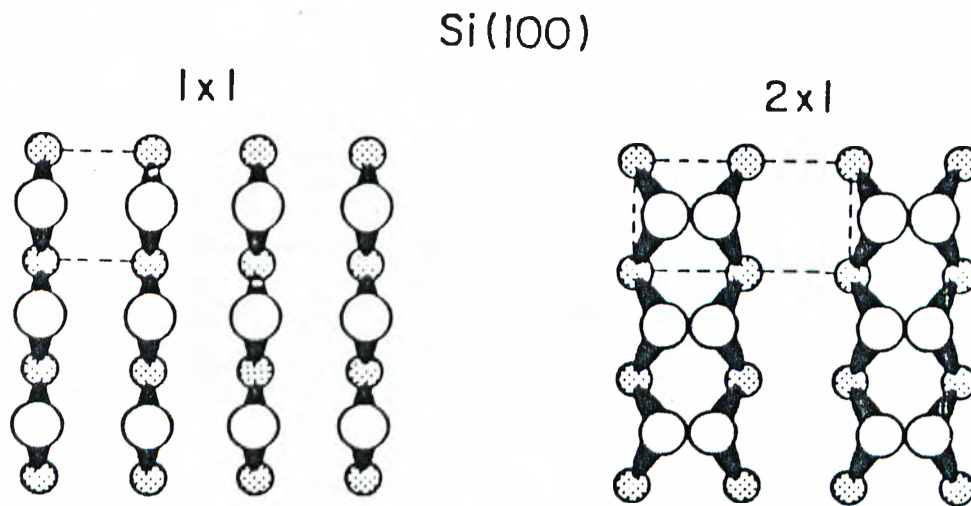


Figure 3.1: Schematic diagram of the Si(001) reconstructed surface. Taken from Ref. 40.

Appelbaum et al. on the dimer and vacancy models,³⁶ and by Kerker et al. on the conjugated chain model,³⁷ were compared with the photoemission data of Rowe.³⁸ The conclusion was that the surface dimer model appeared to explain most of the experimental results.

More than 20 years after the first LEED study, although dimers were generally recognized to be the principal feature of the reconstructed Si(001) surface, some dissatisfaction arose because of an important inconsistency. Again in LEED studies, besides integral and half integral beams, 1/4 order beams were sometimes observed. However, the dimer model could only explain the existence of integral and half integral diffraction.

The invention of Scanning Tunneling Microscope was a turning point in the investigation of the reconstructed Si(001) surface on the atomic scale. The structure of this surface was almost clear with the first STM results of Tromp, Hamers and Demuth.⁴¹ These images, though still having left some problems unresolved, clearly established important points regarding reconstruction of Si(001) surface. The most important one was the verification of the dimer model; the other models seemed not to match the topographic features of the surface. Another interesting point was that asymmetric (buckled) dimers which could give rise to 2×2 or 4×2 symmetries, were observed at the surface together with the

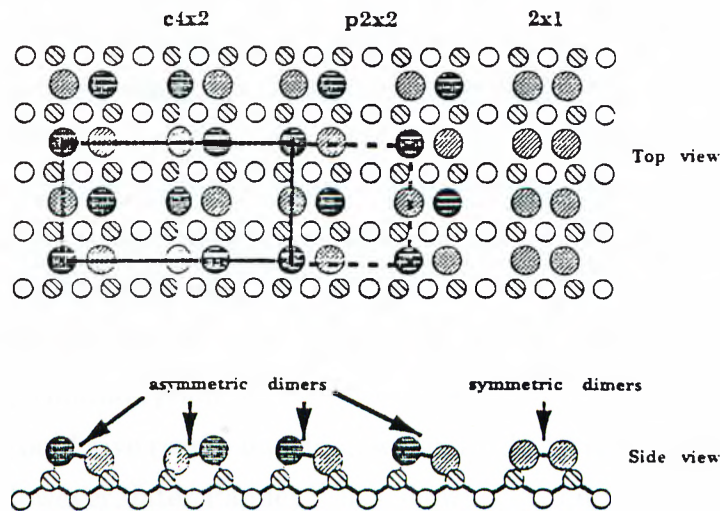


Figure 3.2: Schematics of the $c(4\times 2)$ and $p(2\times 2)$ domains on reconstructed Si(001) surface.

First layer atoms, second layer atoms, symmetric, and asymmetric dimers are indicated. From Ref. 39.

symmetric dimers. Buckled dimer is the dimer in which one atom is at a higher position than the other.

The symmetries $c(4\times 2)$ and $p(2\times 2)$ are due to the orientations of the atoms in the adjacent buckled dimers. Fig.3.2 shows $c(4\times 2)$ and $p(2\times 2)$ configurations schematically. The arrows denote the asymmetric dimer on the surface with the tip of the arrow indicating the up atom of the dimer.

In their later study on the atomic structure of Si(001) surface, Hamers et al. concluded that far from defects only symmetric dimers were observed, while buckled dimers were often observed near surface defects.⁴² They have shown that dimer buckling was easily stabilized by vacancy-type defects and that these defects forced most of the dimers in particular buckling orientations. They have also raised the idea that the dimers might be dynamically buckling about the equilibrium configuration at a certain time period. However, the dimers are observed to be symmetric on the time average since this period is short compared

to the STM measurement time. A suggestion on the reason of such a flipping was that it could be induced by STM tip perturbation.⁴³ Recently, Cho and Joannopoulos⁴⁴ have brought an interesting explanation to the STM induced asymmetry. They have shown that the tip surface interactions are significant enough to flip and bind an asymmetric dimer to the tip. As the tip is then moved along the surface, dimers are flipped tracking the tip and create what appears to be a symmetric image in the scan.

The possible reasons of buckling were tried to be given in a number of studies.⁴⁵⁻⁴⁷ The common point of these studies was that the charge transfer within a single dimer could give rise to buckling, which might be either static or dynamic (oscillating). However, later Pandey⁴⁴ has shown that buckling involving charge transfer to the top atom was an artifact of tight-binding calculations. He found that nonbuckled dimer is energetically most favorable, but buckling up to a dimer tilt angle of 10° did not increase the total energy significantly.

As a result, empirical tight-binding calculations by Chadi,⁴⁵ pseudopotential calculations by Pandey,⁴⁴ Payne et al.,⁴⁶ and Roberts and Needs⁴⁷ did not come up with satisfying conclusions about dimer buckling. Speculative explanations were made on this subject. The question "Which configuration is more stable, buckled or symmetric?" couldn't be answered exactly for years.

Wolkow, during his low temperature STM studies on Si(001) surface, resolved the long-standing problem regarding the dimer configuration.⁴⁸ He showed that on cooling to 120 K, the number of buckled dimers increased at the expense of symmetric appearing dimers, and concluded that only bistable dimers could account for this observation. Wolkow concentrated on the influence of surface defects on the dimer configuration. Symmetric appearing defects, such as "missing dimer" type, do not induce buckling. On the other hand, the defects which are themselves asymmetric, cause buckling in the neighboring dimers. As had been observed by Tromp et al., the magnitude of buckling decayed along a row with increasing distance from a defect. The buckling orientation was alternating from one dimer to the next. Alerhand et al.⁴⁹ presented a simple strain argument to account for this alternating buckling pattern. As shown in Fig.3.3, the up end

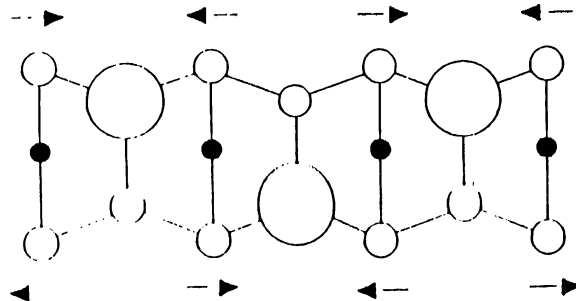


Figure 3.3: A simple schematic view of the lattice strain which acts to couple adjacent dimers in an anticorrelated manner. From Ref. 48.

of a buckled dimer causes second layer atoms to come together while the down end pushes second layer atoms apart. To compensate this distortion adjacent dimers buckle in the opposite direction.

In contrast to room temperature images, images taken at 120 K show extended regions of buckled dimers. At room temperature, buckling decays in length of six to eight dimers, while at 120 K it extends along a row, in most cases, with no apparent decay in magnitude. Adjacent buckled rows can interact in two ways. The first and the most common one is the case in which zigzag pattern of buckled rows are out of phase, that result in $c(4\times 2)$ symmetry. The second one is $p(2\times 2)$ symmetry which results when the zigzag pattern is in phase. If the defects are randomly distributed among the surface, then $p(2\times 2)$ can be seen as often as $c(4\times 2)$.

3.2 Steps

Steps are the fundamental structures of Si(001) surfaces. The stepped Si(001) surface has been intensively studied because of its importance in the heteroepitaxy of III-V semiconductors, particularly GaAs and SiGe on Si. Steps on Si(001) surface display a complex behavior that depends on many factors. Angle of miscut, annealing and growth conditions, contaminants, and surface stress are

examples of those factors.

Step is the boundary between two successive terraces. Because of the tetragonal bond structure of silicon, the dimers on two successive terraces which are separated by a monoatomic step, are perpendicular to each other. More clearly, the dimerization direction changes by 90° through a monoatomic step. Steps are named due to the dimerization direction on the upper terrace. If the dimer rows on the upper terrace run parallel to the step edge, then the step is type A, labeled S_A . Type B is the step the upper terrace of which contains dimer rows aligned perpendicular to its edge, and is labeled as S_B . On a Si(001) surface there are not only single (monoatomic) steps, but double steps as well. Double steps are the ones through which the dimerization direction does not change, i.e. the dimer rows are in the same in both the upper and lower terraces of the step. These steps are also labeled as D_A and D_B depending on their type.

The single step height in the [001] direction for the diamond lattice is $a/4 = 1.36\text{\AA}$, where $a = 5.431\text{\AA}$ is the bulk silicon lattice constant. Surfaces miscut from the [001] direction, known as vicinal surfaces, display a mean distance between single steps, i.e. mean terrace width, given by $a/4 \tan \alpha$ where α is the miscut angle. Surfaces cut toward the $[\bar{1}\bar{1}0]$ or the $[110]$ direction display two distinct types of single steps. When the surface is tilted toward a direction intermediate between $[110]$ and $[\bar{1}\bar{1}0]$, steps of mixed type A and type B character result. Since type A steps are formed by the sides of the dimer rows they are very smooth. On the other hand the ends of dimer rows form the type B steps that these steps have a tendency to form kinks. Surfaces with miscut angle larger than a few degrees have type B double steps. Since the dimerization direction is the same on terraces separated by a double step, these surfaces are referred to as single domain or primitive.

Chadi has proposed models for single and double steps of type A and type B.⁵⁰ These are shown in Fig.3.4. Formation energies of type A and type B single steps were calculated to be 0.01 eV and 0.15 eV, respectively, while type A and B double step formation energies were found to be 0.54 eV and 0.05 eV, respectively. Therefore S_A steps, having the lowest formation energy, seems to be energetically

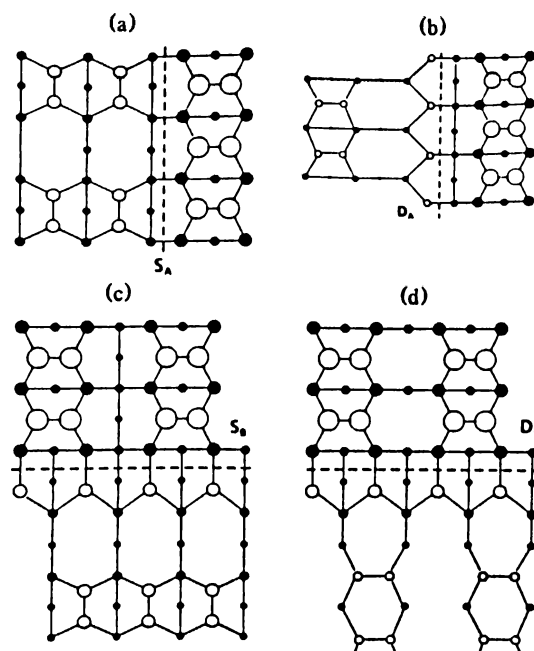


Figure 3.4: (a)-(d) Top views of S_A , D_A , S_B , and D_B steps respectively. The dimerization direction of the topmost atoms is along the $[110]$ direction. The dashed lines indicate the step positions. Open circles denote atoms with dangling bonds. Larger circles are used for upper-terrace atoms. Taken from Ref. 50.

preferred among the others. However, for example, the existence of two terraces on a surface requires two steps of single type, while the number is reduced to one in case of a double step. Since the formation energy of a D_B step is lower than the total of the formation energies of S_A and S_B steps, D_B step is energetically favored over $S_A + S_B$ steps. Hence for years the vicinal Si(001) surfaces had been thought to have only one equilibrium state in which only double steps are present. However, it has been observed later that small vicinal angles, on the order of 1° or less, lead to stable single-stepped surfaces. Alerhand et al. have brought an explanation for these observations. They showed that, at vicinal angles more than 2° , the equilibrium is double stepped, but for small angles single steps are stable.⁵¹

In this chapter a history of the Si(001) surface was given, and the fundamental features of the reconstructed surface, i.e. dimers, steps etc., was explained. The STM images, which are explanatory examples of the features described in this

chapter, will be presented and discussed in the following chapter.

Chapter 4

Results

In Chapter 2 the instruments and preliminaries to get an STM image were explained in detail, and the structure of the Si(001) surface was presented in Chapter 3. In this chapter, the sample cleaning procedure followed by the images of clean Si(001) reconstructed surface will be given. Later, a few images of Si and Ge grown Si(001) samples are going to be shown and discussed in light of the previous studies, both theoretical and experimental.

The samples used in the experiments were cut in the form of 6×8 mm rectangles, from 525 μm thick, P-doped, n-type Si(001) wafers with 1- 10 Ωcm resistivity oriented to within 0.5° of (001) plane. The samples were first cleaned from hydrocarbons by degreasing with a four-step process including trichlorethylene, acetone, methanol and deionized water, respectively. Trichlorethylene, acetone, and methanol steps are performed in ultrasonic bath each lasting 9 minutes.

An *in situ* cleaning process is inevitable to obtain an atomically flat and clean surface, since there is a native oxide layer on silicon wafers, which immediately grows when exposed to atmosphere even after etching. There are three common methods of cleaning silicon surfaces in UHV. The first is the sputter cleaning of the surface with low energy noble ions like Ar^+ , followed by the annealing of the sample to eliminate the damage created by bombardment.⁵² The second method is high temperature etching⁵³ of the native oxide layer on the samples without any

ex situ chemical cleaning. The third method involves both an *ex situ* chemical cleaning and an *in situ* cleaning. The sample is first cleaned chemically with several oxide wet etch-regrowth cycles and finally a passivation layer is grown on the surface. This passivation layer works as a protective layer as well, during carriage and transfer of the samples to UHV. In UHV the passivation layer is evaporated off the surface at a temperature of ~ 900 °C.⁵⁴ This third method is used to clean Si(001) samples in our experiments.

In the following section, cleaning procedures used for Si(001) surfaces in UHV is going to be described by giving examples of uncleaned samples. Then clean Si(001) surface images will be interpreted. The last section is devoted to silicon and germanium growth on Si(001).

4.1 Si(001)(2×1)

The (2×1) reconstruction of the Si(001) surface was explained in Chapter 3. To summarize, every atom of the bulk terminated Si(001) surface has two unsaturated bonds. The large free energy due to this bond breakings is minimized by the pairing of the neighboring atoms. The model of the reconstructed surface was presented in Fig. 3.1. As most of the semiconductor surfaces, Si(001) exhibits a stepped structure. Because of the tetrahedral bonding of Si, the dimers on terraces separated by mono-atomic steps lie perpendicular to each other.

Above the cleaning method was described roughly. The detailed descriptions of both *ex situ* and *in situ* processes are as follows. The chemical cleaning method used for the experiments is the Shiraki⁵⁵ etch-regrowth procedure. This method is used mainly to clean the carbon contamination, but it also works for oxide removal from the surface automatically. After degreasing the wafer from hydrocarbon contamination as described above, it is cleaned by oxide etch-regrowth in aqueous 4% HF and NH₃:H₂O₂:H₂O (1:1:3) solutions, respectively. Ammonia and peroxide solutions were of electronic grade, with 25% and 30% concentrations, respectively. The sample is dipped in the solutions for 30 sec, and rinsed with overflowing deionized water for a minute and dried with blowing

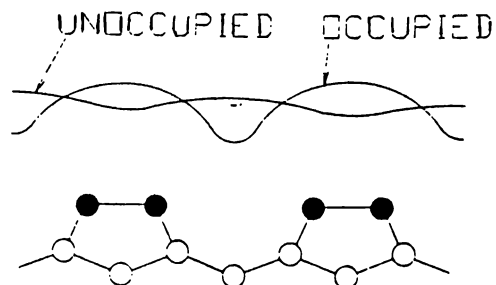


Figure 4.1: Schematic STM occupied and unoccupied state contours and their relation to the underlying dimers. After Ref. 56.

dry nitrogen gas between the etch-regrowth cycles. At least 5 etch and regrowth cycles are performed to clean the samples, the last step being oxide regrowth for a minute. Then the samples are cleaned with overflowing deionized water for 2 minutes. Samples are dried with blowing dry nitrogen gas before transferring into the load-lock chamber. This chemical cleaning is performed on a wet bench inside a Class-100 clean room and the sample is transferred to the STM lab in a covered Petri dish and quickly loaded into the fast entry lock to eliminate contamination or further oxidation.

The sample is then transferred to the UHV system and degassed by e-beam heating at ~ 600 °C for about 10 hours. The pressure is kept in the 10^{-10} torr range during degassing. Then the sample is flashed to ~ 900 °C for 2 minutes followed by a sudden increase to about 1050 °C. After waiting again for 2 minutes at this value the temperature is set to ~ 900 °C for a minute. Finally the sample is slowly cooled down in a few minutes.

The cleaned sample is left on the sample manipulator for about 15 minutes, and then transferred to the sample carousel in order to cool down and for LEED analysis as well, if necessary. The sample temperature drops to the STM temperature in about 1.5 hours. Then the sample is transferred to the slider and it is ready for STM analysis.

Following the procedure described in Section 2.2 tunneling is obtained. In all

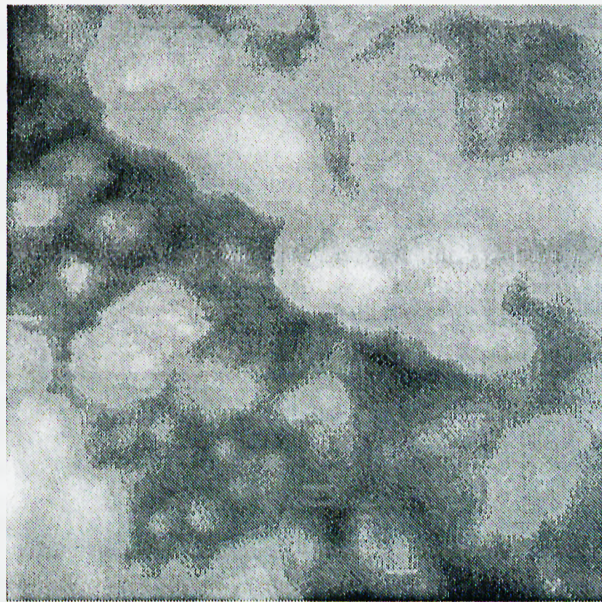


Figure 4.2: An image of a Si(001) surface roughened because of improper preparation. The image size is 194×194 Å. Sample voltage and tunnel current are -2 V and 1 nA, respectively.

experiments, negative sample bias is chosen, because the STM images taken at positive sample bias do not give the exact topograph of the Si(001) surface.⁵⁶ As is schematically illustrated in Fig.4.1, at positive bias, maxima are not observed on dimers but between them. However at negative bias maxima are coincident with dimers. This problem seems to bring only a shift in the image, but for instance, if an S_A type step is imaged at positive bias the dimer rows at the step edge will be seen thinner than they really are. Therefore negative sample bias is more convenient to work with. The images throughout this thesis are all filled state images.

The Si(001) samples were used only for one experiment each. Since a clean sample begins to be contaminated by the residual gases in the UHV chamber after about 10 hours, it must be cleaned for longer experiments. However, Oral²⁶ has recently shown that the number of defects appeared to increase with the number of cleaning cycles. Therefore for each trial a new Si(001) sample was prepared.

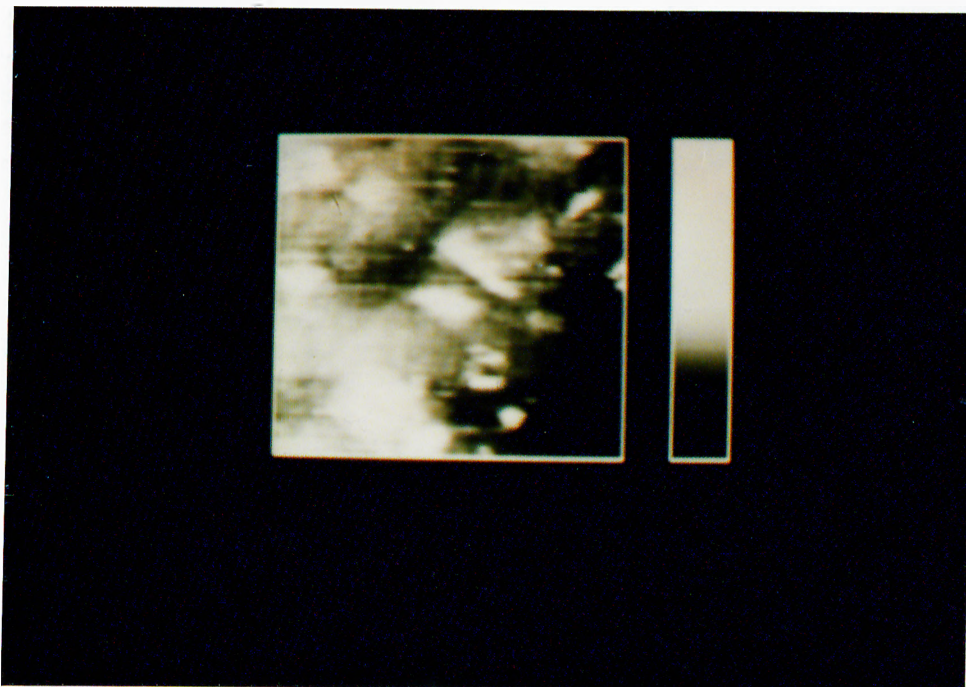


Figure 4.3: A large area scan of a Si(001)(2×1) sample. The image size is 912×912 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

As might be expected, such a critical *ex situ* and *in situ* sample preparation did not routinely end with satisfactory results. Although this cleaning procedure is found to work quite well,²⁶ since most of the processes, from chemical cleaning to e-beam heating, are manually achieved, it was difficult to follow the same steps for every sample, and hence to get clean and defect free samples in every treatment. To analyze the sample with LEED instrument is a good way to understand whether it is clean or not. A sharp diffraction pattern means that the region from which the electrons are diffracted is clean. However, this does not allow us to conclude that the sample is entirely clean. There may be regions that remain still contaminated. Therefore during STM analysis, it is necessary to carry the tip to different regions of the sample until a clean part is found.

It is very important to heat the sample at a right temperature. Exceeding the desired temperature values is as inefficient as heating the sample to insufficient temperatures. Even the speed of sample cooling to room temperature is a critical step. The heating of the Si(001) surface above a critical temperature results in

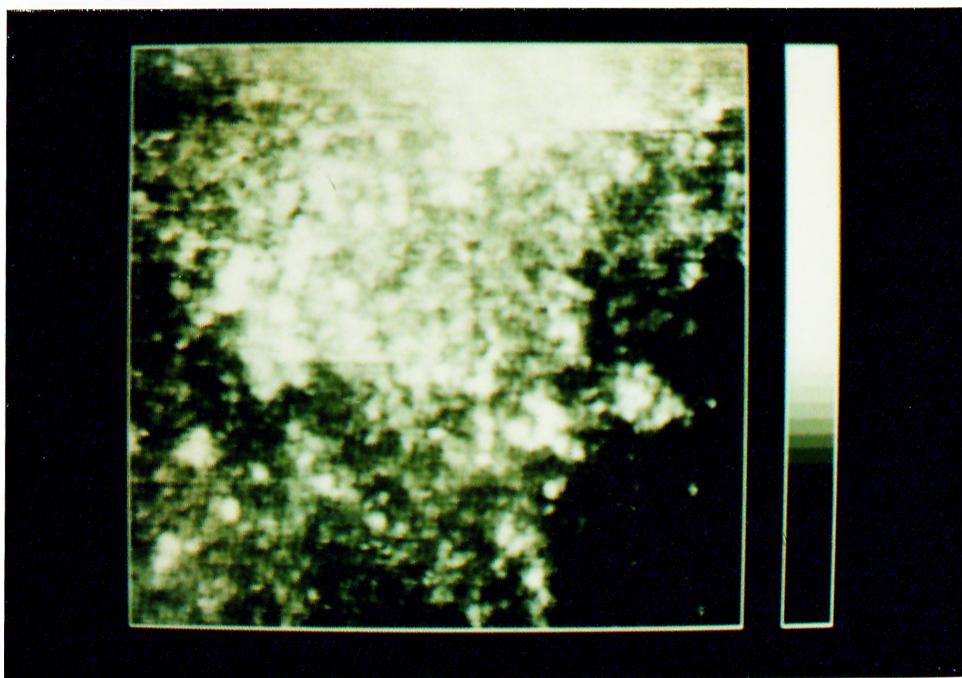


Figure 4.4: A large area scan of a Si(001)(2×1) sample.

The image size is 1215×1215 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

microscopic roughening of the surface.¹² The image of such a surface is shown in Fig.4.2. Two large area images of two different Si(001) sample are given in Fig.4.3 and Fig.4.4. In the first one, near the steps islands appear which seems to be unremoved contamination. These structures are believed to be due to contamination which served as a tiny mask during HF dip or oxide regrowth.²⁶ Fortunately, there are clean regions which may permit for smaller area STM scans. However, the region displayed in Fig.4.4 is almost totally contaminated, most probably by oxides. These two samples were cleaned with the same method as the others. As it is mentioned before, a small unnoticeable deviation from the procedure may have an extremely negative effect on the sample surface cleanliness.

During the optimization of the tip/sample preparation procedures, the initial objective was to get a general view of the surface, and to take images showing the terraces and steps on a relatively large scale, rather than insisting on atomic resolution. Fig.4.5 shows a large area image of Si(001) surface exhibiting a large

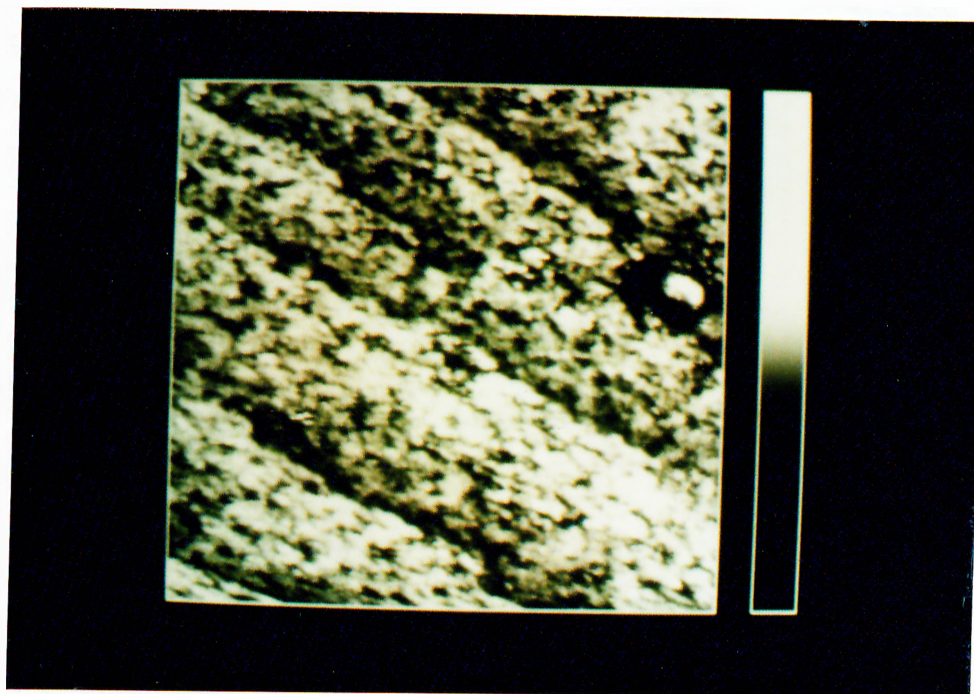


Figure 4.5: An image of Si(001) surface exhibiting a large number of steps. The image size is $608 \times 608 \text{ \AA}$. The sample voltage and tunnel current are -2 V and 1 nA , respectively.

number of steps. The black hole near the top most step in the figure is most probably due to a tip crash during previous scans. As mentioned before, vicinal Si(001) surfaces have an average terrace width dependent on the miscut angle α with the ratio $a/(4 \tan \alpha)$, which gives for our samples of 0.5° miscut an average terrace width of about 160 \AA . From the image in Fig.4.5 the average terrace width is calculated to be approximately 170 \AA which is in good agreement with the expected value.

It was mentioned in Chapter 2 that for vicinal Si(001) surfaces having a miscut angle less than 1° , the single stepped structure is most stable. Thus the Si(001) samples used in this study, being 0.5° misoriented, have a single stepped equilibrium structure. No double steps have been observed in general throughout the experiments. Only at a small region of one sample, a double step was imaged, which is believed to be due mainly to the heat treatment. The image is shown in Fig.4.6. The first step from the left is an S_A type single height step. A small portion of the topmost terrace which ends with an S_B type step was grown

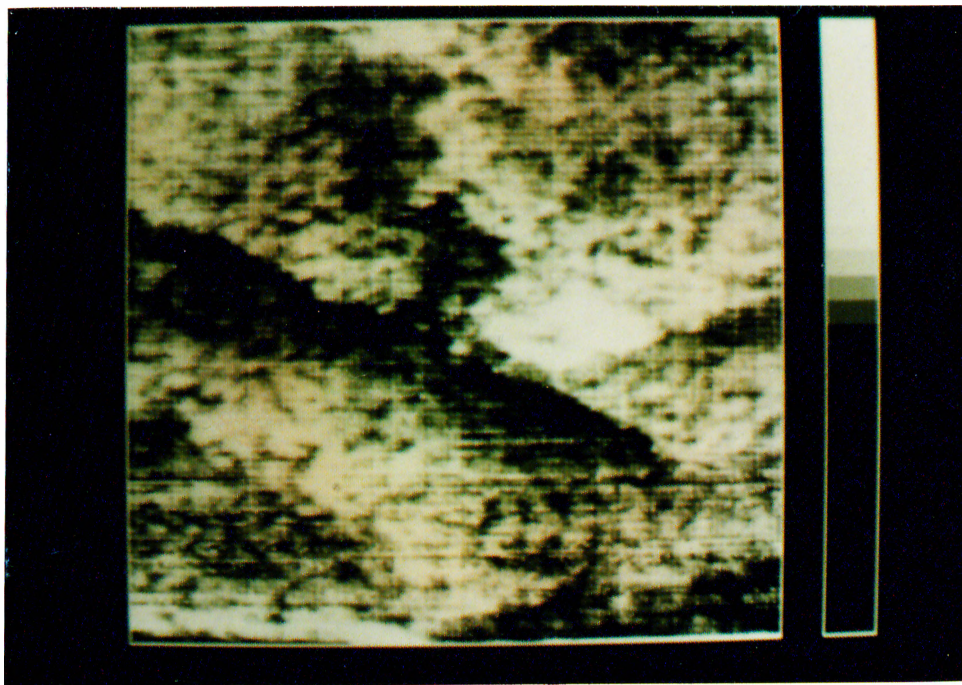


Figure 4.6: An image of Si(001) surface exhibiting a double step. The image size is $486 \times 486 \text{ \AA}$. The sample voltage and tunnel current are -2 V and 1 nA , respectively.

through the S_A type step and stopped there forming D_B type double height step. In addition, a bright region, the reproducibility of which is verified with a few more scans of the same area, i.e. it was not accidental, is seen near the double step. An image of another sample, shown in Fig.4.7, shows a similar behaviour. Again, the topmost terrace caught the underlying terrace, and a double step is formed. Surprisingly, as in the previous figure, there is a contamination near the double step. The contaminations seen in these images are most probably SiC islands, which are known to act as pinning sites for steps.⁵³ The annealing temperature of $1050 \text{ }^\circ\text{C}$ is sufficient to cause the evaporation of oxides from the surface whereas the removal of silicon carbide requires higher temperatures. Some of the determinants of the stepping of Si(001) surface are angle of miscut, annealing and growth conditions, contaminants, and surface stress. In the case of the double stepped sample in Fig.4.6, emphasis must be given to contaminants as the most important determinant. In summary, the particle on top of the terrace, which is believed to be a carbon contamination, is responsible for the formation

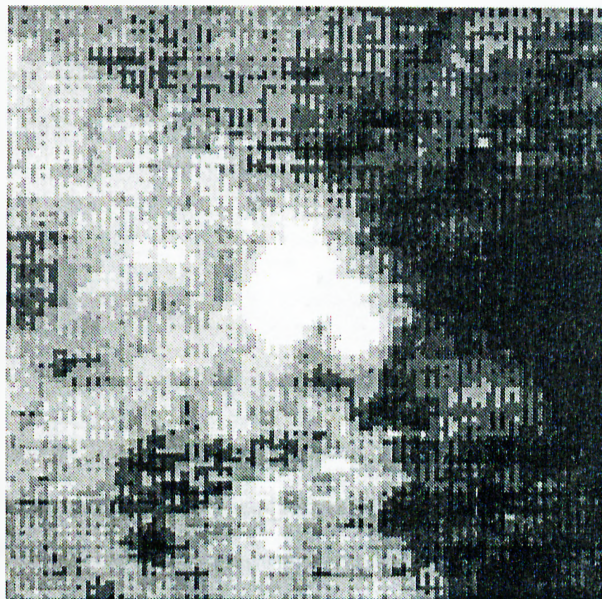


Figure 4.7: Another image of Si(001) surface exhibiting a double step. The image size is 304×304 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

of the double step.

Having been successful in cleaning a few samples and observed steps and terraces on the samples, we determined an imaging strategy for the rest of the study. Usually large area scans were taken first to find a clean and atomically flat region on the sample. If the scanned area was not found to be clean enough, then the sample was moved left/right using the x -slider in order to find an appropriate region. A typical large area scan of a Si(001) sample cleaned with the previously described method is displayed in Fig.4.8. Even though the widely spaced mono-atomic steps are clearly seen, which means that a high vertical resolution was obtained, because of the insufficiency of the number of pixels, the image is far from giving information about the cleanliness and atomically flatness of the sample. In addition, since no lateral atomic resolution was obtained in this image, no conclusion could be drawn out about the characteristics of the steps at a first look. However, since it is known that the ends of the dimer rows form the S_B steps, and the sides of those form the S_A , S_B steps are expected to be rough,

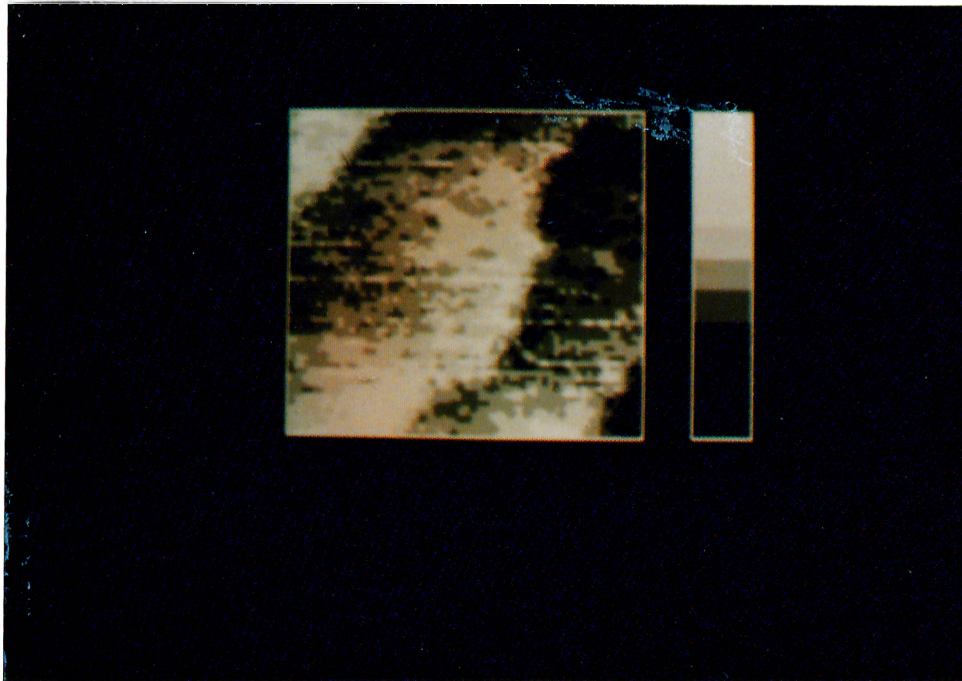


Figure 4.8: A large area scan of a Si(001)(2 \times 1) sample. The image size is 608 \times 608 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

while S_A steps are exhibiting a relatively smooth structure. Consequently it can be argued that the steps at the upper left and lower right corners are S_A type and the one lying between them is an S_B type step.

After finding an appropriate region on the sample, the tip was moved over the surface to an atomically flat section and high resolution images were tried to be taken. Fig.4.9 shows the high resolution scan of the Si(001)(2 \times 1) sample after moving the tip to the lower right corner of the region displayed in Fig.4.8, near the mono-atomic step. The scan area was set in order for the image to include that step. Though not clean enough, the sample exhibits the fundamental feature of Si(001)(2 \times 1) reconstructed surface, namely the dimer rows. The reason for the image not being totally clean is not only the dirtiness of the sample surface, but the tip switches which are clearly seen to occur many times, as well. Because of those tip artifacts the change of dimerization direction, i.e. the passage from (2 \times 1) to (1 \times 2) domain, at the step, and the step itself are not visible. However, the dark region running parallel to the dimer rows is known to correspond exactly

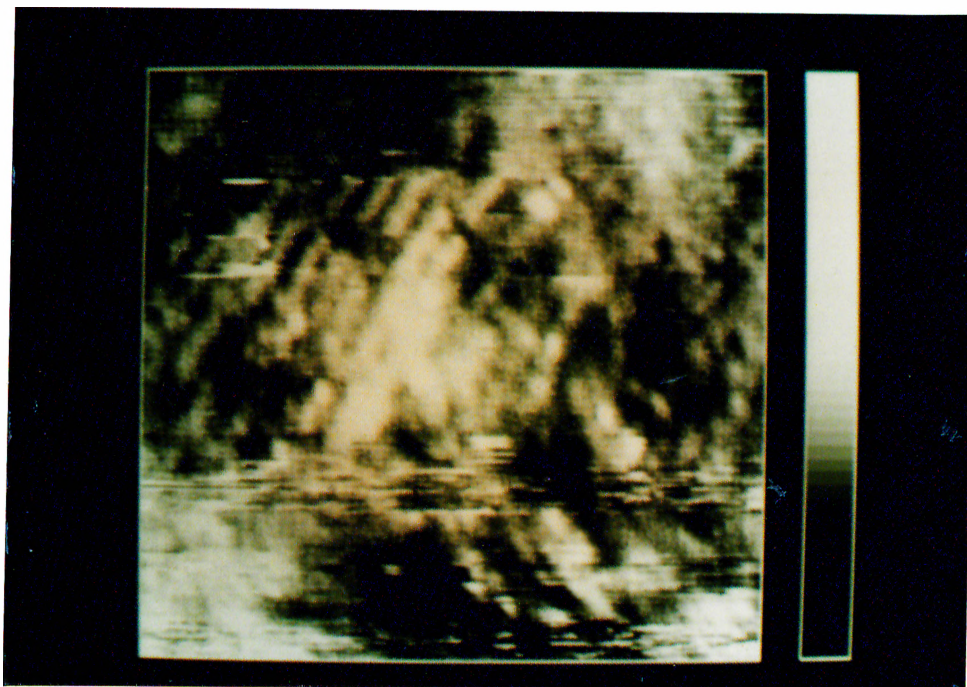


Figure 4.9: High resolution STM image of a Si(001)(2 \times 1) sample. The image size is 194 \times 194 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

to the position of the third step of the image displayed in Fig.4.8. This enabled us to check the validity of the previous argument on the types of steps of the large area scan. The high resolution image clearly tells that the step of interest is S_A type, which is exactly the conclusion of that argument. Thus smoothness was found to be a criteria for the investigation of the stepped surfaces and the determination of the step characteristics.

Again a large area scan of a Si(001)(2 \times 1) sample surface is displayed in Fig.4.10. Three steps, the types of which can not be extracted because of the low resolution, are clearly visible. Then moving the tip near the top most step a high resolution image was taken, which is shown in Fig.4.11. In this image, although the upper terrace of the step was not perfectly traced, the switch from (2 \times 1) domain to (1 \times 2) domain at the S_A type step is obvious. The dimer rows of the upper terrace are only seen near the step, while on the lower terrace individual dimer rows are quite clear. In addition, single, double and multi dimer vacancies, which are the basic types of defects on Si(001)(2 \times 1), can be seen. Single and

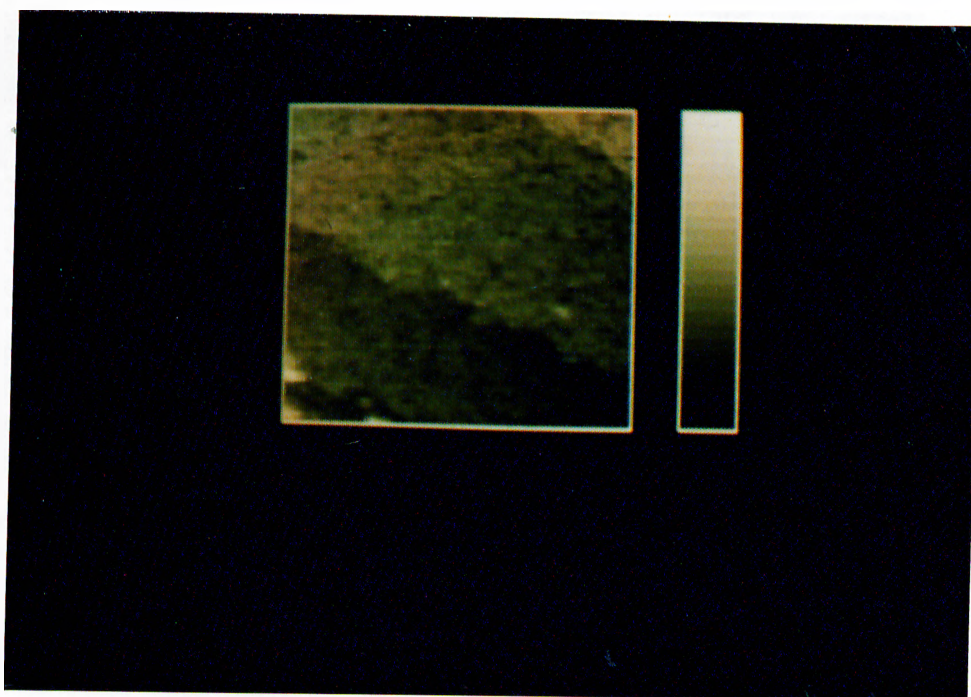


Figure 4.10: A large area scan of a Si(001)(2×1) sample.

The image size is 608×608 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

double missing dimers and a vacancy formed by the disappearance of one of the atoms of two adjacent dimers are shown in Fig.4.12.

The different kinds of vacancies are more clearly visible in the high resolution image presented in Fig.4.13. Pandey proposed missing dimer type defect on the basis of theoretical calculations.⁴¹ When a dimer is missing, four broken bonds are present in the subsurface layer. Dimerization in the second layer in the direction parallel to the dimer rows eliminates those broken bonds. This stabilization is partially offset by the elastic strain induced by the dimerization. However, if the defects are sufficiently far apart so that their elastic strain fields do not overlap, the net energy is lowered.

Another large area image of a sample prepared with the same method is shown in Fig.4.14. The surface is seen to be very clean. The relatively high resolution image given in Fig.4.15 was taken after moving tip to the lower right region of the previous figure. Dimer rows on the upper and lower terraces of an S_A type step can be seen to be perpendicular to each other. Further, the surface has

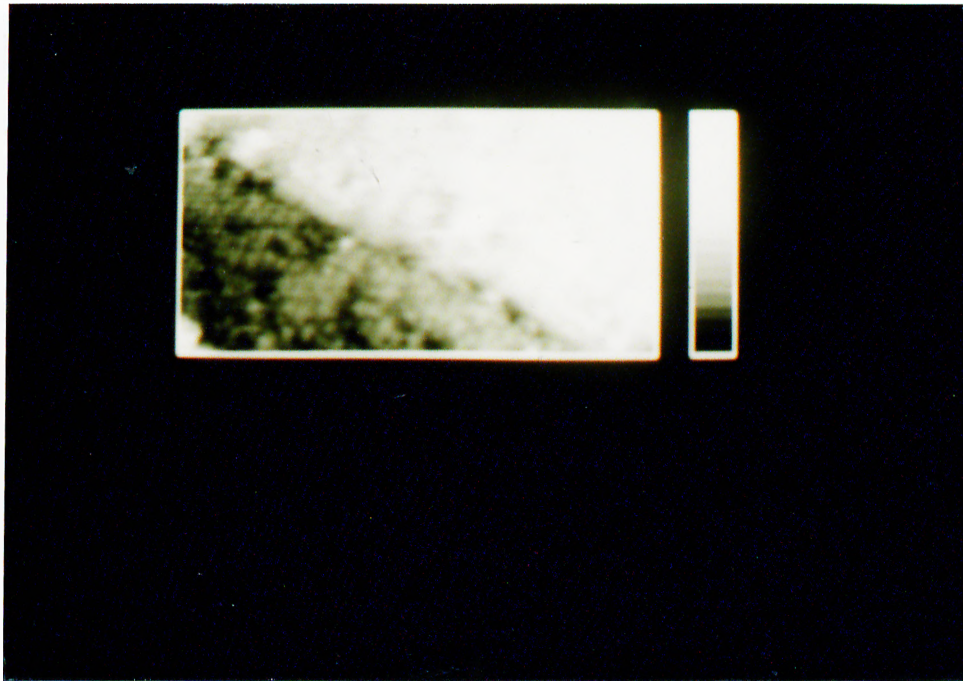


Figure 4.11: A small area scan of a Si(001)(2×1) sample. After moving the tip to the upper right corner of Fig.4.10. The image size is 260×140 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

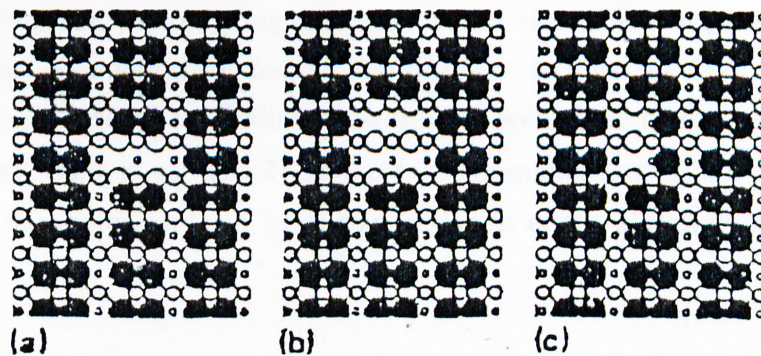


Figure 4.12: The three different types of vacancies on Si(001)(2 × 1) surface. From Ref. 26.

a very high density of defects, such as missing dimers, missing dimer groups. The part of the upper terrace near the lower right corner, if carefully inspected, appears to contain buckled dimer rows. The reason for the dimers to be buckled on this surface is clearly understandable. As it is mentioned previously, surface defects which themselves are asymmetric in nature, are the main reasons of dimer

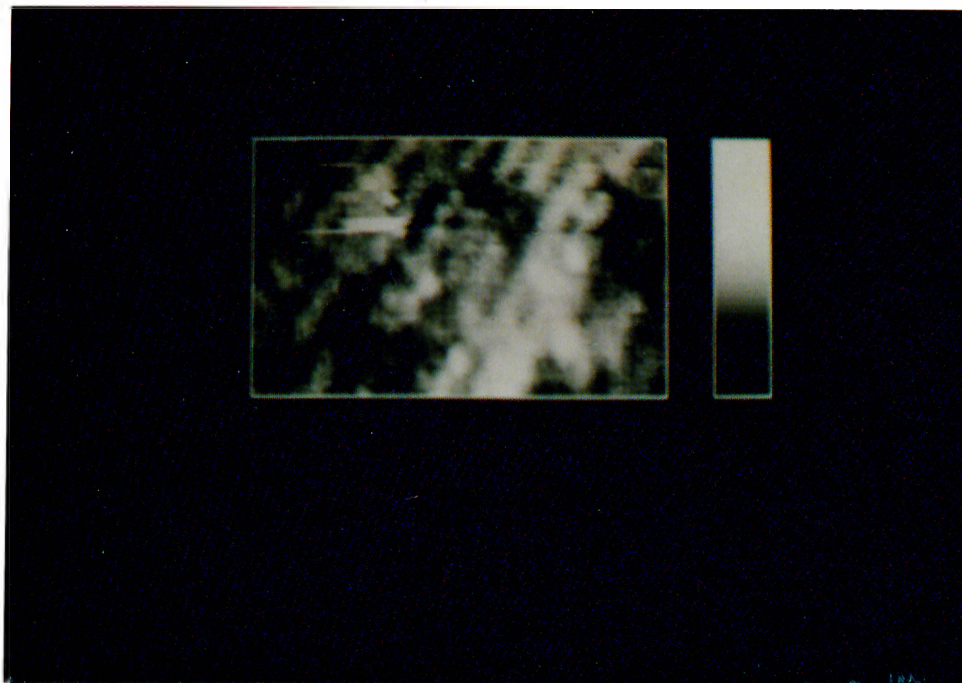


Figure 4.13: A high resolution image of Si(001) surface.

The image size is 115×78 Å. The sample voltage and tunnel current are -2 V and 1 nA, respectively.

buckling. However, the buckling does not extend along the complete dimer rows, rather decays in a length of five to ten dimers. It must be kept also in mind that tip-sample interaction induces buckling as well. Due to the buckling of the dimers, small regions of $p(2 \times 2)$ and $c(4 \times 2)$ domains are visible in the image. As well as vacancies and tip perturbation, step edges also induce buckling of dimers.¹²

4.2 Si and Ge growth on Si(001)

Crystal growth has been a technologically and scientifically attractive area for many years. In the last 20 years, the advent of the techniques such as molecular-beam epitaxy (MBE) and chemical vapor deposition for growing very thin epitaxial films has opened the possibility of the development of useful electronic, optoelectronic, magnetic, bioelectronic devices. In these technologies the growth mechanism is extremely important. For example, achievement of good

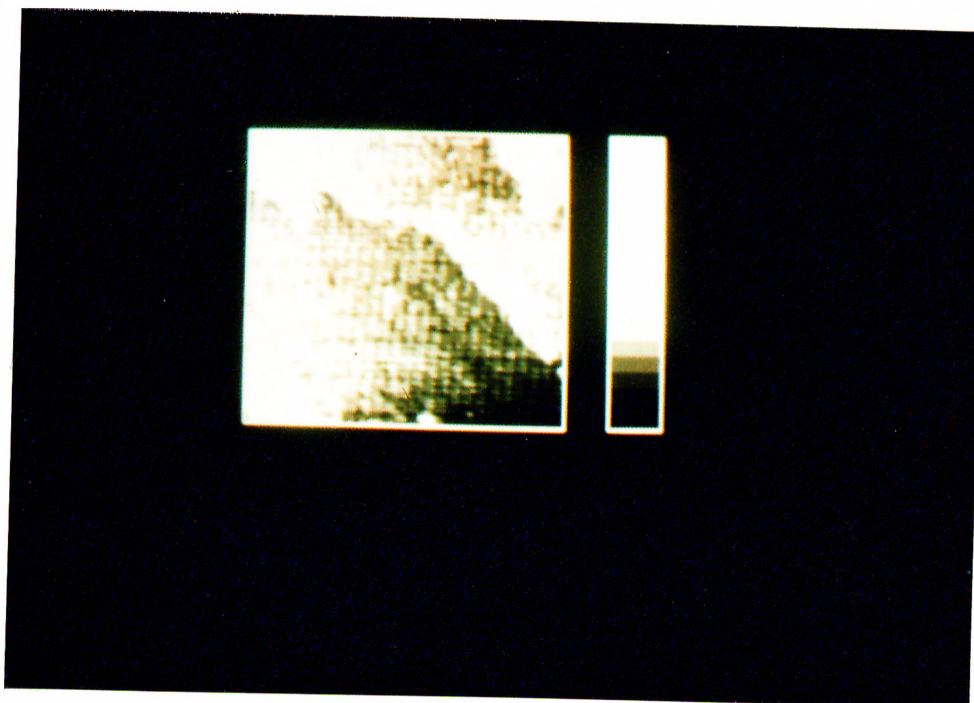


Figure 4.14: An image of a Si(001) surface

The image size is $608 \times 608 \text{ \AA}$. Sample voltage and tunnel current are -2 V and 1 nA , respectively.

performance in electronic or optoelectronic devices requires epitaxial films with thicknesses in some cases as small as a few atomic layers. As a result of the need to fabricate ever smaller and more densely packed microelectronic devices, the covalent materials of groups III, IV and V of the periodic table of elements have been attracting a lot of attention. Especially SiGe based heterostructures, because of their electronic and optical properties, are promising, in addition to being compatible with matured Si technology. They offer potential integration with the conventional silicon integrated circuits. Heterostructure and superlattice active regions in these devices give very high performance.

Si homo-epitaxial and Ge hetero-epitaxial growth on Si(001) have been studied by many groups using STM.^{57,58,61,53,54} It has been found that the substrate temperature, growth rate and the structure of the substrate played an important role in epitaxial growth. Atomistic mechanism of crystal growth can be explained by the terrace-ledge-kink model⁶² as shown in Fig.4.16. The model describes the surface morphology in terms of terraces, steps of a single atom high (the ledges),

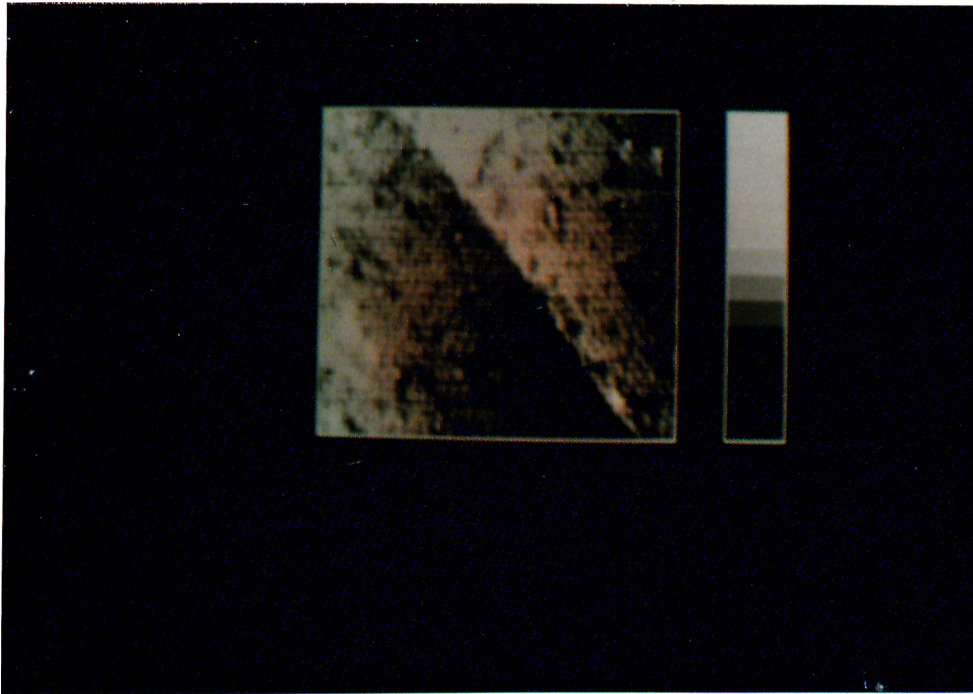


Figure 4.15: A high resolution image of a Si(001)(2×1) surface. The image size is 304×304 Å. Sample voltage and tunnel current are -2 V and 1 nA, respectively.

kinks in these steps, and adatoms and vacancies. Crystal growth from the vapor begins with the creation of excess mobile adatoms on the surface. An atom that has reached the surface will perform a random walk until it meets a step or another adatom. The deposition rate and the magnitude of diffusion coefficient determine the path of the adatom before it meets another. If two adatoms meet, they may together form the nucleus of an island. On the other hand, an adatom may find a step and stick to the step or may cross over the step, before it meets another adatom. Thus there are basically two categories of kinetic processes that an adatom is subject to: motion on a flat terrace and interactions with steps.

There are three different growth modes. The first one is the layer by layer growth in which the crystal layers are formed such that the new layer is not started to grow until the first layer is complete. In 3D island growth, the islands themselves first grow three dimensionally and later unite to form the overlayer. The last mode, Stranski-Krastanov growth, is a mixture of the first two modes. The first few layers are grown layer by layer, and 3D growth takes place then.

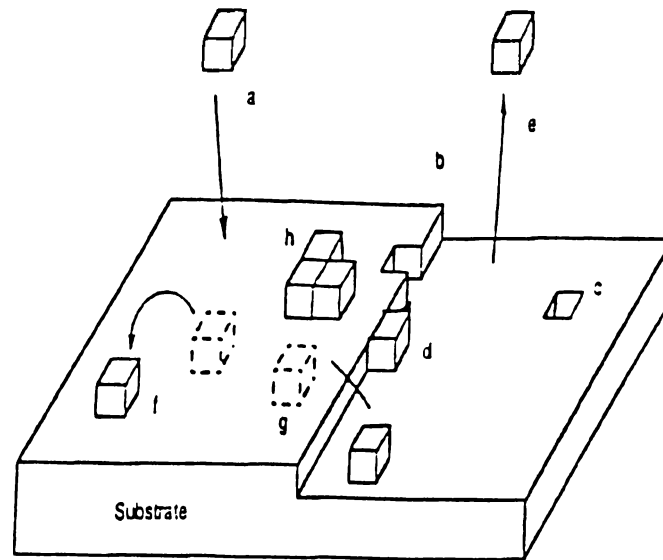


Figure 4.16: Atomic mechanisms of crystal growth in the framework of the terrace-ledge-kink model.

Arriving atoms (a), land on the surface which contains terraces, steps (b), vacancies (c) and kinks (d). Atoms can evaporate (e), move on the terrace (f), cross over steps (g), nucleate new islands (h) or become incorporated into steps. From Ref.(physicstoday)

In the following subsections the images of Si and Ge grown Si(001) samples are going to be displayed and discussed.

4.2.1 Si on Si(001)

Si was grown on Si(001) by using the Si evaporator which was described in Chapter 2. The Si(001) sample was cleaned with the same method as in the previous section. During the degassing of the sample, the evaporator was degassed as well. The Si source had been calibrated before, as to provide a growth rate of 0.073 ML/min at 9.25 A_{rms} current.²⁶ Si was deposited for 1.5 minutes on the sample to obtain a coverage of ~ 0.11 monolayers (ML). The substrate temperature was kept at ~ 300 °C during growth. After a cool down of 1.5 hours the sample was loaded to STM.

A large area scan of the surface taken at -2 V sample bias and 1 nA tunneling

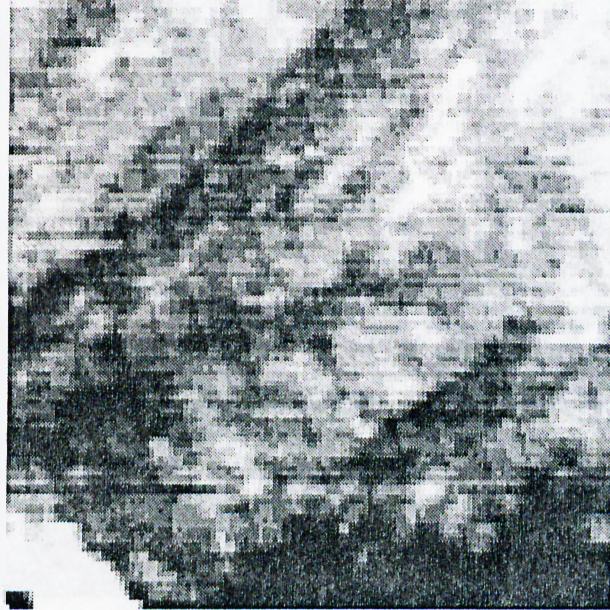


Figure 4.17: STM image of 0.15 monolayers of Si deposited on Si(001) surface. Image size is $608 \times 608 \text{ \AA}$.

current is shown in Fig.4.17. Although the image is not clear enough, the Si islands grown on the substrate can be seen. The islands on successive terraces, obeying the dimerization direction of the substrate, are grown perpendicular to each other. The upper terrace of the S_B step seems to contain a relatively low density of Si islands. The reason will be discussed in the following paragraphs with a more clear image of the same sample taken with a better tip, shown in Fig.4.18.

The islands running perpendicular to the dimer rows of the substrate are clearly visible. The islands are grown rectangular, i.e. there is a strong shape anisotropy. This shape anisotropy is due to the high sticking coefficient at the ends of the dimer rows compared to the sides of them. In addition, the formation energy of S_A type step being lower than that of S_B type step, contribute to the shape anisotropy, as well. More clearly, since the sides of the islands are S_A type steps and their ends are S_B steps, to minimize the formation energies the width of the rectangular islands become as small as possible, sometimes only a few dimers wide. Srivastara et al. considered the collective motion of

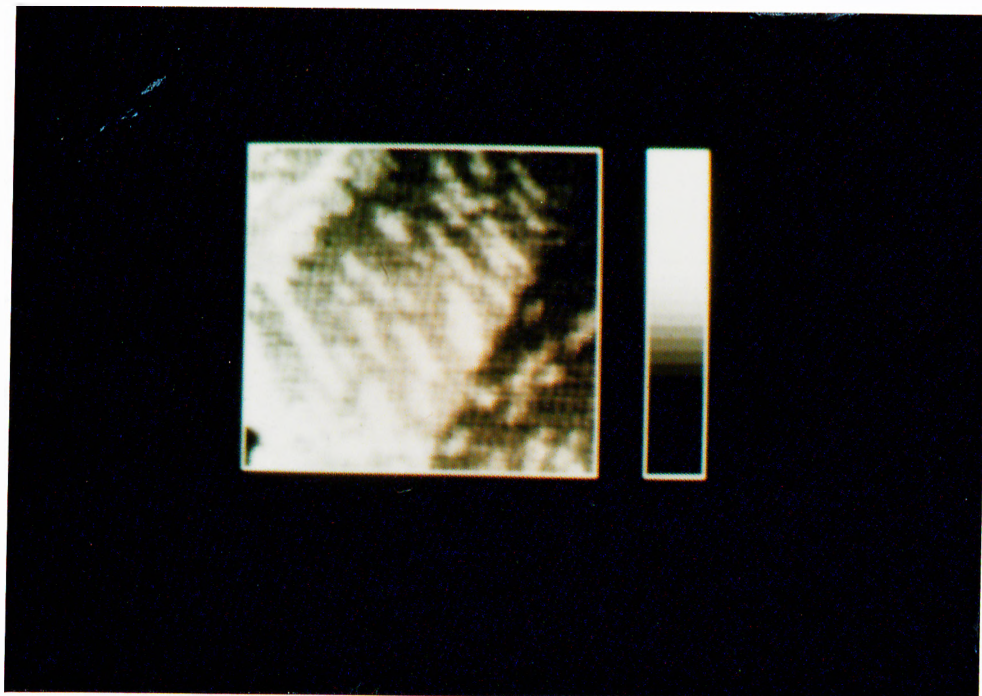


Figure 4.18: STM image of 0.15 monolayers of Si deposited on Si(001) surface. Image size is 608×608 Å.

densely packed adatoms and proposed that the opening of dimer bonds in the underlying layer, to accommodate the new layer, differs in two directions, causing the anisotropic structure.⁵⁹ Mo et al. have explained the anisotropic shape of islands simply by an anisotropic accommodation coefficient.⁶⁰ Accommodation can be understood microscopically in terms of the pathways and transition probabilities for energy transfer so that an arriving atom can stick to an existing island. If the accommodation coefficient of an approaching atom at the side of a growing dimer chain is much less than it is at the end of the chain, atoms will effectively reflect off the side and stick only on the ends. The more the accommodation coefficient differs in different directions, the more anisotropic the growth shape will be.

It is also obvious that the island number density at the middle terrace is higher compared to the other two terraces. The reason is the huge difference between the diffusion coefficients in two perpendicular directions. Mo et al. have calculated the diffusion coefficient along the dimer rows to be approximately 1000 times that in the direction perpendicular to the dimer rows.⁶¹ Consequently, for an

adatom arriving at the middle terrace, it is difficult to travel through the steps, while it is easier to migrate along the substrate dimer rows parallel to the step. The situation is reversed for the other two terraces. The adatom arriving on these terraces prefers to migrate through the step and cross over the step. The diffusion coefficient is strongly dependent on the substrate temperature, as well. An island is observed to merge with the S_B type step at the lower left part of the image. This is a sign of the growth via step flow, which is expected to occur at higher substrate temperatures and high deposition.

4.2.2 Ge on Si(001)

Ge was also grown on Si(001) surface to understand the nature of this heteroepitaxy. The sample was cleaned *ex situ* and *in situ* as described before. The Ge source which supplies a growth rate of 0.13 ML/min at 7.2 A_{rms} current, was also degassed for 4-5 hours during the degas of the sample. Ge was deposited on the sample which was kept at ~ 500 °C, for 25 minutes to obtain a coverage of ~ 3.25 ML. Again the sample was left 1.5 hours to cool down to STM temperature, and loaded into the microscope.

Before presenting the images of the Ge grown Si(001) sample, it will be useful to have a look at the previous STM studies on the heteroepitaxy of Ge on Si(001). Ge growth on Si(001) is a good example of Stranski-Krastanov growth mode. Mo et al. have reported that above a deposition of ~ 3 ML, up to which layer by layer growth is dominant, 3-D growth took place.⁶¹ Pyramidal 3-D islands begin to be form, which were referred to as "hut clusters". They have also shown that in order these hut clusters to grow, the substrate temperature had to be kept lower than 800 K. At temperatures exceeding 850 K macroscopic clusters which are similar to hut clusters in shape but huge compared to them, form the majority of the surface. This 3-D growth is due to the high strain in the epitaxial layers which is a result of 4% lattice mismatch between Si and Ge. The strain is weakened by the first three monolayers and the overgrown 3-D islands on top are inelastically relaxed by forming dislocations.

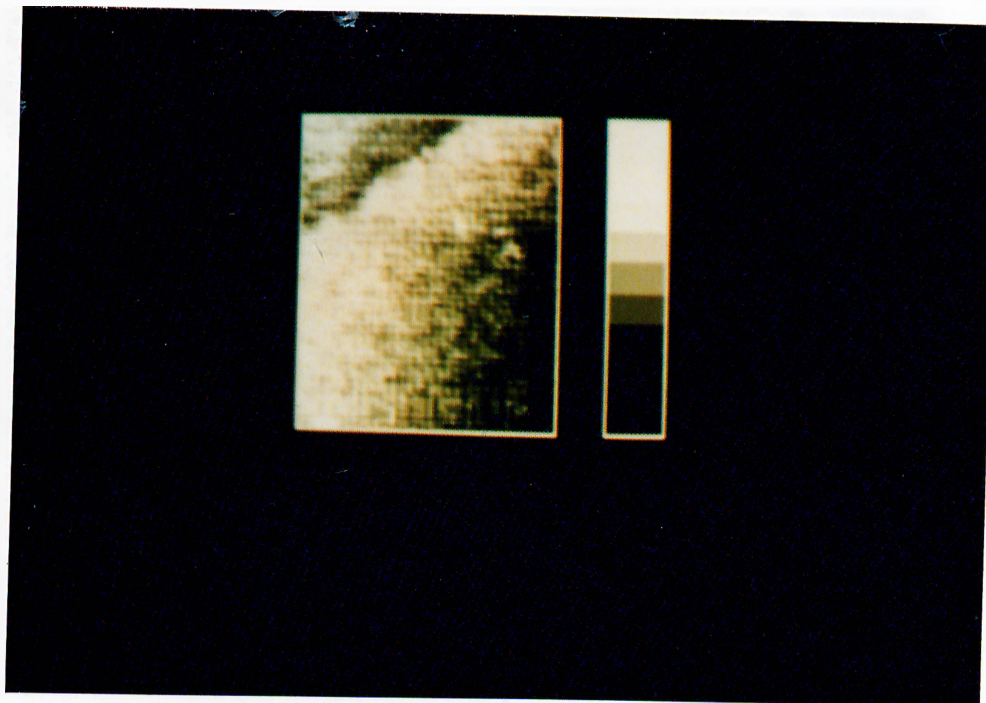


Figure 4.19: STM image of ~ 3.2 monolayers of Ge deposited on Si(001) surface. Image size is $608 \times 608 \text{ \AA}$.

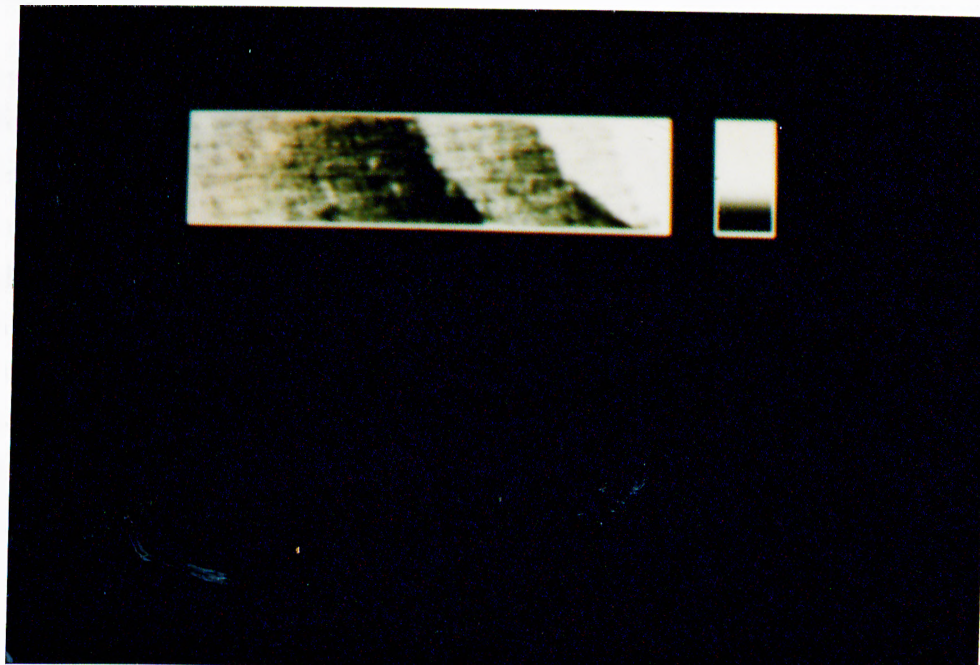


Figure 4.20: STM image of ~ 3.2 monolayers of Ge deposited on Si(001) surface. Image size is $660 \times 160 \text{ \AA}$.

As well as Si/Si(001) and Ge/Si(001), SiGe alloy growth on Si(001) has been

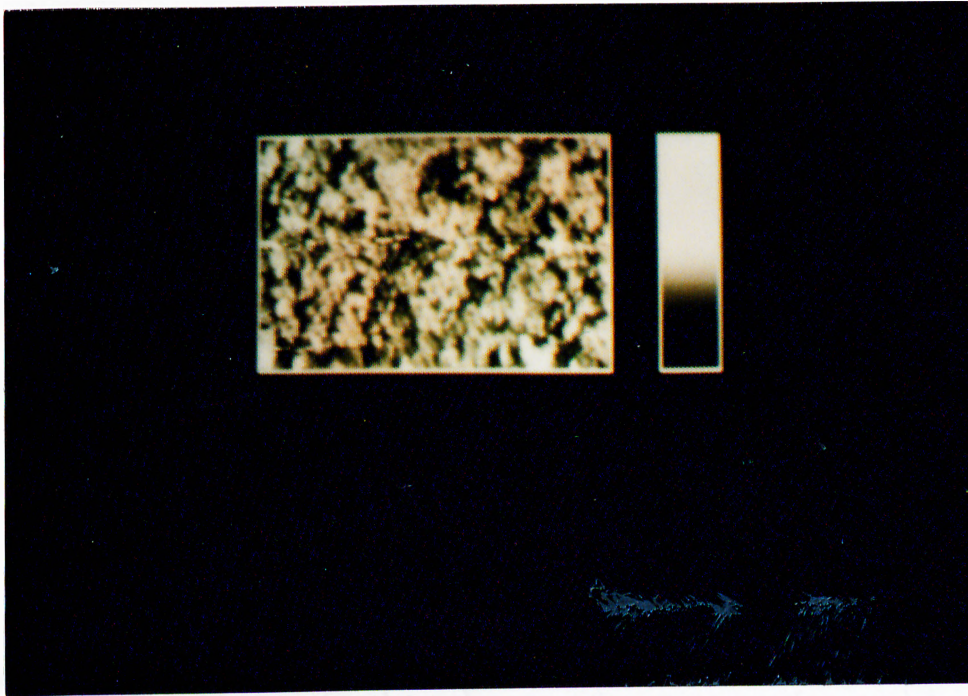


Figure 4.21: STM image of ~ 3.2 monolayers of Ge deposited on Si(001) surface. Image size is 299×215 Å.

the subject to a great deal of interest. In their recent study, Oral and Ellialtioglu⁶³ have investigated the initial stages of SiGe alloy formation on Si(001) surface. They have observed that the high strain due to the lattice mismatch resulted in complete buckling of the top most layer of the substrate as well as the overlayer itself. Consequently, there appears a transition from (2×1) symmetric to $c(4 \times 2)$ antisymmetric configuration. They have also shown that at a low temperature of 310 °C, the growth occurred as island formation with minimal island island interaction, while at a higher temperature, 470 °C, step flow was taking place as the main growth mechanism due to the fact that the diffusion length of an adatom is larger than the average terrace length at such temperatures. At an intermediate temperature of 390 °C, atoms and islands interact with one another but not with the steps, such that they can reach a configuration which was observed to be the formation of missing dimer rows, resulting in $(2 \times n)$ ordering of the alloy.

The image shown in Fig.4.19 is a scan of the 3.2 ML Ge grown Si(001) sample. Only a step the type of which can not be extracted, is seen. There is not any Ge island on the surface. Another region of the sample is imaged, and again no

island formation is observed, as shown in Fig.4.20. A possible explanation may be that it is a step flow growth due to high substrate temperature. Complete monolayers were formed in the first stages of the growth, and then the arriving adatoms rather than interacting with each other, reached the steps and were captured because of the high surface diffusion rate at elevated temperatures.

A relatively high resolution image of the same sample is given in Fig.4.21. The dimer rows of the surface are visible. However, there is a high density of defects, especially missing dimer groups. Under some of the openings from the top layer, the dimerization on the subsurface layer is seen. This image supports the idea that the growth occurred via step flow. Only almost complete overlayers, not individual Ge islands, are observed. Although the dimer rows are seen, the resolution of the image is not sufficient to lead to further interpretations.

In this work, we aimed to observe different types of epitaxial growth. At low temperatures, the island growth mode is obtained whereas at rather high temperatures the growth occurs via step flow. We grew silicon on Si(001) surface at 300 °C displaying island formation and germanium also on Si(001) surface at 500 °C which exhibits step flow mode. I would like to stress that the objective was to compare growth at different temperatures rather than comparing Si versus Ge growth.

Chapter 5

Conclusion

The clean and epi-grown Si(001)(2×1) reconstructed surfaces have been analysed using the UHV-STM, in this thesis work. The tip preparation and sample cleaning techniques were optimized first. To obtain an atomically sharp and clean tip was rather difficult. The samples, cleanliness of which were confirmed with LEED analysis, were observed to contain localized contaminations, such as oxides and SiC.

The surface features like steps and dimers, known to be the building blocks of the reconstruction of Si(001) surface, were observed on clean samples. A high density of defects like missing dimer and dimer groups, were detected on Si(001) surface. The theoretical estimation of the average terrace width for our samples is 160 Å. We have found the average terrace width experimentally to be 170 Å. This is in quite good agreement with the expected value. Our samples were expected not to contain double height steps because of small vicinal angle of 0.5°. However, on a few samples double step formation was observed. We believe that this is due to SiC contamination. This agrees well with the suggestion that SiC islands behave as pinning sites for steps.⁵³ These sites would cause vacancies and dislocations during growth. In Si and SiGe based devices the dislocations would not alter the performance drastically, if the dislocation density is not too high. However, such dislocations may be decorated by impurities during the growth and/or fabrication. Accordingly, silicon carbide mediated defects and dislocations

may cause the degradation of device performances. Although the propagation and interactions of dislocations, especially threaded and misfit dislocations, are well studied in the literature, the nucleation of such dislocations yet have not been investigated thoroughly. We believe that SiC acts as a nucleation site for dislocations.

Buckling of the dimers, which is believed to be induced either by vacancy type defects or tip-sample interaction, was also observed. The buckled dimers were seen along the rows which are close to surface defects. $p(2\times 2)$ and $c(4\times 2)$ symmetric domains, which is a consequence of buckling, are imaged on one clean Si(001) sample.

Finally, Si and Ge were grown epitaxially on Si(001) surface, with 0.11 ML and 3.2 ML coverages, respectively. The Si growth on Si(001) occurred as individual island formation because of the low coverage and low substrate temperature (~ 300 °C). In contrast, Ge growth was determined to occur via step flow due to the high substrate (~ 500 °C) temperature. No individual island formation was observed on terraces. Ge overlayers were found to dimerize like Si.

Further, in Si growth, a strong anisotropy was observed in the shapes of individual Si islands. This anisotropy is due to the larger sticking coefficient at the ends of dimer rows than that at the sides of dimer rows. If the sides of a dimer row are considered to be S_A and S_A type steps a possible explanation of the shape anisotropy may be the following. All the atoms at the edge of an S_A type step are saturated and there are no dangling bonds available for a diffusing surface adatom or dimer. On the other hand, the row of atoms on the lower terrace right next to an S_B type step have not completed their coordination, so that they would behave as active sites for the incoming dimers.

The rectangular islands were grown perpendicular to the underlying dimer rows of the substrate. There was also a diffusional anisotropy. Since it is easier for the adatoms to migrate along the dimer rows than perpendicular to them, the island density on the upper terraces of S_A type steps were found to be larger than that on the lower terraces. Both the shape and diffusional anisotropies in growth can be reduced by increasing the coverage and/or substrate temperature.

For a more detailed study of the growth process, experiments with different coverages and substrate temperatures, must be carried out.

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