# MMIC MIXERS

A THESIS
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND
ELECTRONICS ENGINEERING
AND THE INSTITUTE OF ENGINEERING AND SCIENCES
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

By
Mehmet Özgür
September 1996

# MMIC MIXERS

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND

ELECTRONICS ENGINEERING

AND THE INSTITUTE OF ENGINEERING AND SCIENCES

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Mehmet Özgür

September 1996

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah Atalar(Supervisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Canan Toker

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. İrşadi Aksun

Approved for the Institute of Engineering and Sciences:

Prof. Dr. Mehmet Baray
Director of Institute of Engineering and Sciences

# ABSTRACT

## MMIC MIXERS

Mehmet Özgür
M.S. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Abdullah Atalar
September 1996

New ways of achieving broadband, low-cost, reliable mixers are investigated. Resistive MESFET mixer topology is the main focus of this work. Despite the accurate modeling difficulties of resistive mode operation, promising results are obtained. Three resistive MESFET mixers and one double balanced mixer with a diode quad are designed in the frequency range of 10GHz-20GHz. A new passive balun which can be fabricated using a standard MMIC process is proposed. The all-passive floating FET mixer and its improved version, both of which include the new balun, demonstrate good port isolation and conversion gains at low local oscillator power levels, in very small area. Additionally, a new single balanced mixer topology employing resistive mode MESFETs is presented.

The chips are designed using Microwave Harmonica, layouts are generated using CADENCE microwave design enviroment and the chips are fabricated by GEC-Marconi's 0.5 $\mu$m GaAs (F20) process.

*Keywords :* MMIC, mixer, balun.

# ÖZET

## MONOLİTİK MİKRODALGA TÜMLEŞİK KARIŞTIRICILAR

Mehmet Özgür
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
Tez Yöneticisi: Prof. Dr. Abdullah Atalar
Eylül 1996

Geniş bandlı, düşük maliyetli, güvenilir karıştırıcı tasarım yöntemleri üzerinde çalışıldı. Özellikle direnç modunda çalışan MESFET ile kurulan karıştırıcı tasarımında yoğunlaşıldı. Bu modda çalıan MESFET'lerin modellenmesindeki sorunlara rağmen ümit verici sonuçlar elde edildi. Bu yöntemle çalışan üç, diyot-dörtlüsü ile kurulan bir tane çift-dengeli karıştırıcı olmak üzere dört yonga tasarımı yapıldı. Standart üretim methodları ile üretilebilecek yeni bir balun önerildi. Bu yeni balunun da kullanıldığı tamamen edilgen ve onun gelişmiş sürümünde iyi giriş-çıkış yalıtımı ve yerel osilatörün düşük güç seviyelerinde bile iyi çevrim kazancı, küçük yonga alanlarında elde edilmiştir. Ayrıca kontrollü direnç gibi çalışan MESFET'lerin kullanıldığı yeni bir tekdengeli karıştırıcı tasarımı da sunulmaktadır.

Yongaların simulasyonları Microwave Harmonica, yerleşim planları CADENCE mikrodalga tasarım ortamı kullanılarak yapıldı. Üretimleri ise GEC-Marconi şirketi tarafından 0.5 $\mu$m GaAs (F20) teknolojisi ile gerçleştirilmiştir.

*Anahtar Kelimeler :* Aynı tabana oturtulmuş mikrodalga tümleşik devreleri, karıştırıcı, balun.

**... and to "."**

# TABLE OF CONTENTS


**1 INTRODUCTION** **2**

**2 PRELIMINARIES** **5**

2.1 MIXER . . . . . 5

2.2 BALUN . . . . . 12

2.2.1 Active MMIC Baluns . . . . . 13

2.2.2 Passive MMIC Baluns . . . . . 15

**3 A Novel Compensated Balun** **21**

3.1 Derivations of Relations . . . . . 23

3.1.1 Stage B 25

3.1.2 Stage A . . . . . 26

3.2 Determination of Design Parameters 28

3.2.1 Stage B . . . . . 28

3.2.2 Stage A . . . . . 30

3.2.3 Overall Optimization . . . . . 31

3.3 Discussion and Future Work . . . . . 34

**4 The Floating FET Mixer** **36**

4.1 Introduction . . . . . 36

4.2 Principle of Operation . . . . . 37

4.3 Design . . . . . 38

4.4 Simulations . . . . . 40

4.5 Measurements . . . . . 42

4.6 Discussion and Future Work . . . . . 45

**5 The Single Balanced Mixer** **47**

5.1 Introduction . . . . . 47

5.2 Design . . . . . 48

5.2.1 LO Pre-amplifier . . . . . 49

5.2.2 Balun 52

5.2.3 Single Balanced Mixer . . . . . 57

5.2.4 Low Pass Filter . . . . . 58

5.3 Simulations and Measurements 59

5.4 Discussion and Future Work . . . . . 62

**6 The Improved Floating FET Mixer** **67**

6.1 Introduction . . . . . 67

6.2 Design . . . . . 68

6.2.1 LO Pre-amplifier . . . . . 68

6.2.2 Balun 69

6.3 Simulations and Measurements 70

6.4 Discussion and Future Work . . . . . 72

**7 CONCLUSION** **79**

**APPENDIX** **81**

**A The Double-Balanced Mixer** **81**

**B Nonlinear MESFET Models** **84**

B.0.1 Materka-Kacprzak Intrinsic Model 84

**C Layouts** **88**

**D Coupled Parallel Microstrip Lines** **93**

# LIST OF FIGURES


1.1 Ideal multiplier mixer model . . . . . 4

1.2 Frequency component generated in a mixer . . . . . 4

2.1 Common mixer topologies (a)Single-ended (b)Single-balanced (c)Double-balanced . . . . . 7

2.2 Single-gate a)gate mixer b)drain mixer configurations . . . . . 8

2.3 Dual-gate a)gate mixer b)drain mixer configurations . . . . . 8

2.4 Image-rejection mixer topology 9

2.5 Self-oscillating mixer . . . . . 9

2.6 Simple subharmonically pumped mixer . . . . . 10

2.7 Circuit schematic of a)distributed dual-gate FET mixer with image rejection operation b)Matrix distributed mixer . . . . . 11

2.8 Distributed dual-gate FET mixer schematic 11

2.9 Transmission line model of Pavio's distributed active balun . . . 13

2.10 Schematic of Tsai's active balun . . . . . 14

2.11 Schematic of Robertson's distributed active balun . . . . . 14

2.12 Equivalent circuit of Marchand baluns: (a)2nd order (b-c)3rd order (d) 4th order . . . . . 16

2.13 Schematic of Tsai's Multilayer Marchand Balun . . . . . 17

2.14 Schematic of Rogers' balun realization 19

2.15 Schematic of Tsai's balun realization . . . . . 20

3.1 The proposed novel balun topology . . . . . 22

3.2 (a) Stage A (b) Stage B 22

3.3 The voltage and current direction assumptions of the two-port . 23

3.4 For $Z_3 \approx j20$ the change of $Z_{F3}$ . . . . . 29

3.5 For $C_3 = 0.2$ pF (a) and $C_3 = 0.5$ pF (b) the change of $Z_{F3}$ 29

3.6 For $C_3 = 0.2$ pF $C_{F3} = 0.4$ pF the change of $Z_{inB}$ . . . . . 30

3.7 For $Z_2 \approx j20$ the change of $Z_1$ 31

3.8 For $C_2 = 0.2$ pF (a) and $C_2 = 0.5$ pF (b) the change of $Z_1$ 32

3.9 The optimized novel balun . . . . . 32

3.10 The amplitude balance and matching at Port 1 33

3.11 The phase balance of the output ports 33

3.12 The return losses for the terminations $R1 = 50\Omega$ $R2 = 200\Omega$, $R3 = 200\Omega$ . . . . . 34

4.1 A Floating FET Mixer. . . . . 37

4.2 The Proposed CPL Balun and the reflection from port 1. . . . . 39

4.3 The Amplitude and Phase Balance of CPL Balun. . . . . 39

4.4 The Final Schematic of the FFM chip. . . . . 41

4.5 The bonding for measurements. . . . . 42

4.6 The measurement Test Set. 42

4.7 The Conversion Gain Measurements and Simulations for various IFs. . . . . 43

4.8 The LO-RF and LO-IF Isolations. . . . . 44

4.9 The Return losses from RF and LO ports. 44

5.1 The Single Balanced Mixer Topology . . . . . 49

5.2 The Change in $g_m$ with the total gate width under constant drain condition . . . . . 50

5.3 The Maximum Stable Gain 51

5.4 The Stability Factor (K) before matching network 51

5.5 The $S_{11}^*$ and $S_{22}^*$ (8GHz-20GHz) for 2×100$\mu$m MESFET with crude Input and Output Matching Calculation at 20GHz . . . . 53

5.6 The pre-amplifier . . . . . 54

5.7 The $S_{21}$, $S_{11}$ . . . . . 55

5.8 The stability of amplifier . . . . . 55

5.9 The Planar Edge-coupled Marchand Balun 56

5.10 The Amplitude Balance of the Balun . . . . . 56

5.11 The Phase Balance of the Balun . . . . . 57

5.12 The proposed Single-Balanced Mixer Topology (Balun is not shown) . . . . . 58

5.13 The Low Pass Filter 59

5.14 The Single-Balanced Mixer . . . . . 61

5.15 The Simulation and Measurement Results for Conversion Gain . 63

5.16 The Conversion Gain Measurement Results at IF=3GHz 64

5.17 The LO-RF Isolation . . . . . 64

5.18 The LO-IF Isolation 65

5.19 The Return Loss from RF port 65

5.20 The Return Loss from LO port 66

6.1 The Overall Mixer Topology . . . . . 69

6.2 The Compensated Balun 70

6.3 The Reflection and Transfer Characteristics of the Balun . . . . 71

6.4 The Phase Balance of the Balun . . . . . 71

6.5 The Pre-amplifier . . . . . 73

6.6 The Overall Circuit of the Mixer 74

6.7 The Simulation Results for Conversion Gain . . . . . 75

6.8 The Measurement Results for Conversion Gain . . . . . 75

6.9 The Return Loss from RF port 76

6.10 The Return Loss from LO port 76

6.11 The LO-IF Isolation . . . . . 77

6.12 The LO-RF Isolation . . . . . 77

A.1 The schematic of the double balanced mixer . . . . . 82

A.2 The Marchand balun used in the DBM design . . . . . 82

B.1 Extrinsic Model . . . . . 85

B.2 Materka Intrinsic Model . . . . . 85

C.1 The layout of the double-balanced mixer chip. . . . . 89

C.2 The layout of the FFM chip. . . . . 90

C.3 The layout of the SBM chip . . . . . 91

C.4 The layout of the NFFM chip . . . . . 92

D.1 Schematic diagram of coupled microstrip lines . . . . . 94

# Chapter 1

# INTRODUCTION

For many years the key element in receiving systems has been the crystal detector or diode mixer. At the beginning of the 20th century, detectors were crude, consisting of a semiconductor crystal contacted by a fine wire (whisker) which had to be adjusted periodically so that the detector would keep functioning. The real advance in performance come with the invention by Edwin Armstrong of the super regenerative receiver. Armstrong was also the first to use a vacuum tube as a frequency converter (mixer) to shift the frequency of the incoming signal to an intermediate frequency (IF), where it could be amplified with good selectivity and low noise, and later detected. The superheterodyne receiver which is the major advance in receiver architecture to date is still employed in virtually every receiving system.

The development of microwave mixers was fostered during World War II with the development of radar [1]. Conversion losses achievable in the low microwave range dropped from around 20dB in 1940 to 10dB in 1945. By early 1950s, mixers with conversion losses around 6dB were being produced regularly. Today the theory of mixers is well established, and image-enhanced mixers are regularly produced with conversion losses below 4dB at frequencies around 50 GHz [2].

In the ideal case, in the mixer model illustrated in Fig.1.1, the signal at the

node X is given as

$$M(t)cos(\omega_s t)cos(\omega_p t) = M(t)(\frac{1}{2}cos(\omega_s - \omega_p)t + \frac{1}{2}cos(\omega_s + \omega_p)t) \qquad (1.1)$$

then utilizing a high- or low-pass filter the specific frequency component can be chosen.(sum-frequency:up-conversion, difference-frequency:down-conversion). Here the RF (radio frequency) signal has a carrier frequency $\omega_s$ with modulation $M(t)$, and the local oscillator signal (LO or pump) applied has a pure sinusoidal frequency of $\omega_p$.

The mixer which can consist of any device capable of exhibiting nonlinear performance, is essentially a multiplier. In microwave range diodes and FETs are two popular nonlinear devices. Properly designed active FET MMIC mixers offer distinct advantages over their passive counterparts. This is especially true for dual-face FET mixers; since the additional port allows for some inherent LO-RF isolation. The possibility of conversion gain rather than loss is also an advantage. But the cost of designing active FET mixers is the complexity of using nonlinear analysis tools. But above 100 GHz the diode remains the only device that can be used for frequency conversion applications. Unfortunately, no physical nonlinear device is a perfect multiplier. Thus they contribute noise and produce a vast number of spurious frequency components. For example, the voltage-current relationship for a diode can be described as an infinite-power series,

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + ... \qquad (1.2)$$

where $V$ is the sum of both input signals and $I$ is the total signal current. The frequency components of the current $I$ are

$$\omega_{out} = m\omega_s + n\omega_p \qquad m = 0, \pm 1, \pm 2, .. \quad n = 0, \pm 1, \pm 2, .. \qquad (1.3)$$

For a good design the amplitude of the desired frequency component should be significantly higher than the other frequency components. In Fig.1.2 a typical output spectrum of an mixer from the IF port is given.

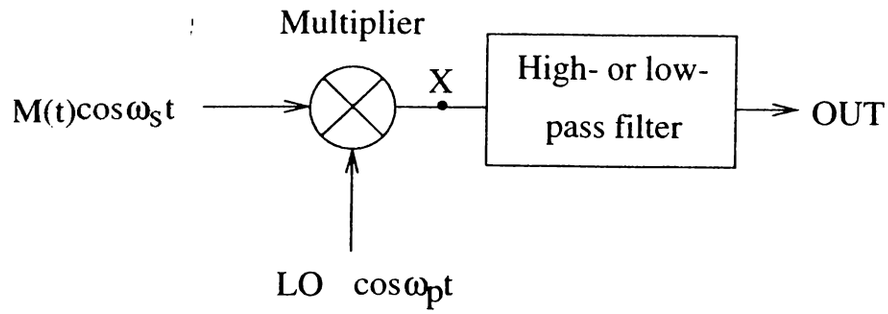



Figure 1.1: Ideal multiplier mixer model

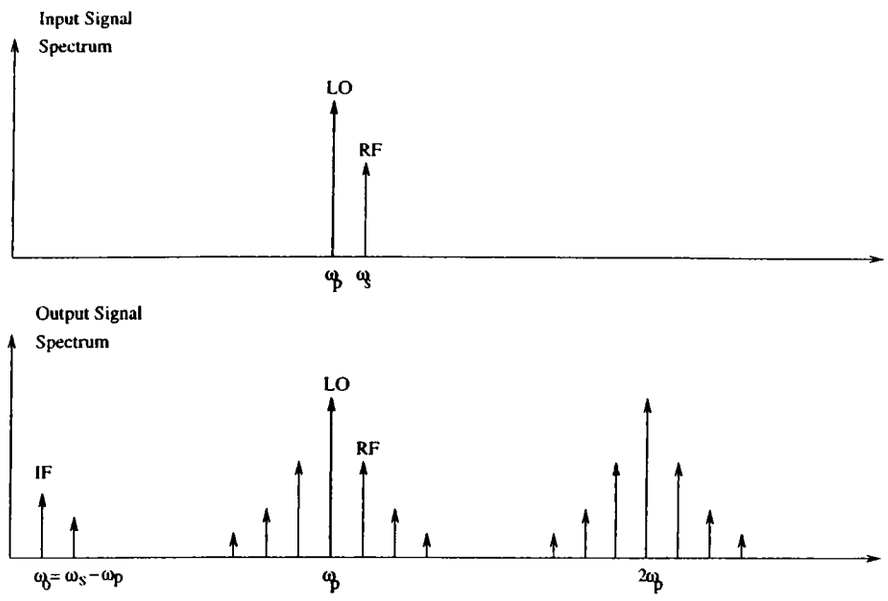



Figure 1.2: Frequency component generated in a mixer

# Chapter 2

# PRELIMINARIES

As a reference to the following chapters, a brief introduction of mixer concept is given here along with some mixer topologies. More detailed theoretical issues can be found in the cited references. Since in the balanced mixer topologies the importance of baluns can not be neglected, for the sake of completeness, a discussion on baluns is included in this chapter. (Baluns perform the function of transforming an unbalanced line like microstrip to a balanced line with equal amplitude and 180° out of phase outputs.)

## 2.1 MIXER

The important mixer design parameters can be summarized as follows

- RF, LO and IF Bandwidths
- The conversion loss
- The return losses from the ports
- LO-RF, LO-IF, RF-IF Isolations

| | Single-Ended | Single-Balanced | Double-balanced |
|---|---|---|---|
| Conversion Gain | High | Moderate | Low |
| Spurious Performance | None | Moderate | High |
| Bandwidth | Narrow | Wide | Wide |
| Pump Power | Low | Moderate | High |
| Isolation | None | Moderate | High |
| Dynamic range | Low | Moderate | High |
| Cost(area) | Low | Moderate | High |

Table 2.1: Mixer Topology Performance Consideration

- The LO pump power
- The area of realization in a given technology
- The DC power consumption, if any active parts included
- Third-order two-tone modulation and 1-dB compression point
- The noise performance

Detailed information about these parameters can be found in [1-5]. Regardless of the nonlinear or switching element employed, mixers can be divided into three classes: **(1)Single-ended, (2)Single-balanced, (3)Double-balanced** (Fig. 2.1). A general performance comparison for these mixer topologies is shown in Table 2.1. It should be noted that these performance traits are quite general and are highly dependent on balun design and operating frequency [1]. The performance of the single- and double-balanced topologies are mainly determined by (center-tapped) transformers in Fig. 2.1b,c. Because of this crucial importance baluns are presented in next section.

Works on MESFET mixers have been reported by many researches, in general there are three types of single-gate FET mixer configurations:

- **The gate mixer:** Both the RF and the LO signals are applied to the gate of the device (Fig. 2.2a). The MESFET is gate biased near pinch-off. This results in efficient mixing since, at this bias condition, the FET's transconductance is very sensitive to the modulation of the externally applied LO signal [6].

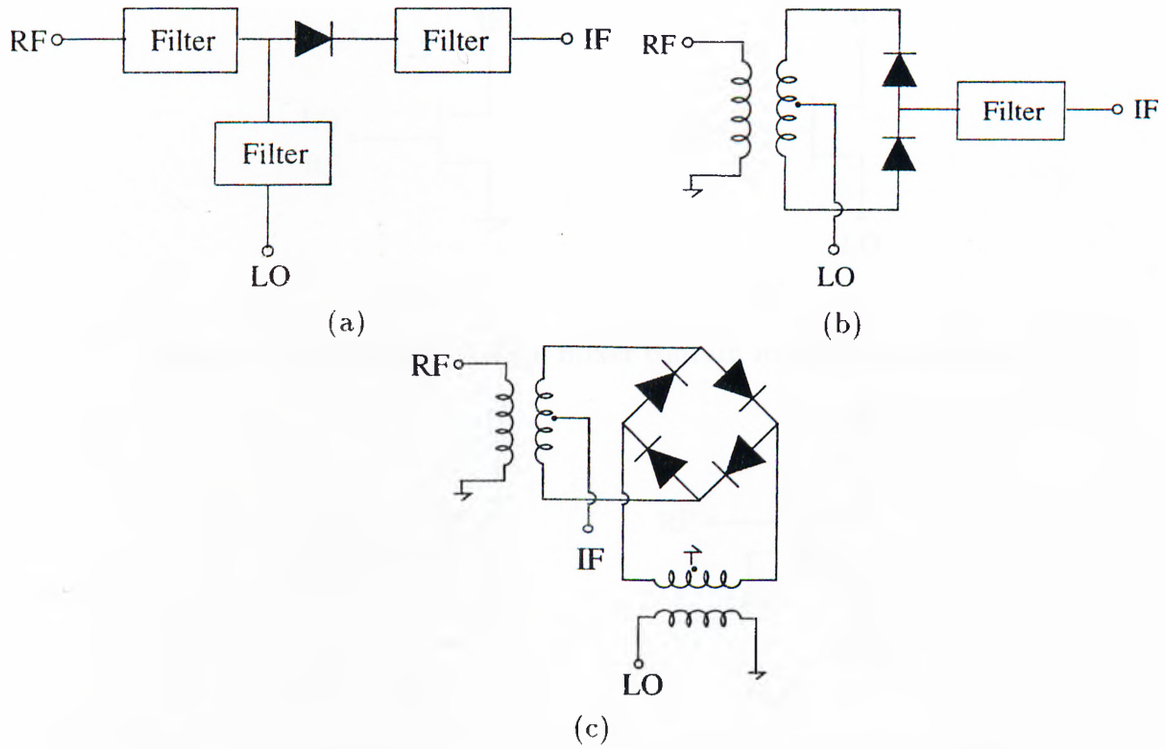



Figure 2.1: Common mixer topologies (a)Single-ended (b)Single-balanced (c)Double-balanced

- **The drain mixer:** The RF signal is applied to the gate, and the LO signal is applied to the drain of a FET (Fig. 2.2b). The device is drain-biased near the knee voltage and is gate-biased to 0V or a small negative voltage. At this bias condition, both the FET's output resistance $R_o$ and the transconductance $G_m$ are very nonlinear, and the voltage amplification factor $u = G_m R_o$ is modulated by the LO signal applied to the drain [7].

- **The resistive mixer:** In this case, the unbiased channel of the device is used as a time-varying resistor whose resistance is modulated by the LO signal applied at the gate. The MESFET resistive mixer is capable of very low intermodulation owing to the weak nonlinearity of the FET's channel resistance.

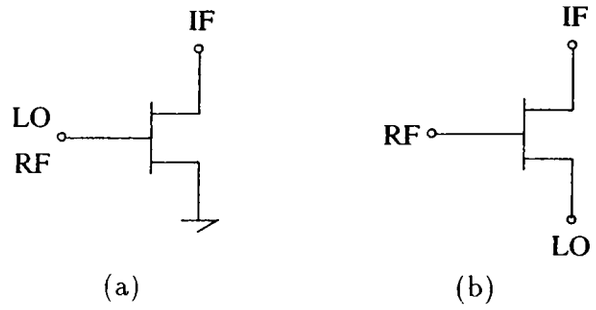



Figure 2.2: Single-gate a)gate mixer b)drain mixer configurations

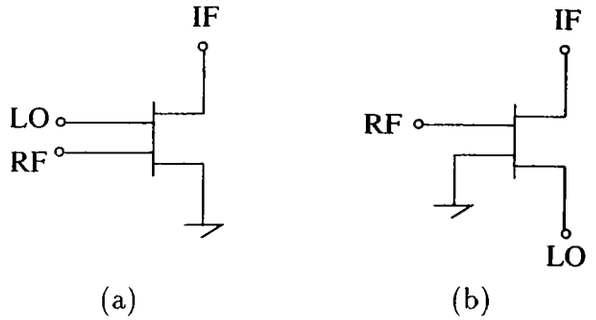



Figure 2.3: Dual-gate a)gate mixer b)drain mixer configurations

There are a variety of interesting mixer topologies in widespread use that perform vital system functions which cannot be simply classified as balanced mixers.

- **Image rejection mixer** (single-sideband mixer): Often, it is not practical to filter out the image because the IF frequency is low, and the image ($f_{im}=2f_{LO}-f_{RF}$ for $f_{RF} > f_{LO}$) is therefore too close to the RF and LO frequencies, because the LO must be broadly tunable, or because the RF and image bands overlap. A solution to this problem is the image rejection mixer. The classic image-rejection mixer shown in Fig. 2.4 consists of two mixers with at least one signal applied in quadrature while the other signal is either combined at the IF output or applied to the IF input in quadrature [8].

- **Self-oscillating mixer:** It has been shown that the MESFET can be used in a self-oscillating mixer circuit where a single device both produces the LO power and mixes the LO with the RF signal. In designing such

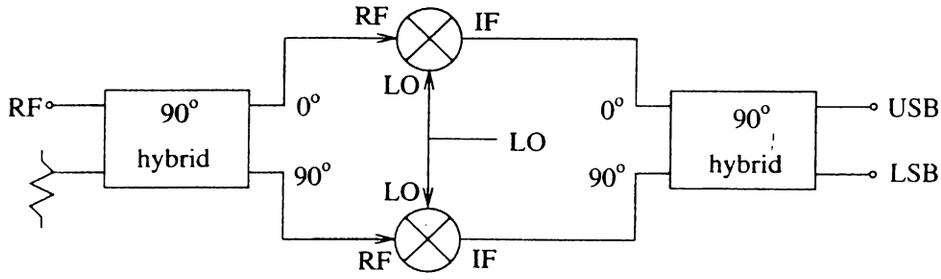



Figure 2.4: Image-rejection mixer topology

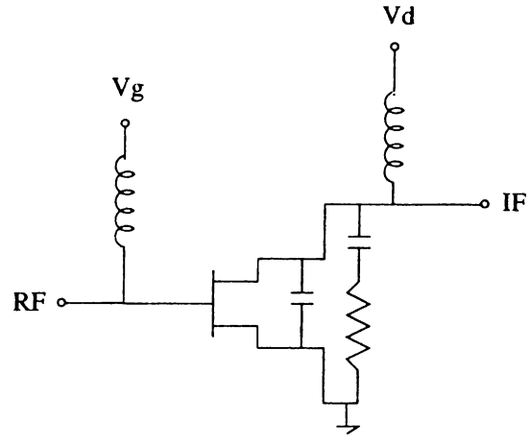



Figure 2.5: Self-oscillating mixer

mixers, care must be taken to prevent the LO signal from being injection-locked to the RF signal [2],[9],[10] (Fig. 2.5).

- **Subharmonically pumped mixer:** For many applications, it is expensive, inconvenient, or even impossible to generate a fundamental-frequency LO. In these cases, it may be wise to use a mixer that is pumped at half the LO frequency, and to mix the applied RF signal with the second harmonic of the junction conductance waveform. For the configuration shown in Fig.2.6 if the diodes are identical, it has no fundamental mixing response [2].

- **Distributed mixer:** There are various distributed mixer configurations reported in the literature [11],[5]. Titus et al. designed a broadband FET image-rejection mixer by using a distributed arrangement of dual-gate FETs [12]. As shown in Fig.2.7a, the RF and IF lines form a traveling

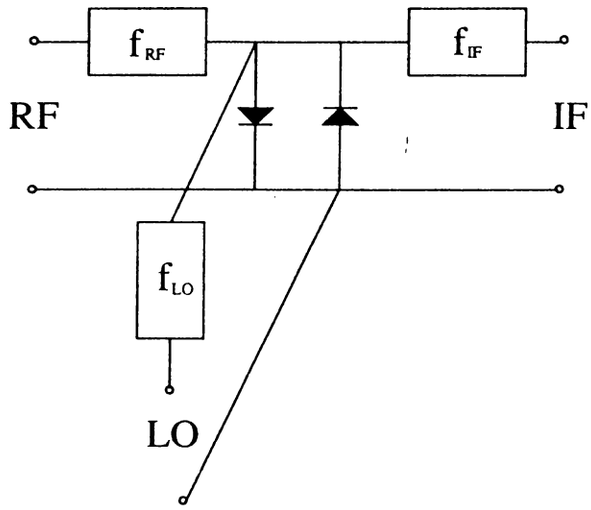



Figure 2.6: Simple subharmonically pumped mixer

wave structure while the LO is fed in phase through a four-way power divider. This mixer is operates under the principle of phase cancelation.

Titus at al. also designed a single-ended mixer using a distributed topology [13]. In this case, the local power is injected into the FETs with the same phase delay as the RF signal by using the traveling wave configuration (Fig.2.8). As a result, IF signals from from all the FETs will have the constant phase and combined at the output port using a matching circuit.

Robertson et al. reported a matrix distributed mixer and a new topology derived from the concepts of transversal filtering and distributed mixing [11].

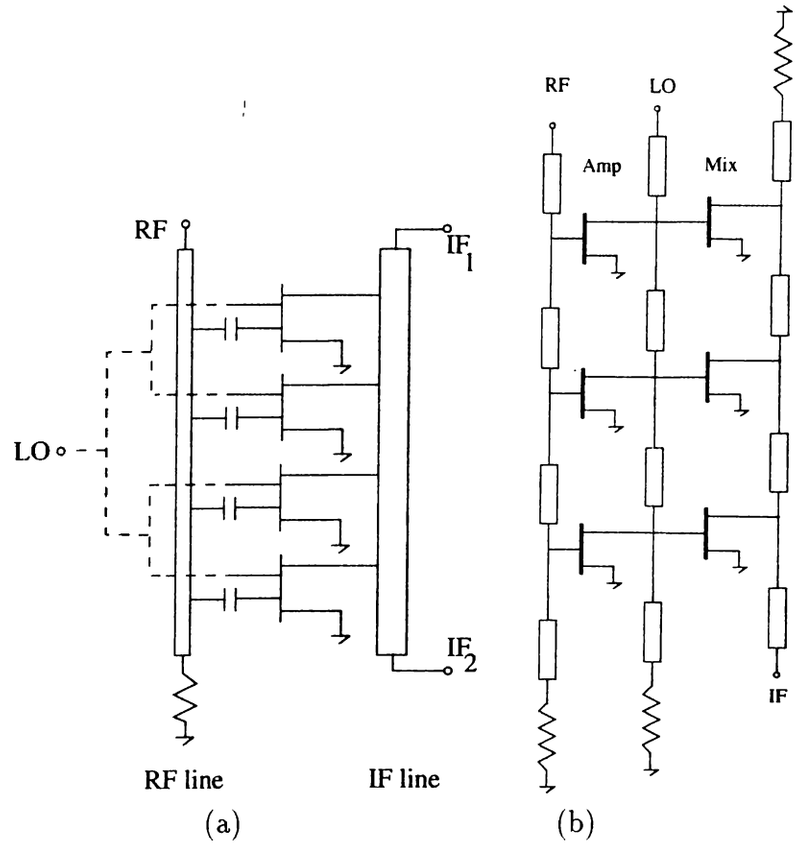



Figure 2.7: Circuit schematic of a)distributed dual-gate FET mixer with image rejection operation b)Matrix distributed mixer

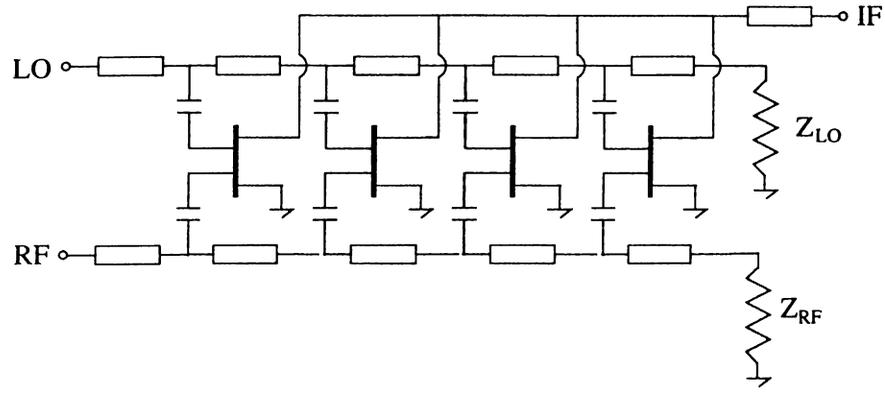



Figure 2.8: Distributed dual-gate FET mixer schematic

## 2.2 BALUN

The development of printed microwave baluns dates from 1969, when S.B.Chon [14] suggested the first microstrip-slot transition. Various microstrip-slot transitions have subsequently been reported [15], following the development of double-sided MIC technology, based on microstrip and slot lines. In fact these well-known microstrip-slot transitions represented only one of the possible realizations of Marchand baluns, although for a long time, they have been designed without the use of the theory of classical baluns [16]. During the last decade, the development of MMIC technology has produced an increasing interest on balun structures.

Baluns are required in key microwave components such as balanced mixers, push-pull amplifiers, multipliers and phase shifters. The need for broadband, low cost, monolithic baluns is increasing as MMIC technology advances.

The important design parameters for a balun can be listed as follows

- The amplitude balance
- The phase balance
- The insertion gain or loss
- The area of realization in a given technology
- The DC power consumption
- The power handling capability
- The noise performance
- The spurious signal performance

The minimization of cost and maximization of operation band are the main forces behind the developing new balun topologies in the last decade.

As given in Table 2.2, the balun topologies can be classified into two main groups; namely, Active and Passive Baluns.

| Active Baluns | Passive Baluns |
|---|---|
| CGCS | Marchand |
| Dist. Gline Ter. | Planar Transformer |
| | Broadside Coupled |
| | Wilkinson Divider |
| | Interdigital Coupler |

Table 2.2: Basic Balun topologies

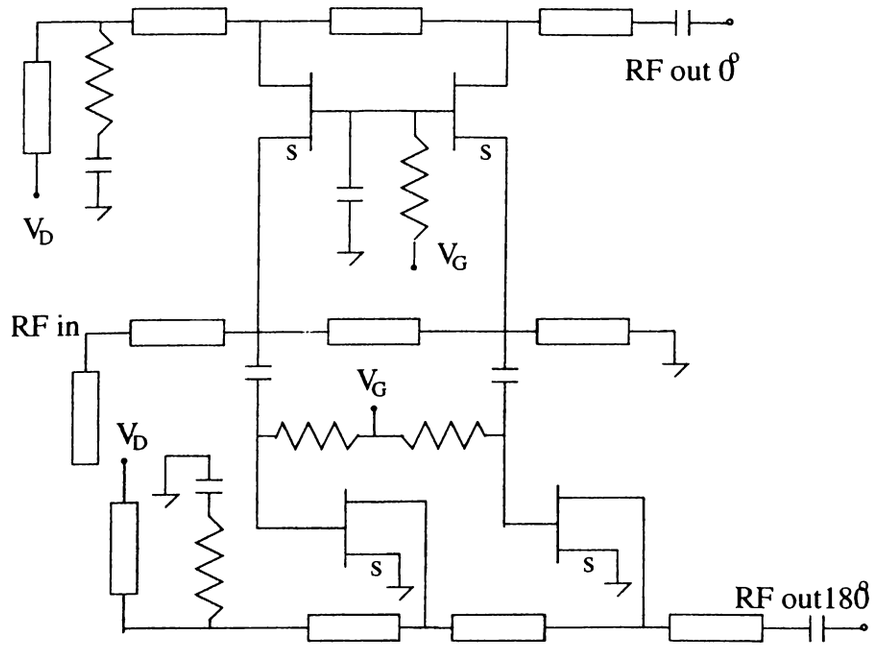



Figure 2.9: Transmission line model of Pavio's distributed active balun

### 2.2.1 Active MMIC Baluns

#### Common-Gate/Common-Source (CGCS) Approach

The common-source FET provides 180° phase shift between gate and drain [17]. The common-gate devices gives 0° phase shift between input and output.

Figure 2.9 shows a schematic of the distributed active balun [1]. The center tapped version of this structure exhibits gains between -4dB and 0dB in the frequency range of 2-18 GHz, and phase unbalance of 15° . By optimizing the

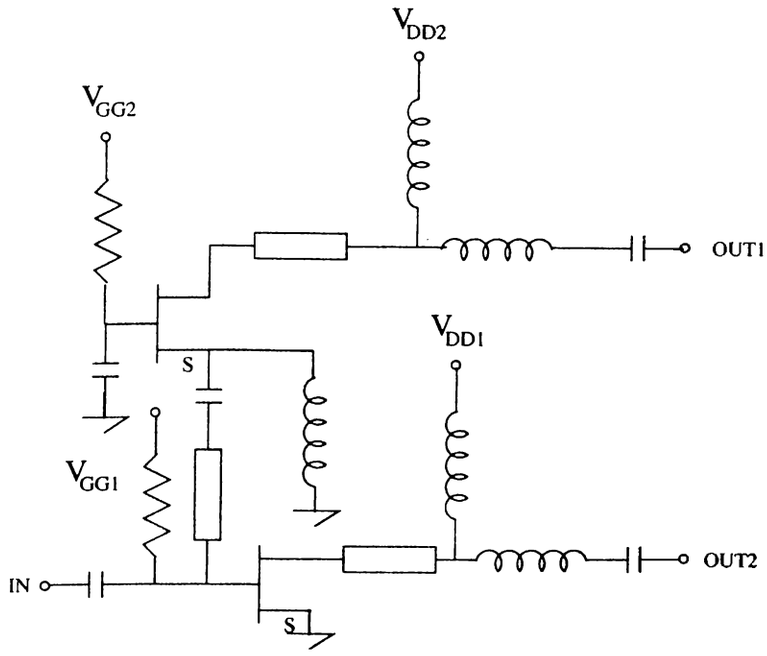



Figure 2.10: Schematic of Tsai's active balun

structure it is possible to obtain bandwidth of 1-25 GHz. There is no data available about the DC power consumption in [1].

Tsai et al. [17] used the CGCS structure illustrated in Fig. 2.10. In this structure there is no center tap which limits its usage, the four different power source requirement buries its small area advantage into a deep shadow. It exhibits gains in the range of -3dB to 4dB and phase unbalance of 10° in the 5-18 GHz band. No data available about the DC power consumption.

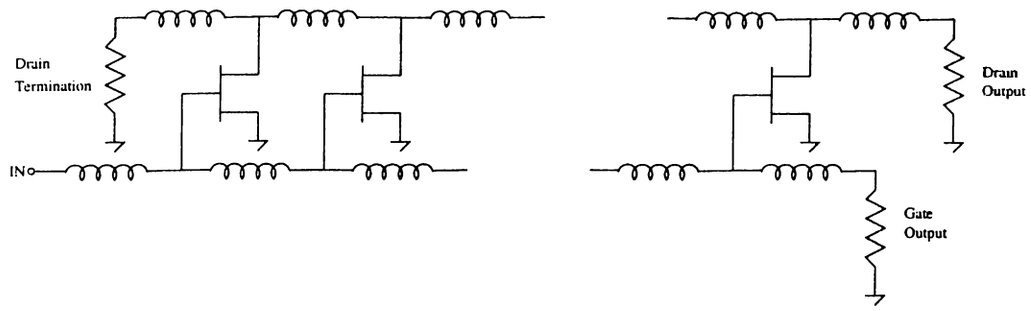



Figure 2.11: Schematic of Robertson's distributed active balun

Although good performance has been achieved with CGCS structure, these techniques again have a bandwidth limitations because the common-gate FETs cause very high attenuation on the input line [18].

#### Distributed Amplifier Gate-Line Termination Approach

Recently Baree and Robertson [18] proposed a new active balun approach. Figure 2.11 shows the circuit diagram of this new technique. The basis of this technique is a distributed amplifier in which the gate line termination is used as an output port. The transistor gate widths are chosen so that the signal from the normal amplifiers equal in amplitude to the signal from the gate output. They obtained from a two-section balun, 10° of maximum phase unbalance with 0dB-to-10dB insertion loss in the 0.5-20 GHZ band. The obvious disadvantage is that the insertion gain is always negative.

### 2.2.2 Passive MMIC Baluns

The active baluns do not only consume DC power but suffer from high noise figure, high spurious responses, low power handling capability, and low 3rd order intermodulation intercept point. Therefore broadband monolithic passive baluns are indispensable elements in realizing high performance low risk MMICs [19].

#### Marchand Baluns

The Marchand baluns were introduced by Marchand [16]. An exact synthesis of Marchand balun having Chebyshev passband response is presented by Cloete [20]. Equivalent circuits of 2nd-to-4th order Marchand baluns are shown in Fig. 2.12

The disadvantage of the approach introduced by Cloete is that the design relations are not given in closed from, which makes them inconvenient for

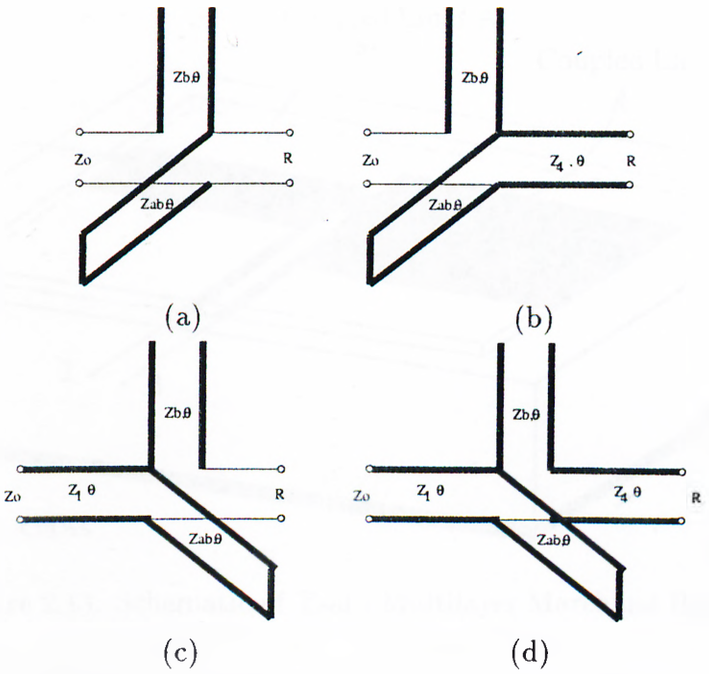



Figure 2.12: Equivalent circuit of Marchand baluns: (a)2nd order (b-c)3rd order (d) 4th order

incorporation into CAD packages. The simple expressions for the design of 4th order Marchand balun can be found in [21].

Among the passive balun structures Marchand topologies have gained very important position. There have been many types applied in different technologies. Some of them briefly explained below:

- **Multilayer** The bandwidth of the baluns (Fig. 2.12) are primarily limited by the highest achievable impedance ratio between the short-circuited and open-circuited lines.

  Chen et al. [19] using a three layer conductor structure realized a 3rd order multilayer Marchand balun. The line impedances are $23\Omega, 63\Omega$ and $67\Omega$, open-circuited, unbalanced, and short-circuited line respectively. The total area is $2.9\times1.5\text{mm}^2$. The amplitude and phase balances are good between 2-16 GHz.

  Another multilayer structure is designed by Tsai [22] which is shown in

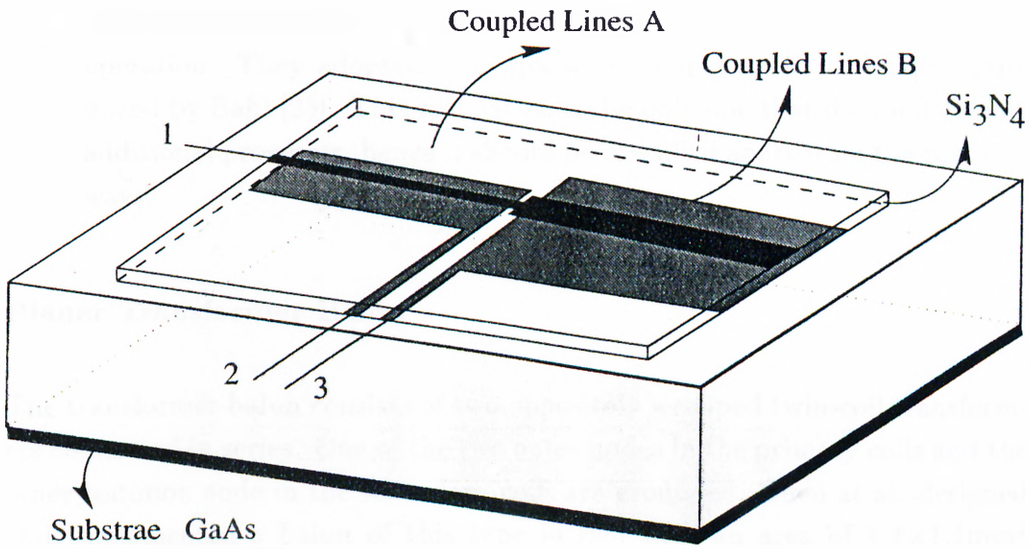



Figure 2.13: Schematic of Tsai's Multilayer Marchand Balun

Fig.2.13. The simulated results are impressive for 25Ω input 50Ω output impedances. They used 6mil GaAs substrate with a 1.8 $\mu$m silicon-nitride. In 4-24 GHz frequency band the return loss, and amplitude and phase balances are good.

- **Coplanar Wave Guide/Slot line**

  Chen et al. [19] designed and implemented a uniplanar CPW/slot line Marchand balun which utilizes CPWs as unbalanced and open-circuited lines and slot lines as balanced and short-circuited lines(Fig. 2.12). The slot-line to CPW transitions are provided for the balanced lines so that the balun can be on-wafer tested. The chip size is 5×4.8mm$^2$. The amplitude and phase unbalance are less then 1.5dB and 15° respectively, over 2-16 GHz frequency band.

  Jokonovic [21] and Eisenberg et al.[23] also used similar realizations.

- **Edge-Coupled CPLs**

  Compatibility with the current MMIC manufacturing technology forces researches to implement the Marchand idea in different ways. Brinlee et al. [24] made use of edge-coupling between closely placed microstrip lines. In this approach the phase velocity difference between the even and

odd modes should be compensated in order to increase the bandwidth of operation. They adopted the capacitive compensation technique introduced by Bahl [25]. This realization is the only one that does not require additional processes, hence it should be classified apart from the previous ways.

### Planar Transformer Balun

The transformer balun consists of two oppositely wrapped twin-coil transformers connected in series. One of the two outer nodes in the primary coils and the inner common node in the secondary coils are grounded. Chen at al. designed and implemented a balun of this type in [19] with an area of $1.4\times1.1\text{mm}^2$ and 25mil thick substrate. The amplitude and phase unbalances between the two balanced ports are less than 1.5dB and 10°, respectively, over the 1.5 to 6.5 GHz and 13 to 24 GHz frequency bands.

### Broadside-Coupled Balun

The broadside-coupled (BCL) balun is a monolithic version of the hybrid double-sided microstrip/strip-line balun. BCL structure has a large even-mode impedance which is essential for good balun performance, but the bandwidth of BCL realization is narrow compared to the other realization [19]. Especially the phase unbalance is disappointingly bad.

### Wilkinson Divider

Rogers et all. [26] designed and implemented a balun which consists of a 3-section Wilkinson divider that provides two well-balanced equal amplitude in-phase signals with a good input/output match and isolation between output ports over a 3:1 bandwidth. Each of these signals is then phase shifted by +90° and -90° (using Lange couplers) respectively resulting in 180° differential phase, equal amplitude outputs. The circuit schematic of the balun is shown in Fig. 2.14. the balun fabricated on 10 mil alumina measures an amplitude

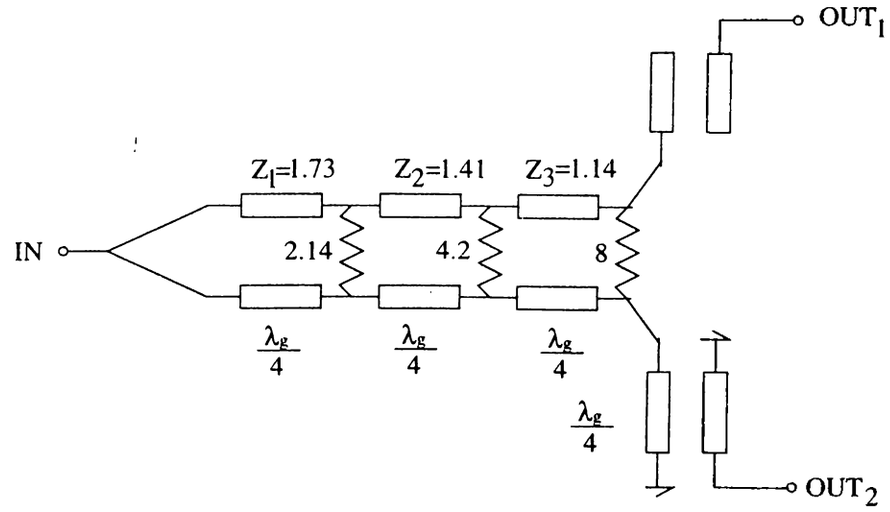



Figure 2.14: Schematic of Rogers' balun realization

unbalance of 1.2dB, average phase unbalance of 7° from 6 to 20 GHz. The obvious disadvantage of this approach is the large size of the chip.

The highpass balun designed by Minnis et al. [27] is very similar to the above structure. (Instead of third order Wilkinson divider he used first order.) But Minnis starts its synthesis from a highpass S plane prototype of degree 3 to arrive this result. The inverting coupler is 4-finger interdigital structure, whereas the noninverting one is a edge-coupled line coupler. Its overall size $0.7\times2\text{mm}^2$ and $\pm1dB$ and 8° are the amplitude and phase unbalances from 6 to 18 GHz, respectively.

The bandpass balun of Minnis is complicated enough to include 6 vias, hence its area is larger than expected $0.7\times1.5\text{mm}^2$. From 6.5 to 13.5 GHz frequency range 1dB and 8° amplitude and phase unbalances are obtained.

### Interdigital Coupler

Tsai [28] implemented the Marchand-balun-idea using interdigital couplers. Although he folded the couplers in order to minimize the area, the length of the coupler is 1660 $\mu$m. The insertion loss of the balun is better than 2dB, 1dB and 5° of maximum amplitude and phase unbalance over 7 to 19 GHz. With

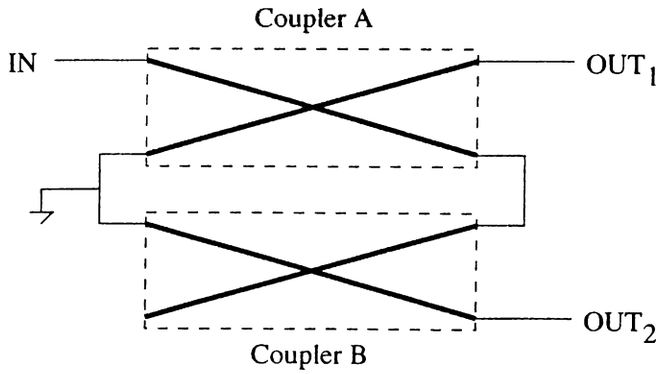



Figure 2.15: Schematic of Tsai's balun realization

$1 \times 2\text{mm}^2$ chip area, its cost-effectiveness remains as a real problem.

# Chapter 3

# A Novel Compensated Balun

There are many passive structures that can be used in realization of a balun, here coupled transmission lines and capacitances are prefered since these two can be easily manufactured using GEC-F20 process. But there may be a planar passive structure that can do the same job with better responses.

It was shown by Sellberg [29],Helszajn [30] and many others [31],[32] that using coupled parallel microstrip transmission lines (CPLs App. D), one can obtain 90° of phase shift between certain input-output port combinations. Therefore it is expected to obtain 180° phase-shift between certain ports under suitable port terminations. That is the starting point for this design.

In Fig.3.1 a general compensated CPL network is illustrated. Treating the problem in this configuration is so computationally intensive that it is very easy to miss the practical issues and the insight lying under cover. Instead the design is considered as consisting of two parts, as shown in Fig.3.2 $Z_{inB}$ is the input impedance of the stage B at frequency of interest. All the external impedances, the width ($w$), the spacing ($s$) and the length of the CPLs ($\theta$) are the design parameters. The port 1 is the input port and the ports 2 and 3 are the output ports at which the voltages are opposite in sign but equal in magnitude.

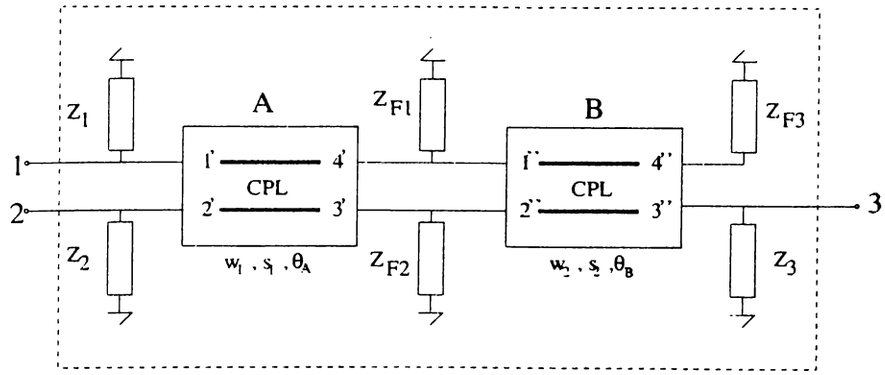



Figure 3.1: The proposed novel balun topology

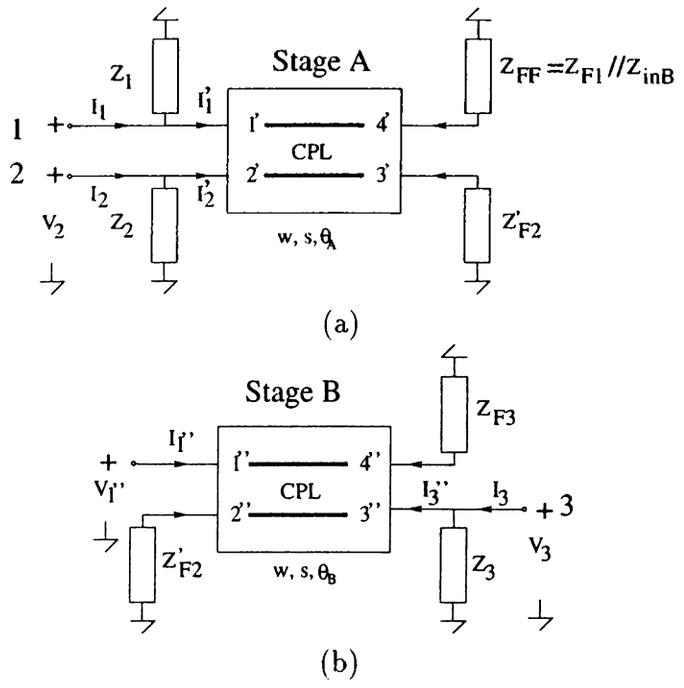



Figure 3.2: (a) Stage A (b) Stage B

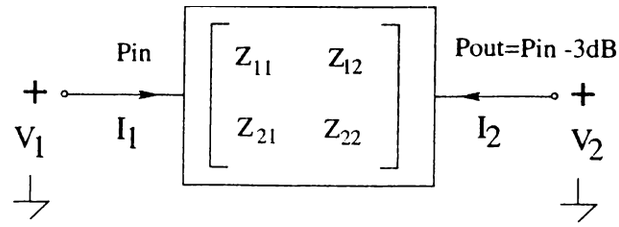



Figure 3.3: The voltage and current direction assumptions of the two-port

In this work, the two stages do not both yield 90° phase shift, instead the first stage (Stage A in Fig.3.2a) is used as just like buffer whereas the second one is merely a 180° phase-shifter.

Since decreasing the width and the spacing between the microstrip lines increases the coupling and the minimum line width allowed in GEC-F20 process is $10\mu m$ for third metal layer M3 and $4\mu$m for second layer M2 it is determined to concentrate on only $5\mu$m width and line-spacing case. This fixing removes two design parameters from consideration for both stages ($w_1 = w_2 = s_1 = s_2 = 5\mu$m). The odd impedance $Z_o$ and the even impedance $Z_e$ becomes 194.5Ω and 48Ω respectively. Therefore $A \approx 121$ and $B \approx 73$ in the equation 7.15 in App.D.

## 3.1 Derivations of Relations

The design of the stage B is considered first. A similar topology was considered by Sellberg [29], but his results cannot be used here since he assumed the same impedances at ports 2″ and 3″.

The derivations given here are based on two-port structures. Using two-port passive structures certain functions can be realized. For us two fundamental functions are examined below:

**Case 1:** First let us drive the impedance relation for a two-port which delays the input signal 180°, and attenuates 3dB (Fig. 3.3).

$$P_{in} = \frac{1}{2}|V|_1|I|_1 \quad P_{out} = \frac{1}{2}|V|_2|I|_2 \tag{3.1}$$

Here $|V|$ and $|I|$ represent the amplitudes of the signals. Since 3dB attenuation means that $P_{in}$ is equal to $2P_{out}$.

$$\frac{|V|_1|I|_1}{|V|_2|I|_2} = 2 \tag{3.2}$$

Then using the 180° phase shift requirement we can write the following relations for the voltages and currents of the two-port.

$$\frac{V_1}{V_2} = -\sqrt{2} \quad \frac{I_1}{I_2} = \sqrt{2} \tag{3.3}$$

The impedance matrix relation for the two port is given as follows

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.4}$$

Then using equations 3.3 and 3.4

$$\frac{V_1}{V_2} = \frac{Z_{11}I_1 + Z_{12}I_2}{Z_{21}I_1 + Z_{22}I_2} = \frac{\sqrt{2}Z_{11} + Z_{12}}{\sqrt{2}Z_{21} + Z_{22}} = -\sqrt{2} \tag{3.5}$$

Finally the following relation is obtained for the two-port with mentioned function:

$$\sqrt{2}Z_{11} + Z_{12} + Z_{21} + \sqrt{2}Z_{22} = 0 \tag{3.6}$$

**Case 2:** In this case the impedance relation of a two port which attenuates the input signal 3dB but does not introduce any phase shift between input and output ports will be derived. The power relations given in Eqn. 3.1 and Eqn 3.2 are valid in this case too. But in order not have any phase shift the port voltage and current relations read as

$$\frac{V_1}{V_2} = \sqrt{2} \quad \frac{I_1}{I_2} = -\sqrt{2} \tag{3.7}$$

Then, again using the impedance matrix relation in Eqn 3.4 and Eqn 3.7, we can write

$$\frac{V_1}{V_2} = \frac{Z_{11}I_1 + Z_{12}I_2}{Z_{21}I_1 + Z_{22}I_2} = \frac{-\sqrt{2}Z_{11} + Z_{12}}{-\sqrt{2}Z_{21} + Z_{22}} = \sqrt{2} \tag{3.8}$$

Finally the following relation is obtained for the two-port without phase delay:

$$\sqrt{2}Z_{11} - Z_{12} - Z_{21} - \sqrt{2}Z_{22} = 0 \tag{3.9}$$

### 3.1.1 Stage B

Since all the elements used in the design (Fig.3.2b) are reciprocal, the resulting impedance matrix becomes symmetric (ie $Z_{12} = Z_{21}$). The initial configuration is further simplified by removing $Z_{F2}$, that is the port 2 is grounded. $Z_3$, $Z_{F3}$ and the length of CPL ($\theta_B$) are the parameters to be determined to obtain 180° phase-shift between ports 1'' and 3.

With the reference direction assumptions illustrated in Fig.3.2b, to have 180° phase-shift between ports 1'' and 3, Eqn 3.6 must be satisfied at the frequency of interest. ( Note that the stage B is treated as a two-port structure: Port 1'' is the input and port 3 is the output port) In order to use the relation in Eqn 3.6, first the two-port impedance matrix should be evaluated for the stage B. We have the 4-port impedance relation for the CPL section

$$\begin{bmatrix} V_1'' \\ V_2'' \\ V_3'' \\ V_4'' \end{bmatrix} = \begin{bmatrix} Z_{11}'' & Z_{12}'' & Z_{13}'' & Z_{41}'' \\ Z_{21}'' & Z_{11}'' & Z_{41}'' & Z_{31}'' \\ Z_{31}'' & Z_{41}'' & Z_{11}'' & Z_{14}'' \\ Z_{41}'' & Z_{42}'' & Z_{31}'' & Z_{11}'' \end{bmatrix} \begin{bmatrix} I_1'' \\ I_2'' \\ I_3'' \\ I_4'' \end{bmatrix} \tag{3.10}$$

Here

$$V_2'' = 0 \tag{3.11}$$

$$V_3'' = V_3 \tag{3.12}$$

$$V_4'' = -Z_{F3} I_3'' I_3'' = I_3 - \frac{V_3}{Z_3} \tag{3.13}$$

By using the definitions of impedance matrix elements the following parameters of stage B are obtained.

$$\begin{bmatrix} V_1'' \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{B11} = \frac{V_1''}{I_1''}|_{I_3=0} & Z_{B12} = \frac{V_1''}{I_3}|_{I_1''=0} \\ Z_{B12} = \frac{V_3}{I_1''}|_{I_3=0} & Z_{B22} = \frac{V_3}{I_3}|_{I_1=0''} \end{bmatrix} \begin{bmatrix} I_1'' \\ I_3 \end{bmatrix} \tag{3.14}$$

$Z_{Bij}$'s are in terms of $\theta$, $Z_3$, $Z_{F3}$. (Their equations are too complicated to include here.) Then using the result of Eqn. 3.6 we can write

$$\sqrt{2} Z_{B11} + 3 Z_{B12} + \sqrt{2} Z_{B22} = 0 \tag{3.15}$$

In the equation 3.15 $Z_{B22}$ is the input impedance seen from port 3 when the port 1'' is open. By choosing $Z_{B22} = 100\Omega$, the load matching for port 3 is optimized for $100\Omega$. Then Eqn. 3.15 is solved for $Z_{F3}$ in terms of $Z_3$ and $\theta_B$. The calculations are carried out by using MapleV [33].

$$Z_{F3}= \frac{(B_1+B_2Z_3)\cos^2(\theta_B)+j(B_3+B_4Z_3)\cos(\theta_B)\sin(\theta_B)+jB_5Z_3\sin(\theta_B)+B_6Z_3+B_7}{(B_8+B_9Z_3)\cos^2(\theta_B)+j(B_{10}+B_{11}Z_3)\cos(\theta_B)\sin(\theta_B)+B_{12}} \tag{3.16}$$

where

| For $w = 5\mu m$ and $s = 5\mu m$ | | | |
|---|---|---|---|
| $B_1$=21678336 | $B_2$=-366025 | $B_3$=28168800 | $B_4$=281688 |
| $B_5$=-254916$\sqrt{2}$ | $B_6$=-133225 | $B_7$=-21678336 | $B_8$=366025 |
| $B_9$=2328 | $B_{10}$=281688 | $B_{11}$=3025 | $B_{12}$=-366025 |

### 3.1.2 Stage A

After the possibility of obtaining 180° phase shift in a single stage has been introduced in the previous section, it can be surprising to add another stage. But a second stage is used here, in order to attain symmetry between ports 2 and 3, hence to enhance the bandwidth. (This does not mean that it can not be achieved in a single stage!). The stage A is considered after stage B, because $Z_{inB}$ must be known initially in order to attempt the design of the stage A. $Z_{inB}$ can be plotted by assigning values to the termination of port 3, $Z_3$ and $Z_{F3}$. With the reference direction assumptions illustrated in Fig.3.2a, to have minimum phase-shift from port 1 to 2 the Eqn. 3.9 must be satisfied at the frequency of interest. As in the section 3.1.1, the two-port impedance matrix of the stage A should be extracted (Port 1 is the input port and port 2 is the output port). We have the 4-port impedance relation for the CPL section A

$$\begin{bmatrix} V_1' \\ V_2' \\ V_3' \\ V_4' \end{bmatrix} = \begin{bmatrix} Z_{11}' & Z_{12}' & Z_{13}' & Z_{41}' \\ Z_{21}' & Z_{11}' & Z_{41}' & Z_{31}' \\ Z_{31}' & Z_{41}' & Z_{11}' & Z_{14}' \\ Z_{41}' & Z_{42}' & Z_{31}' & Z_{11}' \end{bmatrix} \begin{bmatrix} I_1' \\ I_2' \\ I_3' \\ I_4' \end{bmatrix} \tag{3.17}$$

Here

$$V_1' = V_1 \tag{3.18}$$

$$V_2' = V_2 \tag{3.19}$$

$$V_3' = 0 \tag{3.20}$$

$$V_4' = -Z_{FF} I_4' \tag{3.21}$$

$$I_1' = I_1 - \frac{V_1}{Z_1} \tag{3.22}$$

$$I_2' = I_2 - \frac{V_2}{Z_2} \tag{3.23}$$

By using the definitions of impedance matrix elements the following parameters of stage A are obtained.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{A11} = \frac{V_1}{I_1}|_{I_2=0} & Z_{A12} = \frac{V_1}{I_2}|_{I_1=0} \\ Z_{A12} = \frac{V_2}{I_1}|_{I_2=0} & Z_{A22} = \frac{V_2}{I_2}|_{I_1=0} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.24}$$

$Z_{Aij}$'s are in terms of $\theta_A$, $Z_1$, $Z_2$, $Z_{FF}$. (Their equations are too complicated to include here.) Then using the result of Eqn. 3.9 we can write

$$\sqrt{2}Z_{A11} - 3Z_{A12} - \sqrt{2}Z_{A22} = 0 \tag{3.25}$$

In the equation 3.25 $Z_{A22}$ is the input impedance seen from port 2 when the port 1 is open. By choosing $Z_{A22} = 100\Omega$, the load matching for port 2 is optimized for $100\Omega$. It is solved for $Z_1$ in terms of $Z_{FF} = Z_{F1}//Z_{inB}$ (treated as known constant), $Z_2$ and $\theta_A$:

$$Z_1 = \frac{-100\sqrt{2}[(A_1+A_2Z_2)\cos^2(\theta_A)+jA_3(A_4+Z_2)\cos(\theta_A)\sin(\theta_A)+A_5Z_2-A_1]}{(A_6+A_7Z_2)\cos^2(\theta_A)+j(A_8+A_9Z_2)\cos(\theta_A)\sin(\theta_A)+A_{10}Z_2+A_{11}} \tag{3.26}$$

where

| For $w = 5\mu m$ and $s = 5\mu m$ | |
|---|---|
| $A_1 = 86713344$ | $A_2 = 14641Z_{FF}$ |
| $A_3 = 1126752$ | $A_4 = Z_{FF}$ |
| $A_5 = -5329Z_{FF}$ | $A_6 = \sqrt{2}(100A_2-A_1)$ |
| $A_7 = \sqrt{2}(931200-A_2) + 26499Z_{FF}$ | $A_8 = A_3\sqrt{2}(100-Z_{FF})$ |
| $A_9 = -A_3\sqrt{2}+12100\sqrt{2}Z_{FF}+2039328$ | $A_{10} = (5329\sqrt{2}-26499)Z_{FF}$ |
| $A_{11} = (A_1-100A_2)\sqrt{2}$ | |

## 3.2 Determination of Design Parameters

This phase of the design has two stages:

- Initial rough calculations
- The final optimization of the overall topology

Equations 3.16 and 3.26 are used to determine the desired impedance values according to following list of criteria:

- The minimum number of components is desired. If possible use no component or only one (Complexity and area minimization).
- Capacitance is prefered over inductance and both over resistance (Design and fabrication simplicity, lossless network).
- Use minimum possible $\theta$ (Area minimization).

### 3.2.1 Stage B

If $Z_3$ is taken to be purely imaginary and positive (inductive impedance) corresponding $Z_{F3}$ requires always a negative resistance in the range of interest of $\theta_B$ (at 12 GHz). (In Fig.3.4 $Z_{F3}$ is shown for $L_3 = 0.3$ nH case)

If $Z_3$ is taken as a capacitor ($C_3$) then as seen in Fig.3.5 the real part attains very small values. Although it has no zeros, the region near the smallest magnitude (of real part) can be used. In some of the region the required $Z_{F3}$ is inductive, whereas the rest of the region a capacitive compensation is needed. The good news is the replacement of these regions when the $C_3$ is increased. For example, if the value of $C_3$ is increased from 0.2 pF to 0.5 pF (in Fig. 3.5) the useful region moves to smaller value of $\theta$, therefore smaller length of CPL section becomes enough for the desired function. As a results, for this part capacitors will be chosen for both $Z_3$ and $Z_{F3}$.

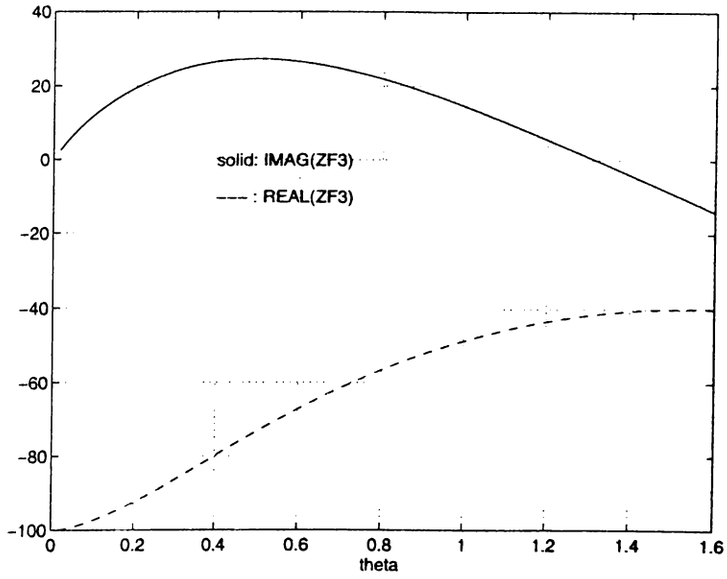



Figure 3.4: For $Z_3 \approx j20$ the change of $Z_{F3}$

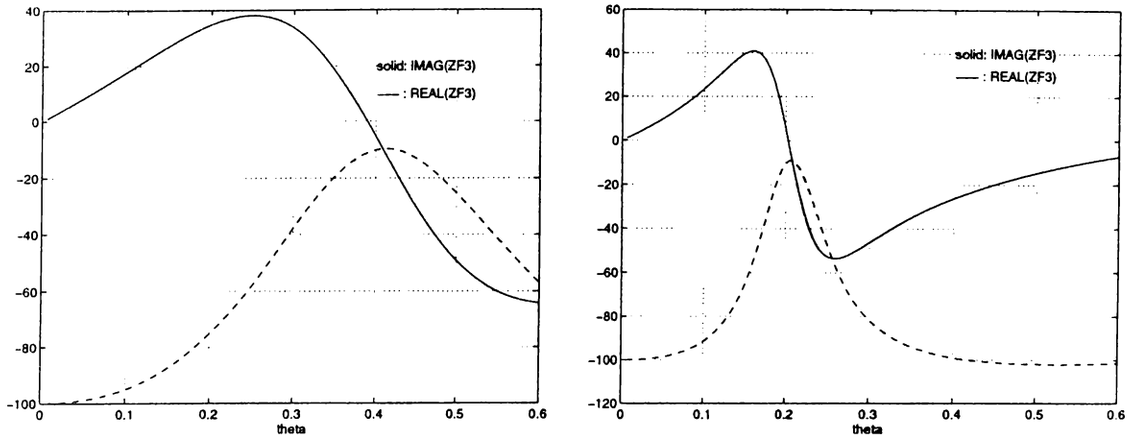



Figure 3.5: For $C_3 = 0.2$ pF (a) and $C_3 = 0.5$ pF (b) the change of $Z_{F3}$

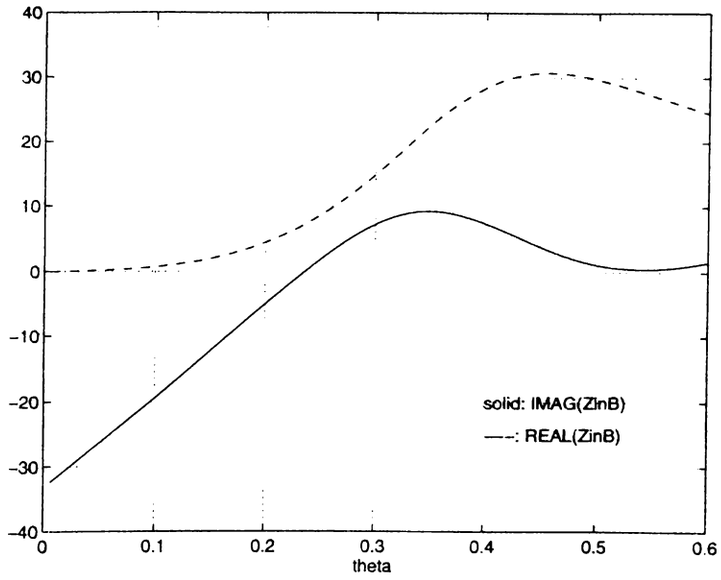



Figure 3.6: For $C_3$=0.2 pF $C_{F3}$=0.4 pF the change of $Z_{inB}$

### 3.2.2 Stage A

It was observed that for the values of impedances satisfying the equation 3.16 the input impedance seen from the port 1'' is real. For $C_3$=0.2 pF, $C_{F3}$=0.4 pF ($Z_{F3}$ ≈-j33 from Fig.3.5(a)) and $\theta_B \approx 0.42rad$ combination as shown in Fig.3.6 we have $Z_{inB} \approx 30\Omega$. (If the Port 3 is terminated with 50Ω, then $Z_{inB} \approx 15\Omega$.) Using this evidence in the design of stage A, $Z_{inB}$ is taken real (in fact 30Ω). Beside phase delay from the Port 1 to Port 2, the phase difference between the Port 2 and unreal Port 4' has to be considered. It was observed that if $Z_{F1}$ is an inductance then the phase difference between the aforementioned ports becomes zero at 12 GHz in our case. (Despite the practical difficulties of obtaining a compact-broadband large inductor, in the design process $Z_{FF} = (0.5nH)//(30\Omega)$ is used.)

According to the governing design equation for stage A 3.26, inductive impedance (0.3 nH) at port 2, yields the plot in Fig.3.7 for $Z_1$. There exists a zero of the real part $Z_1$ below 0.4rad. At this zero $Z_1$ is capacitive. Therefore $L_2$ =0.3 nH, $C_1$ ≈0.2 pF, and $\theta_A$ ≈0.3rad combination a possible solution.

Replacing the inductive with a capacitive impedance gives us yet another

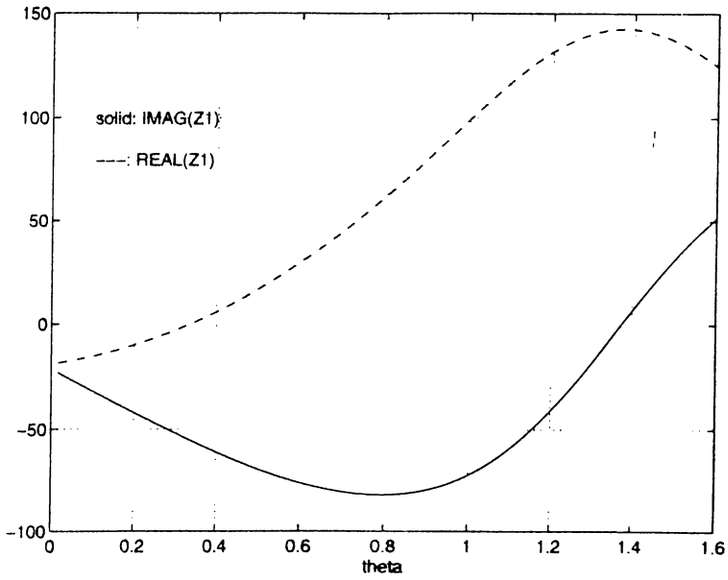



Figure 3.7: For $Z_2 \approx j20$ the change of $Z_1$

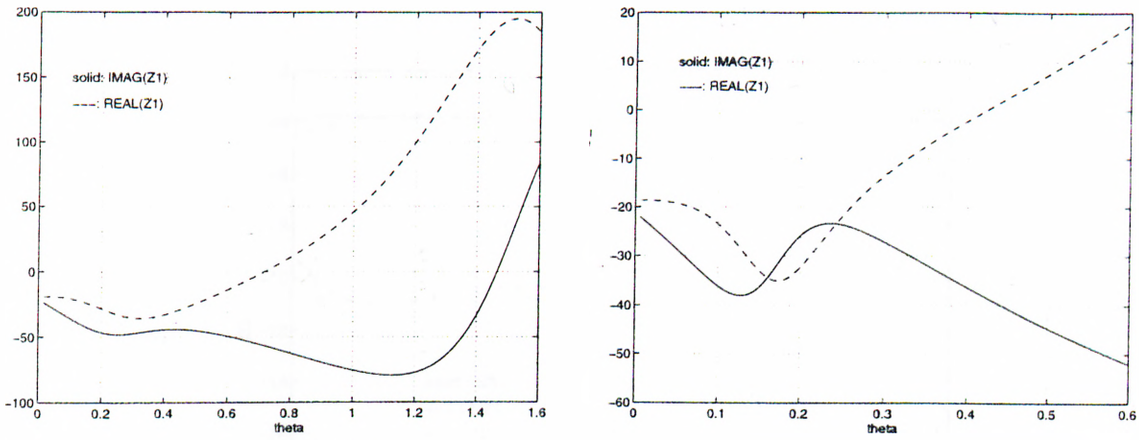
possible solution. As in Fig. 3.8 can be seen there exists a zero for a given capacitive termination of port 2. For the $C_2$ =0.2 pF case the zero is near $\theta$ =0.7rad and the corresponding $C_1$ ≈0.15 pF. The similar replacement behavior is observed in this case,too. (The zero crossing point of real part of $Z_1$ is moving to the right.) The second possible solution to the problem can be $C_2$ =0.2 pF, $C_1$ =0.15 pF and $\theta$ =0.7rad combination.

### 3.2.3 Overall Optimization

The possible solutions have to be combined and the assumptions made have to be checked. The critical issues in choosing a particular alternative are:

- The amplitude and phase balance of the ports 2 and 3 (Bandwidth consideration ).
- The matching of the ports ($R1 = 50\Omega$, $R2 = 100\Omega$, $R3 = 100\Omega$).

The configuration in Fig.3.1 is optimized by Microwave Harmonica for $|S_{11}| < -10$ dB, $|S_{21}|, |S_{31}| > -3.5$ dB in the 8-18 GHz frequency range, starting




(a) (b)

Figure 3.8: For $C_2 = 0.2$ pF (a) and $C_2 = 0.5$ pF (b) the change of $Z_1$

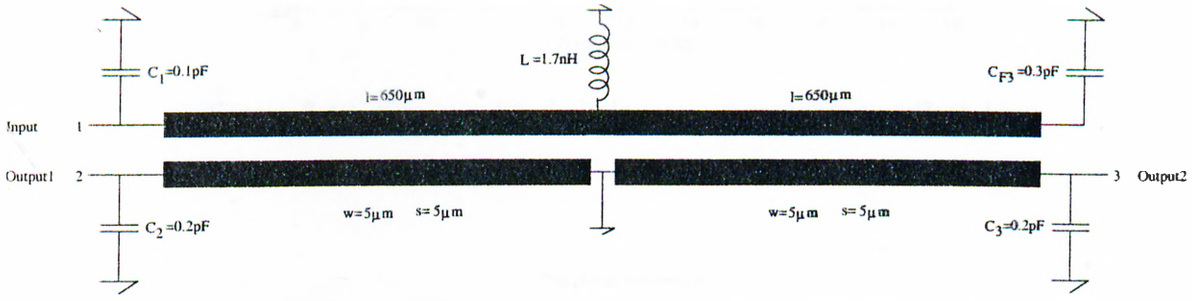



Figure 3.9: The optimized novel balun

by the initial values of $\theta_A$ =0.7 rad, $\theta_B$ =0.43 rad, $C_1$ =0.15 pF, $C_2$ =0.2 pF, $C_3$ =0.2 pF, $L_{F1}$ =0.5 nH, and $C_{F3}$ =0.4 pF. After 10 gradient optimization steps the responses shown in Fig.3.10,3.11 are achieved with following optimized values: $\theta = \theta_A = \theta_B \approx 0.4$ rad $\approx 650$ $\mu$m (at 12 GHz), $C_1$ =0.1 pF, $C_2 = C_3$ =0.2 pF, $L_{F1}$ =1.7 nH, and $C_{F3}$ =0.3 pF. The final structure is shown in Fig. 3.9.

The return losses from the output ports is given in Fig.3.12. It is observed that the ports 2 and 3 see almost the same impedances at 12 GHz is $\approx 200\Omega$. The matching of the output ports to $100\Omega$ is not satisfied in broader frequency range as expected.

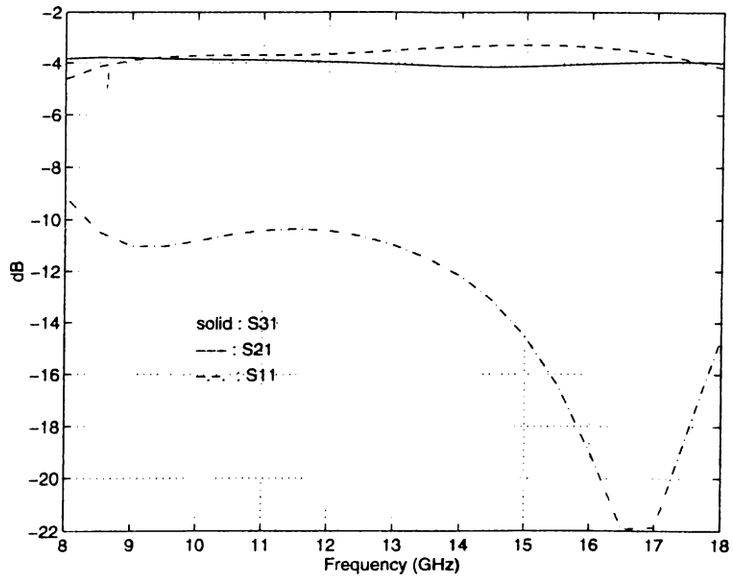



Figure 3.10: The amplitude balance and matching at Port 1

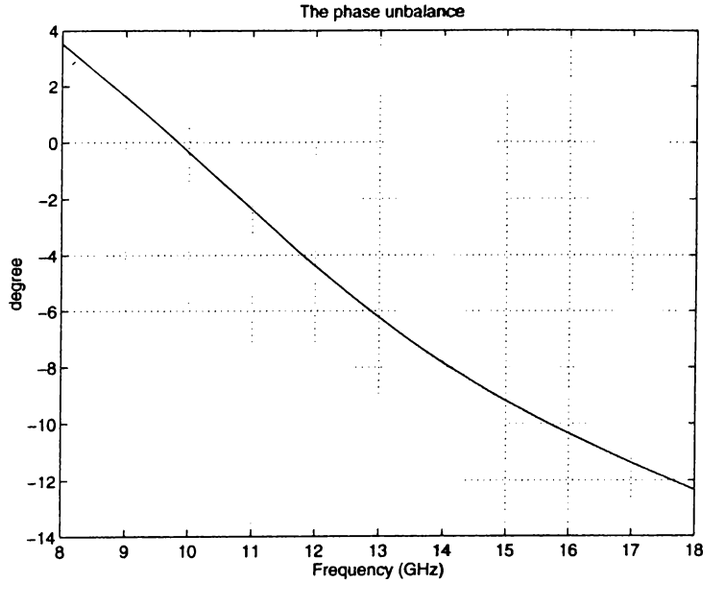



Figure 3.11: The phase balance of the output ports

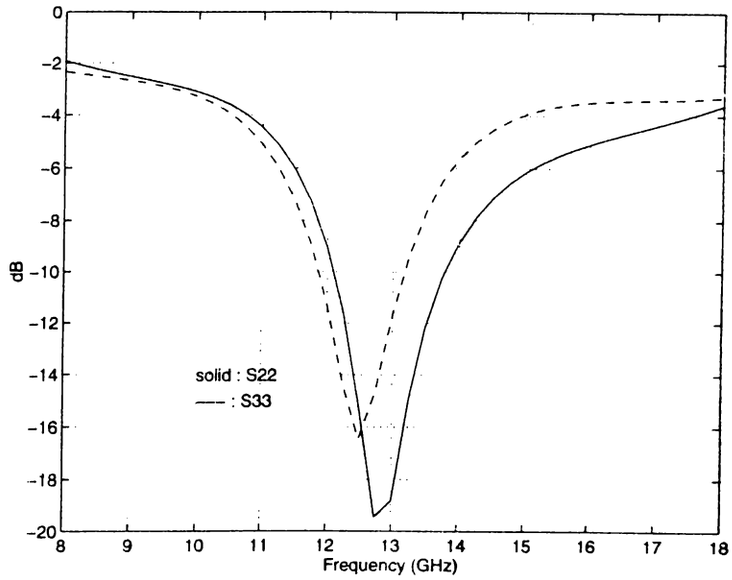



Figure 3.12: The return losses for the terminations $R1 = 50\Omega$ $R2 = 200\Omega$, $R3 = 200\Omega$

## 3.3 Discussion and Future Work

Using homogeneous, symmetric coupled parallel microstrip lines and readily available MMIC components a novel broadband passive balun is designed. It exhibits maximum phase error of 12° and maximum 1dB amplitude unbalance over the frequency range of 8-18 GHz. If CPL sections are simulated using SONNET and their S parameters are used in MH, the phase error is observed to be less than 8°. Best to our knowledge, it is the smallest balun achieving such a level of performance and it is the first example of its kind.

Although in the design the intention was to attain 1:2 impedance transformation, the optimized structure gave much better results for 1:1 case.

In practical realization two weaknesses are experienced. The first one is the deficiency of a suitable center tap. In mixer applications center tap has an important utility. Usually IF signal is extracted very efficiently if there is one. But in most of the balun structures the same problem remain unresolved. In the presented case, the grounded (isolated) ports can be used for this purpose, although a modified design process should be applied to treat such a problem.

The second weakness is the inductance-sensitivity of ports $3'$ and $2''$ (Fig.3.1). In chapter 6 a possible solution to this problem is suggested. Both of the weaknesses hint us the need for much efficient use of ports $3'$ and $2''$ without increasing the practical realizability problems.

As the theoretical characterization and rough calculation suggest it is possible to obtain $180^{\circ}$ phase shift using a single stage of CPL. One may obtain a more compact balun than the presented here, though in such a configuration the center-tap-problem will remain unresolved. Consequently there are two directions for future work; to solve the problems of two-stage-CPL balun approach and to develop a new one-stage-CPL balun approach.

# Chapter 4

# The Floating FET Mixer

The idea of "Floating FET" as a mixer was successfully realized at 900 MHz and 1800 MHz [34]. It brings a cost effective mixer structure needed by wireless applications. Here using the same idea a new mixer is presented using a novel balun structure. In 8 GHZ to 14 GHZ frequency range, it demonstrates conversion losses 8.5 dB-13 dB, and excellent LO-RF and LO-IF isolations. According to our knowledge with its 0.44 $mm^2$ area it is the smallest mixer operating at the given frequency range.

## 4.1 Introduction

The need for faster communication shifts the interest to higher and higher frequencies. The increasing demand forces new ways of design and new structures which result in low cost, small size, high reliability and good electrical performance. Double balanced mixers (in Chapter 2) are the choice of those who need good isolations between the ports, and broadband operations. The major drawback for the double balanced mixers is their large size hence their high cost. The presented mixer structure is realized in very compact chip area. Since it does not require a DC biasing, it can be used as an in-line mixer. The

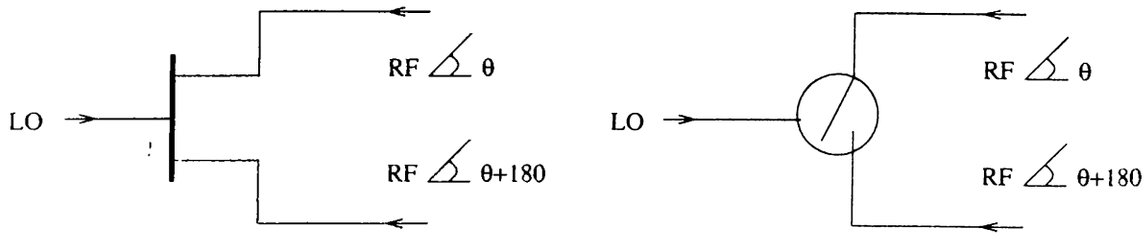



Figure 4.1: A Floating FET Mixer.

port isolations are comparable to those of the double balanced mixers.

## 4.2 Principle of Operation

The FFM topology presented here stems from the idea of using transistors in their passive mode. (Some of the researchers call this mode as resistive mode [35],[36] while Mourant calls as floating FET [34].) In this mode of operation, no DC voltage is applied over the FET channel. A large signal (LO) is fed to the FET gate, resulting in a change of channel resistance between high and low values. As can be seen in Fig. 4.1, the drain and source terminals of a FET are floated above ground through a balun [34].

But in order to do this switching (modulation) operation effectively the gate of the FET should be biased near the pinch-off voltage. This is simply realized by a capacitor connected in series to the gate of the FET. Such a capacitor charges with the LO voltage through the Schottky diode of the FET, hence lower the gate voltage relative to ground. Using such a "self-biasing" scheme results in lower LO power levels.

The other important part of a FFM is the transformer to float the FET. It is most difficult part of the FFM to realize. A balun topology similar to the one presented in Chapter 3 is used here.

One of the most promising features of the FFM structure beside its compactness is the good isolation characteristics. There are two important factors for such an result: the gate to source isolation of a FET and the port isolation

of the balun. The effect of first one decreases with the increasing frequency and $C_{gs}$, the gate to source capacitance of the FET becomes the key role player above 15 GHZ. Fortunately, the balun cancels what leaks from the gate. As a result the LO-RF and LO-IF isolations are expected to be comparable with those of double balanced mixer structures.

## 4.3 Design

Since the aim is to obtain an all-passive structure active baluns are not considered as an alternative. There are several passive broadband balun structures (in Chapter 2), either they require special manufacturing processes or their area is quite large. In Fig.4.2, the balun is illustrated. The addition of IF extraction node, keeping it virtually ground at the center frequency requires a resonance circuit. At this configuration IF actually extracted over the capacitor of the resonance circuit. Although the addition of the resonance circuit limits the bandwidth, its effect is not very crucial in the simulations.

The parameters shown in the Fig. 4.2 are optimized using the resulting network theory and then Microwave Harmonica (MH). The final values of the parameters are given below: (at f=15 GHZ)

$$\begin{aligned} C_R = 0.4pf \quad C_F = 0.25\,pf \\ \theta_A = \theta_B = \theta = 32^o \\ w_{1A} = w_{2A} = w_{1B} = w_{2B} = w = 10\,\mu m \\ s_A = s_B = s = 10\,\mu m \end{aligned} \tag{4.1}$$

The length of one of the CPLs is only 700 $\mu$m. In the frequency band of interest, the values of the capacitances, $C_R$ and $C_F$ drastically effects the matching at the RF port and the overall response of the structure. The final response is given in Fig.4.3.

For the design a 0.5×75 $\mu$m four-finger MESFET is chosen. The capacitor, $C_B$ in Fig. 4.4 is used self-biasing purposes. The addition of $C_B$ worsens the matching problems at the gate side. Using a shunt capacitor and a series

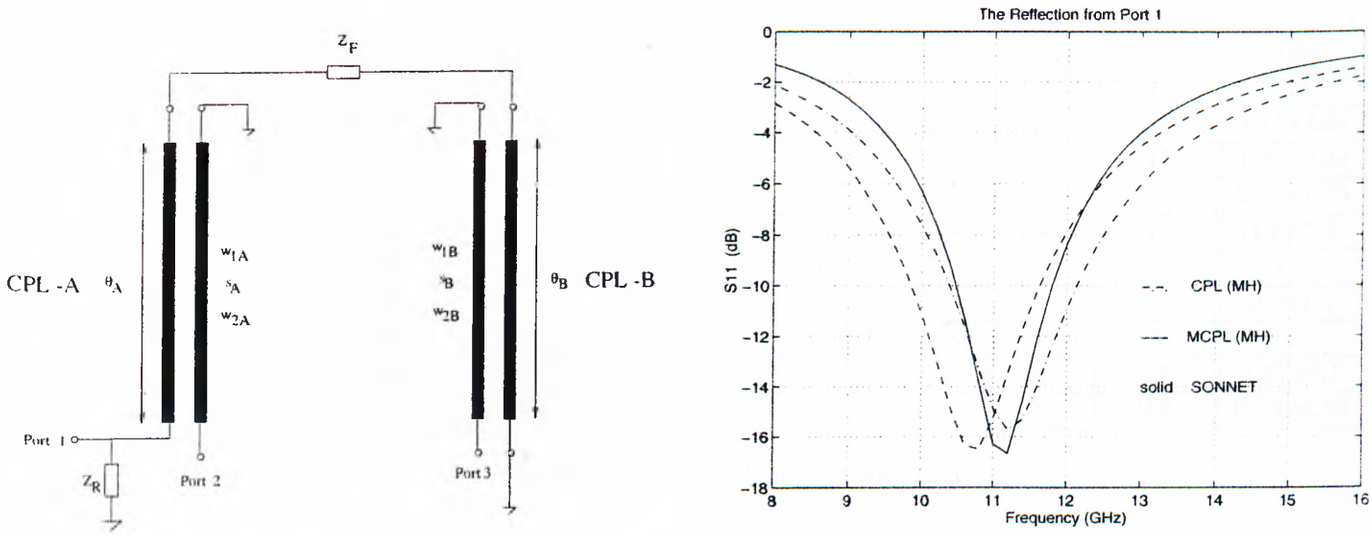



Figure 4.2: The Proposed CPL Balun and the reflection from port 1.

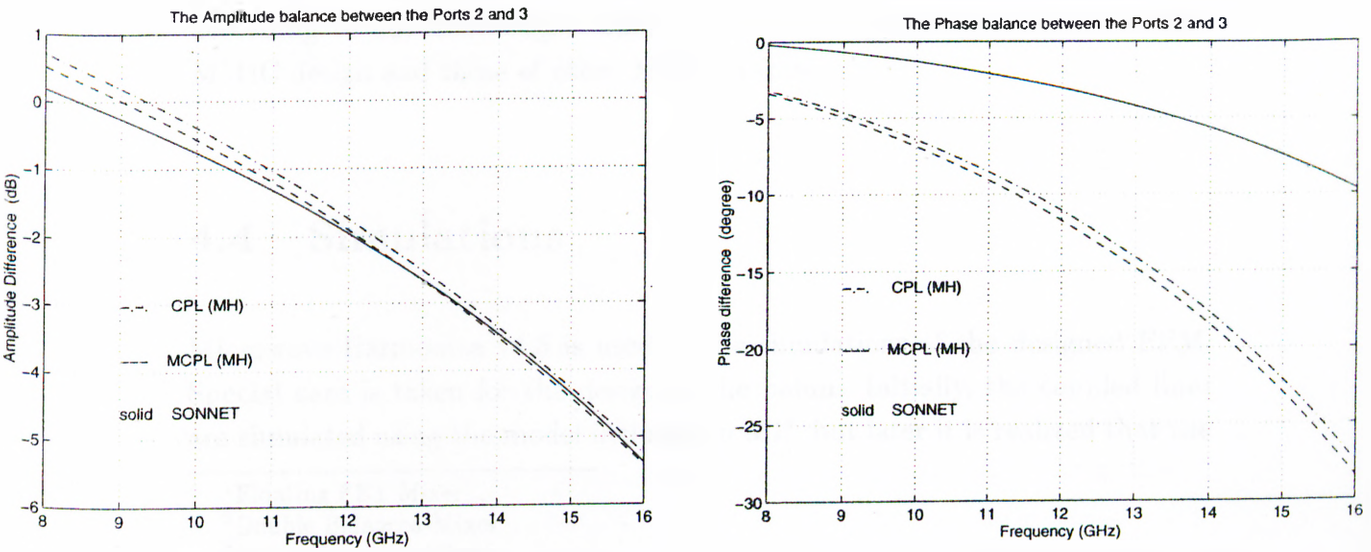



Figure 4.3: The Amplitude and Phase Balance of CPL Balun.

| Design | Ref. | Top. | LO&RF Freq ( GHZ) | Conversion Loss | | | Isolations | | Typical LO (dBm) | Size ($mm^2$) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | IF ( GHZ) | Typ. (dB) | Max. (dB) | LO-RF (dB) | LO-IF (dB) | | |
| MA-COM | [34] | FFM[1] | 0.8-0.92 | 0.1 | 7.5 | ?[8] | 40 | ? | 17 | 0.68 |
| MA-COM | [34] | FFM | 1.7-2.0 | 0.1 | 7.5 | 9 | 30 | ? | 17 | 0.5 |
| Litton | [24] | DBM[2] | 6-18 | 1.0 | 8 | 9 | 15 | 17 | 16 | 3.15x4.67 |
| TI | [24] | DBM | 6-18 | 0-3.0 | 7.4 | 12.3 | 15 | 19 | 15 | 1.27x2.54 |
| TRW | [19] | DBM | 4-6 | 1.0 | 7.5 | 10.5 | ? | ? | ? | 2.25x1.75 |
| NTT | [8] | IRM[3] | 24-26 | 1.0 | 6 | 8 | ? | ? | 10 | 1.6x1.3 |
| Raytheon[7] | [17] | DBM | 4-18 | 1-2 | -9 | -12 | ? | ? | 7 | 3x2 |
| ATR[7] | [37] | GM[4] | 3-10 | ? | 2 | ? | ? | ? | 10 | 0.9x1.4 |
| Robertson[7] | [37] | DFM[5] | 2-12 | ? | -3 | ? | ? | ? | 6 | ? |
| Varian | [38] | DDBM[6] | 8-18 | 2-7 | 7.5 | 9.8 | 23 | 20 | 17 | 4.57x6.1 |
| Bilkent | | FFM | 8-14 | 0-1 | 8.5 | 13 | 17 | 25 | 12 | 0.74x0.58 |

Table 4.1: Mixer Comparison

inductor the matching at the LO port improved.

The final design and the layout of the FFM chip is given in Fig. 4.4, C.2(in App.C). The chip was submitted to July 1995 run of GEC-Marconi. The manufactured chip was received in December 1995. Occupying a size of only 0.745mm×0.5885mm (0.44 $mm^2$), it is the smallest known planar MMIC mixer according to our knowledge. Table 4.1 lists the typical parameters for this MMIC design and those of other MMIC mixers.

## 4.4 Simulations

Microwave Harmonica v4.5 is used in the simulations of the designed FFM. Special care is taken for the design of the balun. Initially, the coupled lines are simulated using the model included in MH, but later it is realized that the

[1]Floating FET Mixer
[2]Double Balanced Mixer
[3]Image Rejection Mixer
[4]Gate Mixer
[5]Distributed FET Mixer
[6]Double-Double Balanced Mixer
[7]Active Mixer
[8]Data is unavailable

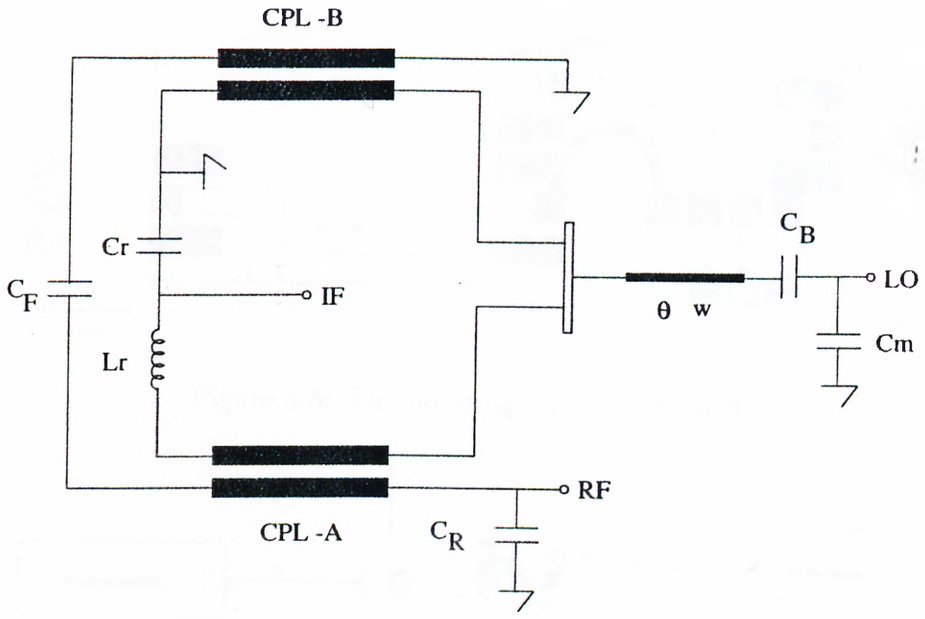



Figure 4.4: The Final Schematic of the FFM chip.

are simulated using the model included in MH, but later it is realized that the CPLs have to bended in order to use the chip area more effectively. Therefore in order to accurately characterize the bended CPLs an electro-magnetic simulator (SONNET) is used.

In the simulation of the novel compensated balun the reference impedances for all ports are taken to be 50Ω. Using SONNET, the coupled lines are simulated with the process descriptions given by GMMT. In the Fig. 4.2 and Fig. 4.3 MCPL corresponds to the multiple coupled lines in MH. The simulations of CPL and MCPL cases do not include the bends shown in the chip layout. The amplitude balance for all the simulations are in close agreement and after 10 GHZ the amplitude unbalance between the ports increases disturbingly. But the phase balance (Fig. 4.3) plots are not in agreement generally. The resonant frequency of MCPL and SONNET matches but it is observed that MH is more pessimist than SONNET. 10° phase unbalance obtained from SONNET is really promising. The FET is simulated using modified Materka model. [39],[10]. The model parameters for 0.5×75 $\mu$m four-finger MESFET is given in Table

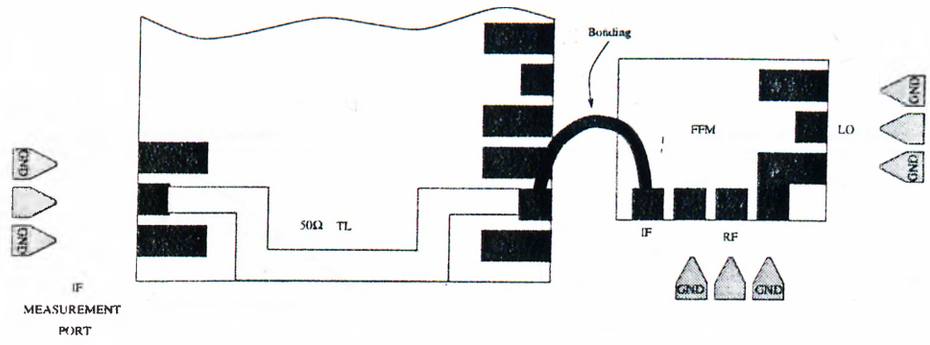



Figure 4.5: The bonding for measurements.

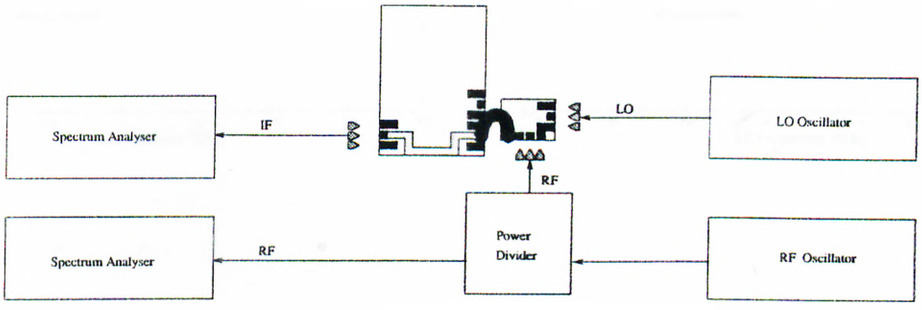



Figure 4.6: The measurement Test Set.

B.1 (in appendix B).

## 4.5 Measurements

While drawing the layout of the chip, in order to minimize the area a single pad is used for the IF output/input. At the beginning for the IF frequencies up to 3 GHZ we could not see any problem. But after we go for testing we realized that the coaxial probe introduce wildly changing insertion losses between 0dB and 20dB. In order to carry out a reliable measurement, between the IF pad of FFM chip and the pad for 50Ω through calibration on another chip is bonded as shown in Fig. 4.5.

The measurement set-up is given in Fig. 4.6.

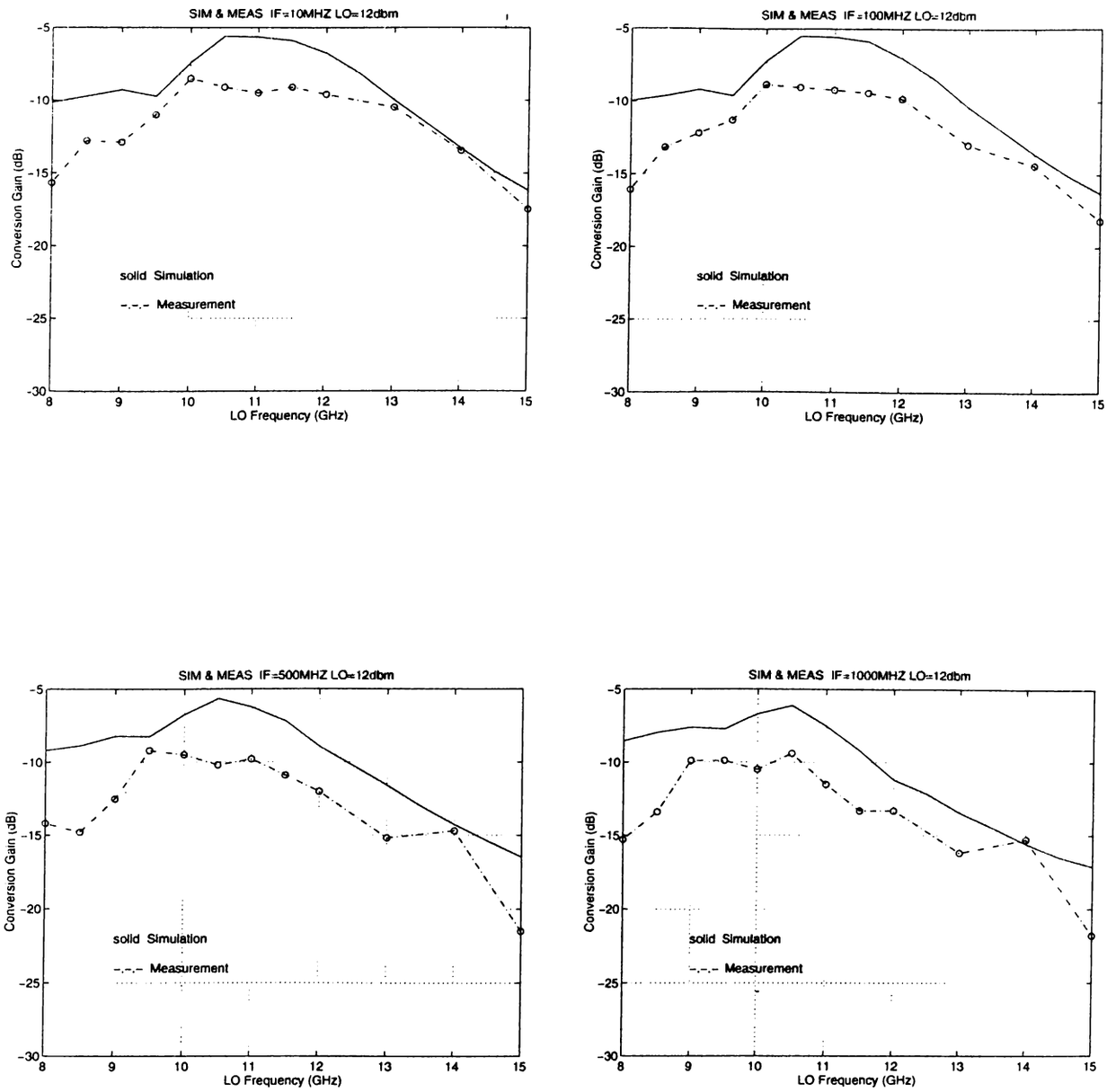



Figure 4.7: The Conversion Gain Measurements and Simulations for various IFs.

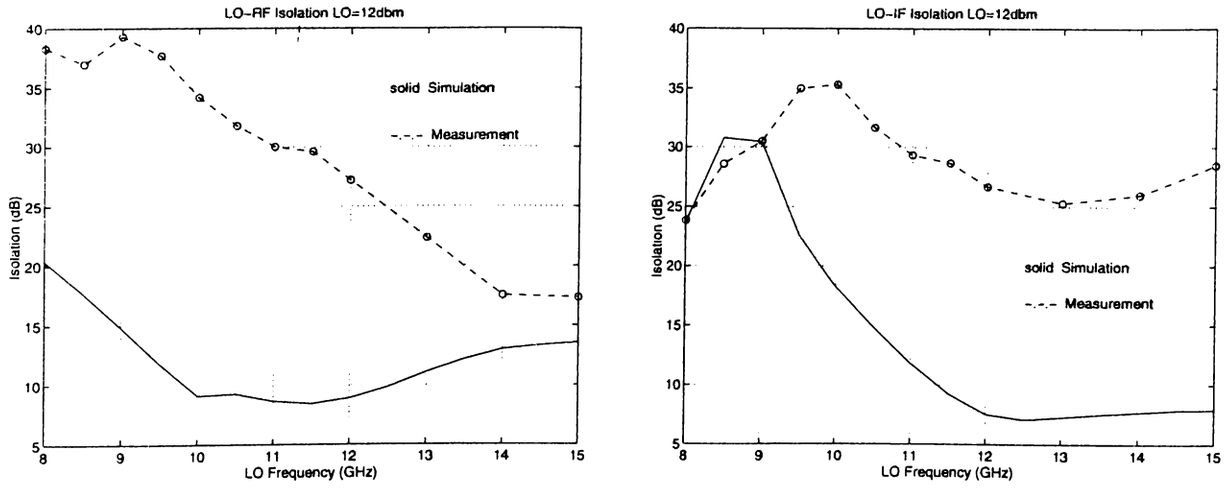



Figure 4.8: The LO-RF and LO-IF Isolations.

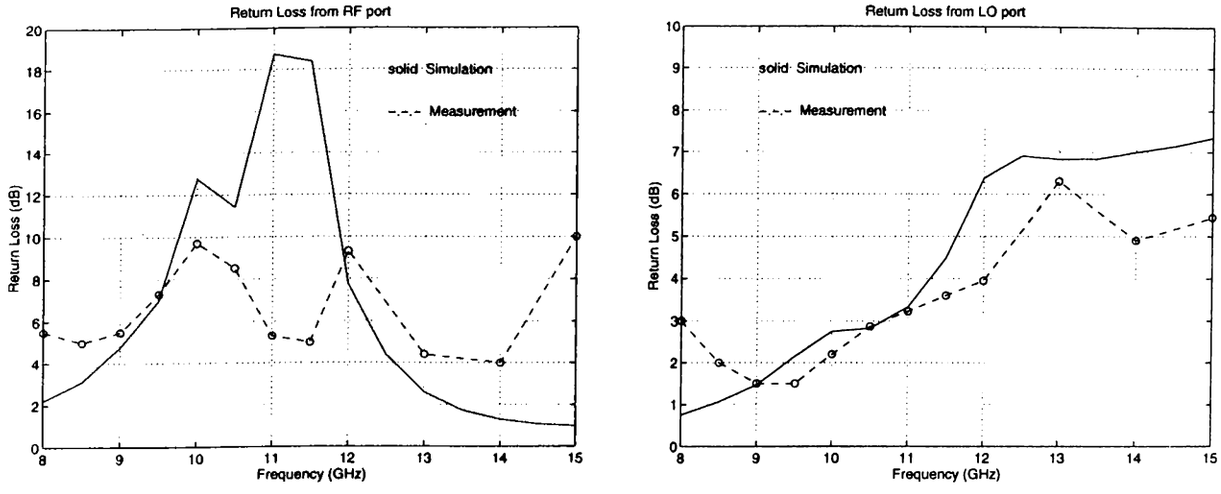



Figure 4.9: The Return losses from RF and LO ports.

## 4.6 Discussion and Future Work

The mixer introduced here uses a novel planar balun. It is formed by edge-coupled microstrip lines and MIM capacitors. It is believed that with its 0.44 $mm^2$ chip size the designed mixer is one of the smallest MMIC mixers. It was designed to operate in 8 GHz to 12 GHz bandwidth with conversion loss better than 8dB for 12dBm LO drive power.

It is observed that the conversion loss simulation and measurement results for IF frequency in 10MHz to 1000MHz range, differ in magnitude although they behave in the same manner. The simulation results tend to be 1dB-4dB better than measurement results. The source of this deviation can be considered under two groups.

The first one includes the measurement problems, as explained in the previous section, in order to increase the reliability of the measurements two chips bonded which might effect the measurements. The calibration error between the spectrum analyzers, the unbalanced division of the RF at the power divider, as well as the losses of cables at the probe station among the other sources of error in measurement.

The second important error-source group is the simulation errors. Most nonlinear device models available in commercial nonlinear simulators are mainly designed for active-mode operation and cannot accurately describe the device behavior in the linear region where the resistive mixer operates [35],[17]. Dortu et al. in their comparative study [40], mentioned the inadequate performance of the models even for the large-signal amplifier simulations. (Since the most of the large-signal models including Modified Materka used in the presented simulations are actually proposed for amplifier simulations [39],[41],[42].) Additionally, the supplied parameters for Materka may not be accurate enough. Because of this characterization problems usually designers develop their transistor models, especially for resistive mode mixer designs. There are also problems with the balun simulation. As seen in simulations section there are quite a big difference in phase balance for MH and SONNET cases.

Because of the on wafer calibration problems the reflection measurement

data are not reliable. The measured isolation data are found to be much better than simulation data. The difference points the importance of the simulation tools and models. It can only be explained by the deviation of behavior described by the models and the real life.

Possible improvements for this design are as follows :

- The matching at the LO port should be improved.
- A more suitable MESFET can be used instead of $4\times75$.
- The extraction of IF over a resonator limit both LO and IF bandwidth of the chip. New ways of extracting balanced IF from the mixer have to be developed. Without such an improvement increasing the bandwidth of balun will yield limited gain.
- The bandwidth of the balun can be increased. In this work the balun is realized at the M3 metal layer. Although the loss of this layer less than M2 metal layer, the minimum feature size (10 $\mu$m for M3) is the main reason of loose coupling. Using M2, or combination of M2 and M3 layers, with a new compensation technique may avail broader bandwidth. (M2 and M3 are the first and the second level interconnect metalization in the fabrication process, respectively.)

# Chapter 5

# The Single Balanced Mixer

A monolithic single balanced mixer is presented which exhibits low conversion loss, good isolation characteristics at low LO drive power levels. This is achieved for LO and RF signals in the 10GHz to 18GHz frequency range with an IF bandwidth from DC to 4GHz. The minimum LO power needed for operation of the mixer is 1dBm.

## 5.1 Introduction

The mixer design specifications are supplied by MIKES[1] are given in Table 5.1. These parameters are important to decide the mixer topology. In order to satisfy LO-RF isolation requirement a balanced mixer topology has to be used. There are three important balanced topologies that can be used to achieve the desired isolation criteria:Single-Balanced Mixer (SBM), Double-Balanced Mixer (DBM), and Resistive FET Mixer (RFM or FFM). The latter one has to be improved because of bandwidth limitations as a result of IF extraction problem, and narrow bandwidth of RF balun. The DBM topology is eliminated as well, mainly because the available power to the mixer is very limited. Hence

[1]MIKES:Microwave Electronic Systems

| IF Bandwidth | 2GHz - 4GHz |
|---|---|
| RF Bandwidth | 7.5GHz - 18GHz |
| LO Bandwidth | 11.5GHz - 17.5GHz |
| LO Power | 1dBm - 7dBm |
| Conversion Loss | -11.5dB (max) |
| LO-IF Isolation | 30dB (min) |
| LO-RF Isolation | 25dB (min) |
| RF Return Loss | 8dB (min) |
| LO Return Loss | 6dB (min) |
| Power Supply | 12V 15mA |

Table 5.1: The Requirements for the Mixer Design

the only plausible topology left is the SBM topology. The SBM topology presented here neither includes two baluns as Chen et al. [35] used, nor is similar to the general SBM topology described by Pavio et al. [1]. It includes one balun and two resistive mode FETs, which make this topology a new variation to the SBM topology.

Although a self-biasing scheme is used, a passive mixer realized with GEC-Marconi's F20 technology can not work with 1dBm power, even 7dBm power is considerably low for operation. This problem can be solved by using a pre-amplifier at the LO port which has a 10dB gain over the LO frequency range. A passive structure is chosen for the balun used at the LO port. LO-IF isolations can be realized by means of low pass filter.

## 5.2 Design

The overall design consists of four parts as seen in Fig. 5.1. The mixer is designed for the worst case; the worst case conditions are IF=4 GHz, $LO_{Bandwidth}$ =11 GHz-18 GHz, $LO_{Power}$ =1dBm, $RF_{Power}$ =-5dBm. The design of each part is considered separately and given in the following sections.

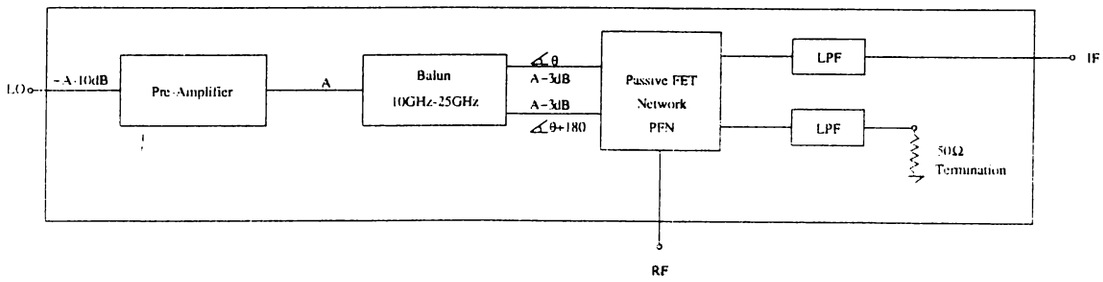



Figure 5.1: The Single Balanced Mixer Topology

### 5.2.1 LO Pre-amplifier

The stability is one of the most important issues in amplifier design. The amplifier must be unconditionally stable at all frequencies: below the band, in the band and above the band, moreover, it must be stable for all terminations that will be connected (ie not just 50Ω termination). Even for a single stage designs, this may not be an easy problem if you are restricted to lossless matching circuitry. Therefore, there may be need to add resistors to the amplifier for stability [1].

- Due to the stringent current requirements, the maximum parameter ratings were used.
- Since only one power source is given, the transistors are self biased using a bypassed source resistance. In order to ensure the biasing conditions will be satisfied, first the bias current is let to flow trough a current limiter bias transistor, then it is feed to the amplifier transistor(s). In such a configuration, the total periphery of the transistor(s) strongly depends on the bias transistor.
- Using maximum value for drain current per gate width 0.2mA/$\mu$m, it is calculated that to have $I_{dss}$ =25mA one must have, 125$\mu$m gate width. In this design 2×65 MESFET is used in the bias circuitry, mainly for current limiting purposes.
- The next step was to decide the $I_d/I_{dss}$ ratio to obtain optimum gain with the given bias current. It was seen that using a single stage it is very difficult to obtain a broadband operation. Although it is possible

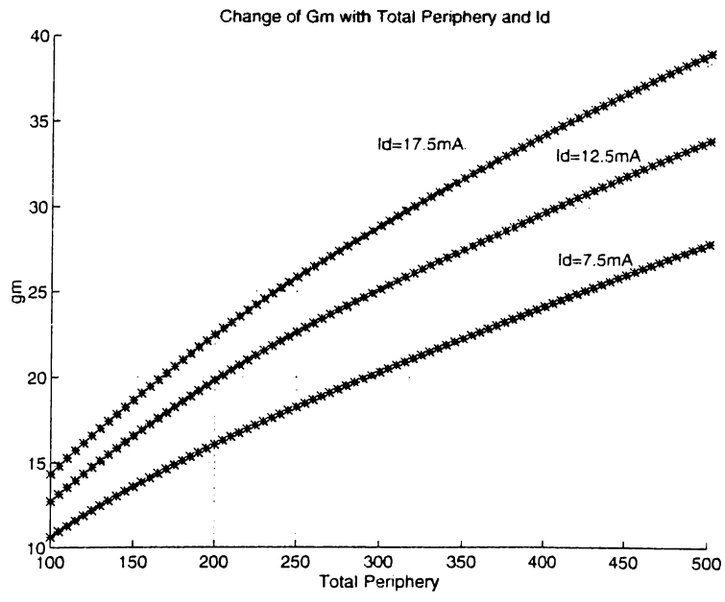



Figure 5.2: The Change in $g_m$ with the total gate width under constant drain condition

to obtain a broadband operation using feedback, it decreases the gain considerably. Therefore a two-stage structure without any feedback was designed.

- At the beginning the tendency was to bias the first stage with less current, since the second stage needs more power, but it was soon realized that in order to have broadband frequency of operation, the stages have to operate at different frequency ranges. (Mainly because there is no feedback used.) Therefore the two stages are equally greedy for bias power. That is why two stages in the final design have equal bias currents.

- Since $I_{ds}/I_{dss}$ ratio depends on the total gate width, one can choose a ratio under constant current condition. In Fig.5.2 the change of $g_m$ versus the total gate width for different drain currents is calculated. (There is no effect of the number of fingers.) For the current design $200\mu$m total gate width MESFETs were chosen and realized by two fingers.

- Having choosing the size of FET used in the design, the maximum stable gain and the stability factors were calculated and given in Fig.5.3 and Fig.5.4 respectively.

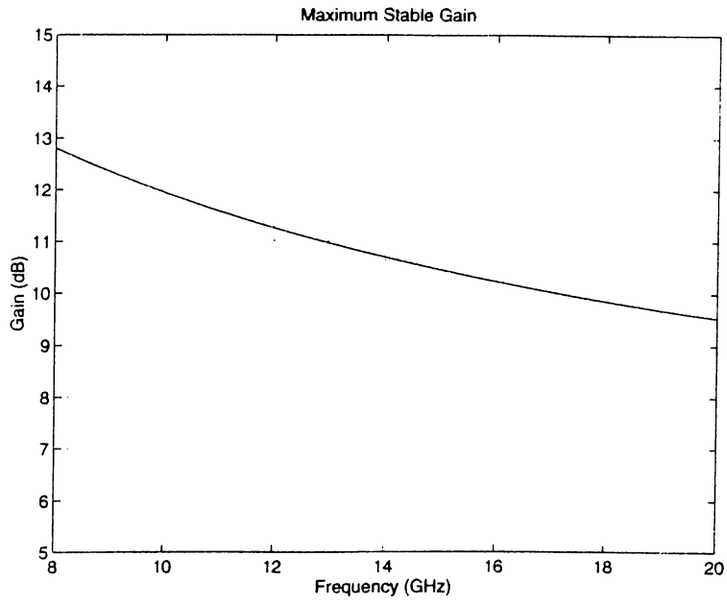



Figure 5.3: The Maximum Stable Gain

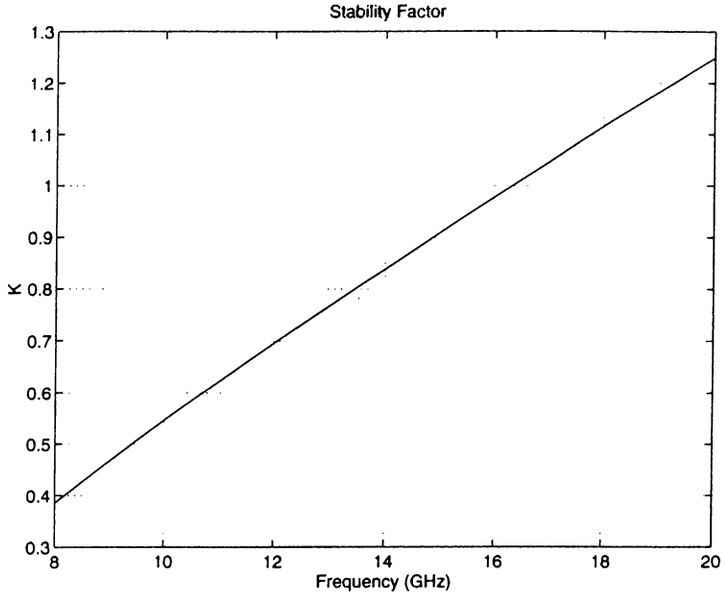



Figure 5.4: The Stability Factor (K) before matching network

- A crude matching network calculation is illustrated in Fig.5.5.
- For stability purposes a resistance is introduced in series with shunt inductor at the input matching network (Fig.5.5). In the overall simulation an unexpected sensitivity to the bias circuitry was observed. It was thought that the termination of the amplifier with the balun that matters, but later the investigation yielded the result that the amplifier prefers to have low output impedance. This was realized by a capacitance in parallel with the bias transistor. The final schematic of the amplifier is shown in Fig.5.6.
- The linear simulation results of the LO pre-amplifier are given in Fig.5.7 and Fig.5.8.

### 5.2.2 Balun

There are two possible configurations that can be used here: **1)Amplifier+Passive balun, 2)Active balun** The latter one seems attractive because of its simplicity but from the explanation given in Chapter 2, there is no obvious active balun topology which can give the desired 7dB gain in the 10-18GHz frequency band. This leaves us with the first choice. Planar Edge-coupled Marchand Balun topology is prefered among the passive structures [16],[24],[21],[28]. But it should be pointed out again that using a new active balun structure with the desired performance can ease the design problems encountered in the first choice.

In Fig. 5.9 the final version of balun is given. The coupled transmission lines (CPL) are symmetric, their widths are $w = 10\mu m$ and their spacing is $s = 5\mu m$. The length of each CPL section is $1500\mu m$, which corresponds to almost $70^{\circ}$ at 14GHz. The balun is folded to minimize the area of the chip. The simulation of this balun carried out by Microwave Harmonica (MH) [10] and SONNET [43]. The amplitude balance and phase balance are given in Fig.5.10 and Fig.5.11 respectively. In the overall simulation of the circuit the results of SONNET was used.

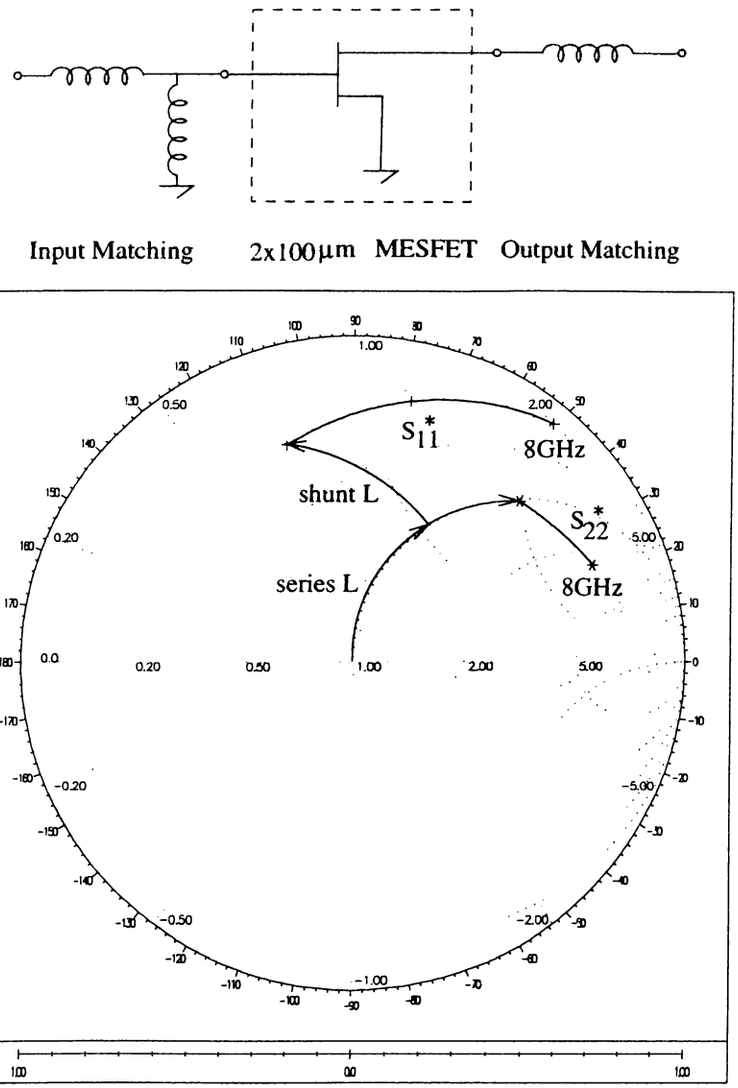



Figure 5.5: The $S_{11}^*$ and $S_{22}^*$ (8GHz-20GHz) for $2\times100\mu$m MESFET with crude Input and Output Matching Calculation at 20GHz

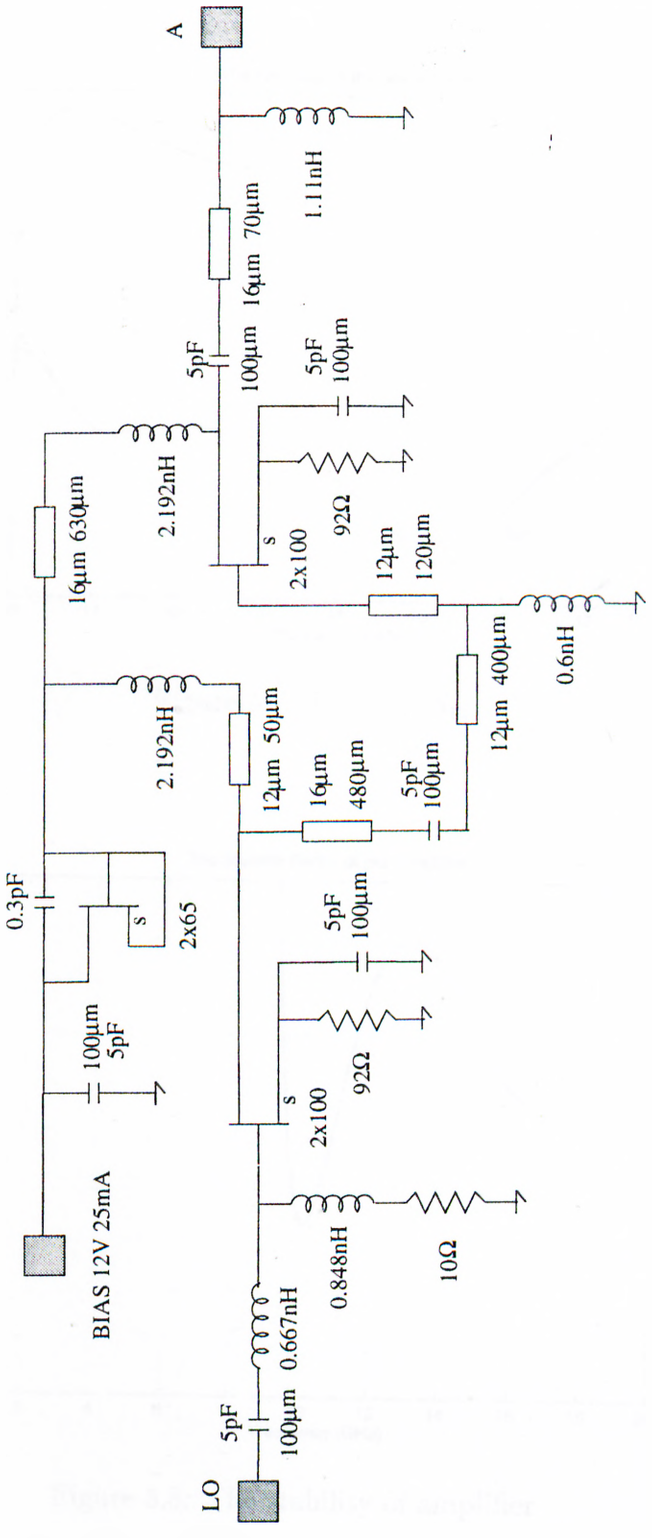



Figure 5.6: The pre-amplifier

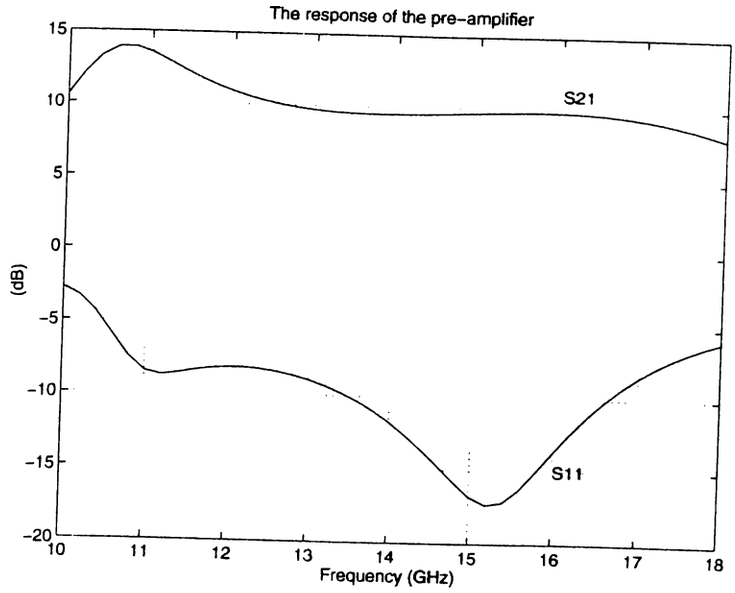



Figure 5.7: The $S_{21}$, $S_{11}$

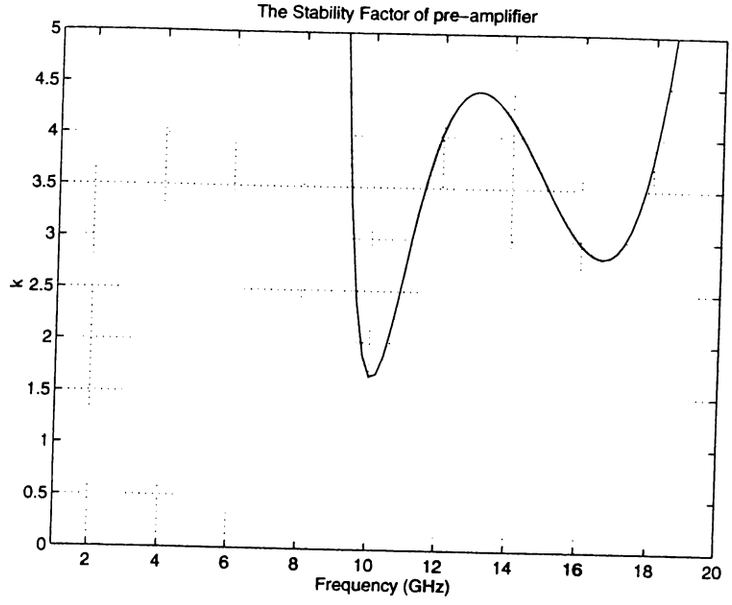



Figure 5.8: The stability of amplifier

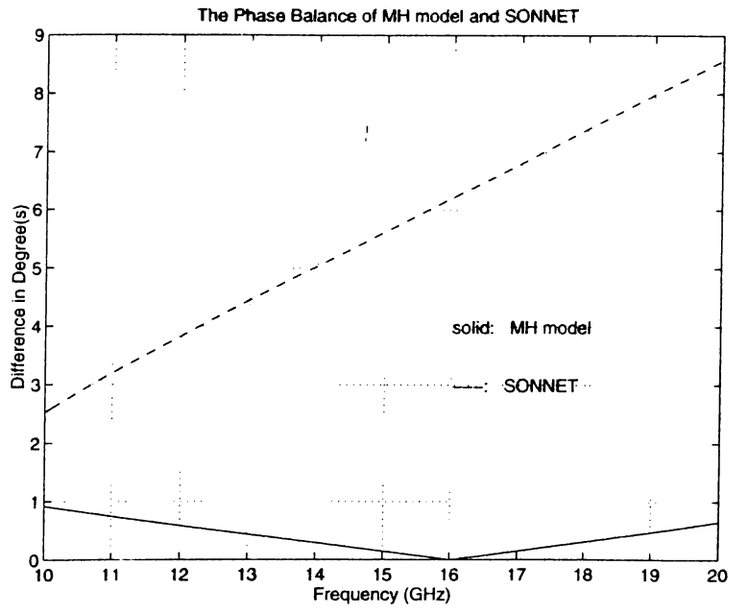



Figure 5.11: The Phase Balance of the Balun

### 5.2.3 Single Balanced Mixer

FETs will be used again in their resistive modes. The isolation problem at high frequencies is circumvented by using an RF balun (Chapter 4). Here a new approach is applied to solve the problem (Fig.5.12). If the FETs F1 and F2 are chosen identical, then looking from node 1, the leakages of $LO_1$ and $LO_2$ cancel each other. (In Fig.5.12 no phase difference is shown between the signal applied to the gate and the signal leaked to the source. This is solely to demonstrate the idea of cancelation of leakage signals at node 1.) In order to have good isolation:

- The amplitudes of $LO_1$ and $LO_2$ have to be equal whereas their phases have to differ exactly by $180^o$.
- The circuit should be symmetrical around node 1. Hence looking from the gates of the FETs the impedances seen are equal to each other which results the same leakage for FETs.

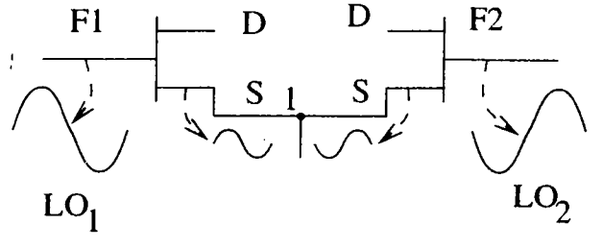



Figure 5.12: The proposed Single-Balanced Mixer Topology (Balun is not shown)

The first condition can be satisfied using a balun which is explained in previous section. There are two ways to satisfy the second condition: IF balun and symmetrical Low Pass Filter (LPF) implementation. The first choice is the obvious solution to this problem, but it requires very large area to implement a passive balun at IF frequency band. Instead in this design the second one is chosen. In order to maintain the symmetry one of the drains is terminated with exactly the same LPF and 50Ω.

Finally to optimize the performance of the SBM structure, both FETs are self-biased using series capacitance, (Fig.5.14) since it is known that the gate to source voltage should be close to pinch-off voltage for low LO power operation. After the addition of the series capacitors, the matching between the outputs of the balun and self-biased gates enhanced using the shunt transmission line and resistor combination.

### 5.2.4 Low Pass Filter

The main aim in the design of the low pass filter is to minimize its area. At least 40dB attenuation above 10GHz and as small loss as possible up to 4.5GHz in the passband are desired. Although it is possible to attain this goal in smaller area if transmission line filter techniques are used, the 40dB attenuation requirement is difficult to satisfy. By applying improvements over the basic transmission line techniques, it is still difficult to meet the desired performance level. Here, a fifth order LC filter is implemented using elements

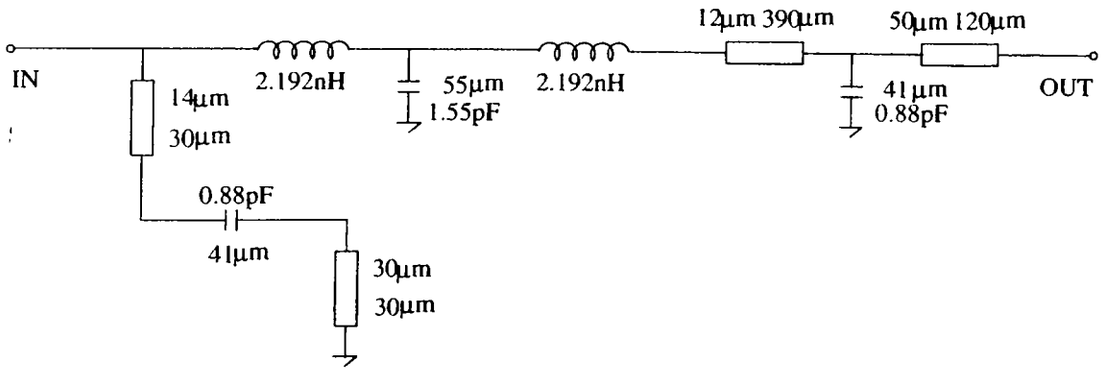



Figure 5.13: The Low Pass Filter

available in the library. In Fig.5.13 the final version of the filter is shown. If the available models are used in the simulation the passband loss is observed to be larger than expected. It is desired to be as small as possible because it directly effects the IF output. The passband loss linearly increasing from 0dB to 2dB at 4GHz band edge.

## 5.3 Simulations and Measurements

The simulations were carried out using the nonlinear simulator MH. The structure simulated for the worst case mentioned in design section. The "Modified Materka" active models (App.B) were used for the passive FETs in the PFN block (Fig.5.1). Unfortunately, the simulation of the pre-amplifier was done using small signal models of the transistors. (Because we do not have their large signal models.) Hence there is an important assumption about the validity of the linear simulation for this case. The 1dBm input signal level case can be treated as small signal, but the 7dBm input signal level is close to the 1dB compression points of the transistors. Since 1dBm LO level is taken as worst case, the results will not be very different from the large signal simulation case. For the 7dBm case, the gain of the pre-amplifier is expected to be smaller then 7dB, but as far as the amplitude of the main harmonic is above 10dBm, the response of the mixer will not be affected. The matching network is derived using the linear models of the FETs. (The derivation is partly explained in the

Fig. 5.5.) The matching network used in the RF port is obtained by nonlinear simulations, because the FETs seen from the RF port should be modeled nonlinearly. The overall structure consisting of both linear and nonlinear models is optimized before going to the layout-drawing step, then because of physical constraints the circuit is modified and reoptimized. This iterative process continues until both the physical constraints are satisfied and the desired responses are obtained.

In Fig. 5.6, 5.14, C.3 (in App.C) the final circuit and layout of the chip are given. The dimensions of the chip are 1.795mm$\times$1.166mm.

The measurement results deviate from the expected results. In some cases the deviations are in better direction and in the rest of them the results turn out to be worser. (In Figures from 5.15 to 5.20.)

The conversion gain, as the most important criteria in a mixer design is observed to be much less then the simulation indicates. There can be several possible explanations for this result. The clear difference between the curves of input LO power values of 1dBm and 5dBm (shown in Fig. 5.15, 5.16) indicates an important difference between measurement and simulation when the input LO power increased. (In simulation the 5dBm conversion gain curves are much closer to 1dBm curves.) This difference can be seen as an evidence of violation of the small signal assumption in the pre-amplifier simulation.

While measuring the isolations, if the power of the amplifier is turned off the leaked LO power would decreased approximately 10dB in magnitude (at IF port). It can be seen as an indication of amplification which means that the pre-amplifier works as expected. Hence the cause of less conversion gain should be searched in other parts of the design. Actually the results obtained in the LO-IF isolation measurement is surprising, because the attenuation of the IF filter should be larger than 30dB above 11 GHz. Therefore the leaked power should be well below of -30dBm. As can be seen in Fig. 5.18, the measured values are at least 10dB worser, or the simulator overestimated the performance of the IF filter greatly. (It should be stressed that the IF filter has an crucial value on IF output.)

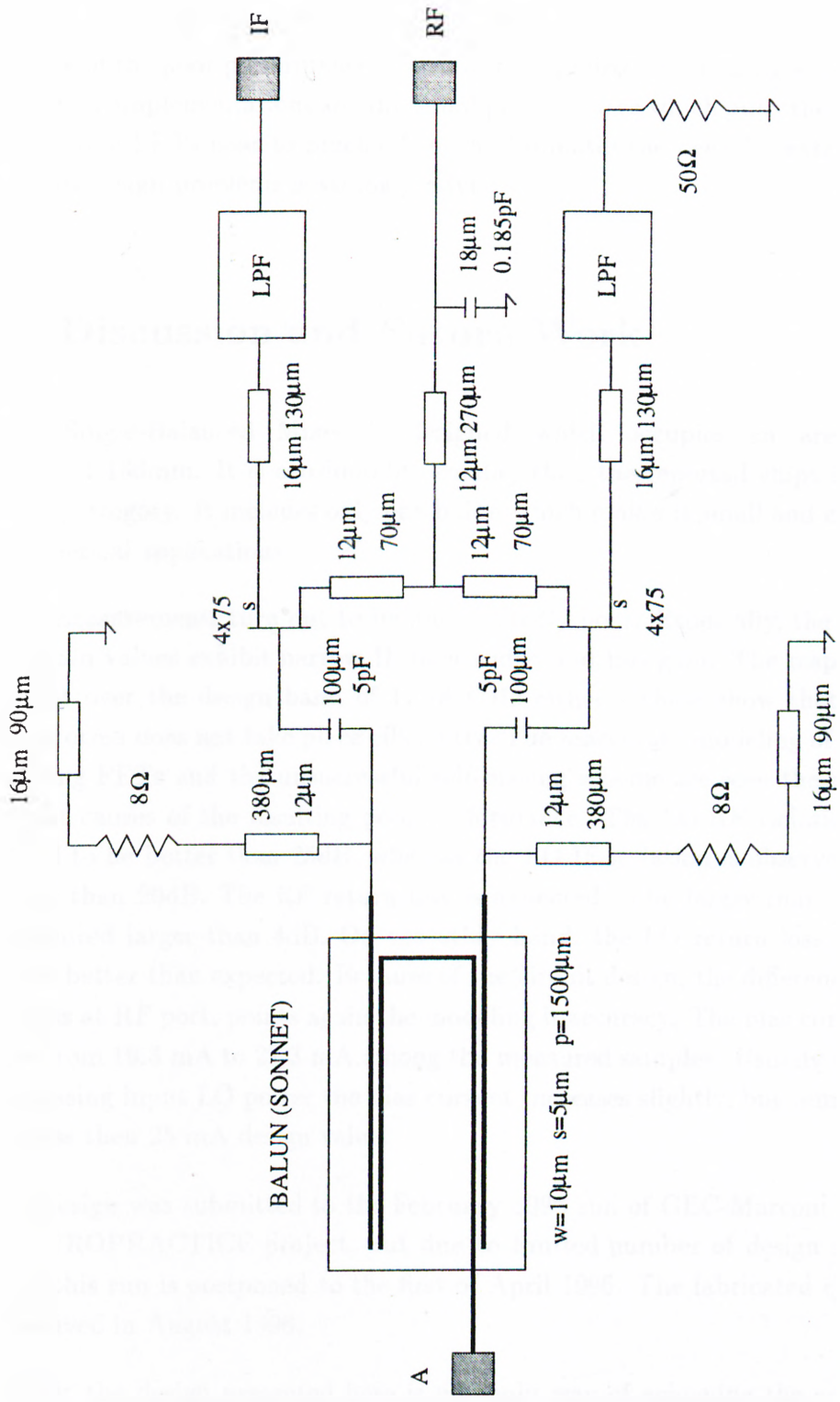



Figure 5.14: The Single-Balanced Mixer

Beside the modeling problems of the passive mixing FETs, the most important cause of the poor performance is seen as the applied "self-biasing scheme". In the future implementations an additional power source which pulls the gates of the passive FETs near to pinch-off, both eliminates the need for extra LO power and design problems is strongly advised.

## 5.4 Discussion and Future Work

A new Single-Balanced Mixer is designed which occupies an area of 1.795mm$\times$1.166mm. It is considerably smaller than the reported chips in its operation category. It includes only one balun which makes it small and cheap for commercial applications.

The measurements turn out to be unexpectedly poor. Especially, the conversion gain values exhibit narrow IF bandwidth and less gain. The response is not flat over the design band of 11-18 GHz either. These show that the mixing process does not take place efficiently. The inaccurate modeling of passive mixing FETs and the unsuccessful self-biasing scheme are seen the most important causes of the resulting poor performance. The LO-RF isolation is measured to be better than 25dB, whereas the LO-IF isolation is observed to be better than 20dB. The RF return loss is expected to be larger than 7dB, but measured larger than 4dB. On the other hand, the LO return loss turn out to be better than expected. Because of the circuit design, the difference of return loss at RF port, points again the modeling inaccuracy. The bias current changes from 19.3 mA to 22.3 mA among the measured samples. Usually with the increasing input LO power the bias current increases slightly, but remains always less then 25 mA design value.

The design was submitted to the February 1996 run of GEC-Marconi F20 under EUROPRACTICE project, but due to limited number of design submissions this run is postponed to the first of April 1996. The fabricated chips were received in August 1996.

Finally, the design presented here is not only way of achieving the goals,

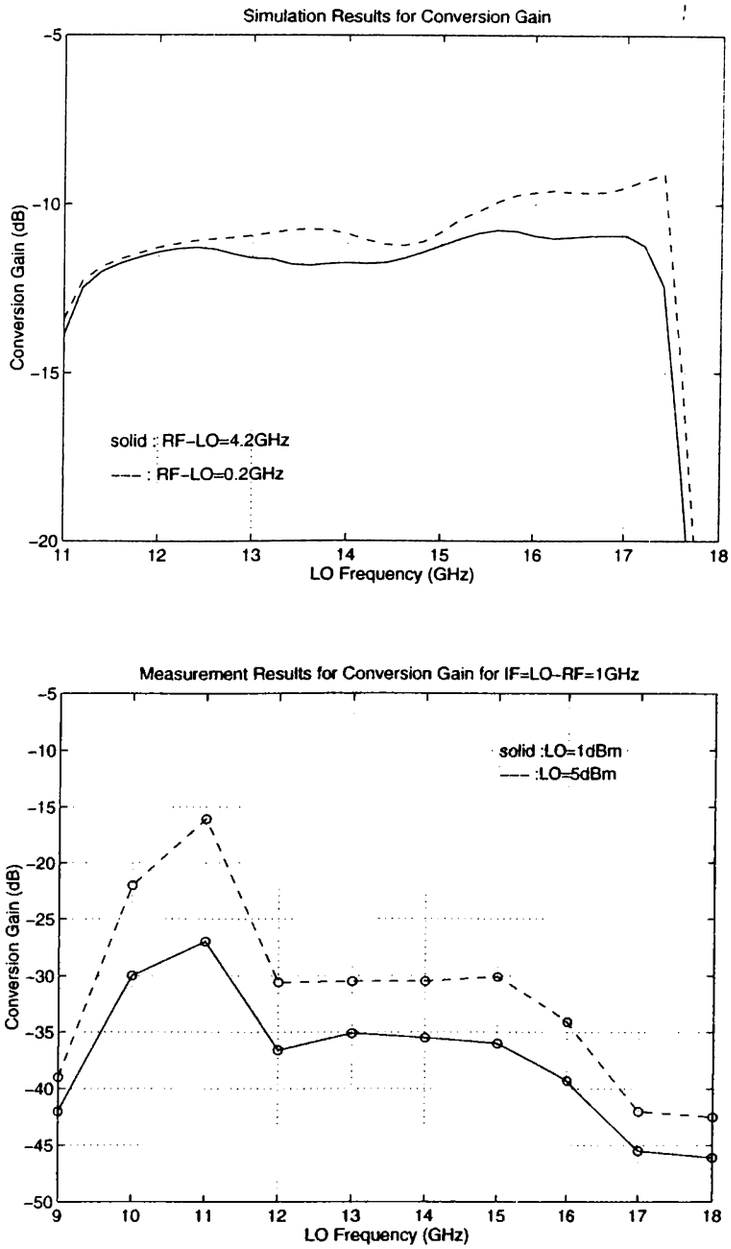



Figure 5.15: The Simulation and Measurement Results for Conversion Gain

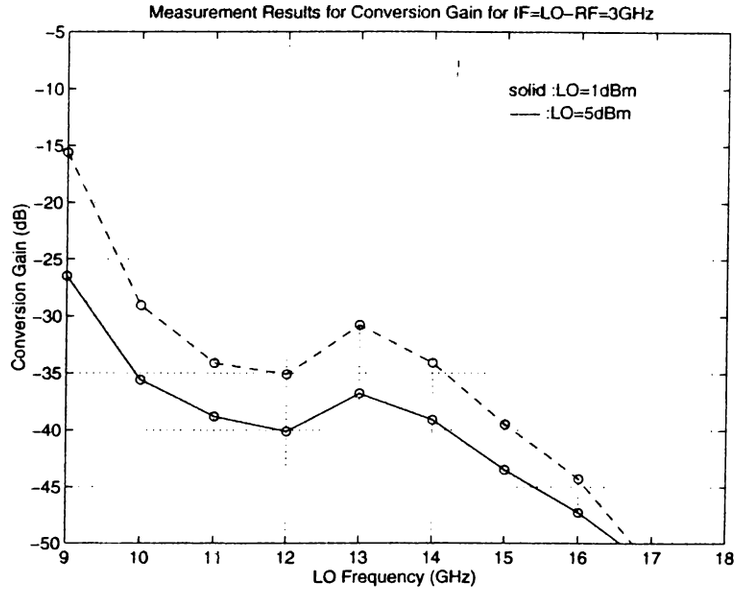



Figure 5.16: The Conversion Gain Measurement Results at IF=3GHz

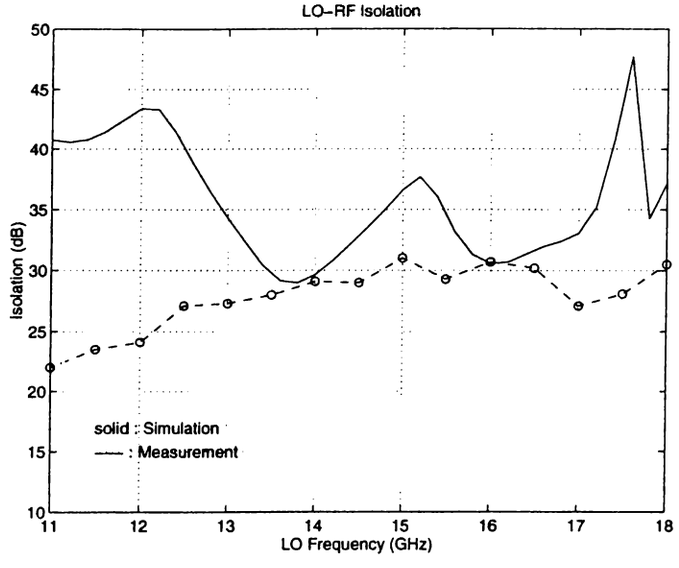



Figure 5.17: The LO-RF Isolation

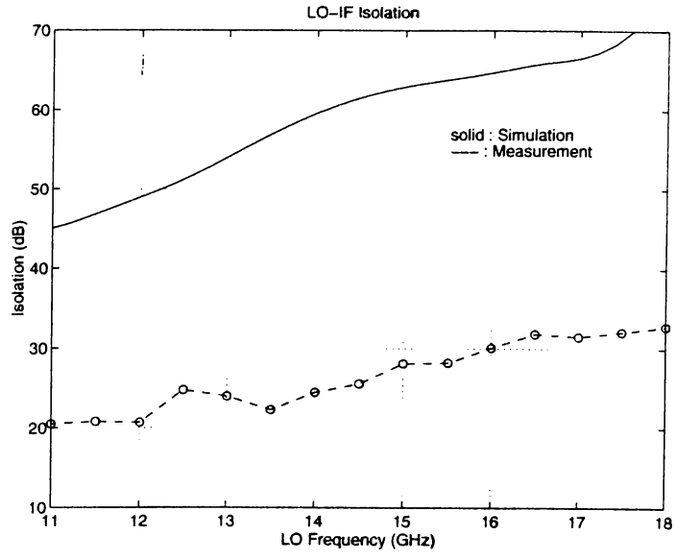



Figure 5.18: The LO-IF Isolation

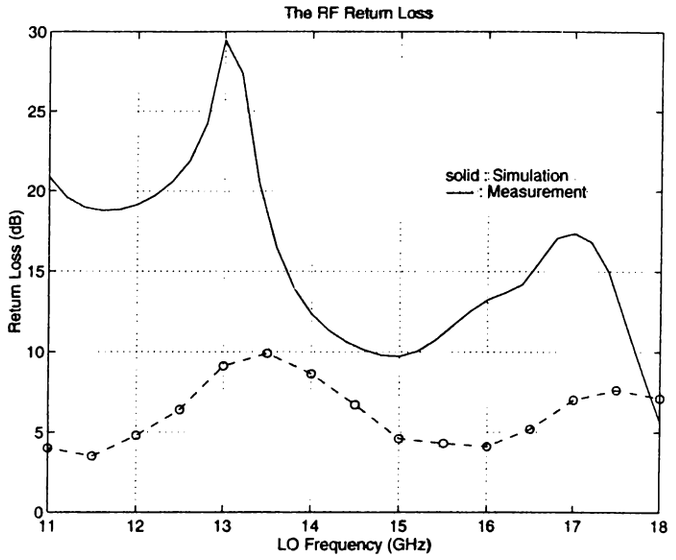



Figure 5.19: The Return Loss from RF port

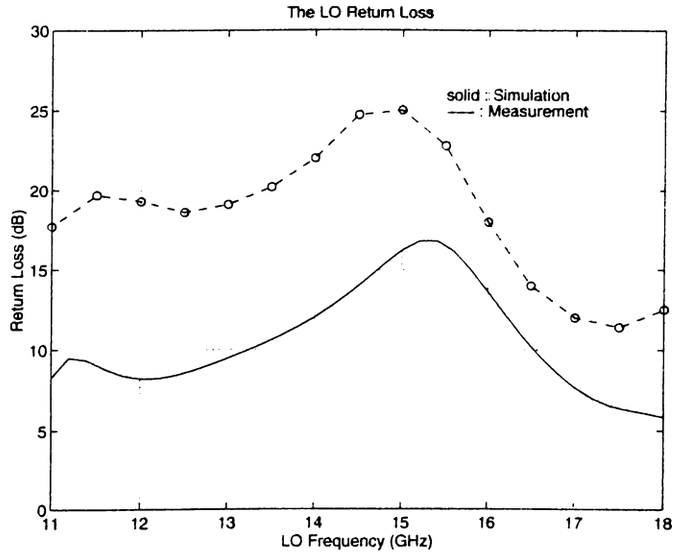



Figure 5.20: The Return Loss from LO port

keeping the SBM topology, one may choose to use an "active balun" instead of "pre-amplifier + passive balun" combination. If such an structure is found with low power consumption, then the total area of the chip may be reduced further. Another improvement to this design will be the addition of an IF amplifier which may eliminate the need for LPF and increase the conversion gain considerably. The implementation of such an IF amplifier is much easier compared to the broadband, relatively large signal pre-amplifier. It is also possible to use the "active balun + IF amplifier" combination effectively to obtain wider LO frequency range. There is still another possibility that may yield far better performance and in smaller area. In Chapter 4 a FFM with a novel balun topology was successfully designed. It can be improved to satisfy the requirements given in Table 5.1.

# Chapter 6

# The Improved Floating FET Mixer

A new MMIC mixer is presented which exhibits low conversion loss at low LO drive power levels and low DC power consumption. This is achieved for LO and RF signals in the 8 GHz to 18 GHz frequency range with an IF bandwidth from 2 GHz to 4 GHz. This new design outperforms the previous single balanced mixer (in Chapter 5) in all fields of comparison except the isolation and IF bandwidth criteria.

## 6.1 Introduction

The desired parameters for the design presented in the Table 5.1 besides the possible ways of enhancing the performance of the design. The use of an active balun structures were investigated. Unfortunately, their performance were not good enough to replace our pre-amplifier-balun structure. (Their gain are less than expected and the DC power consumption intolerably high.)

In this chapter an improved version of (The Floating FET mixer) FFM

topology with pre-amplifier is used. Although all the problems with the topology has not been solved significant improvements have been obtained in LO-RF frequency bandwidths.

The main operating principle of FFM topology has already presented in Chapter 4. By this topology LO power is used much efficiently, hence decreasing the strain on the LO pre-amplifier. Although self-biasing schemes were employed in mixer sections of the previous designs, here no self-biasing is used.

In this design, the main concern is neither to achieve the isolation goals nor to satisfy the power consumption requirements; instead, the design goal was to attain the minimum conversion loss in the broadest frequency band using minimum DC power. This design will show us the attainable limits of a mixer centered on the idea of using resistive mode FET(s).

## 6.2 Design

The overall design consists of two parts as seen in Fig. 6.1. The removal of the balun after the amplifier section has loosened the gain requirement approximately 3dB. Following this freedom, the bandwidth is increased to at least 3 GHz.

In the mixer part, the bandwidth of the compensated balun is increased in order to utilize the bandwidth gained in the amplifier section. The MESFET used in this part has 300 $\mu$m total gate periphery.

### 6.2.1 LO Pre-amplifier

The pre-amplifier is very similar to one given in the SBM design. The improvements can be listed as :

- The bandwidth is increased from 7 GHz to 10 GHz.

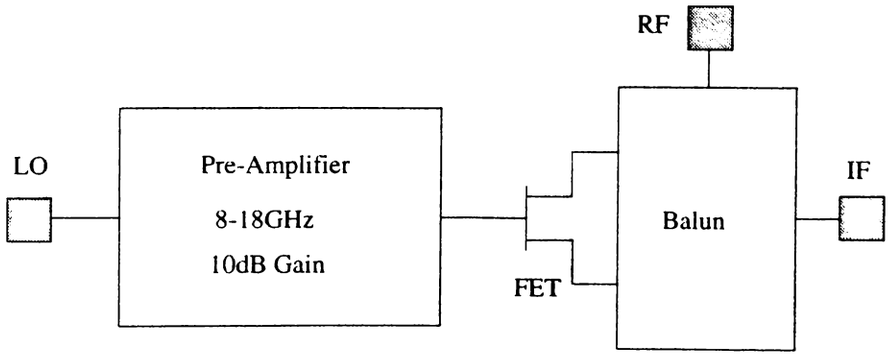



Figure 6.1: The Overall Mixer Topology

- 2×100 FETs are biased at 0.2 $I_{dss}$, which means maximum 8mA current for each stage. Total of 16mA current at 12V, is important improvement over the first design which require 25mA of bias current.

The bias circuitry is changed slightly. Since one can not use a buffer transistor at the bias circuitry for such an small current values, resistors are used for this purpose. The stages are self-biased as before. The final circuit of the pre-amplifier is given in Fig.6.5.

### 6.2.2 Balun

In this design the balun is used on the RF side instead of LO side. Beside this role change, the type of the balun is changed too. Here an improved version of compensated balun is used. The amplitude and phase balances of the balun are extended over 10 GHz. In Fig. 6.2 the final version of balun is given. The coupled transmission lines (CPL) are symmetric, their widths are w=5 $\mu$m and their spacing is s=5 $\mu$m and their length is 400 $\mu$m.

Its small area makes such an structure very attractive, but it has a major disadvantage: Center Tab Problem. To extract IF signal, in this case, poses an important problem which result in disturbance of the balance. The electromagnetic simulation of folded symmetric coupled lines (by EM from SONNET [43]) is used in linear simulation of Microwave Harmonica (MH) [10]. The results without IF extraction are shown in Fig.6.3 and Fig.6.4.

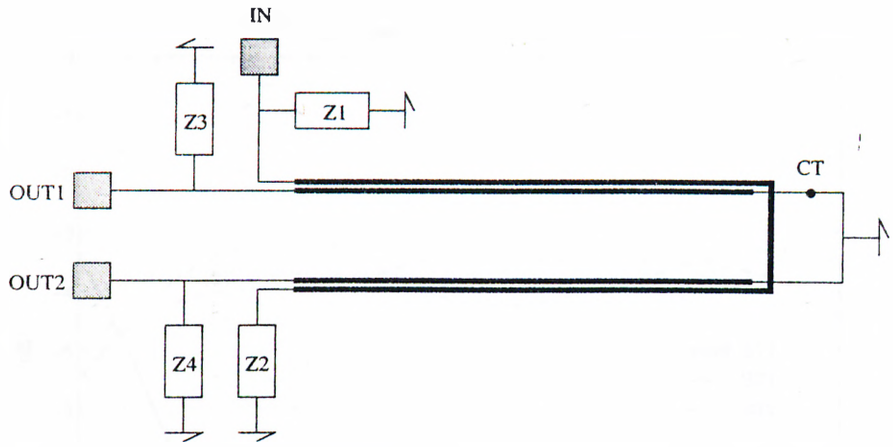



Figure 6.2: The Compensated Balun

In the design the IF signal is extracted over the shunt capacitance (at the point of CT in Fig 6.2). No efficient way of decreasing of the unbalance introduced by this capacitance and port could be found. Therefore both RF and LO signals can leak to the IF port. But such a frequency-separated leakage from the IF port can always be prevented using a low pass filter at the expense of 1.5dB conversion loss.

## 6.3 Simulations and Measurements

In the simulations, both linear and nonlinear techniques are used. The pre-amplifier (in Fig. 6.5) is simulated using the small signal models of the transistors, although for more reliable results a large signal simulation is required. We may attempt the similar kind of justification as given in the previous designs.

The folded CPLs are simulated using EM, then the data file is inserted in nonlinear simulation file of MH. A 4×75 FET with its Modified Materka active model is used in the FFM block. (Fig. 6.6)

Despite the additional -1V power supply, 12V and 15mA power requirements are satisfied. The bias current is in the range of 14-15.5mA in the measured samples. The amplifier is not sensitive to the applied DC voltage, at

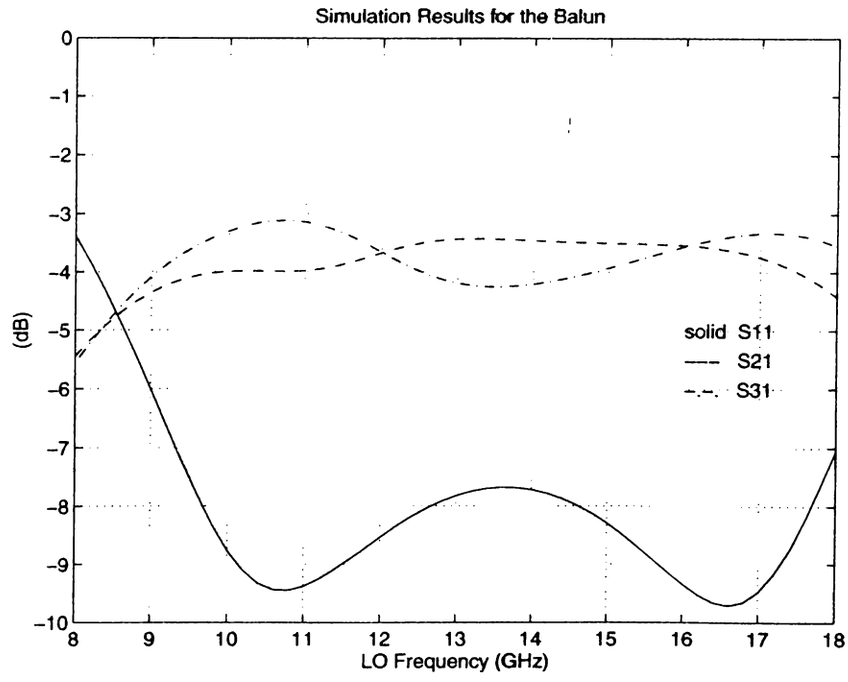



Figure 6.3: The Reflection and Transfer Characteristics of the Balun

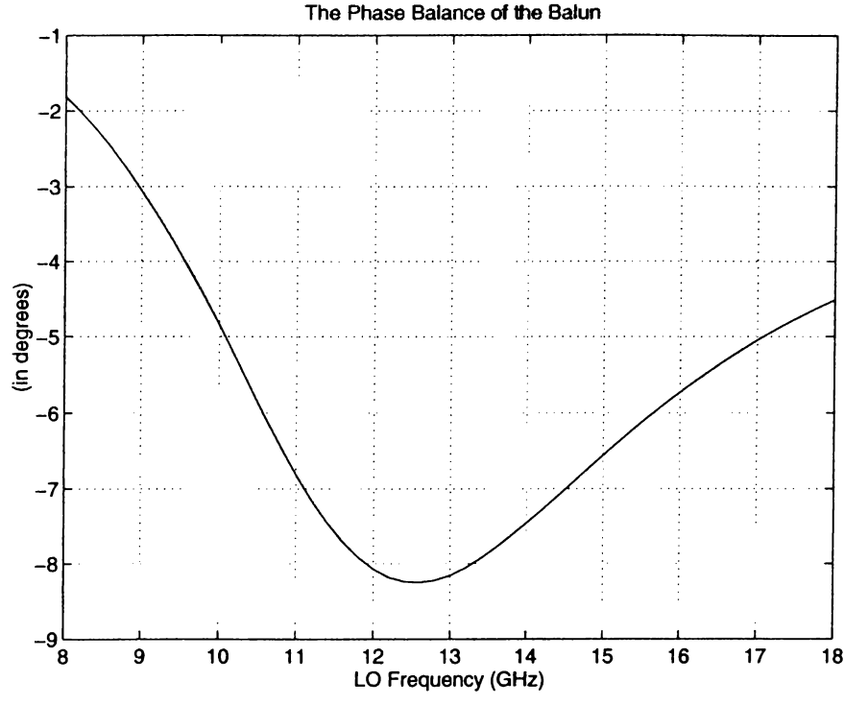



Figure 6.4: The Phase Balance of the Balun

10V its performances do not change. Since the additional source is connected to the gate of the FET, it does not supply any current and the only power consumption takes place in the amplifier.

The measurement results are as expected. In the previous FFM case (chapter 4), there have been similar discrepancies between measurement and simulation. The conversion gain (Fig. 6.7, 6.8), turns out to be approximately 5dB less then the corresponding simulation results. The difference increases while the LO frequency is increasing, because at the high end the performance of MESFETs decreases considerably. The dependence of conversion gain to the input LO power is as expected small (ie 4dBm increase in input LO power, does not raise the conversion gain curve more than 2dB.).

The isolations in Figures 6.11, 6.12 are measured to be better than the simulations. The reflections in Figures 6.9, 6.10 also turn out to be better in the measurement. As a results this improved FFM chip demonstrates better responses in a smaller area for less DC power consumption.

The layout was drawn using Cadence 4.3 (Fig. C.4). A grounding problem raised while drawing the layout of the chip. The length of the transmission line between ground and the CPL pair which is connected to the source of the mixing FET posed significant disturbance to the overall response of the circuit. (Fig. 6.6) That is why this point is close to the ground. In this configuration it can not be done shorter than given here. (Fig. C.4 in App.C)

## 6.4 Discussion and Future Work

A new MMIC Mixer is designed which occupies the area of 1.57mm×0.99mm. In fact, the mixer occupies an area of 1.31mm×0.99mm, but since the minimum cost of a chip corresponds to the area of 1.5mm$^2$, some balun test parts were added to the layout which made the total area a little larger than that minimum area. (At the left side of Fig. C.4) The added parts, though do not make up a balun, one can study the effects of CPLs and compare it with the

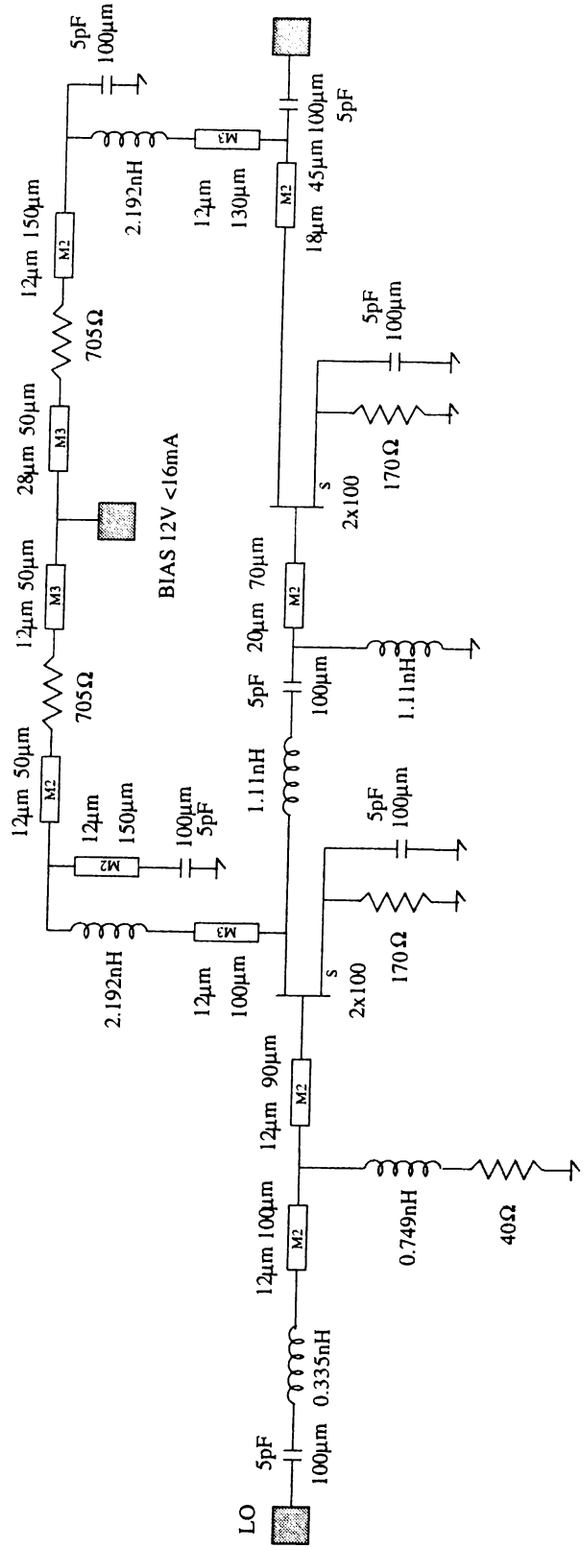



Figure 6.5: The Pre-amplifier

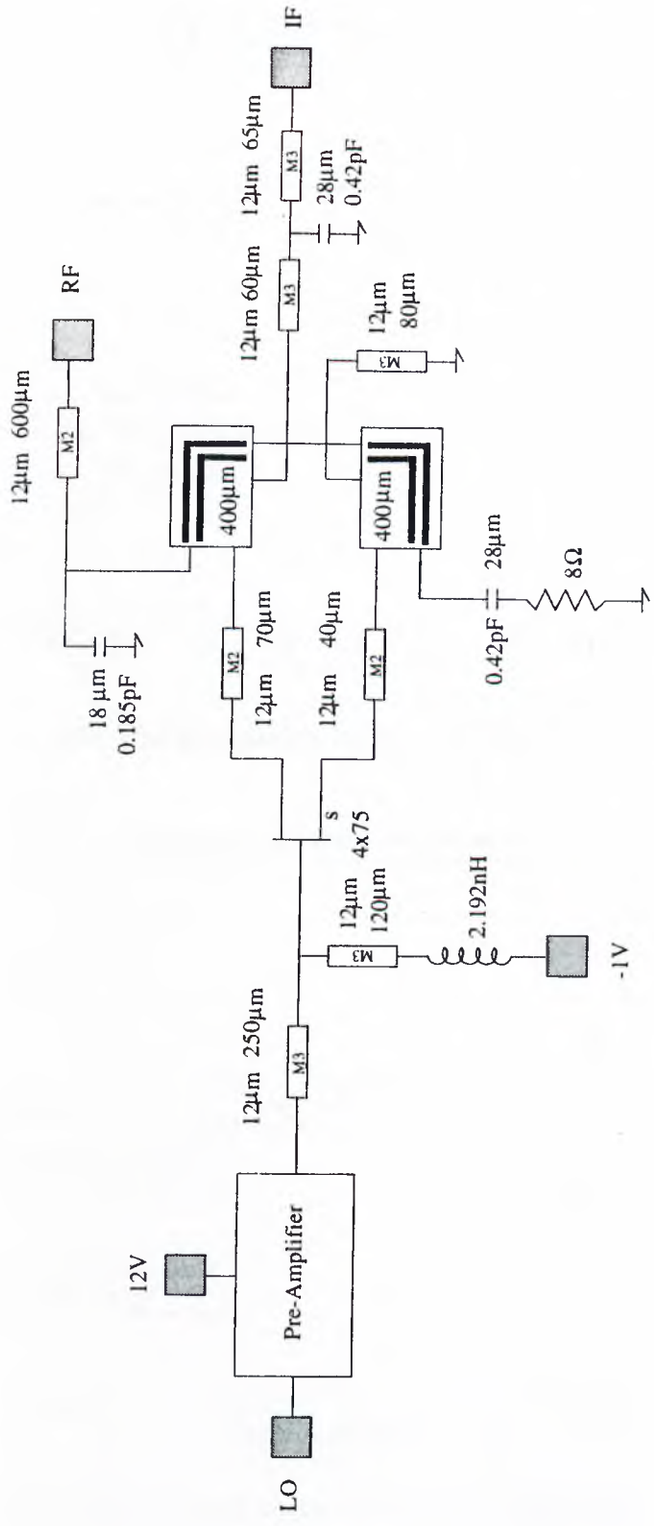



Figure 6.6: The Overall Circuit of the Mixer

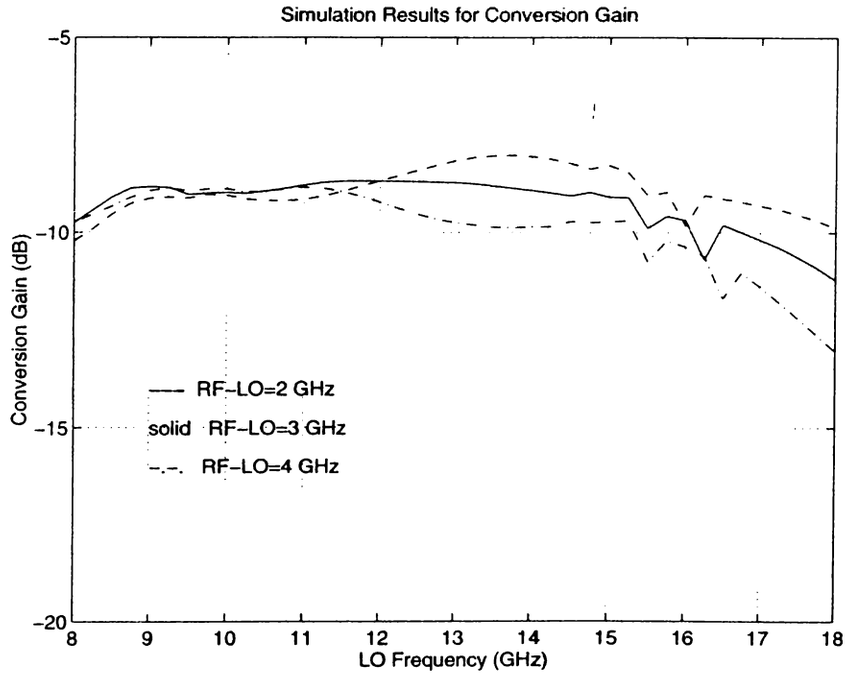



Figure 6.7: The Simulation Results for Conversion Gain

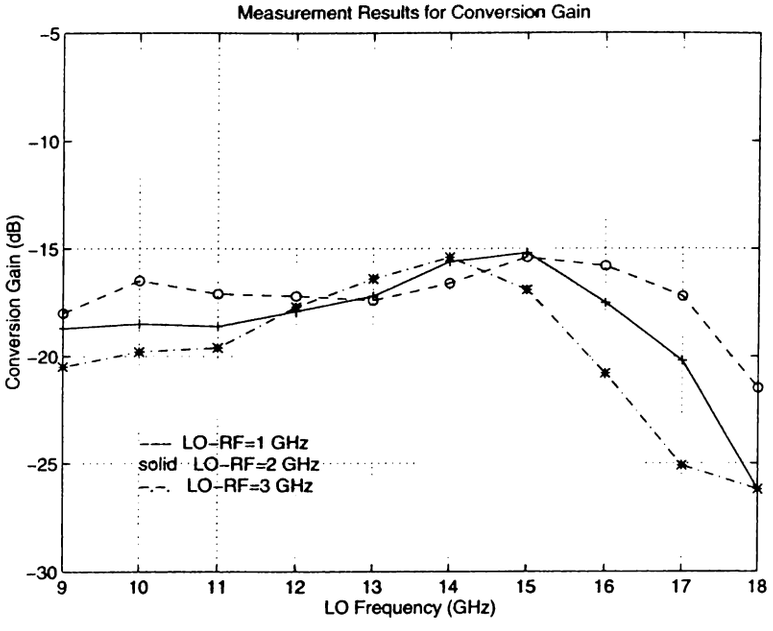



Figure 6.8: The Measurement Results for Conversion Gain

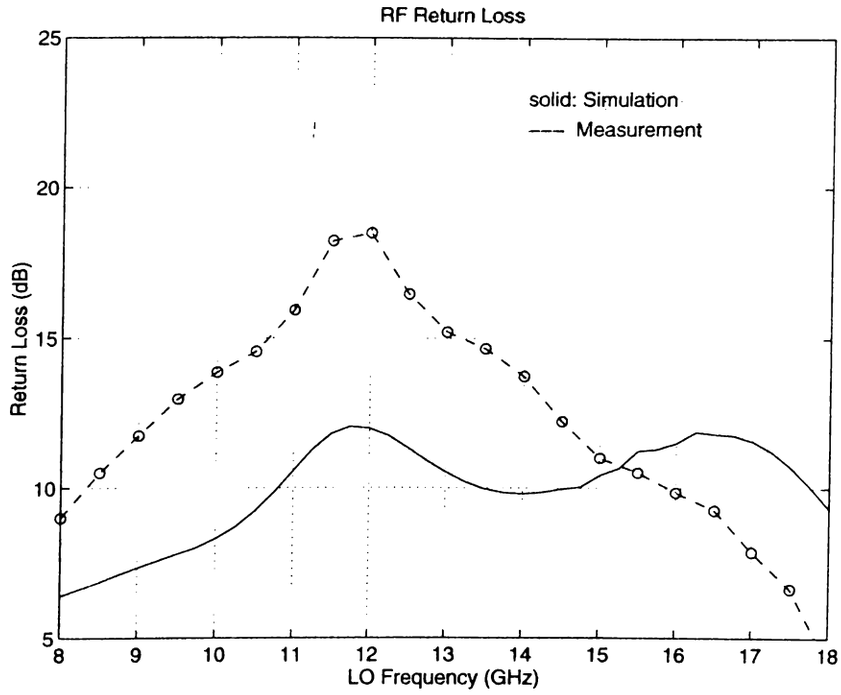



Figure 6.9: The Return Loss from RF port

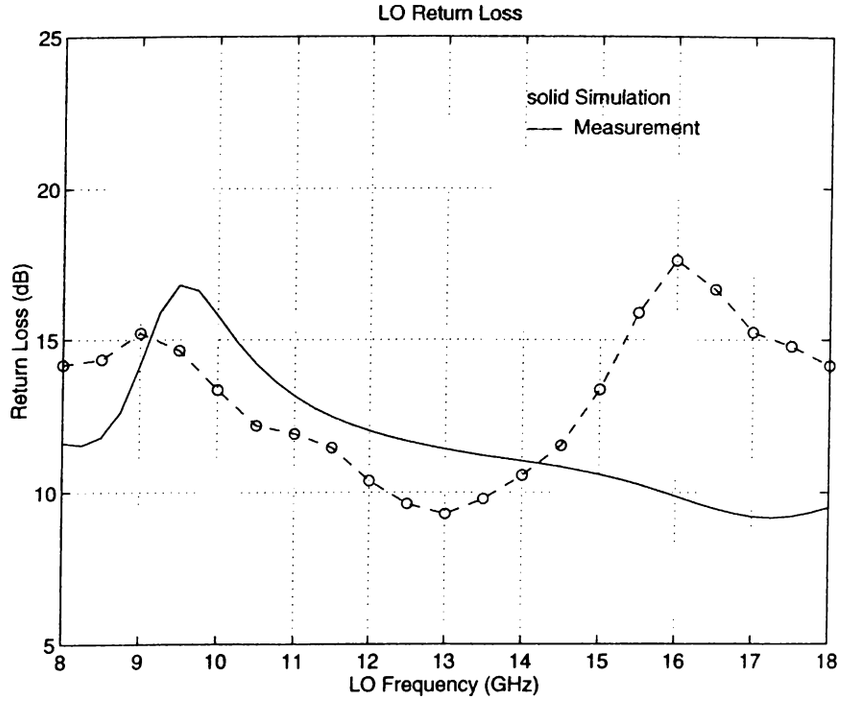



Figure 6.10: The Return Loss from LO port

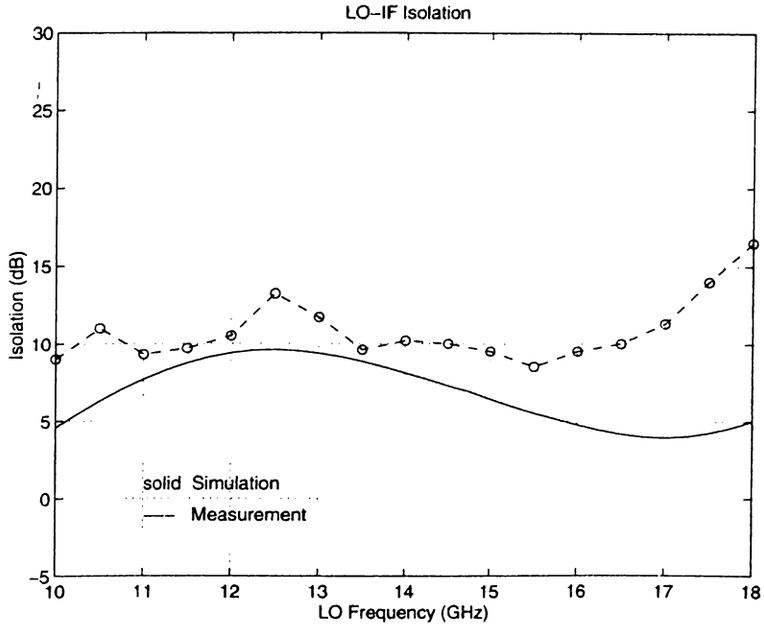



Figure 6.11: The LO-IF Isolation

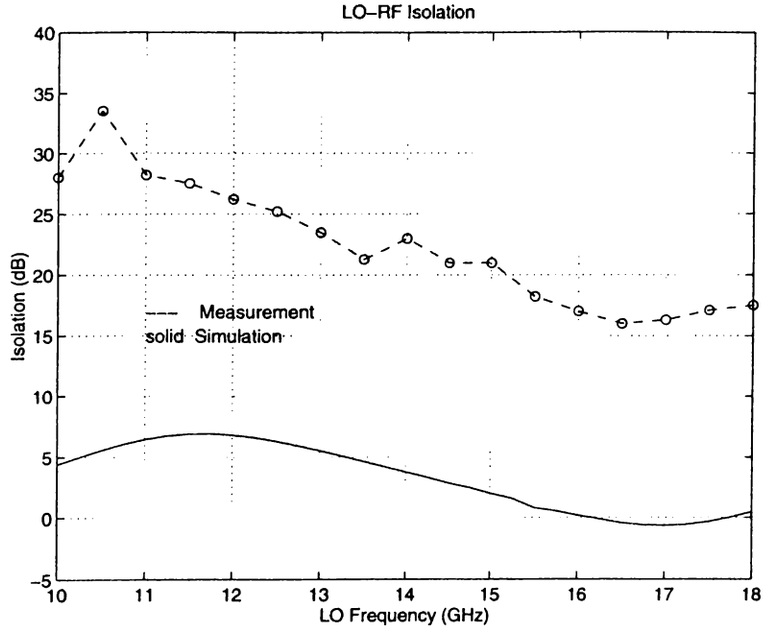



Figure 6.12: The LO-RF Isolation

| | Simulation | Measurement |
|---|---|---|
| Conversion Gain | >-11dB | >-17dB(@1GHz) >-20dB(@3GHz) |
| LO-IF Isolation | >0dB | >12dB |
| LO-RF Isolation | >0dB | >18dB |
| RF Return Loss | >8dB | >9dB |
| LO Return Loss | >6dB | >9dB |
| Power Supply @12V | <16mA | 14mA-15.5mA |

Table 6.1: The Specifications of the Improved FFM Chip

simulations, hence it can be seen as a preliminary work for future balun implementations.The design was submitted to the postponed February 1996 run of GMMT under EUROPRACTICE project. The fabricated chips were received in August 1996.

For LO=1dBm, RF=-5dBm, IF=3 GHz, (12V and -1V) power supplies and 16mA maximum bias current, in 8 GHz-18 GHz frequency range the following specifications given in Table 6.1 are obtained.

There is still room for improvements in this design. They can be classified under two headings: Isolation improvements and by-passing the additional voltage supply.

- A new extraction method for IF signal can be applied so that the balance of the balun is not much effected.
- A new balun structure with a more stable center tap can yield better isolation structures, but the area of such an alternative balun will be the additional cost.
- One may get around the additional -1V DC supply problem, by using 1V as a ground, then the bias circuitry of the pre-amplifier should be rearranged for the remaining 11V. (The response does not change if the bias voltage decreased from 12V to 10V.)

# Chapter 7

# CONCLUSION

There are many different specifications for a mixer design, some of them may carry more importance than the others under certain conditions. Therefore some of the designs can be treated as application specific. While going from the low frequencies to higher ones the use of nonlinear elements and technology is changing extremely, hence the difficulty and the cost. Here our main goal is to obtain a cost-effective and reliable mixers operating in the frequency range from 10 GHz to 20 GHz. With the introduction of new balun and mixer topologies, important alternative designs were added to the already-well-developed mixer-treasury.

Four MMIC mixers were designed in this work. Except the first one, all of the mixers employ FETs in resistive mode. By developing a novel balun topology, the area of the mixers reduced considerably, without introducing any performance degradation. In the FFM design and its improved version a single FET is used whereas in the SBM design two resistive mode FETs are employed in a modified single balanced configuration. In the unsuccessful first design, double balanced mixer configuration is used with a diode quad.

The difficulty of mixer design mainly stems from the use of nonlinear analysis techniques. Both the nonlinear characterization of devices and the nonlinear optimization of the overall circuit should be improved in order to obtain much

successful designs. Especially, currently available nonlinear FET models can not simulate correctly the resistive mode FETs. New models should be developed which give much realistic intermodulation simulation results without increasing the computational cost. If an electromagnetic simulator (and/or optimizer) is integrated into a harmonic balance optimizer, the burden of designing mixer with a passive balun structure will be reduced considerably.

From the viewpoint of switching (modulation) theory of mixer operation, the more effective the switching, better the mixing. The power needed in the switching can be minimized by using a suitable biasing and by optimizing the device architecture. I believe that the fundamental performance increase in mixers could be achieved if better switching devices are designed and fabricated.

# APPENDIX A

# The Double-Balanced Mixer

In most receiver applications the IF is usually much lower and sufficiently separated from the RF and LO, and so isolation can be obtained simply by using a low pass filter at the output. For the applications where the IF and RF bands are very close and possibly overlap, it is not possible to filter out the unwanted band. Balanced mixers are usually used to provide the necessary isolation.

A double-balanced mixer was designed using the GMMT[1] rules. A similar combination is proposed by Brinlee et al. [24]. For 11dBm of LO power, in the 8-12 GHz frequency band the conversion loss is better than 7dB. The mixer designed here uses a planar balun developed along the lines of Marchand [24]. It is formed by edge-coupled microstrip lines and MIM capacitors. This simultaneously adjusts the impedance matching between the diode ring and 50-ohm input, increases the coupling between the lines, and compensates the phase velocities between the even and odd modes. The diodes were formed by a 4×50 MESFET with its source and drain connected together and an IF signal diplexed off from the RF side. The area of the chip is 1.8×0.92 $mm^2$. It is possible to reduce the area by folding the branches of the balun. The layout is given in Fig.C.1 (in App.C). The schematic of the design and the balun are illustrated in Fig.A.1 and A.2.

[1]GEC-Marconi Materials Technology

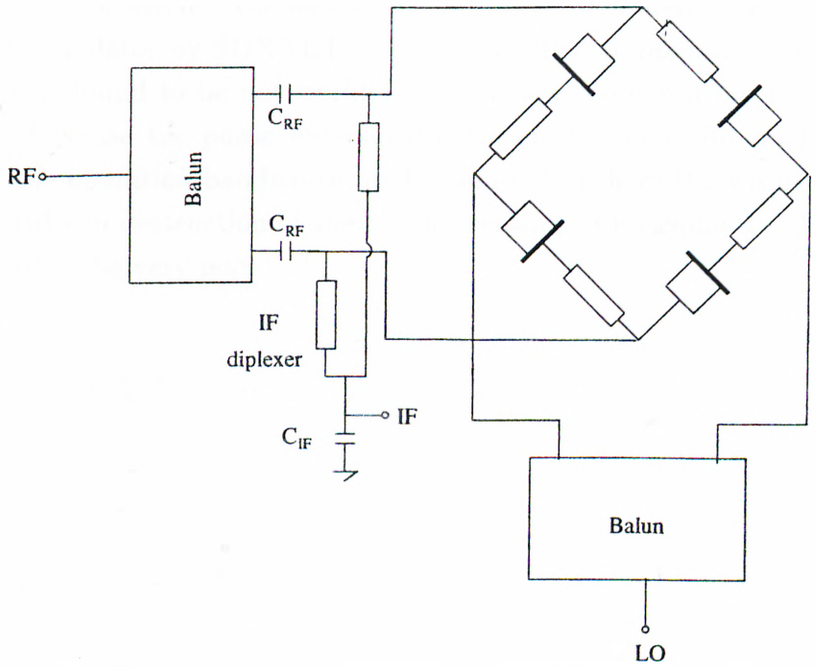



Figure A.1: The schematic of the double balanced mixer

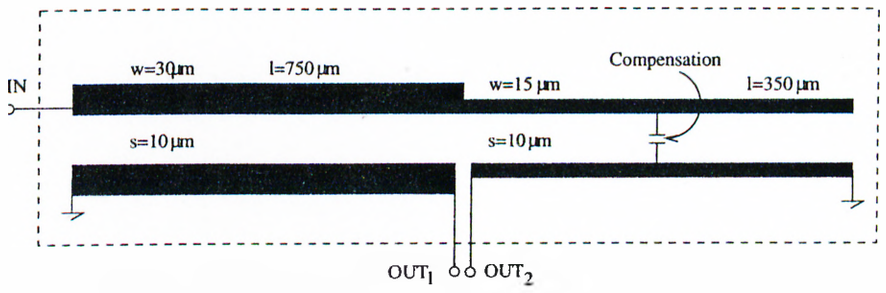



Figure A.2: The Marchand balun used in the DBM design

Unfortunately the measurements did not turn out as expected. The conversion loss is measured to be at least 10dB larger than the expected value. After seeing this inconsistency the balun structure is re-simulated using the electromagnetic simulator by SONNET [43]. The applied compensation method in the balun is found to be not working. The phase compensation is applied in order to decrease the phase unbalance between even and odd modes, hence increase the operation bandwidth of the balun. But, here the wrong compensation results in destruction of the balun operation. Consequently, the mixing is observed to be very poor.

# APPENDIX B

# Nonlinear MESFET Models

The following intrinsic models are supported by Microwave Harmonica [10]:

- Modified Materka-Kacprzak Model
- Curtice Quadratic Model
- Curtice Cubic Model
- Raytheon (Statz) Model
- Triquint (TOM) Model

The topology prefered in the design is the first one, tough many times inadequate for our purposes. Extrinsic model for all intrinsic models is shown in Fig.B.1.

### B.0.1 Materka-Kacprzak Intrinsic Model

The topology is given in Fig.B.2. Some of the Materka parameters are listed here. But the device equations are not reproduced, they are available in [10].

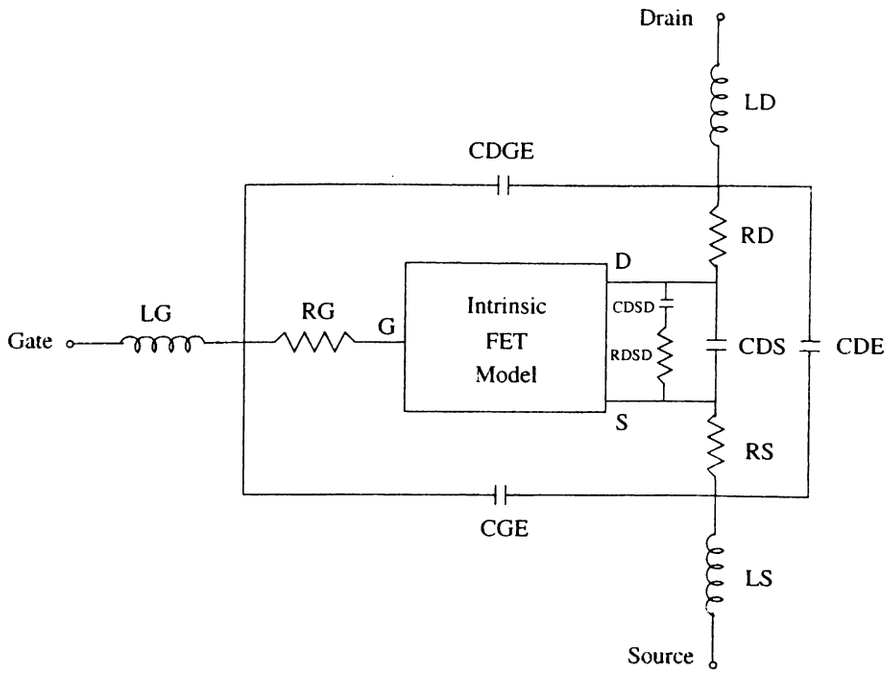



Figure B.1: Extrinsic Model

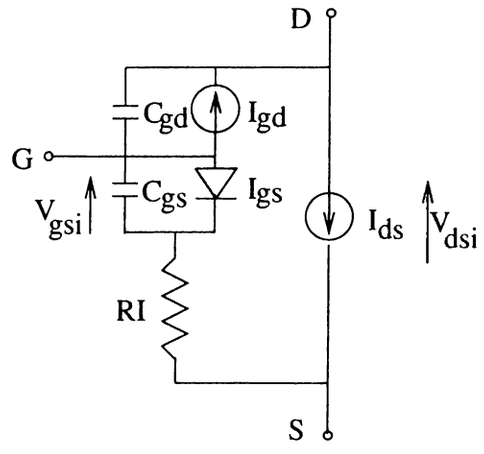



Figure B.2: Materka Intrinsic Model

| Key | Description |
|---|---|
| $I_{dss}$ | Drain saturation current for $V_{gs} = 0$ |
| $V_{p0}$ | Pinch-off voltage for $V_{ds}$ |
| $Gama\ (\gamma)$ | Voltage solpe parameter of pich-off voltage |
| $E$ | Constant partof power law parameter |
| $K_E$ | Dependence of power law on $V_{gs}$ |
| $K_G$ | Drain dependence on $V_{gs}$ in the linear region |
| $K_R$ | Slope factor of intrinsic channel resistance |
| $K_I$ | Slope parameter of gate-source capacitance |
| $K_F$ | Slope parameter of gate-darin capacitance |
| $S_S$ | Slope of the drain characteristics |
| $S_L$ | Slope of the $V_{gs} = 0$ drain characteristics in the linear region |
| $C_{I0}$ | Gate-source schottky barrier capacitance for $V_{gs} = 0$ |
| $C_{F0}$ | Gate-darin feedback capacitance for $V_{gd} = 0$ |
| $R_{I0}$ | Intrinsic channel resistance for $V_{gs} = 0$ |
| $I_{g0}$ | Saturation current of gate-source Schottky barrier |
| $AFAG$ | Slope factor of gate conduction current |
| $C_{IS}$ | Constant parasitic component of gate-source capacitance |
| $T\ (\tau)$ | Channel transit time |
| $AFAB$ | Slope factor of breakdown current |
| $V_{BC}$ | Breakdown voltage |

GEC-Marconi asserts that in all cases the models give excellent fits to the DC I/V curves, but, because of the inherent limitations of the commercial simulators the gate and drain capacitances are only correct above the knee of the I/V characteristics. The parameters for $4 \times 75\mu m$ GEC-F20 MESFETs is supplied in TableB.1. Simulations for different device geometries can be achieved by changing the parasitic elements in accordance with the table given for the scaleable FET model [44].

| Extrinsic Parameters | | |
|---|---|---|
| $R_G = 1.2\Omega$ | $R_S = 2.4\Omega$ | $R_D = 3.25\Omega$ |
| $L_G = 0.02nH$ | $L_D = 0.007nH$ | $L_D = 0.015nH$ |
| $C_{DS} = 0.058pF$ | $RDSD = 425$ | |
| Modified Materka Parameters | | |
| $I_{dss} = 50.75mA$ | $V_{p0} = -1.62$ | $\gamma = -0.106$ |
| E=1.825 | $C_{10} = 0.36pF$ | $\tau = 2.8pS$ |
| $C_{F0} = 0.03pF$ | $K_E = -0.173$ | $S_L = 124mS$ |
| $K_G = -0.09$ | $S_S = 9.22mS$ | $R_{10} = 2.67$ |
| $K_R = 0.527$ | $I_{g0} = 1.42x10^{-10}A$ | |

Table B.1: The Modified Materka Model of $4 \times 75$ MESFET

# APPENDIX C

# Layouts

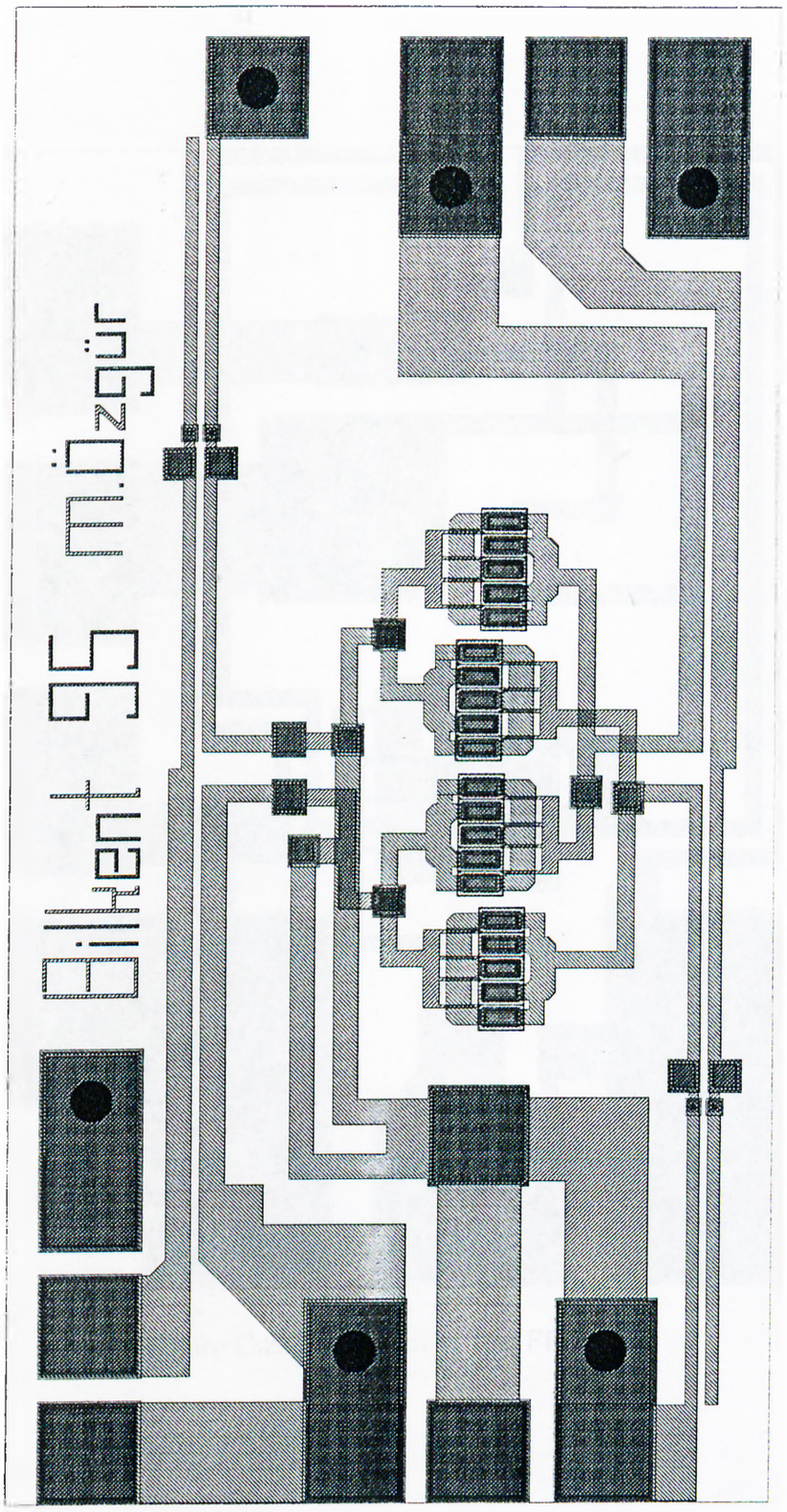



Figure C.1: The layout of the double-balanced mixer chip.

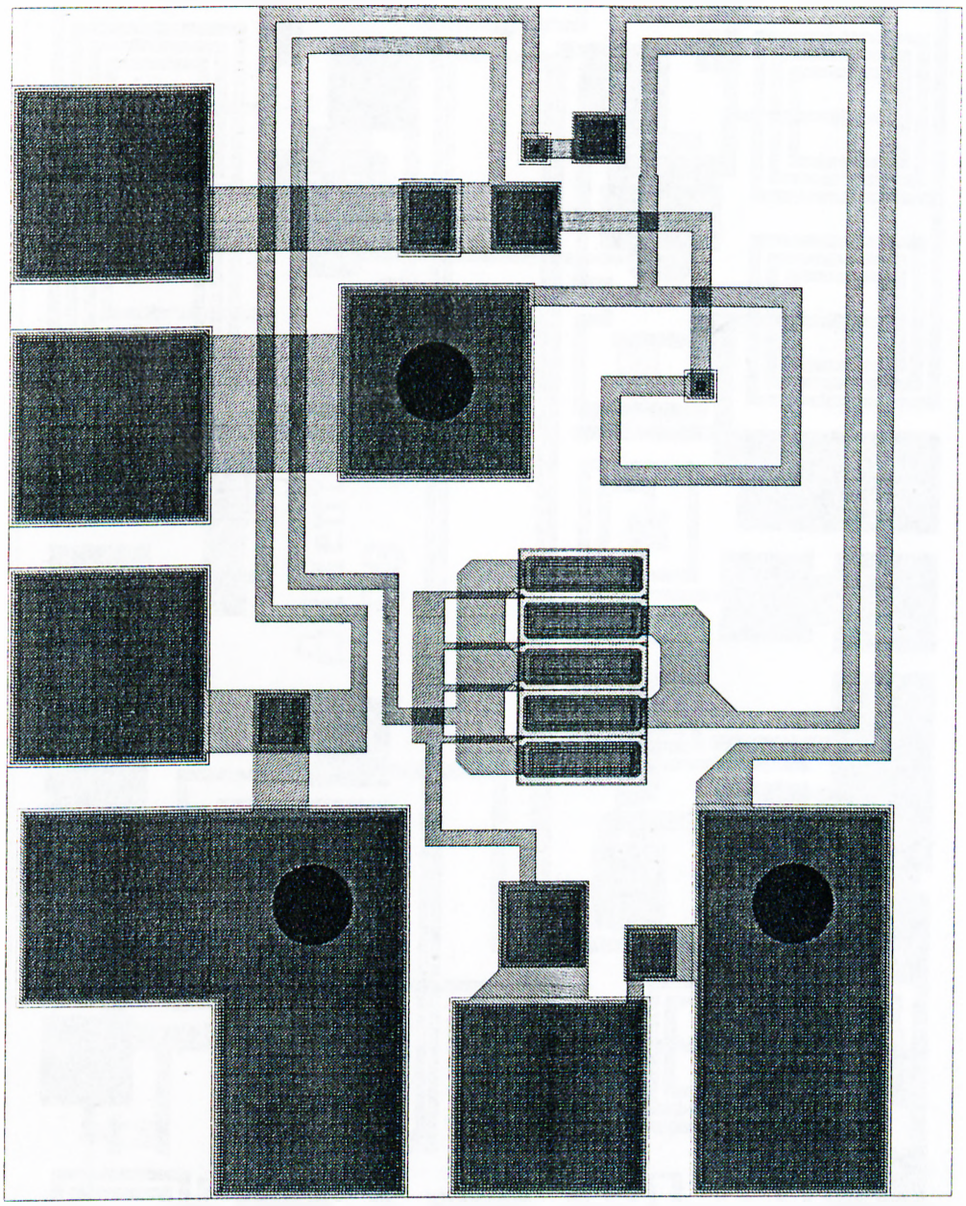


Figure C.2: The layout of the FFM chip.

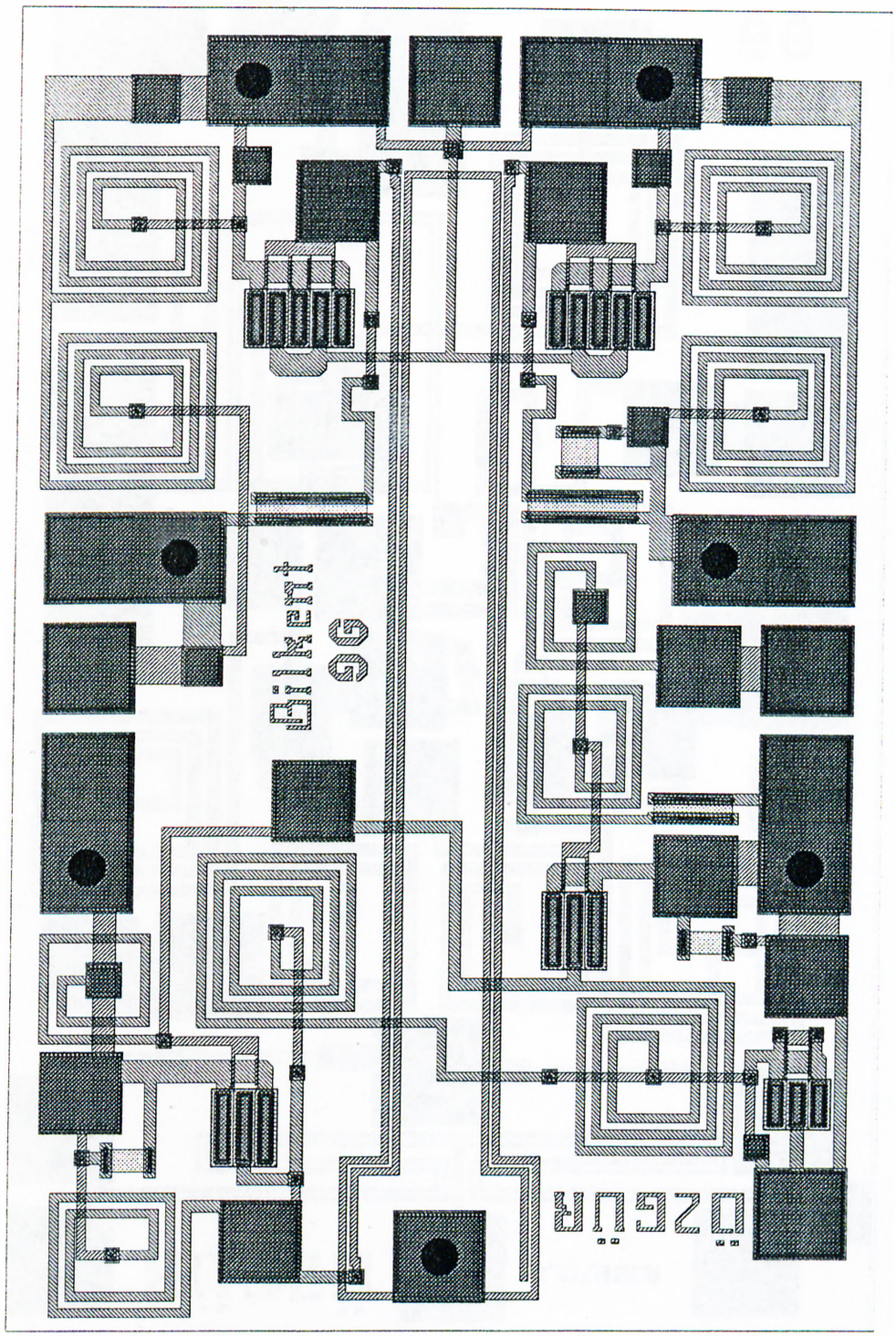


Figure C.3: The layout of the SBM chip

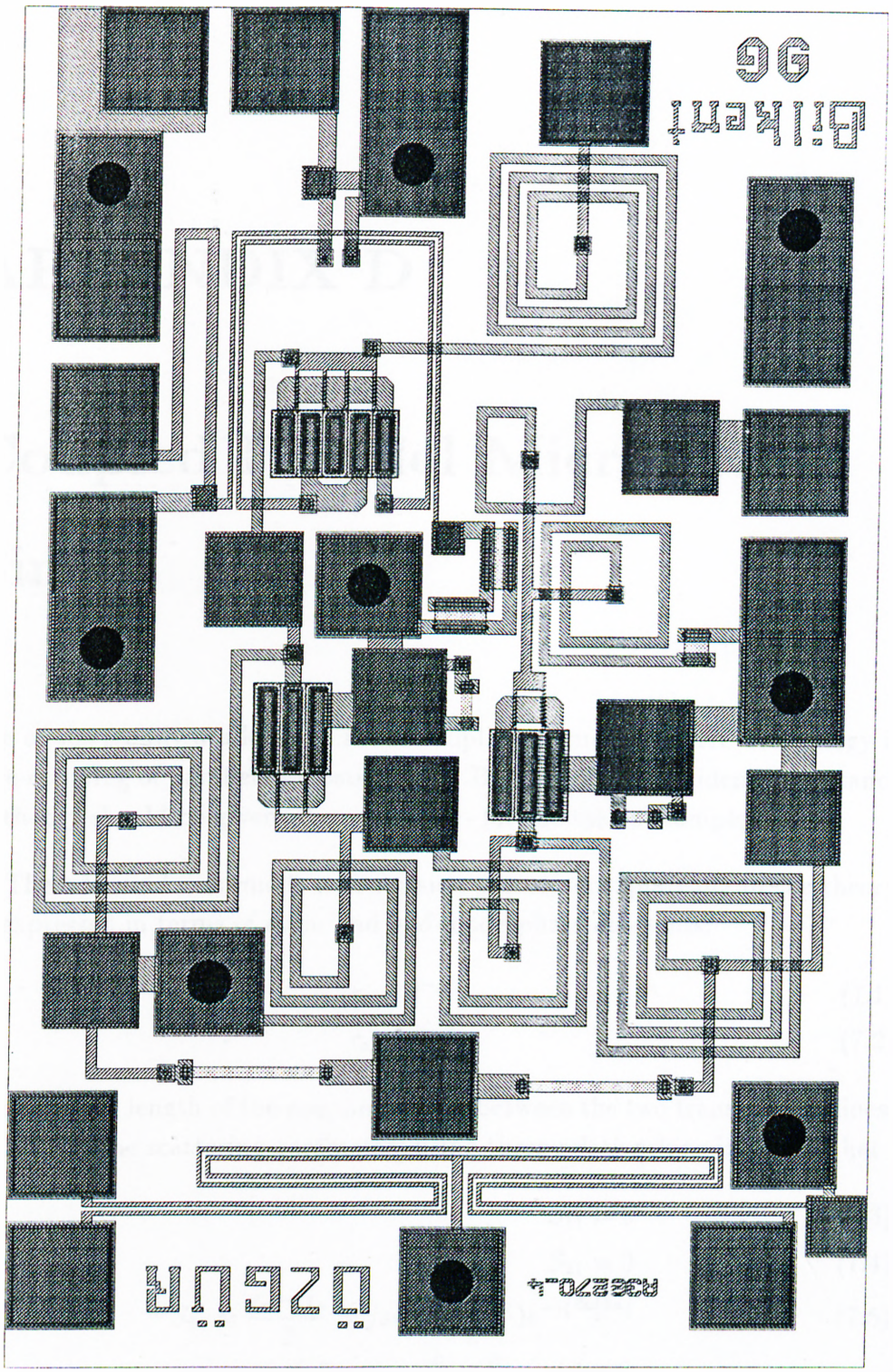


Figure C.4: The layout of the NFFM chip

# APPENDIX D

# Coupled Parallel Microstrip Lines

One of the readily available means of coupling in current MMIC technology is edge-coupling of parallel microstrip lines. Because of their evident importance its theory should be given -though briefly- for the sake of completeness.

The odd- and even-mode transmission parameters appearing in the theory be expressed in terms of even- and odd-mode phase constants:

$$\tau_e = e^{-j\theta_e} \tag{7.1}$$

$$\tau_o = e^{-j\theta_o} \tag{7.2}$$

where l is the length of the coupling region between the two transmission lines. Evaluating the scattering parameters using these relationships indicates that

$$S_{11} = 0 \tag{7.3}$$

$$S_{21} = 0 \tag{7.4}$$

$$S_{31} = \frac{\tau_e - \tau_o}{2} = jsin(\frac{\theta_e - \theta_o}{2})e^{-j(\frac{\theta_e+\theta_o}{2})} \tag{7.5}$$

$$S_{41} = \frac{\tau_e + \tau_o}{2} = cos(\frac{\theta_e - \theta_o}{2})e^{-j(\frac{\theta_e+\theta_o}{2})} \tag{7.6}$$

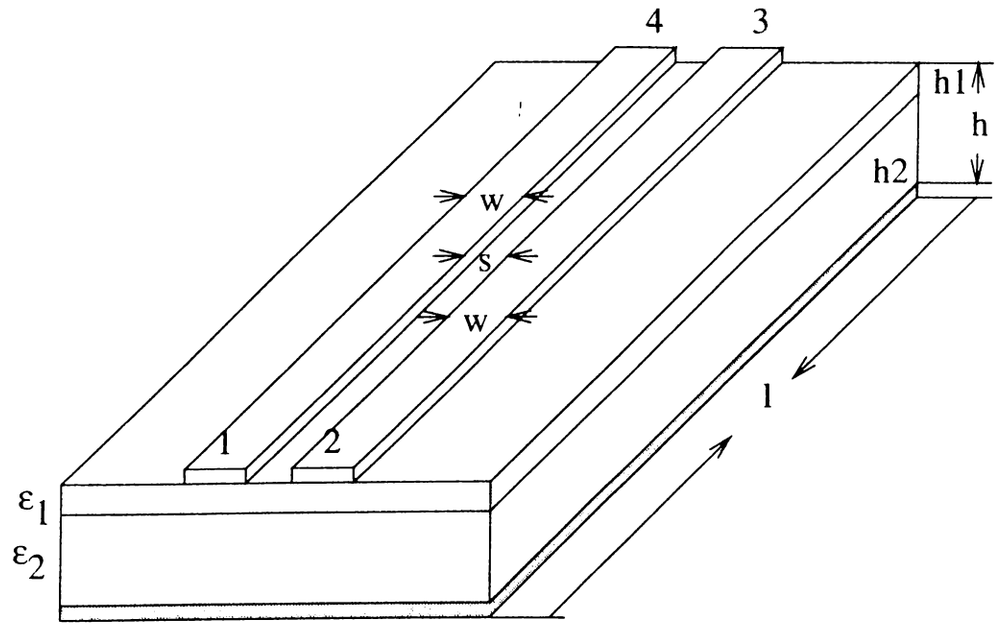



Figure D.1: Schematic diagram of coupled microstrip lines

The scattering matrix is given as

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{41} \\ S_{21} & S_{11} & S_{41} & S_{31} \\ S_{31} & S_{41} & S_{11} & S_{14} \\ S_{41} & S_{42} & S_{31} & S_{11} \end{bmatrix} \tag{7.7}$$

Making use of the bilinear transformation between the scattering and the impedance matrices.

$$Z = (I + S)(I - S)^{-1} \tag{7.8}$$

Evaluating the open-circuit parameters indicates that the impedance matrix is defined by

$$Z = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{41} \\ Z_{21} & Z_{11} & Z_{41} & Z_{31} \\ Z_{31} & Z_{41} & Z_{11} & Z_{14} \\ Z_{41} & Z_{42} & Z_{31} & Z_{11} \end{bmatrix} \tag{7.9}$$

where for

$$A = \frac{Z_e + Z_o}{2} \tag{7.10}$$

$$B = \frac{Z_e - Z_o}{2} \tag{7.11}$$

$$Z_{11} = -jA\cot(\theta) \tag{7.12}$$

$$Z_{12} = -jB\cot(\theta) \tag{7.13}$$

$$Z_{13} = -jA\operatorname{cosec}(\theta) \tag{7.14}$$

$$Z_{14} = -jB\operatorname{cosec}(\theta) \tag{7.15}$$

# REFERENCES


[1] G.D.Vendelin, A.M.Pavio, U.L. Rhode . *Microwave Circuit Design using Linear and Nonlinear Techniques.* John Wiley & Sons, 1990.

[2] S.A. Maas . *Microwave Mixers.* Artech House, 1986.

[3] Edited by Yoshihiro Konishi . *Microwave Integrated Circuits.* Marcel Dekker, 1991.

[4] Inder Bahl, Prakash Bhartia . *Microwave Solid State Circuit Design.* John Wiley & Sons, 1988.

[5] Edited by Ravenger Goyal. *Monolithic Microwave Integrated Circuits: Technology & Design.* Artech House, 1989.

[6] C.C-Penalosa, C.S. Aitchison "Analysis and design of MESFET gate mixers," *IEEE Trans. on Microwave Theory Tech.*, vol. 35, pp. 643-651. July 1987.

[7] M.J. Rosario, J.C. Freire "Design technique for MESFET mixers for maximum conversion gain," *IEEE Trans. on Microwave Theory Tech.*. vol. 38, pp. 1972-1979, December 1990.

[8] A. Minakawa, T. Hirota "An extremely small 26GHz monolithic image-rejection mixer without DC power consumption," *IEEE Trans. on Microwave Theory Tech.*, vol. 41, pp. 1634-1637, September 1993.

[9] V.D. Hwang, T. Itoh "Quasi-optical HEMT and MESFET self-oscillating mixers," *IEEE Trans. on Microwave Theory Tech.*, vol. 36, pp. 1701-1705. December 1988.

[10] Super Compact Software. "Microwave Harmonica v4.5 reference manual,".

[11] A.H. Baree, I.D. Robertson "A new technique for obtaining high isolations in microwave mixers based on the concepts of distributed mixing and transversal filtering," in *IEEE MTT-S Digest*, pp. 209–212, 1995.

[12] W.Titus, Y.Tajima, R.A.Pucel, A.Morris "Distributed monolithic image rejection mixer," in *GaAs IC Symp. Tech. Digest.*, pp. 191–194, 1986.

[13] W.Titus, M.Miller "2-26GHz MMIC frequency converter," in *GaAs IC Symp. Tech. Digest.*, pp. 181–184, 1989.

[14] S.B. Cohn "Slot line on dielectric substrate," *IEEE Trans. on Microwave Theory Tech.*, vol. 17, pp. 768–778, October 1969.

[15] B. Schuppert "Microstrip/slotline transitions modelling and experimental investigation," *IEEE Trans. on Microwave Theory Tech.*, vol. 36, pp. 1272–1282, August 1988.

[16] N. Marchand "Transmission line conversion transformers," *Electronics*, vol. 17, pp. 142–145, December 1944.

[17] M.C.Tsai, M.J.Schindler, W.Struble, M.Ventresca, R.Binder "A compact wideband mixer," in *IEEE MTT-S Digest*, pp. 135–138, 1994.

[18] A.H. Baree, I.D. Robertson "Analysis and design of multi-octave MMIC active baluns using a distributed amplifier gate line termination technique," in *IEEE MTT-S Digest*, pp. 217–220, 1995.

[19] T.Chen, K.W.Chang, S.B.Bui, H.Wang, G.S.Dow, L.C.T.Liu, T.S. Lin, W.S.Titus "Broadband monolithic passive baluns and monolithic double-balanced mixer," *IEEE Trans. on Microwave Theory Tech.*, vol. 39, pp. 1980–1986, December 1991.

[20] J.H. Cloete "Graps of circuit elements for the marchand balun," *Microwave J.*, pp. 125–128, May 1981.

[21] Velimir Trifunovic, Branka Jocanovic "Review of printed marchand and double Y baluns: Characterics and applications," *IEEE Trans. on Microwave Theory Tech.*, vol. 42, pp. 1454–1462, August 1994.

[22] C.T.Tsai, K.C.Gupta "A generalized model for coupled lines and its applications to two-layer planar circuits," *IEEE Trans. on Microwave Theory Tech.*, vol. 40, pp. 2190–2198, December 1992.

[23] J. Eisenberg, J.Panelli, W, Ou "A new double-double balanced MMIC mixer structure," in *IEEE MTT-S Digest*, pp. 69–72, 1991.

[24] W.R.Brinlee, A.M.Pavio, and K.R.Varian "A novel planar double-balanced 6-18 GHz MMIC mixer," in *IEEE MTT-S Digest*, pp. 139 -142, 1994.

[25] Inder J. Bahl "Capacitively compensated high performance parallel coupled microstrip filters," in *IEEE MTT-S Digest*, pp. 679–682, 1989.

[26] J. Rogers, R. Bhatia "A 6 to 20 GHz planar balun using a wilkinson divider and lange couplers," in *IEEE MTT-S Digest*, pp. 865–868, 1991.

[27] B.J. Minnis, M.Healy "New broadband balun structures for monolithic microwave integrated circuits," in *IEEE MTT-S Digest*, pp. 425–428, 1991.

[28] M.C. Tsai "A new compact wideband balun," in *IEEE MTT-S Digest*, pp. 141–143, 1993.

[29] F. Sellberg "Formulas useful for the synthesis and optimization of general, uniform contradirectional couplers," *IEEE Trans. on Microwave Theory Tech.*, vol. 38, pp. 1000–1010, August 1990.

[30] J. Helszajn. *Microwave Planar Passive Circuits and Filters.* John Wiley & Sons, 1994.

[31] R. Levy "New equivalent circuits for inhomogeneous coupled lines with synthesis applications," *IEEE Trans. on Microwave Theory Tech.*, vol. 36, pp. 1087–1094, June 1988.

[32] A.A.M. Saleh "Transmission-line identities for a class of interconnected coupled-line sections with application to adjustable microstrip and stripline tuners," *IEEE Trans. on Microwave Theory Tech.*, vol. 28, pp. 725–732, July 1980.

[33] Waterloo Maple Software. "First leaves: A tutorial introduction to MapleV,". Springer-Verlag 1992.

[34] Jean-Marc Mourant "A low cost mixer for wireless applications," in *IEEE MTT-S Digest*, pp. 519-522, 1995.

[35] T.H.Chen, K.W.Chang, S.B.T.Bui, L.C.T.Liu, G.S.Dow, S.Pak "Broadband single- and dounle-balanced resistive HEMT monolithic mixers," *IEEE Trans. on Microwave Theory Tech.*, vol. 43, pp. 477-484, March 1995.

[36] K.Yhland, N.Rorsman, H.H.G.Zirath "Novel single device balanced resistive HEMT mixers," *IEEE Trans. on Microwave Theory Tech.*, vol. 43, pp. 2893-2867, December 1995.

[37] Y.Konishi "GaAs devices and the MIC applications in satelite broadcasting," in *IEEE MTT-S Digest*, pp. 1-6, 1990.

[38] J.Eisenberg, J.Panelli, W.Ou "A new planar double-double balanced MMIC mixer structure," in *IEEE MTT-S Digest*, pp. 69-72, 1991.

[39] A. Materka, T.Kacprzak "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. on Microwave Theory Tech.*, vol. 33, pp. 129-135, February 1985.

[40] J.Dortu, J.Muller, M.Pirola, G.Ghione "Accurate large-signal GaAs MESFET and HEMT modeling for power MMIC amplifier design," *Int.J. of Microwave and Milimiter-Wave Computer-Aided Engineering*, vol. 5, pp. 195-209, 1995.

[41] W.R. Curtice "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. on Microwave Theory Tech.*, vol. 25, pp. 448-456, May 1980.

[42] W.R. Curtice, M. Ettenberg "A nonlinear GaAs-FET model for use in the design of output circuits of power amplifiers," *IEEE Trans. on Microwave Theory Tech.*, vol. 33, pp. 1383-1393, December 1985.

[43] Sonnet Software, Inc. "EM user's manual,".

[44] GMMT GaAs Foundry Services. "Design manual,".