MMIC VCO DESIGN

A THESIS
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND
ELECTRONICS ENGINEERING
AND THE INSTITUTE OF ENGINEERING AND SCIENCES
OF BİLKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

Aykut ERDEM
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By

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tarafından bağışlanmıştır

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah Atalar(Supervisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Canan Toker

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. Mehmet Ali Tan

Approved for the Institute of Engineering and Sciences:

Prof. Dr. Mehmet Baray
Director of Institute of Engineering and Sciences

To *Birsel* and to the memory of my father

ABSTRACT

MMIC VCO DESIGN

Aykut Erdem
M.S. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Abdullah Atalar
September 1995

In this study, three voltage controlled oscillator (VCO) circuits are realised using Monolithic Microwave Integrated Circuit (MMIC) technology. Two of the VCOs are in the capacitive feedback topology, whereas the last one is designed by using the inductive feedback topology. GaAs MESFETs are used as both active devices and varactor diodes. Designed for a 50Ω system, the circuits operate in 8.88-10.40GHz, 8.71-10.23GHz and 8.96-12.14GHz ranges. Their output powers are well above the 9.5dBm for most of the oscillation band. All three VCOs have harmonic suppressions better than 30dBc. Both small signal and large signal analysis are carried out. The layouts are designed by GEC Marconi's F20 process rules and the circuits are produced in this foundry.

Keywords : MMIC, VCO, varactor

ÖZET

MMIC VCO TASARIMI

Aykut Erdem
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
Tez yöneticisi: Prof. Dr. Abdullah Atalar
Eylül 1995

Bu çalışmada üç adet voltaj kontrollü osilatör (VCO) devresi tek tabana oturtulmuş tümleşik devre teknolojisiyle tasarlanmıştır. Bunlardan ikisi kapasitif geri-besleme yöntemini sonuncusu ise indüktif geri-besleme yöntemini kullanmaktadır. GaAs MESFET transistörler hem aktif eleman hem de varaktör diyot olarak kullanılmıştır. 50Ω'luk sisteme göre tasarlanan bu devreler sırasıyla 8.88-10.40GHz, 8.71-10.23GHz ve 8.96-12.14GHz band aralığında çalışmaktadır. Devrelerin çıkış güçleri osilasyon bandının büyük bir kısmında 9.5dBm'den oldukça yukarıdadır. Bu üç VCO devresinin harmonik bastırması taşıyıcıya göre 30dB'den daha aşağıdadır. Bu devrelerin hem küçük işaret hem de büyük işaret analizleri yapılmıştır. Yongalar GEC Marconi firmasının sunduğu F20 tasarım kuralları ile yapılmış ve devreler bu firma tarafından üretilmektedir.

Anahtar Kelimeler : MMIC, VCO, varaktör

ACKNOWLEDGMENTS

I would like to thank Dr. Atalar for his supervision, guidance, suggestions and encouragement through the development of this thesis.

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Chapter 1

INTRODUCTION

The current trend in microwave technology is toward miniaturization and integration. Component size and weight are prime factors in the design of the electronic systems for satellite communications, electronic warfare, and other airborne and commercial applications. Microwave integrated circuits (MICs) promise higher reliability, reproducibility, better performance, smaller size and lower cost than conventional waveguide and coaxial microwave circuits.

A MIC can be a hybrid MIC or a monolithic MIC (MMIC). A hybrid MIC has solid state devices and passive circuits elements which can be fabricated separately and can be connected to each other on a dielectric substrate. However MMIC is a technique by which both active devices and the associated matching and biasing circuitries are fabricated onto a single chip of GaAs [1].

Hybrid MICs can be divided into two categories:(1) hybrid MICs and (2) miniature hybrid MICs. Hybrid MICs use the distributed circuit elements that are fabricated on a substrate using a single-level metalization technique. Other circuit elements, such as inductors, capacitors, resistors, and solid state devices, are added to the substrate. Miniature hybrid MICs use multilevel elements, such as inductors, capacitors, resistors,and distributed circuit elements, deposited on the substrate and solid state devices attached to the substrate. The circuit fabricated using this technology is smaller in size than hybrid MICs but larger than MMICs.

MMICs provide low cost, improved reliability, reproducibility, small size, low weight, broadband performance, circuit design flexibility, and multifunction performance on a single chip.

Monolithic is a multilevel process approach comprising all active and passive circuit elements and interconnections formed into the bulk or onto the the surface of a semi-insulating substrate. By 1980 many researches in MMIC had been reported. The reason for the recent increase in MMIC research can be summarized as follows:

1. Rapid development of GaAs material technology
2. Rapid development of low-noise MESFETs up to 60 GHz and power MESFETs up to 30 GHz
3. MESFETs, dual-gate MESFETs, Schottky-barrier diodes, and switching MESFETs can be fabricated simultaneously using the same process and almost any microwave solid state circuit can be realized using these devices
4. Excellent microwave properties of semi-insulating GaAs substrates (high dielectric constant and low loss tangent)
5. Availability of CAD tools for reasonably accurate modeling and optimizing of microwave circuits.

Now, many of microwave circuits, such as amplifiers, mixers, oscillators, phase shifters are implemented using MMIC technology.

In this thesis three MMIC voltage controlled oscillators (VCOs) are designed, and the design steps are explained from basic concepts, such as negative resistance concept to the final designs.

Chapter 2

OSCILLATOR CIRCUITS and DESIGN TECHNIQUES

Oscillator circuits are very similar to amplifier circuits [3]. An amplifier amplifies signals supplied by a signal source whereas an oscillator amplifies the noise caused by thermodynamic effects. The amplifier's and oscillator's block diagrams are shown schematically in Fig. 2.1. For the amplifier shown in Fig. 2.1, to extract the maximum power from the source, the lossless matching circuit M_1 is used. The output lossless matching structure M_2 should be designed to deliver the maximum power to the load. This amplifier is simultaneously conjugately matched at input and output ports and the design of this circuit is only possible when the stability factor is sufficiently large ($k > 1$).

Design of the oscillator is a similar problem. The important difference is the stability factor which must be less than 1 ($k < 1$) for this case. The load receives the power in the same way. A feedback circuit may be required to bring $k < 1$ at the frequency of interest. M_3, the input network is used for resonating the input port, whereas M_4 is just a matching network which transfers the maximum power to the load.

Oscillators are nonlinear devices whose nonlinearity is primarily related with the output power transferred to the load. Although the nonlinear calculations or simulations are necessary for oscillator design, the small signal approach constitute a very important design step especially for start-up oscillations.

For oscillator circuits, many small signal design techniques exist. Two of

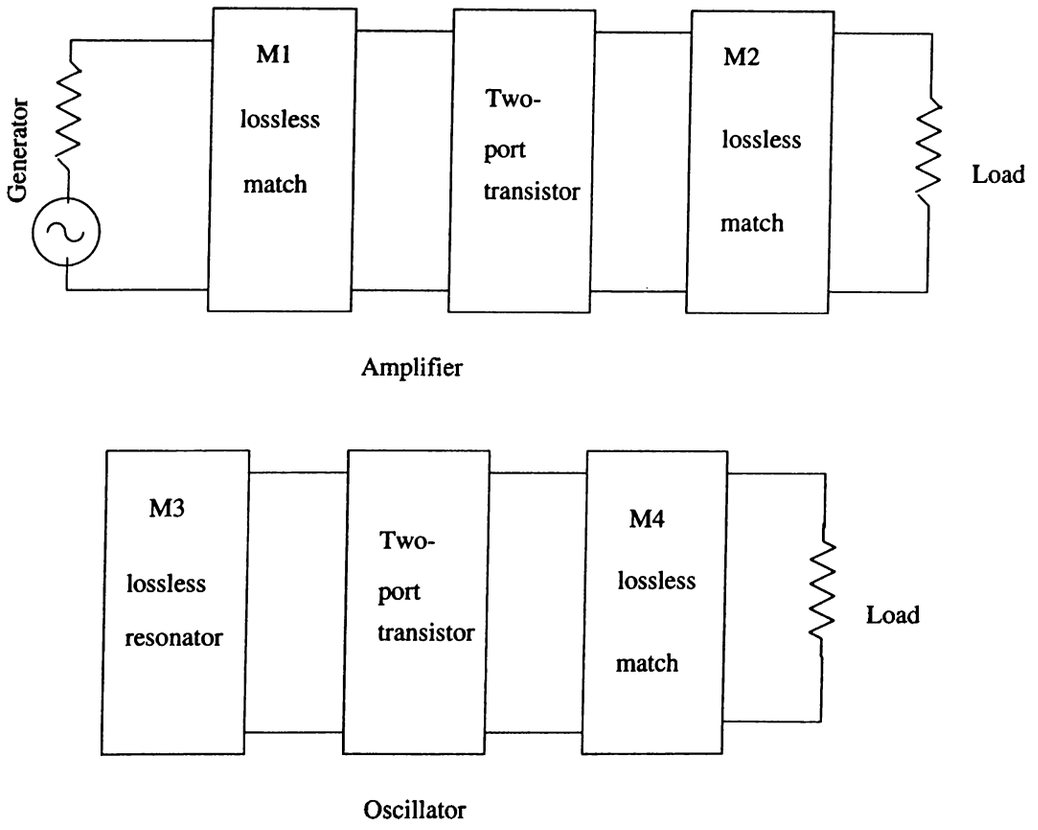

Figure 2.1: Block diagrams for amplifier and oscillator design

them, the best known and commonly used ones are:
1- Negative resistance approach
2- Reflective amplifier approach
Although the reflective amplifier method is more powerful in some cases, the negative resistance approach is usually preferred by designers.

2.1 Negative Resistance Concept

The negative resistance can be considered as follows: When a voltage V is applied across the negative resistor, -R, a current,

$$I = -V/R \tag{2.1}$$

flows out of the negative resistor, generating a power I^2R into the generator (may be a noise source).

From another point of view, the negative resistance means that the reflection coefficient is greater than unity in magnitude. So, the reflection coefficient

for a negative resistance termination is defined as:

$$\Gamma = \frac{-R - Z_0}{-R + Z_0},\ |\Gamma| = \frac{R + Z_0}{|R - Z_0|} > 1 \tag{2.2}$$

where, Z_0 is the characteristic impedance of the system.

2.2 One Port Negative Resistance Oscillators

The negative resistance circuits have the amplitude and frequency-dependent impedance [2] as shown in Fig. 2.2.

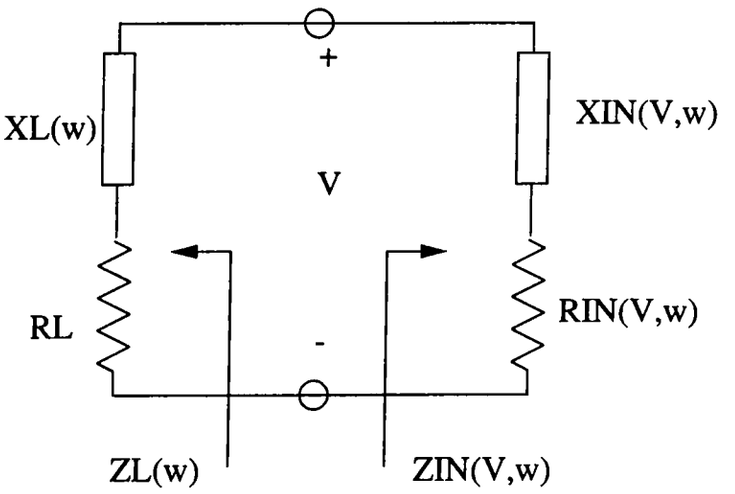

Figure 2.2: One port oscillator topology

$$Z_{IN}(V, w) = R_{IN}(V, w) + jX_{IN}(V, w) \tag{2.3}$$

where,

$$R_{IN}(V, w) < 0$$

By connecting the negative resistance device to a passive load impedance called,

$$Z_L(w) = R_L + jX_L(w) \tag{2.4}$$

an oscillation can be built-up. Note that the one-port network in Figure 2.2 is stable if;

$$Re[Z_{IN}(V, w) + Z_L(w)] > 0 \tag{2.5}$$

and oscillates when,

$$\Gamma_{IN}(V, w)\Gamma_L(w) = 1 \tag{2.6}$$

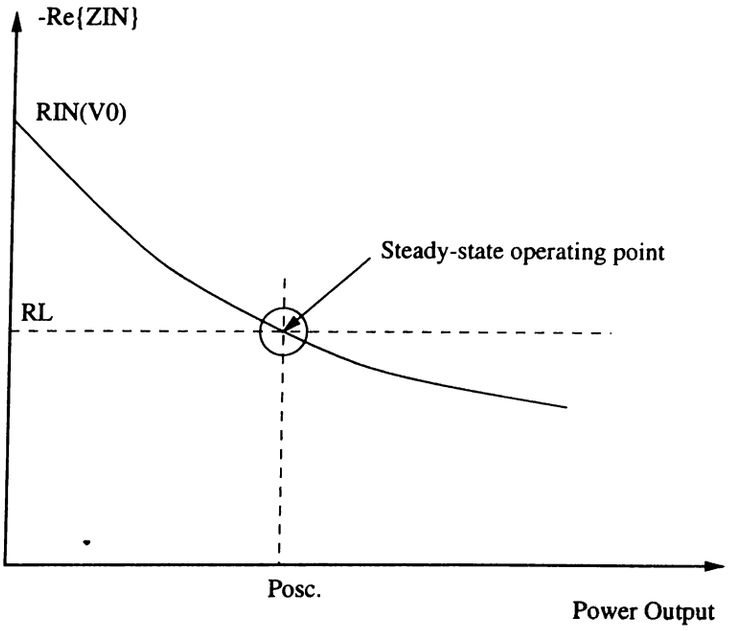

Figure 2.3: Amplitude dependence of negative resistance

or,

$$R_{IN}(V, w) + R_L = 0 \tag{2.7}$$

In other words, the device is defined to be unstable over some frequency range $w_1 < w < w_2$ if $R_{IN}(V, w) < 0$. The one-port network is unstable for some w_0, in the range if the net resistance of the network is negative, that is:

$$|R_{IN}(V, w_0)| > R_L \tag{2.8}$$

Any perturbation due to noise in the circuit will initiate an oscillation at the frequency w_0, for which the net reactance of the network is equal to zero,

$$X_L(w_0) = -X_{IN}(V, w_0) \tag{2.9}$$

As a result, a growing sinusoidal current at w_0 will flow through the circuit and the signal will continue to build up as long as the net resistance is negative. At steady state the amplitude of the voltage reaches its final value, called V_0, which occurs when the loop resistance is zero.

To satisfy the conditions given in Eq. 2.7 and 2.8, the impedance $Z_{IN}(V, w)$ must be amplitude dependent. This can be seen in Fig. 2.3. In summary, the oscillation conditions are as follows [1]:

1. Oscillation start conditions

$$Re[Z_L] < |Re[Z_{IN}]| \tag{2.10}$$

where,

$$Re[Z_{IN}] < 0$$

and,

$$Im[Z_L] = -Im[Z_{IN}]$$

2. Steady state oscillation conditions

$$Re[Z_L] = |Re[Z_{IN}(V_0)]| \tag{2.11}$$

where,

$$Re[Z_{IN}] < 0$$

and,

$$Im[Z_L] = -Im[Z_{IN}]$$

Even if these conditions are met, the oscillation may not be stable. Fortunately, the stability can be guaranteed by using small signal properties of the active device with the help of Edson's stability criteria [20]. Edson's stability criteria states that:

$$\frac{\partial R}{\partial w} > 0 \quad , and \quad \frac{\partial X}{\partial w} > 0 \tag{2.12}$$

where,

$$R = R_{IN}(V, w) + R_L$$

and,

$$X = X_{IN}(V, w) + X_L$$

2.2.1 Series or Parallel Resonance

Oscillators can be considered as, series-resonant or parallel-resonant oscillators [3], as shown in Fig. 2.4. For the series-resonant circuit, the negative resistance of the active device must exceed the load resistance R_L at start-up of oscillation.

Practically, for start-up of oscillation,

$$R_G > 1.2R_L \tag{2.13}$$

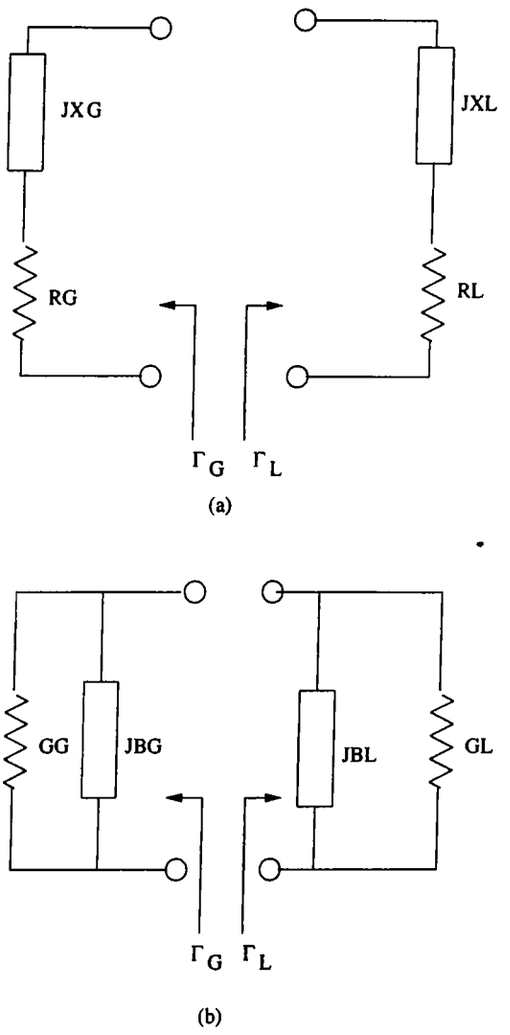

Figure 2.4: Oscillator equivalent circuits (a) series-resonant, (b) parallel-resonant

for resonance,

$$R_G + R_L = 0 \ , \ X_G + X_L = 0 \tag{2.14}$$

Note that, all the discussions of one-port oscillator approach given above are in the series resonant case since it is commonly used.

For the parallel-resonant case, the negative conductance G_G of the active device must exceed the load conductance G_L for start-up oscillation condition.

$$G_G > 1.2G_L \tag{2.15}$$

for resonance,

$$G_G + G_L = 0 \ , \ B_G + B_L = 0 \tag{2.16}$$

2.3 Two-Port Oscillator Design

Usually, the input port is resonated with a passive high-Q circuit at the desired frequency of resonance. Note the Fig. 2.1, where M_3 is the lossless resonator and M_4 provides lossless matching for maximum power transfer to the load. If the first port (resonator port) oscillates the output port resonates also or vice versa. Thus any of the ports can be used for load termination.
The proof is as follows:

$$1/\Gamma_{IN} = \Gamma_G \quad (oscillation\ condition\ at\ port\#1) \tag{2.17}$$

The input reflection coefficient Γ_{IN} is given by,

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.18}$$

where,

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

and,

$$\Gamma_G = \frac{1 - S_{22}\Gamma_L}{S_{11} - \Delta\Gamma_L} \tag{2.19}$$

For the output port, the reflection coefficient is,

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - \Delta\Gamma_G}{1 - S_{11}\Gamma_G} \tag{2.20}$$

Including Γ_G into the last equation,

$$\Gamma_{OUT} = \frac{S_{22} - \Delta(\frac{1-S_{22}\Gamma_L}{S_{11}-\Delta\Gamma_L})}{1 - S_{11}(\frac{1-S_{22}\Gamma_L}{S_{11}-\Delta\Gamma_L})} \tag{2.21}$$

After some ,

$$1/\Gamma_{OUT} = \Gamma_L \quad (oscillation\ condition\ at\ port\#2) \tag{2.22}$$

A design procedure for a two-port oscillator is as follows:
1. Use a potentially unstable transistor or make it unstable at the frequency of interest by using proper feedback techniques (i.e., make $k < 1$).
2. Design an output load matching network that gives $|\Gamma_{IN}| > 1$ over the desired frequency range.
3. Design a resonator which resonates the input port. The resonator Q factor must be as high as possible in order to satisfy the start-up oscillation condition ($\Gamma_G\Gamma_{IN} \geq 1$) and to improve the noise performance of the oscillator.

2.4 Reflective Amplifier Approach

Although the negative resistance approach is commonly used for microwave oscillator design, there is a fundamental problem [14] in viewing oscillators this way. The problem is that; S-parameters are more commonly used by microwave engineers and those parameters are more meaningful than impedances due to the difficulty to correlate the mathematics with the actual measurement.

Consider a one-port circuit with input S-parameter S_{11} and a resonant load with a reflection coefficient Γ (Fig. 2.5). A noise signal considered as E which

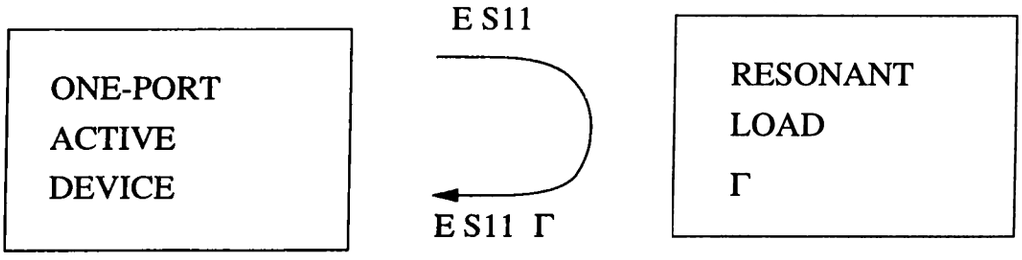

Figure 2.5: Oscillator with one port active circuit and a resonator

is incident on the port 1 and the reflected wave is given by $S_{11} * E$. This will then be re-reflected by the load giving $S_{11} * E * \Gamma$, which will again be incident on port 1. For oscillation to occur the following conditions must be satisfied together:

$$|S_{11}E\Gamma| > |E| \tag{2.24}$$

and,

$$ang(S_{11}) + ang(\Gamma) + ang(E) = ang(E) \tag{2.25}$$

or,

$$|1/S_{11}| < |\Gamma| \tag{2.26}$$

$$ang(1/S_{11}) = ang(\Gamma) \tag{2.27}$$

If $1/S_{11}$ is plotted on a Smith chart, R and X can be read and multiplied by -1 to get the values of the negative resistance and reactance. The proof is as follows:

$$S_{11} = (Z_S - Z_0)/(Z_S + Z_0) \quad (for\ port\#1) \tag{2.28}$$

$$1/S_{11} = (Z_S + Z_0)/(Z_S - Z_0) \tag{2.29}$$

Let $Z_1 = -Z_S$,

$$1/S_{11} = (Z_1 - Z_0)/(Z_1 + Z_0) \tag{2.30}$$

In order to get Z_S, $1/S_{11}$ is plotted onto a Smith chart, Z_1 is read and then multiplied by -1.

The negative resistance approach may give erroneous results. To illustrate this, consider the cases A and B shown in Figure 2.6.

For case A:

$$Z_S = -40 + j0\ \Omega$$

$$|1/S_{11}| = .111$$

$$ang(1/S_{11}) = 180$$

$$Z_\Gamma = 20 + j0\ \Omega$$

$$|\Gamma| = .428$$

$$ang(\Gamma) = 180$$

The net reactance is zero and the resistance is negative. Thus, one can see that an oscillations occurs considering the negative resistance approach.

For case B: The oscillations are again met. The source and the load impedances are:

$$Z_S = -150 + j0\ \Omega$$

$$|1/S_{11}| = .5$$

$$ang(1/S_{11}) = 0$$

$$Z_\Gamma = 200 + j0\ \Omega$$

$$|\Gamma| = .6$$

$$ang(\Gamma) = 0$$

The phase cancelation again occurs, but the net resistance is positive. So, the negative resistance approach fails (one can easily see that an oscillation can not occur). The answer to this problem lies in whether one uses a series or a parallel model for R_s.

2.5 Large Signal Oscillator Design

Actually, the oscillators are the large signal devices. Thus, the small signal analysis do not support close estimation of the oscillation frequency. In addition, some important properties such as, output power, efficiency, harmonic

content etc., can not be predicted by using small signal analysis. Nevertheless, the small signal analysis is a very important design step.

The oscillation begins by any transient excitation in the system if the start-up oscillation conditions are met. When the oscillation begins, the output power increases while decreasing gain and bandwidth. This phenomena can be seen in Fig. 2.6.

Large signal analysis is necessary for the optimum design [13] (i.e., for maximum power output). However, for this purpose the large signal S-parameters are needed. These parameters are obtained with the following procedure: Small signal S-parameter measurements are used with a computer program to compare the packaged and mounted device equivalent circuit. Large signal measurements are made by varying the input signal power level. Once the equivalent circuit has been computed from the small signal S-parameters, those parameters varying under large signals are incrementally altered until large signal S-parameters are obtained corresponding to the oscillator maximum output power.

There are six oscillator topologies for optimum power output. Three shunt and three series configurations are given in Figures 2.7, 2.8. The embedding elements, B_1, B_2, B_3, X_1, X_2, and X_3 are calculated by using Y and Z-parameters. The references [11], [13], [24] give the detailed expressions for embedding elements. The Y and Z-parameters can be obtained by conversion process from S-parameters.

On the other hand, it is not so easy to obtain the large signal S-parameter of an active device. Since the large signal parameters are power dependent and the oscillation power can not be known at the beginning of the analysis, this analytical method is difficult for starting the design. Therefore, some simulation tools such as LIBRA and MICROWAVE HARMONICA are used for large signal oscillator design. These programs simulates the circuit by using "Harmonic Balance" analysis (see Appendix A).

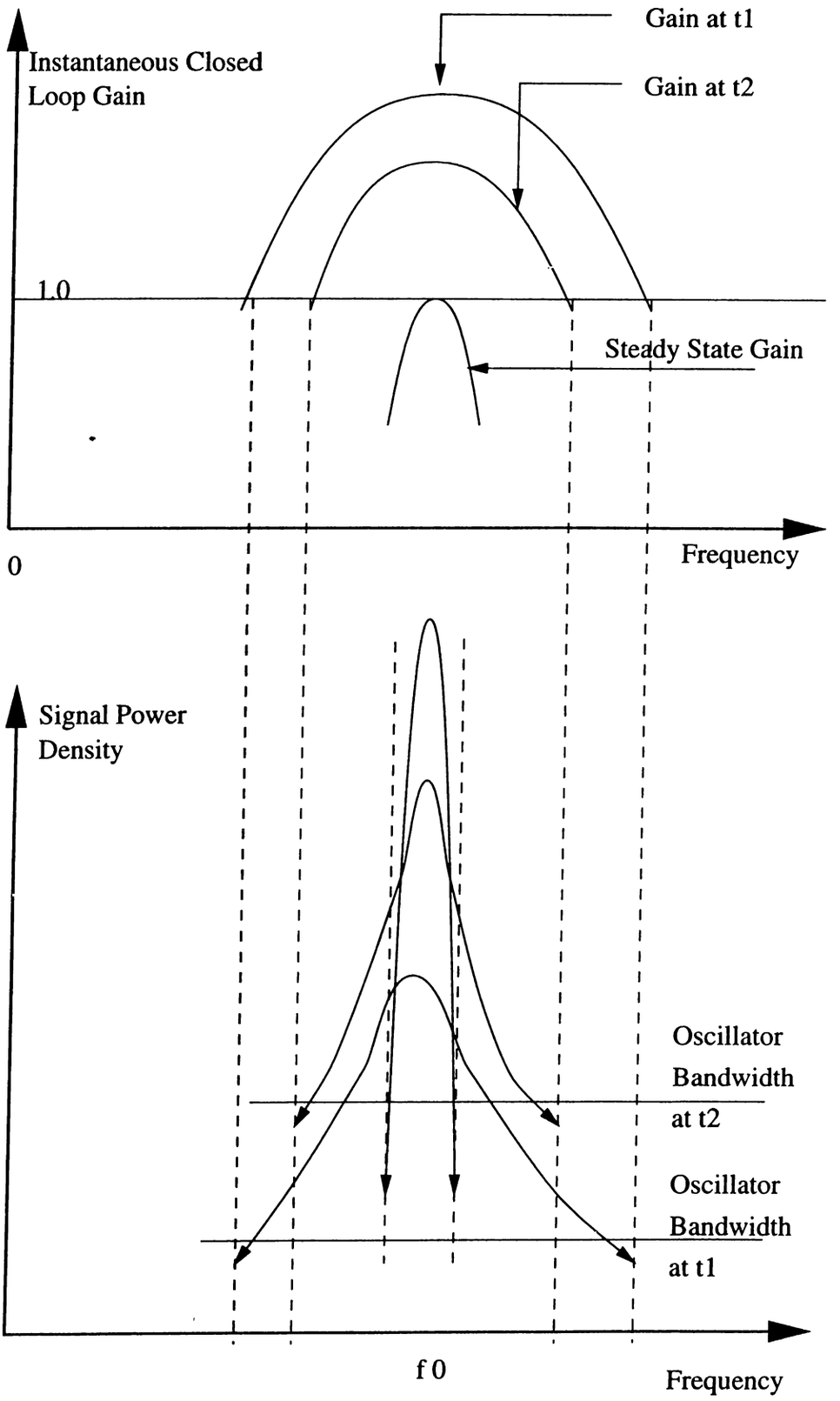

Figure 2.6: Oscillator signal growing

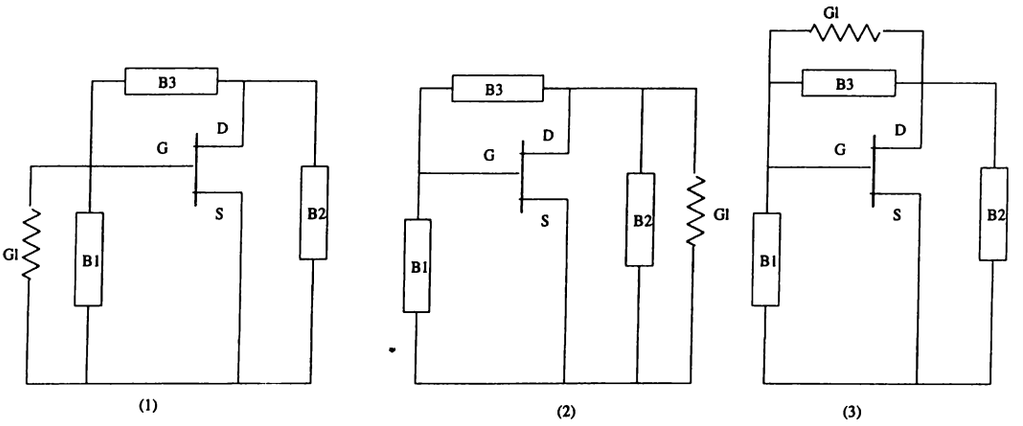

Figure 2.7: Three shunt configurations

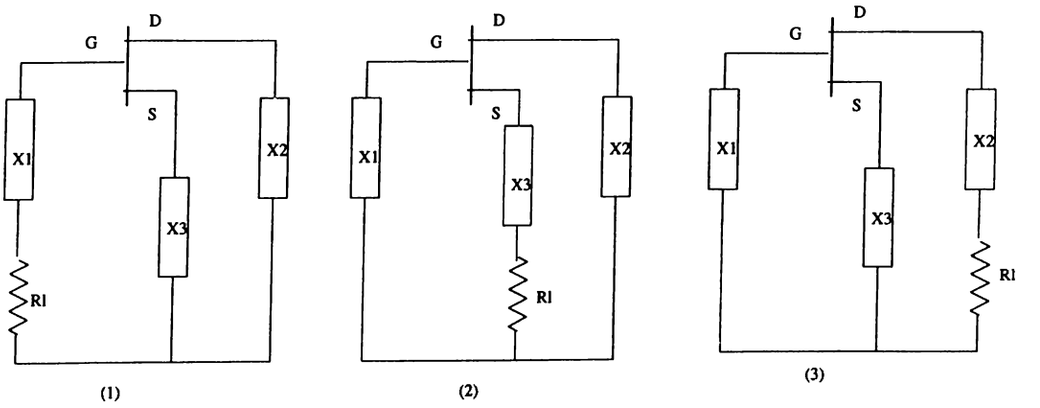

Figure 2.8: Three series configurations

2.6 Low Noise Feedback Oscillator Design

When an amplifier has a sufficient fraction of its output signal applied in phase to its input, the conditions for oscillation are met. In a low noise design it is essential to limit these sufficient conditions to a very narrow band [5]. If the oscillation conditions are limited to an infinitely narrow band, the oscillator will oscillate only at that unique frequency.

In other words, if there are no changes or variations in phase around the loop, the output is a single coherent frequency resulting no FM noise. However an amplifier has imperfections that cause small random changes to its phase shift. The output frequency fluctuates to maintain an integral multiple of 360 degrees. Thus, the phase noise sidebands are produced.

Consider the Fig. 2.9 to examine this problem graphically. In this figure, the frequency of oscillation occurs where the phase of the amplifier and the phase of the feedback circuit add-up to zero. If any phase shift occurs at the amplifier output port resulting from the amplifier noise or any external perturbations, the oscillation moves to the frequency where the phase condition is again met (i.e., the sum of the phases again adds to zero). One can see that, the frequency fluctuations can be reduced by reducing the phase fluctuations of the amplifier or by increasing the phase slope of the feedback. That requires designing a low noise amplifier with a high-Q feedback circuit.

Fig. 2.10 shows a block diagram of one possible low noise oscillator configuration. In order to obtain high phase slope a high-Q narrow band filter is used. The BPF filters the wide band noise but no specific high phase slope is represented in the feedback loop. The phase and magnitude adjustments of feedback is represented by a resistor. Due to the existence of BPF, the internal feedback characteristics are altered to a higher phase slope by the reflections of the high-Q resonant circuit.

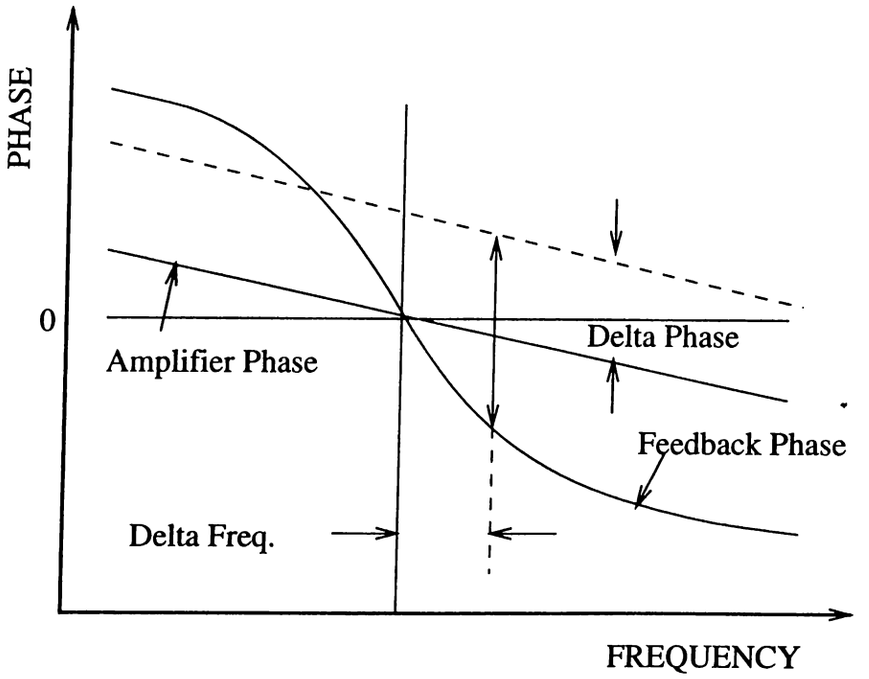

Figure 2.9: Phase noise

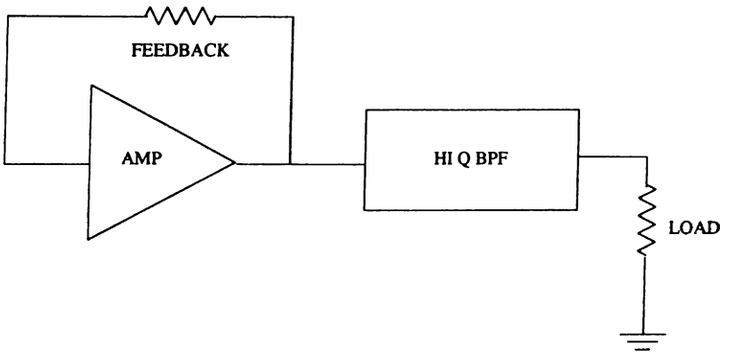

Figure 2.10: A low noise oscillator design topology

Chapter 3

GaAs MESFET and VARACTOR

3.1 GaAs Material Overview

Gallium arsenide (GaAs) is the most important of the III-V compound semiconductors today to fabricate high speed devices such as FET, bipolar transistors, solid-state lasers and integrated circuits. The most advantageous properties of III-V materials are [25]:

1. Higher speed electrons
2. Lower voltage operation
3. Semi-insulating substrates
4. Monolithic integration of optical and electronic functions
5. Radiation hardness

Because of the significantly higher electron drift velocity in gallium arsenide relative to silicon, the transit time delay in a GaAs FET is much less than a silicon FET. Thus, it operates at higher frequency than a silicon FET does. Commercially, GaAs FETs that operate up to 50 GHz are available.

3.2 Basic Device Structure

Fig. 3.1 shows a cross section of a GaAs MESFET. The MESFET is a unipolar device (i.e., it is a majority carrier device unlike the BJT). The basic structure

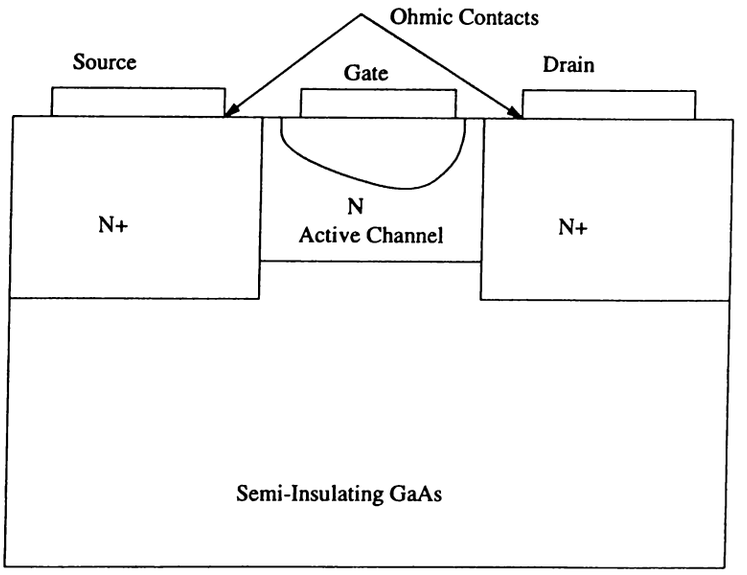

Figure 3.1: Cross section of a GaAs MESFET

of a MESFET consists of a thin film of N-type gallium arsenide with two ohmic contacts, called the source and the drain. N-doped epitaxial layer is used to realize the active channel. The third contact is the Schottky-barrier gate. A FET gate is a long, thin strip of metal that forms a Schottky barrier contact along the middle of a FET's GaAs channel. Usually, AuG (Gold Germanium) is used as the ohmic contact material. On the other hand, some choices are possible to form the gate metalization [1]:

- Aluminum
- Chromium
- Titanium
- Molybdenum
- Gold

These metals are preferred because of their relatively slow diffusion into GaAs, high conductivity and good adhesion properties.

3.3 Operating Mechanism

The MESFET is biased by the two sources shown in Fig. 3.2: V_{ds}, the drain-source voltage, and V_{gs}, the gate-source voltage. The voltages control the channel current by varying the width of the gate-depletion region. Consider the Fig. 3.2.a where, $V_{gs} = 0$ and V_{ds} is raised from zero to some low value. When $V_{gs} = 0$ the depletion region under the Schottky-barrier gate is relatively

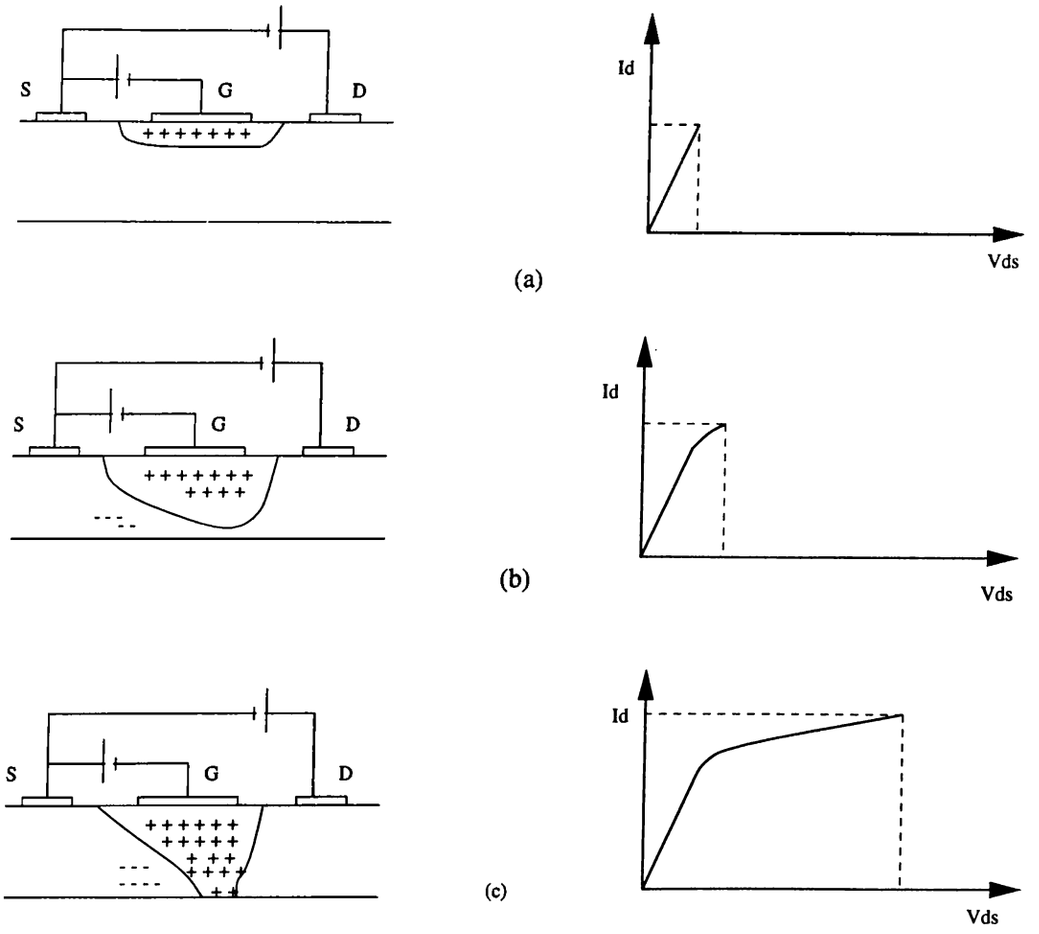

Figure 3.2: MESFET operation: (a) low V_{ds}; (b) V_{ds} at the saturation point; (c) hard saturation

narrow, and as V_{ds} is increased, a longitudinal electric field is created resulting a current in the channel. Since the drain voltage is higher than the source voltage, the depletion region is greater at the drain end than at the source end. When V_{ds} is low, the current is approximately proportional to V_{ds} . In other words, for a small V_{ds} the active layer behaves like a linear resistor. However when the gate reverse bias is raised while the drain bias is held constant, the depletion region widens reducing the current. If $V_{gs} = V_p$ (at the pinch-off voltage) the channel is fully depleted and the drain current is zero. For a larger V_{ds}, the channel current increases and the conductive channel becomes narrower. Since the average velocity of the electrons can not exceed the saturated drift velocity, the current-voltage characteristics fall below the initial resistor line as shown in Fig. 3.2.b. After that point, the electron concentration rather than velocity must increase in order to maintain current continuity. If V_{ds} is increased further, the electron flow starts to saturate (Fig. 3.2.c).

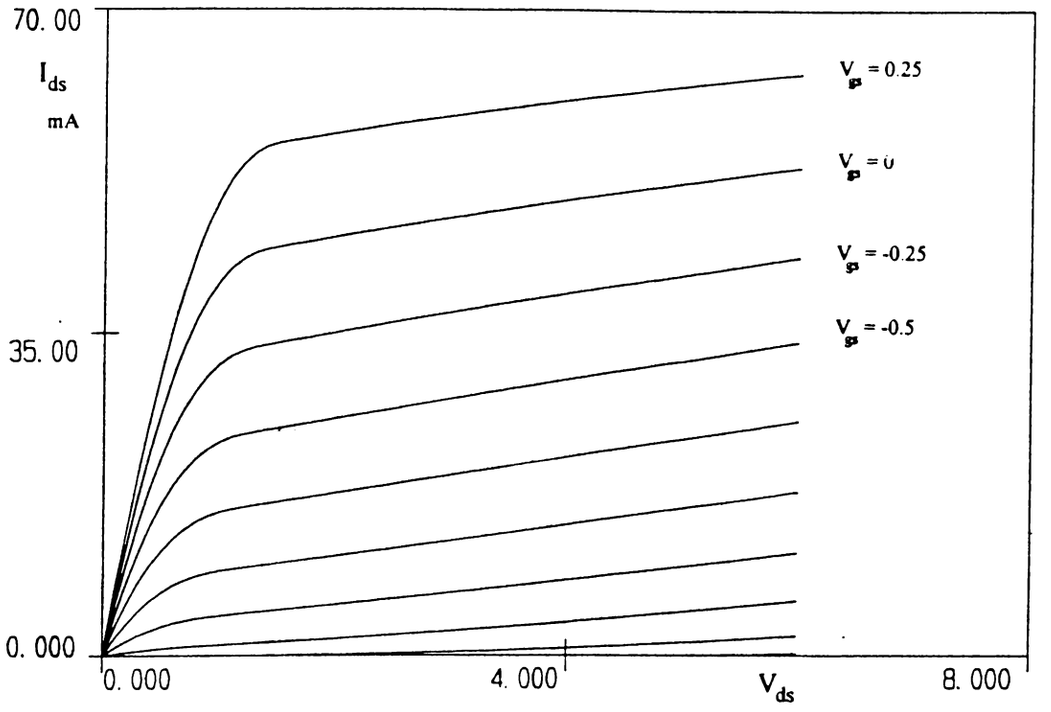

Figure 3.3: $4 * 75$ GEC MESFET $I_{ds} - V_{ds}$ curves

In conclusion, the operation of the MESFET is controlled by the active thin layer, whose thickness can be varied by the depletion layer under the gate resulting a current control by V_{gs} and V_{ds}. The I_{ds}-V_{ds} curves are obtained by using LIBRA for GEC Marconi $4 * 75$ FET (4 finger FET with each finger $75\mu m$ wide) are shown in Fig. 3.3.

3.4 MESFET's Small Signal Model and Equivalent Circuit

Modeling a device is very important task to provide a agreement between the measured data and the electrical processes occurring within the device. Each element in the equivalent circuit provides a lumped element approximation to some aspect of the device physics. Physically, the active channel should be represented by a distributed RC network. However, simple lumped linear element equivalent circuits are used to describe and equivalently represent the linear FET behavior in order not to complicate the circuit designers' task. These models are verified in representing the FET up to 20 GHz [23]. A

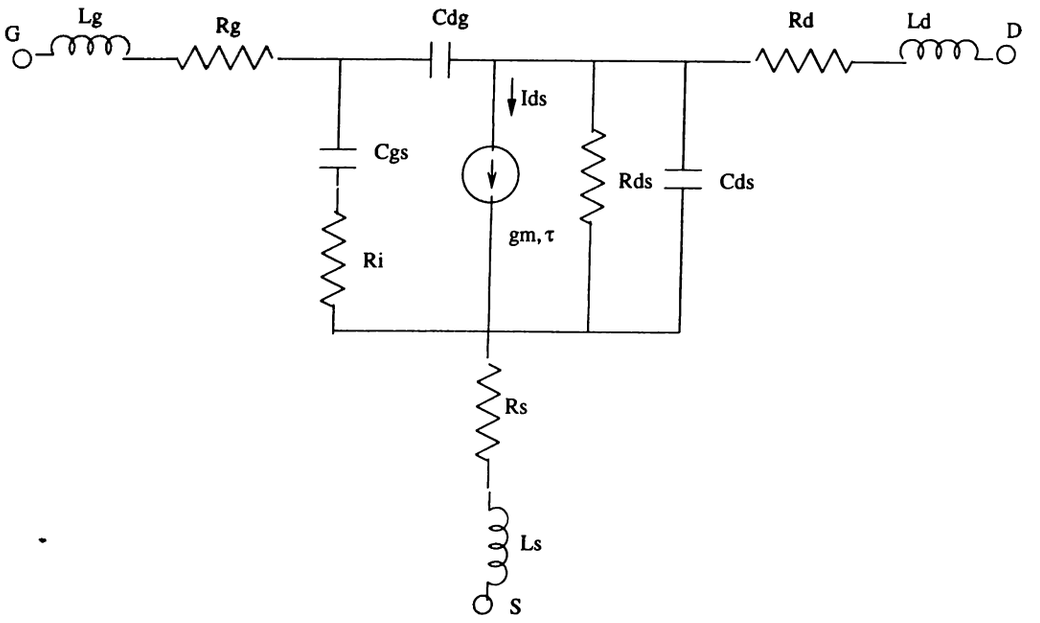

Figure 3.4: Small signal model of a MESFET

commonly used model is given in Fig. 3.4 . Some of the elements are extrinsic and the others are intrinsic.

The extrinsic elements are: R_s and R_d represent both the ohmic contact resistance and the resistance of the doped layer under the electrode and the element R_g is the gate metal resistance (reduced when the number of gate fingers increased). C_{ds} represent the coupling capacitance between the drain and the source through the substance. L_g, L_d and L_s are the parasitic inductances associated with the metalizations.

The intrinsic elements C_{dg} and C_{gs} represent the fringing capacitance between the drain and the gate, and the gate to source, respectively. The charging resistance in the channel represented by R_i and R_{ds} shows the effect of drain-source channel resistance. Lastly, the transconductance $g_m = g_{m0}e^{-jw\tau_0}$ where g_{m0} is independent of frequency and τ_0 is a phase delay. This delay corresponds to the time required for electrons to traverse the gate length at the scattering-limited velocity.

3.5 Nonlinear Modeling of MESFET

Since the foundry, GEC Marconi supplied only the Curtice cubic model for LIBRA, this model has been briefly investigated here and illustrated in Fig.

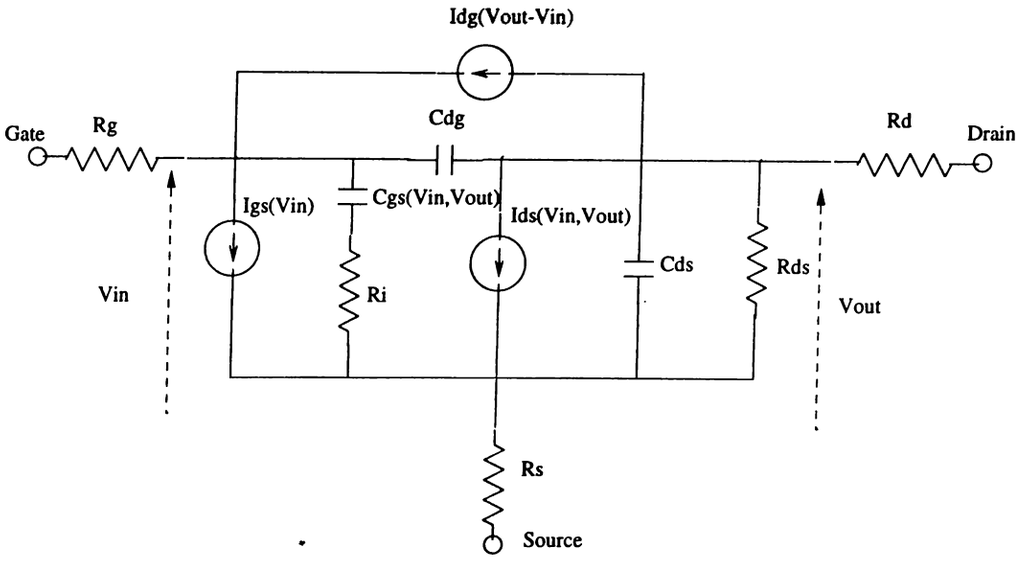

Figure 3.5: Curtice-cubic nonlinear MESFET model

3.5 wherein three voltage-controlled current sources determine the main non-linearity of the device.

This is an empirical model. Thus, some equations given below are valid for only the given conditions. These equations are as follows:

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3)\tanh(\gamma V_{out}(t)) \tag{3.1}$$

where, V_1 is the input voltage that is given by,

$$V_1 = V_{in}(t - \tau)[1 + \beta(V_{out}^0 - V_{out}(t))] \tag{3.2}$$

here,
β:the coefficient for pinch-off voltage change,
V_{out}^0:the output voltage to evaluate the constants A_0, A_1, A_2 and A_3,
τ:the internal time delay of the FET under consideration.
Eq. 3.1 is valid only when $V_d > 0$ (i.e., $V_{out} > 0$), because the drain I/V characteristic is not symmetrical about the origin of the I/V and must be used with the constraint $I_d = 0$ when $V_g < V_p$

$$I_{dg} = \begin{cases} (V_{dg}(t) - V_B)/R_1 & , V_{dg} > V_B \\ 0 & , V_{dg} < V_B \end{cases}$$

where,
R_1:the approximate breakdown resistance
$V_B = V_{b0} + R_2 I_{ds}$

R_2:the resistance relating breakdown voltage to channel currents.

$$I_{gs} = \begin{cases} (V_{gs}(t) - V_{bi})/R_f & , V_{in}(t) \geq V_{bi} \\ 0 & , V_{in}(t) < V_{bi} \end{cases}$$

where,
V_{bi}:the built-in voltage,
R_f:the effective value of the forward-bias resistance.

$$C_{gs,gd} = C_{gs0,gd0}[1 - V_{applied}/Vbi]^{-1/2} \tag{3.3}$$

where,
$V_{applied}$:the gate-source or gate-drain voltage,
$C_{gs0,gd0}$:the zero bias gate-source or gate-drain capacitance.
The other elements' values are obtained from the Fukui measurements [28] and the small signal model. Further knowledge about nonlinear models can be obtained from the M.Sc. Thesis works of F. Öztürk [22] and F. Üstüner [23].

3.6 Varactor Diodes

The varactor is a semiconductor capacitor whose capacitance value can be changed (or controlled) by the voltage applied across its terminals. They are widely used in the microwave circuits such as VCOs, parametric amplifiers, frequency multipliers, etc.

Varactor diodes are constructed from both silicon and gallium arsenide. A cross section of a varactor diode is shown in Fig. 3.6. The active layer is in a necked portion of the diode called a mesa. The use of the mesa is to provide diode area control by selective etching.

The doping profile of an abrupt junction and the hyperabrupt junction varactor diodes are given in Fig. 3.7.

A varactor supports current flow when forward biased above its barrier potential. Under reverse-bias conditions, a depletion region forms within the N region of the diode. While increasing the reverse voltage this region of space charge (depletion layer) widens, until it extends across the entire N region. Since the depletion region is positively charged in N region, the equal amount of negative charge exist in the P region and these charge layers act as if parallel plate capacitor. Increasing the reverse voltage, these layers move apart from each other causing a decrease of junction capacitance value. As the charges

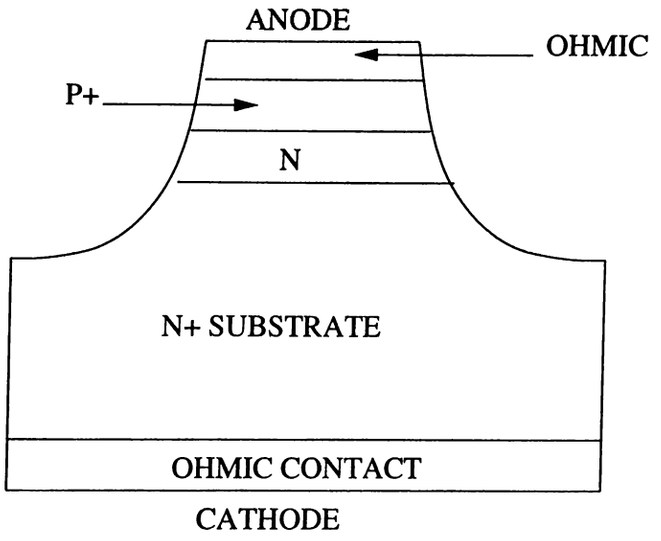

Figure 3.6: Cross-sectional diagram of a varactor

are depleted, by increasing voltage, the capacitance of the diode decreases accordingly to the relationship:

$$C = \epsilon A/d$$

where, d is the nominal separation between charges and A is their effective area. The varactor diode can be represented by a simple series RC circuit as shown in Fig. 3.8. The series resistance decreases as the reverse voltage increases. The reason is the depletion region widening while increasing the reverse bias voltage.

Most microwave-frequency varactors are realized in silicon. The minority carrier lifetime in silicon is greater than in GaAs so for lower frequency operation (i.e. below about 20 GHz), and the charge-storage properties of silicon diodes are better than those of GaAs devices. However, at higher frequencies, GaAs has the advantage of lower series resistance and consequently higher dynamic Q.

The expressions for capacitance and resistance of an abrupt or a hyper-abrupt junction diodes, as a function of applied reverse bias voltage are as follows:

$$C_j(V) = A[\frac{\epsilon en}{2(\Phi + V)}]^\gamma = AK(\frac{n}{\Phi + V})^\gamma = \frac{C_j(0)}{(1 + \frac{V}{\Phi})^\gamma} \tag{3.4}$$

$$R_s(V) = \frac{l - w}{en\mu a} \tag{3.5}$$

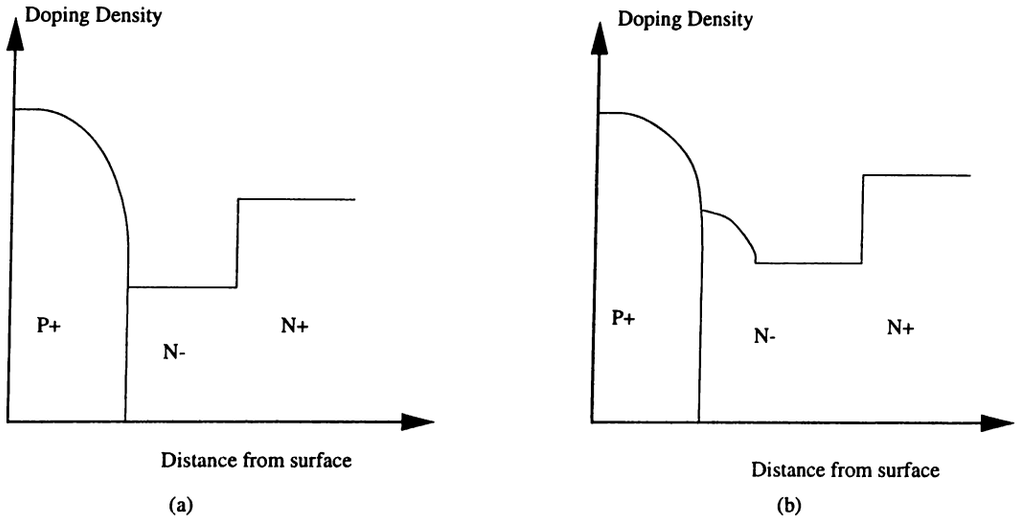

Figure 3.7: Doping profiles of abrupt(a) and hyperabrupt(b) junction varactors

$$w(V) = [\frac{2\epsilon(\Phi - V)}{en}]^{\gamma} \tag{3.6}$$

where,
Φ:built-in potential,
$C_j(0)$:a constant(mathematically equal to junction capacitance when $V = 0$),
γ:capacitance-voltage slope exponent,
A:junction area(cross-sectional area) of the diode,
ϵ:semiconductor dielectric constant,
n:average doping of the active region,
V:applied reverse voltage,
e:electronic charge,
l:active region length,
w:depletion layer width,
μ:semiconductor mobility in the active region,
K:constant.

For simple abrupt junction varactors, gamma is constant and nominally equal to 0.5. The junction is referred to as hyperabrupt when $\gamma > .5$ and for most commercially available varactors, the value of γ varies widely with applied voltage.

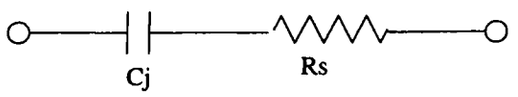

Figure 3.8: A simple model of a varactor

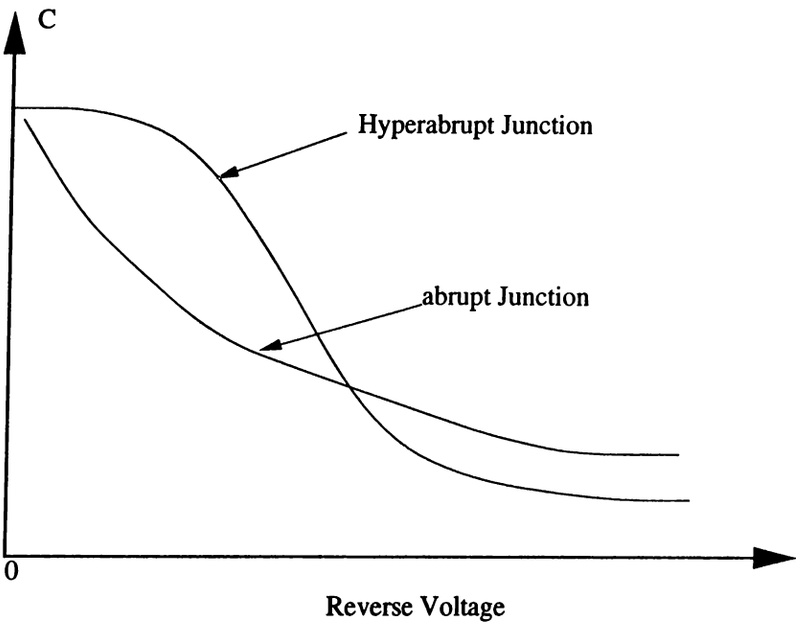

Figure 3.9: Capacitance tuning characteristics of an abrupt and a hyperabrupt junction varactors

Fig. 3.9 shows the comparison between the capacitance of a hyperabrupt diode and the capacitance of an abrupt diode. The hyperabrupt junction varactors have a non-uniform N region doping profile, which is tailored, resulting the more rapid capacitance change than in abrupt junction diodes.

Typically, a varactor-tuned oscillator's frequency and tuning voltage have a nonlinear relationship. The amount of tuning nonlinearity can be reduced by using any one of the three following methods:

1. Reducing the tuning range
2. Using hyperabrupt junction diodes.
3. Employing external linearizer circuits.

Usually, the value γ varies with applied voltage. However, to achieve linear frequency tuning without the use of a linearizer, the constant gamma hyperabrupts are needed [9]. For a simple resonant circuit comprised of an inductance, L and the varactor junction capacitance $C_j(V)$, the frequency-voltage relationship is given by:

$$f_r(V) = \frac{1}{2\pi\sqrt{LC_j(V)}} = \frac{1}{2\pi\sqrt{LC_0}}(1 + \frac{V}{\Phi})^{\gamma/2} \tag{3.7}$$

and the desired γ for linear tuning is 2.0 . However, in nearly all microwave circuits the varactor is not the only capacitance in the resonator. Instead, the capacitance of the active element $(C_j(V))$ is only a portion of the capacitance of

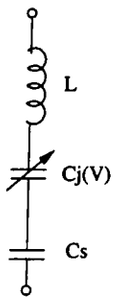

Figure 3.10: A series resonant circuit with a coupling capacitor C_s

the complete resonant circuit. An analysis were performed by A. E. Moysenko [9] for the simple series resonant circuit illustrated in Fig. 3.10 wherein a fixed capacitance, C_s, is used in series with the varactor. The result provides guidance to the selection of a suitable γ for the circuit designer.

The total capacitance is:

$$\frac{1}{C_T(V)} = \frac{1}{C_s} + \frac{1}{C_j(V)} = \frac{1}{C_s} + \frac{1}{C_0}(1 + \frac{V}{\Phi})^{\gamma} \tag{3.8}$$

Let,

$$C_{T0} \equiv C_T(V = 0)$$

Define, $K_s = \frac{C_{T0}}{C_0}$, coupling factor $(0 \leq K_s \leq 1)$

$$\frac{1}{C_{T0}} = \frac{1}{C_s} + \frac{1}{C_0} \tag{3.9}$$

$$\frac{1}{C_0} = \frac{K_s}{C_{T0}} \tag{3.10}$$

$$\frac{1}{C_s} = \frac{1}{C_{T0}} - \frac{1}{C_0} = \frac{1}{C_{T0}} - \frac{K_s}{C_{T0}} = \frac{(1 - K_S)}{C_{T0}} \tag{3.11}$$

Hence,

$$\frac{1}{C_T(V)} = \frac{1}{C_{T0}}[1 - K_s + K_s(1 + \frac{V}{\Phi})^{\gamma}] \tag{3.12}$$

and the resonance frequency,

$$f_r(V) = \frac{1}{2\pi\sqrt{LC_T(V)}} = \frac{1}{2\pi\sqrt{LC_{T0}}}\sqrt{1 - K_s + K_s(1 + \frac{V}{\Phi})} \tag{3.13}$$

When $K_s = 1$, the varactor is fully coupled and the corresponding optimum value for $\gamma = 2.0$. When K_s approaches zero, the varactor becomes heavily decoupled and only narrow-band frequency tuning is possible and the optimum γ approaches 1.0. For intermediate vales $(0 < K_s < 1)$, an optimum value of constant γ for linear frequency tuning is predictable for any particular tuning

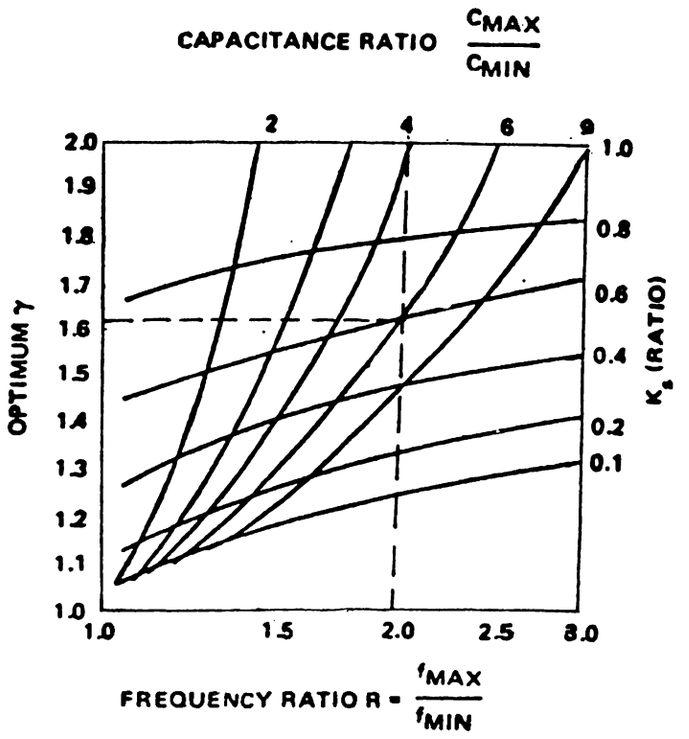

Figure 3.11: Constant γ selection plot for linear tuning [9]

bandwidth by using the results of the analysis [9] as shown in Fig. 3.11, on which the optimum γ value is plotted versus the frequency ratio, f_{max}/f_{min}, with the coupling factor, K_s, as a parameter.

From the circuit designer's viewpoint, this simplified analysis can be used for selection of constant gamma hyperabrupts. For example, suppose this circuit specification requirement is for a tuning ratio of 2:1, the designer could select γ =2.0 and fully couple the varactor with $C_{max}/C_{min} = 4$. Alternatively, K_s can be chosen as 0.6, where γ should be chosen as 1.6 and $C_{max}/C_{min} \geq 6$. Further decoupling can also be selected to improve resonator Q with correspondingly lower γ. However there is a limit for K_s, since C_{max}/C_{min} has a limited value.

The FM noise in an oscillator is inversely proportional to the resonator's Q, so high Q resonators are very desirable for minimizing the FM noise. In a varactor-tuned resonator, Q is inversely proportional to its tuning range. This nonlinear behavior can be included in the equivalent circuit of the varactor diode [29] as shown in Fig. 3.12.

The conductivity G(V) is given as:

$$G(V) = \frac{qI_s}{kT} e^{\frac{qV}{kT}} \tag{3.14}$$

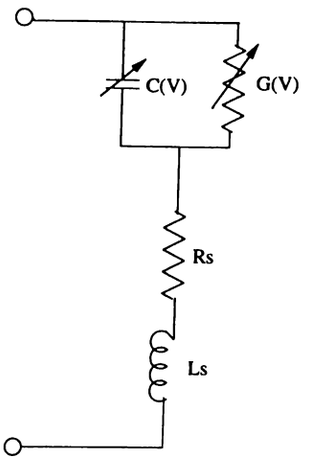

Figure 3.12: Nonlinear model of a varactor

where,
I_s: is the reverse saturation current,
k: is the Boltzmann's constant,
T: is the absolute temperature.

3.7 MMIC Varactor Design By Using MESFET

Usually, MMIC VCO's are designed in two ways with respect to the varactor diode used in the circuit. The first method is to use an off-chip varactor diode. This means that, the varactor diode is connected to the circuit externally by using additional bonding wires. Although a higher Q varactors with a large capacitance ratio can be obtained, the bonding wires and the connection pads show unpredictable effects (i.e., unpredictable impedance values). Commercially, this is difficult to realize. The other method is to use on-chip varactors which are realized monolithically with the other parts of the circuit. Monolithic varactors have low quality factors and smaller capacitance ratios. The following paragraphs introduce a design method for monolithic varactors.

As mentioned before, the gate-source capacitance of a MESFET is voltage dependent and given by the following equation.

$$C_{gs} = C_{gs0}[1 - \frac{V_{gs}}{V_{bi}}]^{-1/2} \tag{3.15}$$

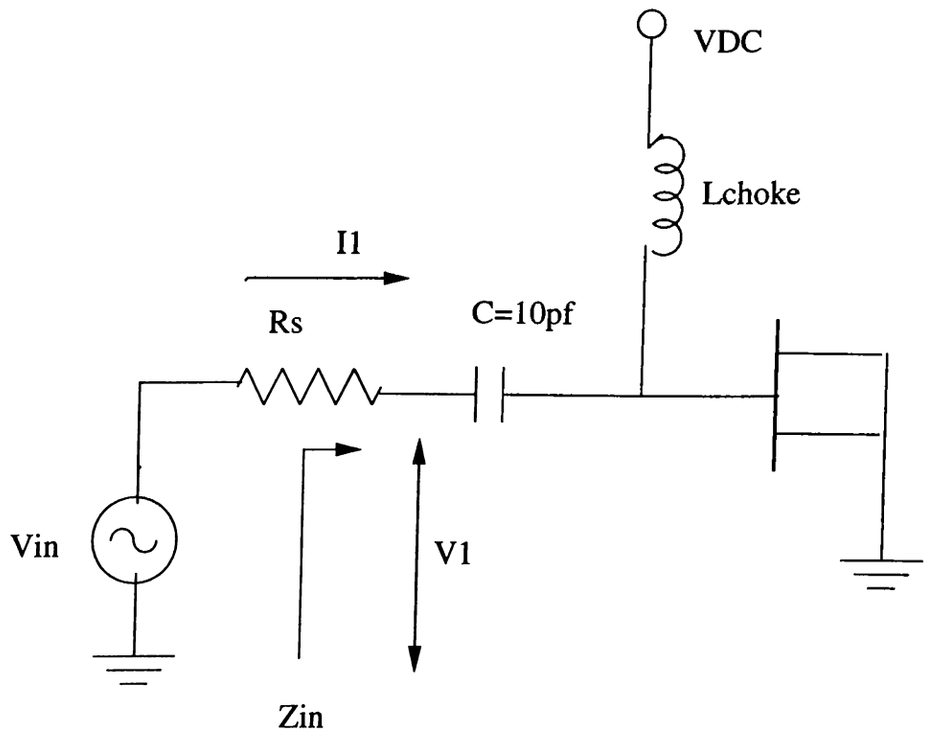

Figure 3.13: A MESFET varactor circuit

Note that the gate-source capacitance is maximum when the applied voltage across the gate and the source, is zero. While increasing the negative gate-source voltage, C_{gs} approaches the minimum value.

Fig. 3.13 shows the circuit diagram of the simulated varactor MESFET. Note that the drain and the source terminals are grounded in order to minimize the effects of the other nonlinear elements and the parasitics. Zin can be modeled as a simple series RC circuit [21] in which both the resistor and the capacitor are voltage dependent nonlinear elements. The simulation results show that the resistance and the capacitance remain nearly constant for a constant bias voltage in the frequency of interest.

Here, DC block capacitor is 10pF GEC silicon-nitride capacitor and R_s is the 50Ω source resistance used for current measurements. The choke inductor L provides the gate biasing and it is an ideal choke inductor. The circuit is simulated by applying an AC source voltage having a small magnitude and Z_{in} is found by taking the ratio of the fundamental component of the gate voltage V_1 to the fundamental component of the current I_1 flowing through the source resistor. Since the value of the series DC blocking capacitor is large enough (10pF), the input impedance Zin is approximately equal to the actual gate-source impedance.

Since the input impedance does not change much up to 2.5 V of AC source signal level, all the varactor simulations have been carried out by applying a signal of 0.01 V in magnitude, resulting a considerable decrease in computation time, compared to that for the 1 V of input signal which is the estimated voltage value [21] across the resonator (or the varactor). In order to compute the fundamental components, eight harmonics were taken into account in the simulation.

Figures 3.14 and 3.15 show the nonlinear variations of the input impedance for different input signal levels. Note here that, the variations for both the capacitance and the series resistance are not large. The Fig. 3.14 shows the capacitance versus frequency variation at a constant -2.0 V DC tuning voltage for different input AC voltage levels. Similarly, the Fig. 3.15 shows the input resistance variations at the same DC bias points.

The capacitance and the resistance variations versus frequency for different DC bias voltages, are illustrated in Figures 3.16 and 3.17, respectively. Since the conduction begins when the gate-source bias voltage, V_{DC} increases to the positive values, the impedance variations are not small enough to be negligible in the frequency of interest for the values of V_{DC} exceeding 0 V. The simulation file is given in Appendix C.

As V_{DC} changes from 0 V to V_p (pinch-off voltage), which is about -2.0 V for GEC $4*75$ FET, the C_{gs} varies from approximately 0.55pF to 0.3pF due to the enlargement of the depletion region, and the series resistance value is less than 4.5Ω. Although the capacitance ratio is small for the voltage range of 0 to V_p, the upper limit can be raised up to a value of 1.87 pF but the series loss resistance is about 13.5Ω for .65V tuning voltage at a frequency of 10 GHz. In addition, the lower limit of C_{gs} can be shifted to a value of 0.24 pF with a 2Ω series resistance. Figures 3.18 and 3.19 illustrate these arguments.

In fact, some extra transmission lines and non-ideal elements take part in the actual varactor circuit. For our finished layout, the first and the second VCOs are implemented with a varactor circuit given in Fig. 3.20. The third VCO's varactor circuit has no such a transmission line. The comparison between the actual varactor and the one without transmission lines is tabulated on Table 3.1. By inspection, one can easily see that, the capacitance ratio is improved but the loss especially caused from the series transmission line between the gate of the transistor and the silicon nitride capacitor becomes more important.

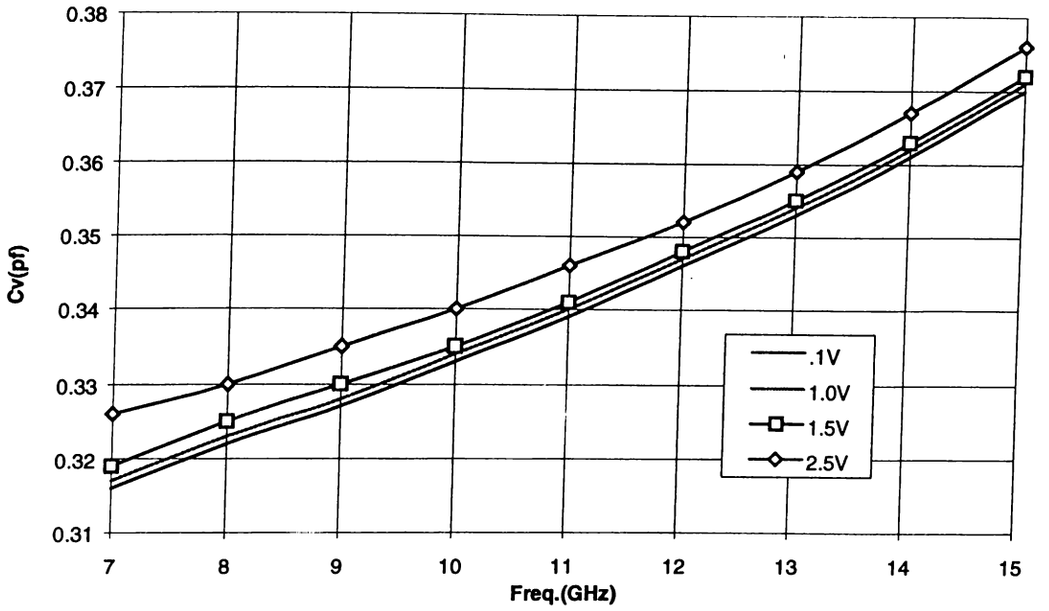

Figure 3.14: C_v versus frequency at different input power levels (V_{tune}=-2V)

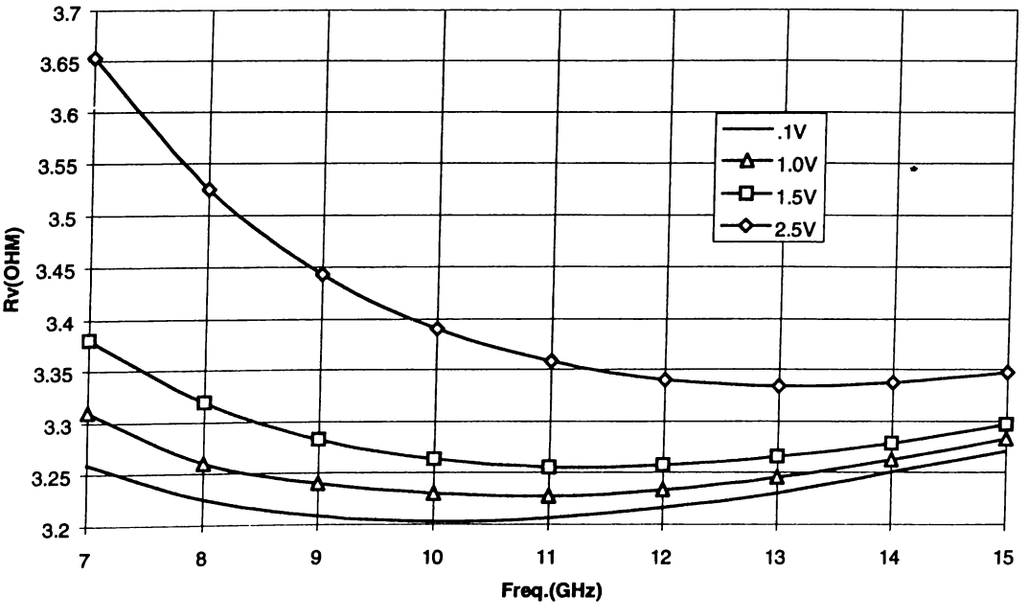

Figure 3.15: R_v versus frequency at different input power levels (V_{tune}=-2V)

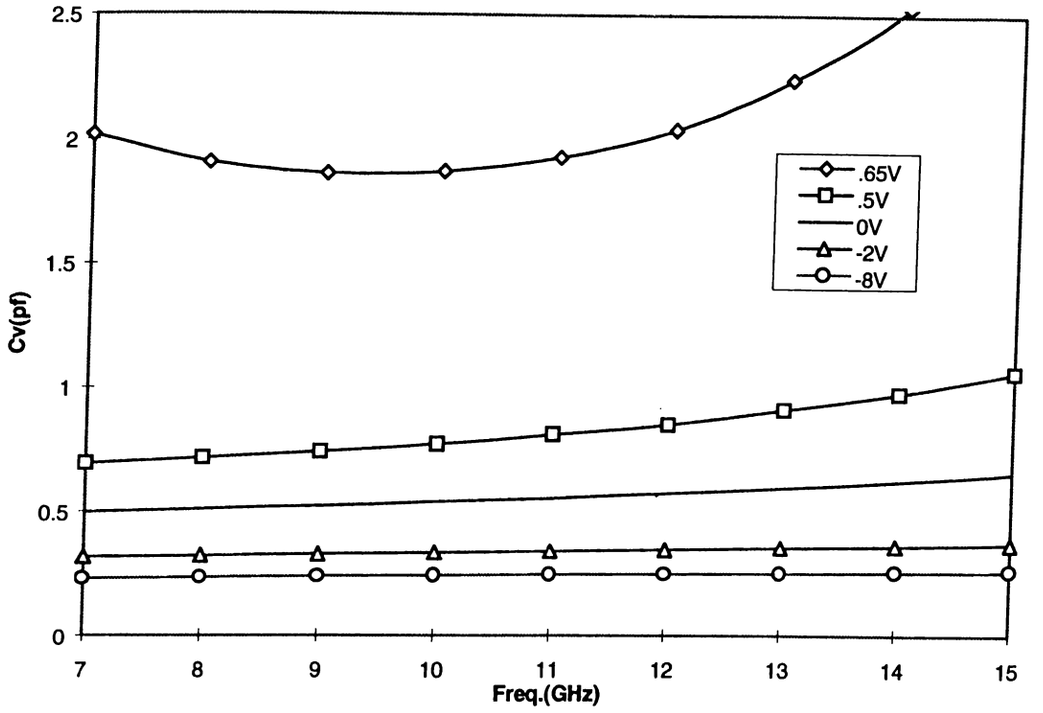

Figure 3.16: C_v versus frequency for different tuning voltages (V_{in}=.01V)

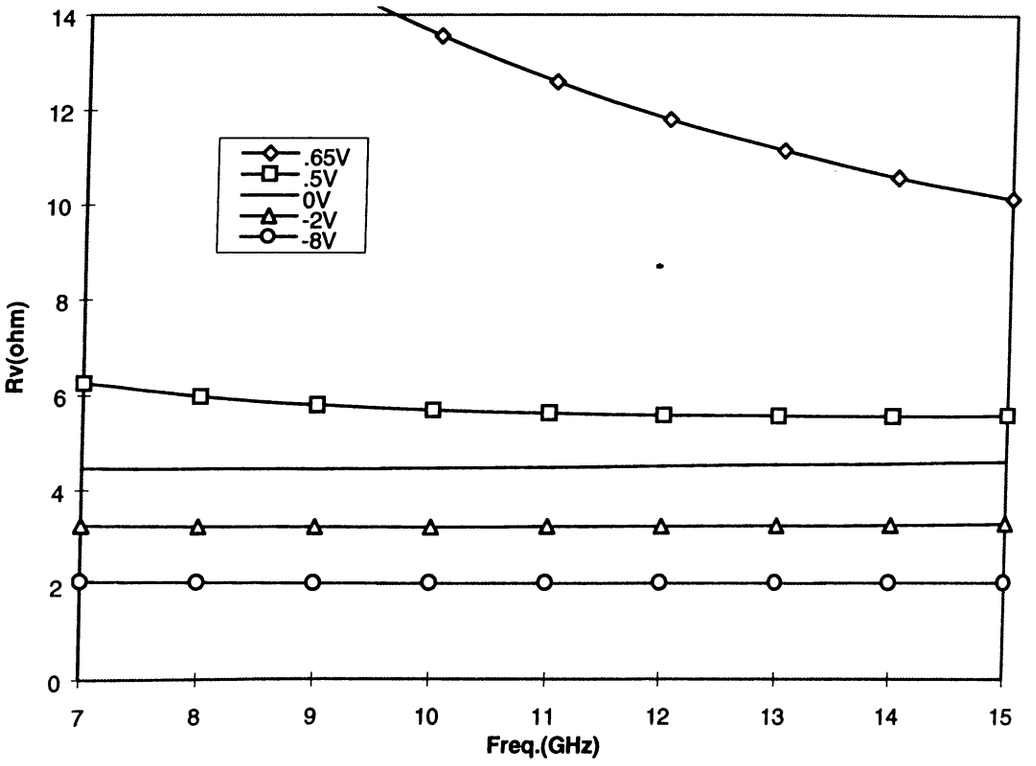

Figure 3.17: R_v versus frequency for different tuning voltages (V_{in}=.01V)

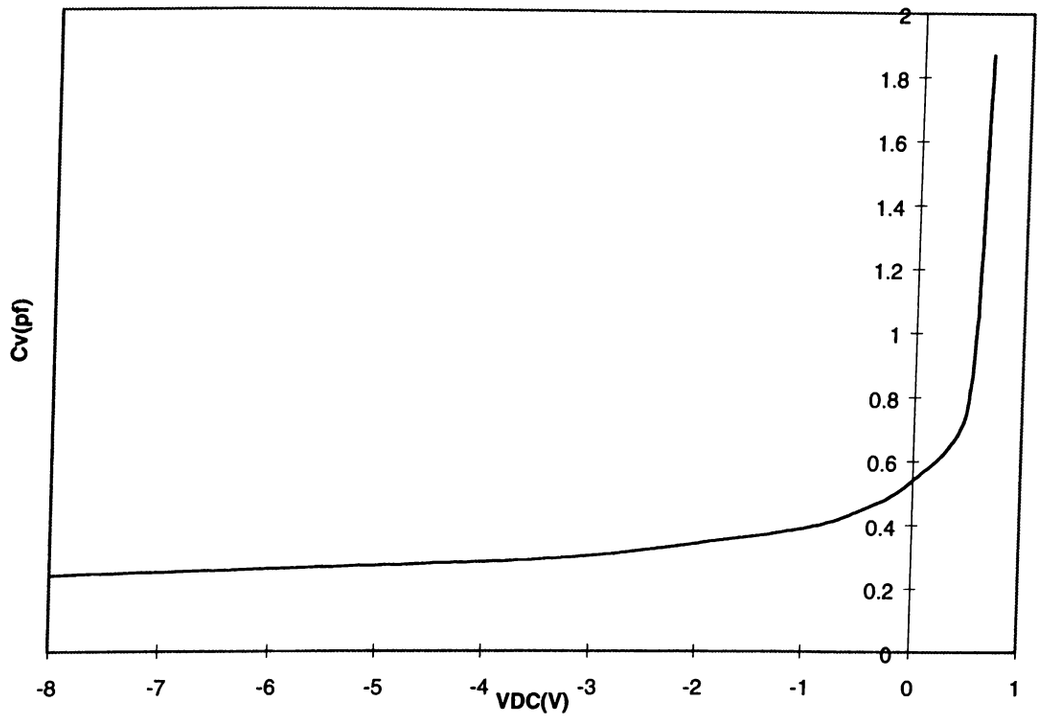

Figure 3.18: C_v versus V_{tune} @ 10GHz (V_{in}=.01V)

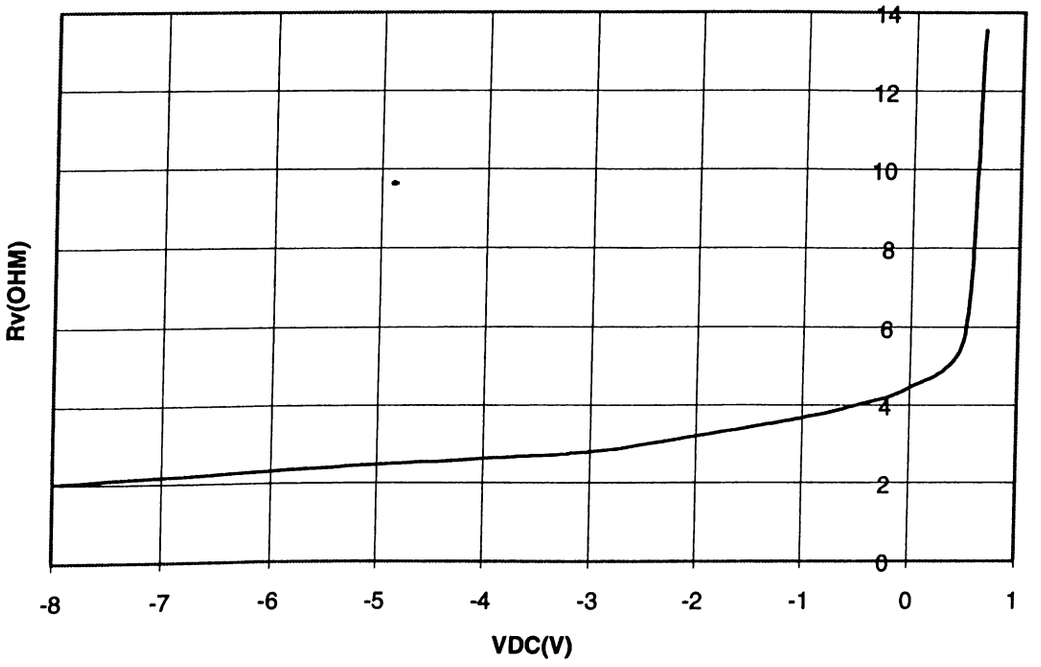

Figure 3.19: R_v versus V_{tune} @ 10GHz (V_{in}=.01V)

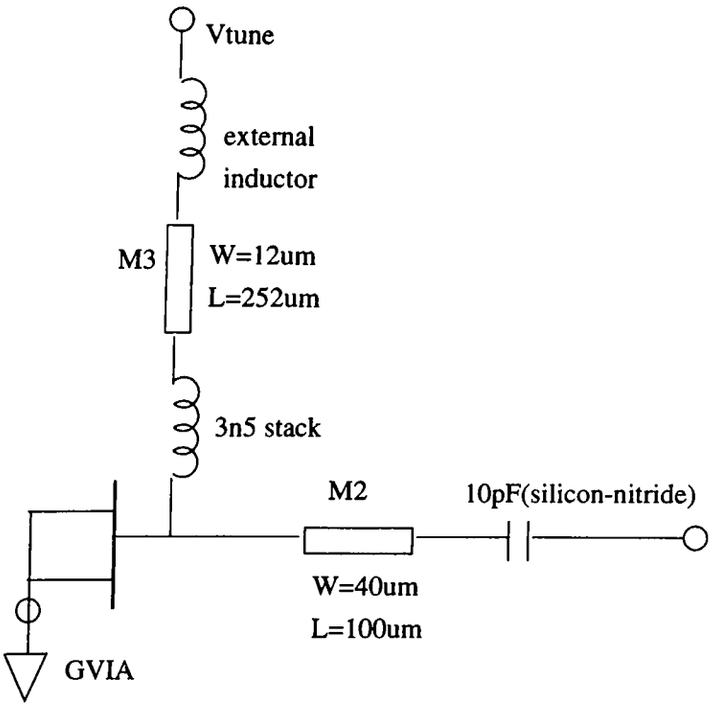

Figure 3.20: MMIC varactor with extra transmission lines for connections

	without t.lines		with t.lines	
$V_B(V)$	$C_V(pF)$	$R_V(\Omega)$	$C_V(pF)$	$R_V(\Omega)$
-8	.239	2.016	.227	6.5
-4	.28	2.61	.275	5.92
-3	.3	2.79	.298	5.71
-2	.34	3.2	.334	5.69
-1	.39	3.67	.4	5.63
-.5	.44	3.98	.463	5.61
0	.54	4.44	.588	5.697
.5	.77	5.68	.93	6.58
.65	1.87	13.56	2.48	14.18

Table 3.1: The MESFET varactor performance

Chapter 4

MONOLITHIC DESIGN

4.1 Feedback Techniques

In order to produce sustained steady-state oscillations at microwave frequencies, the active device must possess negative resistance. For two terminal devices, like IMPATT, Gunn diode and tunnel diode, etc., the negative resistance condition can be obtained by simply applying DC bias to the device. The three terminal devices such as bipolar devices and FETs, on the other hand, do not possess this property and the negative resistance condition has to be simulated by suitably coupling the input and the output ports of these devices. If the correct feedback circuit is added to a properly selected device configuration, oscillations can occur from very low frequencies to approximately f_{max} of the active device. There are two basic arrangements as shown in Fig. 4.1, for a general three terminal device. The device may be in common source, common gate or common drain arrangement. In the series-feedback arrangement, the feedback element is the common current-carrying element between the input output ports while in the parallel arrangement, it is the common voltage transforming element between the two ports. A combination of series and shunt feedback elements and higher order feedback elements can also be used (Fig. 4.2).

These feedback elements are usually reactive and can be in the form of lumped or distributed components.

Although too many arrangements are possible to improve the negative resistance seen at the resonator and the output ports, the most common technique

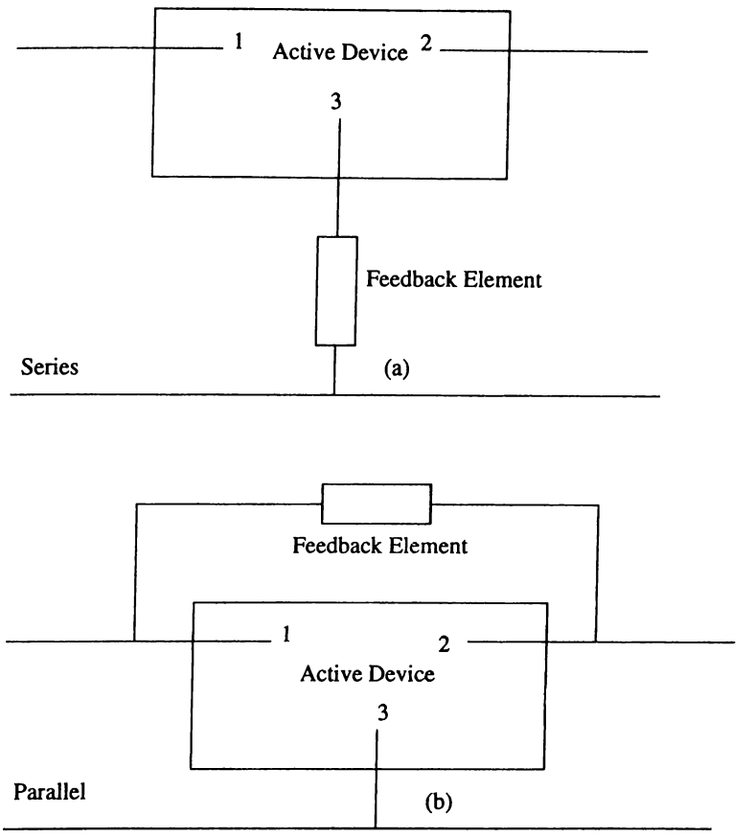

Figure 4.1: Feedback circuit arrangements: series (a), parallel (b)

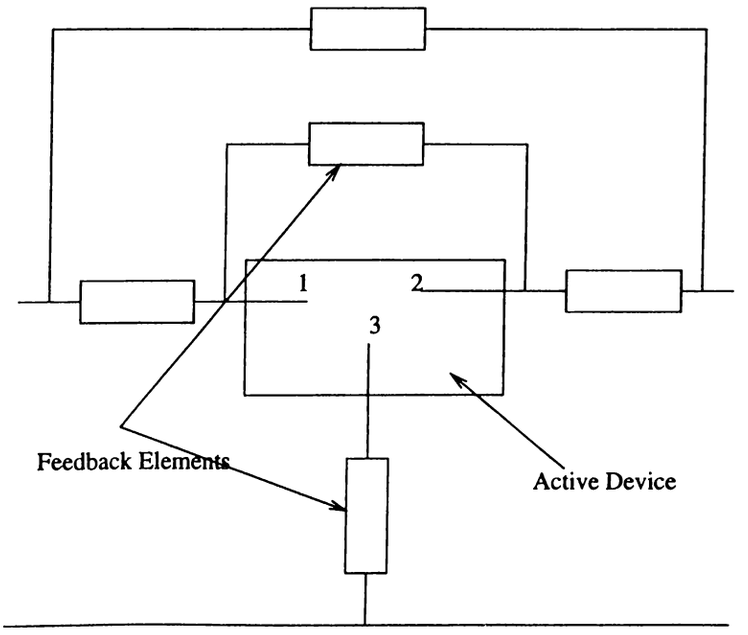

Figure 4.2: Compound feedback arrangement

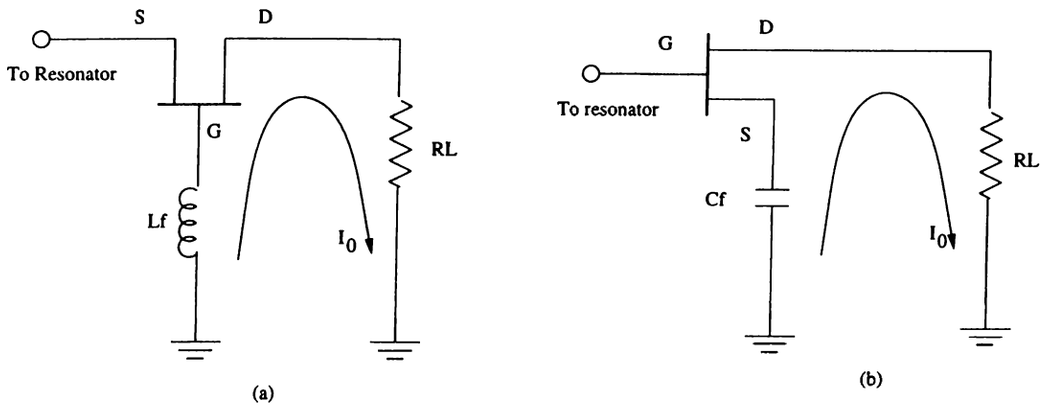

Figure 4.3: Feedback techniques: inductive(a), capacitive(b)

element can be capacitive or inductive depending upon the transistor whether it is common source or common gate. These topologies are given in Fig. 4.3.

Here, both circuits provide feedback by circulating the output RF current, I_0, through the feedback element. This current then, develops a voltage across the feedback element, which becomes part of the input (resonator) signal. Therefore, the feedback elements L_f and C_f take part in the feedback process. Thus, the quality factor of L_f and C_f must be as high as possible in order to minimize the extra loss in each cycle of the positive feedback process and to minimize the phase noise of the output signal. The value of L_f or C_f for a given configuration is optimized by using a simulation tool, such as LIBRA, TOUCHSTONE or S.COMPACT. Writing a simulation file for the basic circuit under consideration (Fig. 4.3), the optimum values of L_f or C_f can be obtained for a goal of maximum negative resistance at the input port over a band of interest.

In order to improve the negative resistance condition while increasing the bandwidth simultaneously, a reactive output matching network can be used. This network may be simply a shunt LC or a few order of matching network which transforms 50Ω load impedance to a smaller value or a filter which provides both the impedance transformation and the harmonic suppression. The goal of the optimizer is just to achieve the start-up oscillation conditions over the desired bandwidth. The variables are the feedback element, the output matching network elements, and some prime losses such as series resistances of physical elements which must be taken into account if possible and if the results are meaningful. Some nominal forward gain or loss should also be a goal of the optimization process, because excessive loss from the resonator to the load will cause that power generated at the resonator can not be transferred to the load.

4.2 Broadband VCO Circuit Topologies

There are three VCO topologies which are commonly used for broadband applications. The first one is the capacitive feedback topology as shown in Fig. 4.4. In this circuit, positive feedback is created by forcing the drain current into the gate by presenting a high reactance on the source using a capacitance. Since the feedback circuit is capacitive, the impedance seen by looking into the FET is also capacitive. To compensate the reactive part of this impedance, a series inductor is used, resulting an oscillation at a fixed frequency. Tuning is achieved by adding a varactor in series with the gate inductor.

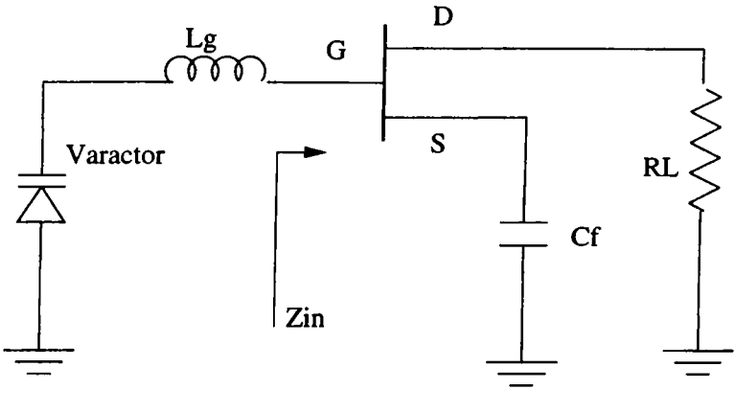

Figure 4.4: Common source, capacitive feedback VCO

The second topology is to use an inductive feedback (Fig. 4.5). For this structure the input impedance Z_{in} has positive reactive part and the varactor is used to show a negative reactance for phase cancelation. This topology is similar to the first one. The only difference is the tuning element, gate inductor or the source capacitor. Although they are very similar, the second topology is used for more broadband applications. An extra inductor parallel to the varactor magnifies the apparent capacitance ratio available from the varactor [8].

In order to design a more broadband VCO, a compound structure [10] is used, as the last topology (Fig. 4.6).

For all the topologies, the FET is usually biased to the point $I_d = I_{dss}/2$. This selection for drain current provides the best compromise among gain, saturated power, and low harmonic output. In this thesis, the first two topologies are concentrated on.

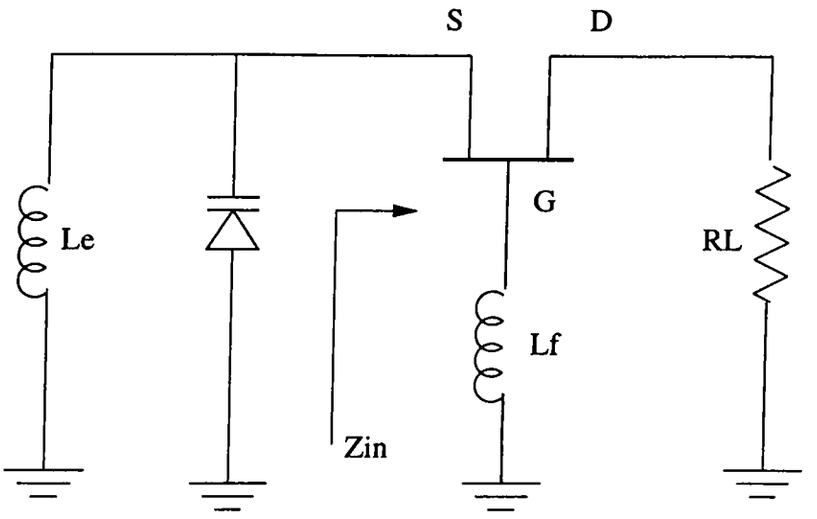

Figure 4.5: Common gate, inductive feedback VCO

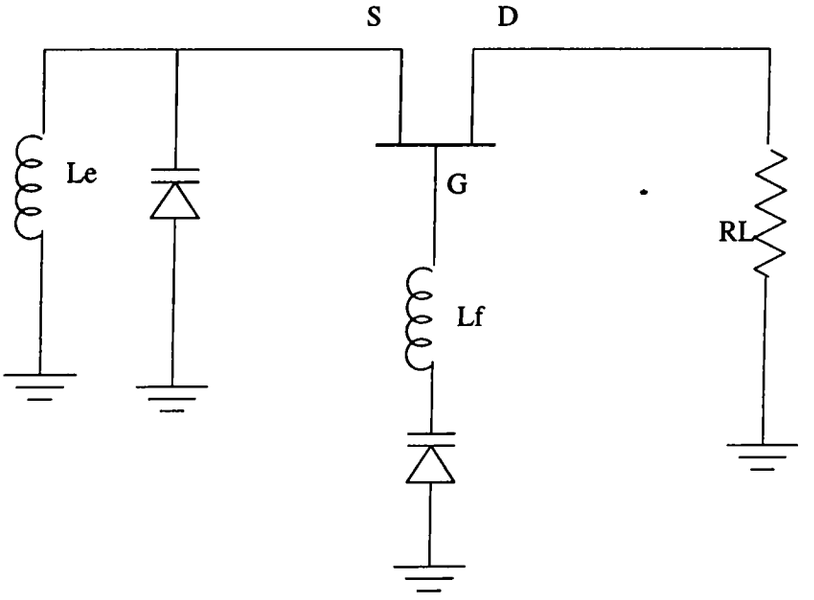

Figure 4.6: Double varactor VCO

4.3 Initial Design for Common Source Circuit Topology

Initial circuit topology including the bias circuitry and the coupling capacitor is shown in Fig. 4.7.

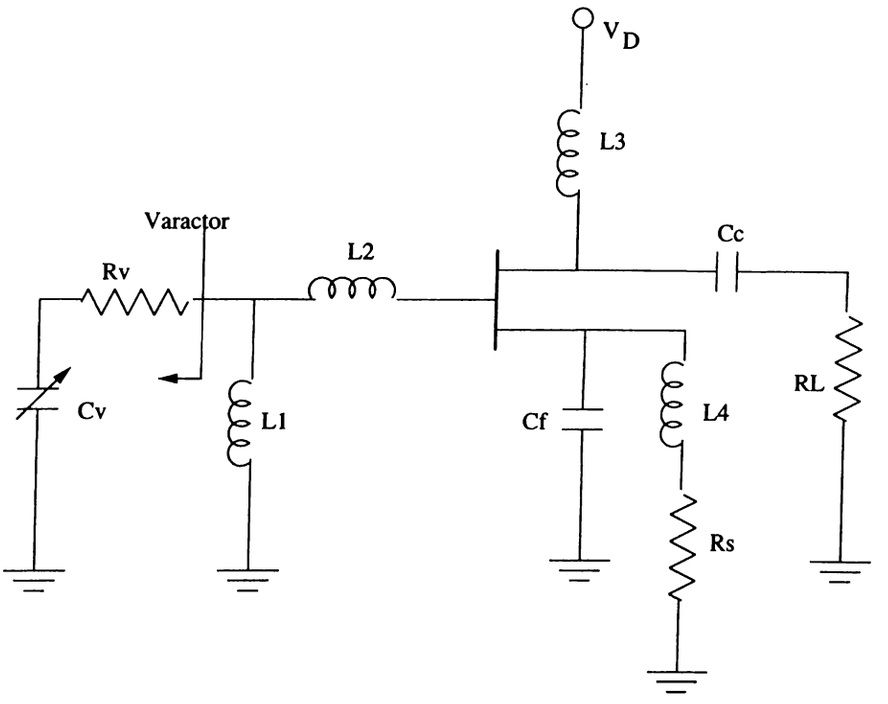

Figure 4.7: Initial capacitive feedback VCO topology

Here, the chokes L_3 , L_4 and the source resistor Rs conduct the bias current by self biasing the FET. The gate is DC grounded by inductors L_1 and L_2. L_1 may be a choke just to ground the gate for DC, or a small inductor for which may also be considered as a part of the resonator.

C_c is the coupling capacitor and is high enough to be short at operating frequency, L_2 is the series resonator inductor, and C_f is used for feedback purposes. The varactor is simply modeled as a variable capacitor and a series connected resistor.

4.3.1 Small Signal Design for Start-up Oscillations with GEC $4 * 75$ FET

As mentioned in section 3.4, a FET's small signal equivalent model includes intrinsic and extrinsic elements. This parameters have been measured by GEC Marconi with input RF signal levels which are at least 20dB down from the 1dB compression point. Table 4.1 gives the equivalent circuit parameters at Vds=5V and $I_d = I_{dss}/2$.

Parameter	4*75	4*150	2*100	6*50
$L_g(pH)$	28.57	57.15	53.1	28.0
$L_d(pH)$	17.7	35.4	14.5	25.0
$L_s(pH)$	15.75	15.75	15.75	19.1
$R_g(\Omega)$	1.6	3.2	4.3	0.85
$R_d(\Omega)$	1.2	0.6	4.62	3.25
$R_s(\Omega)$	2.38	1.19	3.19	1.05
$R_{ds}(\Omega)$	270	135	423	286
$R_i(\Omega)$	3.25	1.63	4.75	4.70
$C_{dg}(pF)$	0.0272	0.0489	0.0166	0.0319
$C_{gs}(pF)$	0.275	0.490	0.179	0.309
$C_{ds}(pF)$	0.0616	0.1048	0.0458	0.062
$g_m(mS)$	35.2	70.3	23.6	34.4
$\tau(pS)$	2.83	2.83	2.89	2.77

Table 4.1: Small-signal equivalent circuit parameters at $V_{ds} = 5V, I_{ds} = I_{dss}/2$

Although the foundry supplies the small signal models for all the models of $2 * 100$, $4 * 150$, $4 * 75$, and $6 * 50$, the large signal model is supplied for only $4 * 75$ model. Thus, in this thesis, all the VCOs are designed by using $4 * 75$ model.

In small signal design, the first step is to write a TOUCHSTONE (or LIBRA, S.COMPACT) file for the basic circuit topology shown in Fig. 4.8. By optimization, the start oscillation conditions of this circuit can be extended over the entire band of interest. The varactor diode is modeled as 3Ω series resistance, R_v and a variable capacitance, C_v ranging from 0.2 pF to 2pF for initial design, and it is included as a part of the oscillator circuit, so that all varactor losses are accounted for directly.

First, the optimizer tries to maximize negative resistance, $(Re[Z_{in}])$, and forward gain $dB(S_{21})$. Next, the varactor's capacitance, C_v, is varied through

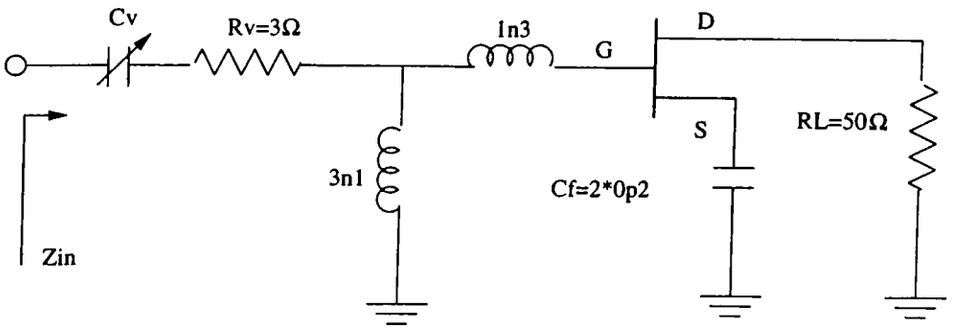

Figure 4.8: The schematic representation for two port small signal simulation

its operating range to ascertain that the entire frequency range will be covered (i.e., $Im(Z_{in}) = 0$).

The Fig. 4.9 shows the simulation result for $C_v = 0.2pF$ which defines the maximum oscillation frequency, and similarly $C_v = 2.0pF$ determines the lowest end of frequency-band for start-up oscillations. Notice that both the reactance and the resistance slopes are positive that satisfies the stable oscillation condition

$$\frac{\partial I_m(Z_{in})}{\partial w} > 0 \tag{4.1}$$

and,

$$\frac{\partial R_e(Z_{in})}{\partial w} > 0 \tag{4.2}$$

Note also that the gain is approximately maximum at the oscillation frequency ; for instance dB(Gain)=8.15 at fosc=11.6GHz which is the maximum gain for $C_v = 0.2pF$. While tuning the variable capacitor from 0.2pF to 2pF, this maximum gain point shifts to the lower oscillation frequencies which is 9 GHz and the gain is 11.65 dB for 2pF.

For this simulation, the electrical models of Marconi components have been used. Thus, spiral inductors, silicon nitride and polyimide overlay capacitors are modeled as small sub-circuits composed of ideal lumped elements. As can be seen in section 4.6, the Q of the polyimide capacitor increases when it's prime capacitance value increases in opposite to the planar inductors.

In this circuit, the feedback capacitor is composed of two 0.2pF polyimide capacitors connected in parallel. Although smaller capacitors can be used to get higher negative resistance, 0.4pF (0.2pF + 0.2pF) and 0.5pF (0.25pF + 0.25pF) capacitors have been preferred for the first and the second VCOs, respectively. There are two main reasons:

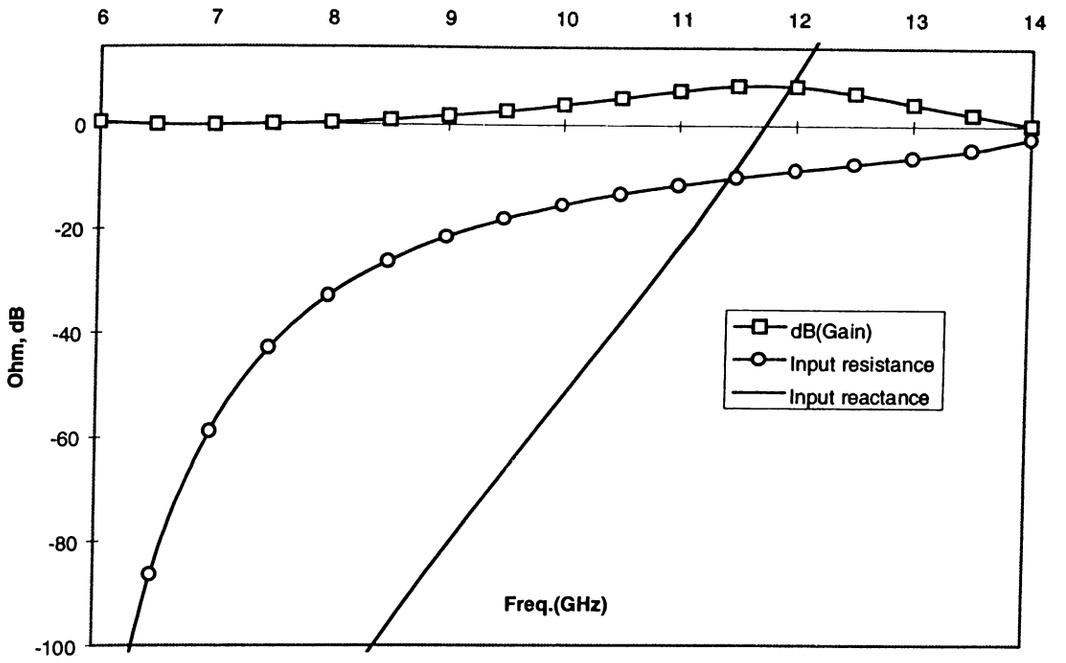

Figure 4.9: Start-up oscillation condition for C_v=.2pF

1. As mentioned above, smaller the prime capacitance is smaller the quality factor which causes an increase in the loss of the resonator loop. As a result, the phase noise of the output signal is magnified.
2. In order to obtain a desired band of oscillation the series inductance (L_1) must be increased while decreasing the value of the C_f, due to the phase cancelation condition at oscillation frequency. Higher the prime inductance will cause a smaller quality factor which result an extra loss in the resonator loop, resulting again a phase noise. On the other hand, if the value of C_f is further increased then the circuit may not oscillate.

The reason why two capacitors are connected in parallel instead of using a single capacitor, is just to use both of the source terminals of the GEC FET to minimize the parasitic effects. Table 4.2 shows the start-up oscillation frequencies of the VCOs, having feedback capacitances: $2 * 0p2$ and $2 * 0p25$, respectively. In section C.3 (Appendix C), the small signal simulation file of the first VCO (with $2 * 0p2$ feedback) is given.

Feedback capacitance	$C_V(pF)$	$f_0(GHz)$
$2 \times 0p2$	2.0	9.0
	0.2	11.6
$2 \times 0p25$	2.0	8.8
	0.2	11.5

Table 4.2: The band of oscillations for the initial VCOs with $2 \times 0.2pF$ and $2 \times 0.25pF$ feedback capacitances

4.4 Initial Design for Common Gate Circuit Topology

Fig. 4.10 shows the initial circuit topology. The bias circuitry is the same as the previous circuit topology. Here, only the L_2 provides DC grounding for the gate, whereas the common source topology needs an extra inductor L_1 connected between L_2 and the ground.

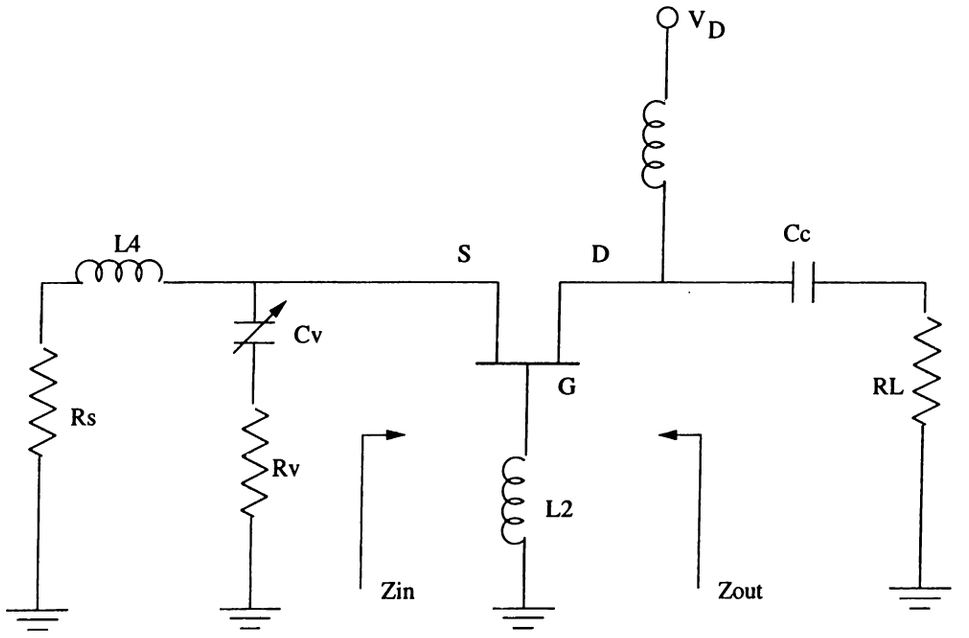

Figure 4.10: Initial common gate circuit topology

From the RF point of view, the shunt inductor L_1 may cause undesired low frequency oscillation especially for small values of C_f if L_1 is not properly selected (Fig. 4.7). Here, no such a problem exists due to direct grounding by L_2.

4.4.1 Small Signal Design for Start-Up Oscillations

Although two port device method given in section 2.3 can be applied for this topology, one port device method have been chosen to be familiar to this method (Fig. 4.11).

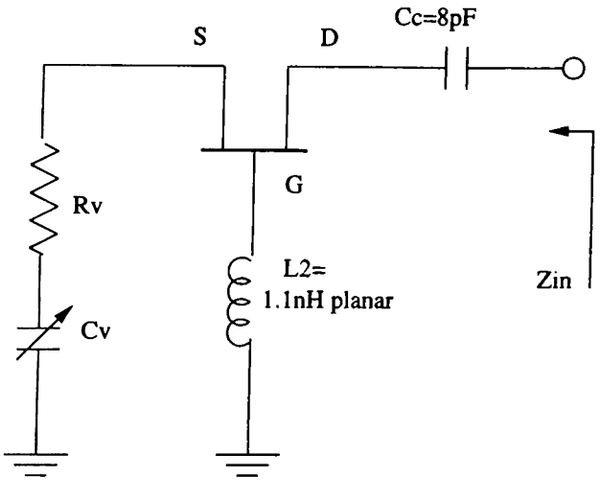

Figure 4.11: Schematic representation for one port analysis

Here, L_2 is optimized in order to obtain the maximum bandwidth which covers the frequency band of interest while taking care of the output negative resistance to exceed 50Ω load resistance. If the value of the feedback inductor L_2 decreases, a larger bandwidth can be obtained, but this results in a shift to upper frequencies and a considerable reduction in negative resistance, which may stop the oscillation. During the optimization equivalent models of elements are used and the optimum value for L_2 is found as 1.1nH for the initial design.

If an extra inductor is connected in parallel to the varactor diode as in Fig. 4.12, the beneficial effect of magnification in the apparent capacitance ratio available from the varactor is seen [8]. For its small values, the band of oscillation becomes wider. However in this case , parasitic problems dominate, which limits the bandwidth. The reduction in the value of this inductor cause another problem: negative resistance decrease in magnitude. To show the effect of this inductor which is optimized as 1.1nH, Table 4.3 is given.

Fig. 4.13 shows the start-up oscillation condition for the circuit given in Fig. 4.12 for $C_v = 0.6pF$. Notice that the negative resistance is maximum when the phase cancelation occurs at the start-up oscillation frequency of 9.4 GHz.

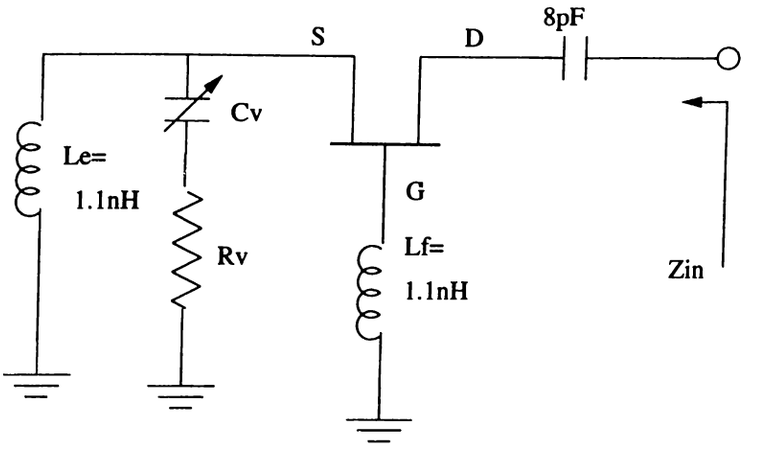

Figure 4.12: Bandwidth improvement by L_e

	$C_V(pF)$	$f_0(GHz)$
with L_e	2.0	8.55
	0.2	12.4
without L_e	2.0	8.5
	0.2	10.55

Table 4.3: The band of oscillations for the initial VCO with inductive feedback

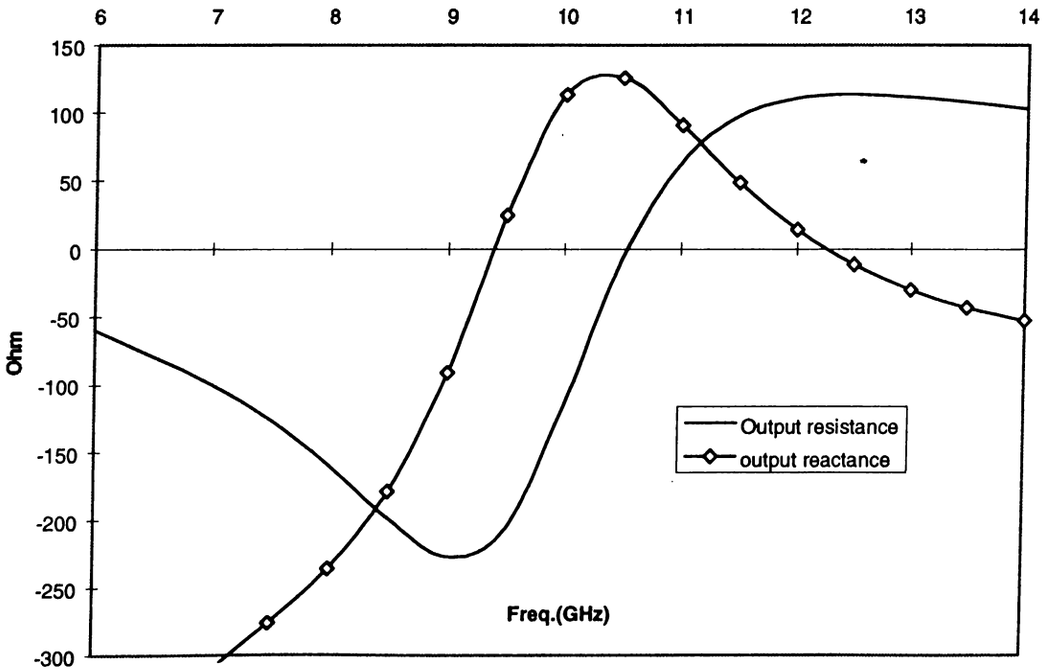

Figure 4.13: Start-up oscillation condition for C_v=.6pF

4.5 Improvement of Varactor's Quality Factor

In the previous section, the varactor diode has been assumed as a variable capacitor C_v and a series R_v having a constant value of 3Ω . However this is not the case for implementing the complete circuit; varactor model must be replaced with MMIC components. As mentioned in section 3.7, the MMIC varactor implemented by $4 * 75$ GEC FET has no constant resistance value, rather it varies between approximately 2Ω and 15Ω depending upon the applied tuning voltage. The loss of the varactor is very high especially for positive tuning voltages which correspond to the higher capacitance values. In order to reduce the loss a small polyimide capacitor is connected in parallel to the varactor (i.e., between the gate and the source of the varactor FET) shown in Fig. 4.14.

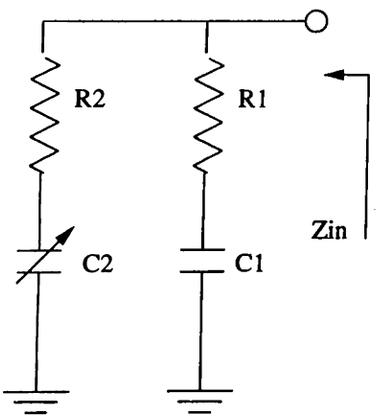

Figure 4.14: Quality factor improvement

If $R_1 = R_2 = R$ assumed for simplicity,

$$\frac{R_e(Z_{in})}{R} = 1 - \frac{2C_1C_2}{4R^2w^2C_1^2C_2^2 + (C_1 + C_2)^2} < 1 \tag{4.3}$$

for instance, if $C_1 = .1pF, C_2 = 1.5pF, f = 8.5GHz$, and $R = 5\Omega$

$$\frac{R_e(Z_{in})}{R} = 0.883 \tag{4.4}$$

Notice that the loss resistance is reduced by about 12% . However, in order not to reduce the capacitance ratio too much, the polyimide capacitor must be in the order of 0.1-0.2 pF.

4.6 Equivalent Models for GEC Passive Elements

If it is desired to get accurate results from the simulation tools (TOUCHSTONE, LIBRA, COMPACT), the circuit elements must be defined with their parasitics. Some of the commonly used lumped elements are: spiral and stacked inductors, polyimide and silicon-nitride capacitors.

A simple lumped equivalent circuit supplied by GEC is capable of modeling planar spiral behavior up to 80% of the S_{21} resonant frequency. Fig.4.15 shows the graph of the self resonance frequency versus prime inductance for 12/12 GEC planar inductors (i.e., trackwidth=12μm, trackgap=12μm).

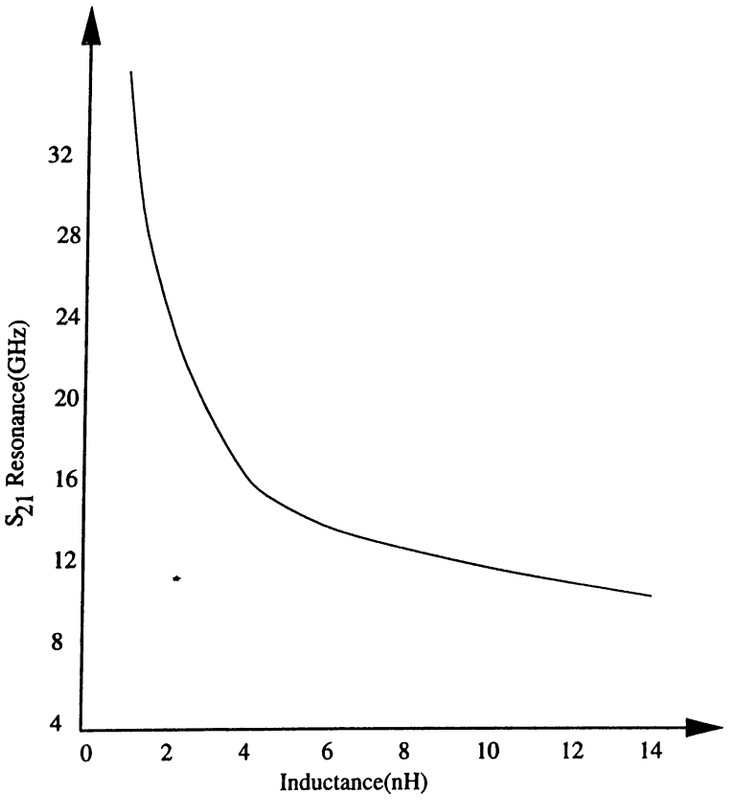

Figure 4.15: Prime inductance versus frequency of the first S_{21} resonance for planar inductors

These inductors are formed using M3, second level metal only. The M3 is joined to M2 using a M2-M3 interconnect. After passing to M2 layer, connection to the center of the inductor is made using an under-pass in M2 first metal layer.

The lumped equivalent circuit is given in Fig.4.16. In this circuit L is the

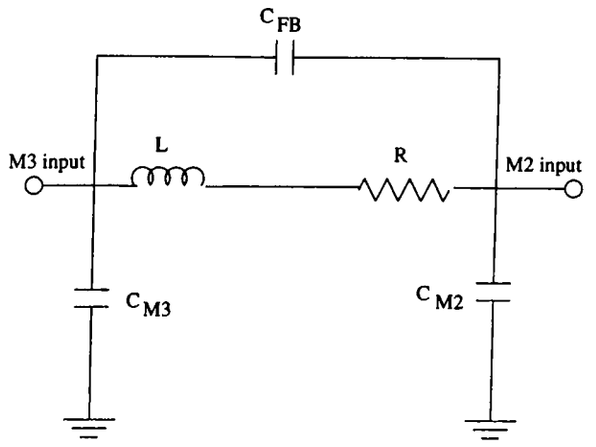

Figure 4.16: Planar spiral equivalent circuit

prime inductance, C_{FB} is the feedback capacitance, R is the loss resistance, C_{M3} and C_{M2} are the shunt capacitances for the first and the second level metalizations. The parasitic terms are all related to the number of turns and are given given by polynomial expressions. These expressions can be found in GEC F20 Design Guide.

A stacked inductor consist of two spirals overlaid one on top of the other. The lower spiral is constructed using M2 first level metal and the upper spiral is constructed using M3 second level metal. The two spirals are connected in the center using a M2-M3 interconnect. The isolation is provided by the dielectric materials, polyimide and silicon-nitride. Since the first level metalization M2 is more lossy, compared to the M3 layer, stacked spirals are low-Q inductors and have too many parasitics resulting a lower self-resonance frequency. On the other hands, stacked inductors occupy relatively small area. Thus, they are widely used in bias circuits. Fig.4.17 shows the equivalent circuit.

Polyimide capacitors are formed by using both M2 and M3 layers together, M3 forms the capacitor top plate whereas M2 forms the bottom plate. The dielectric between the plates is composed of polyimide and silicon-nitride. Since both of dielectric layers are used together, these capacitors are used for the values less than 1.3pF. A lumped element equivalent circuit is capable of modeling capacitor behavior up to 20GHz. The equivalent circuit is shown in Fig.4.18 . These are the lossy capacitors and the loss resistances are much more higher for low prime capacitance values.

Silicon-nitride capacitors are again formed using M2 and M3 metal layers but the dielectric is silicon-nitride only. A polyimide dielectric via is used to

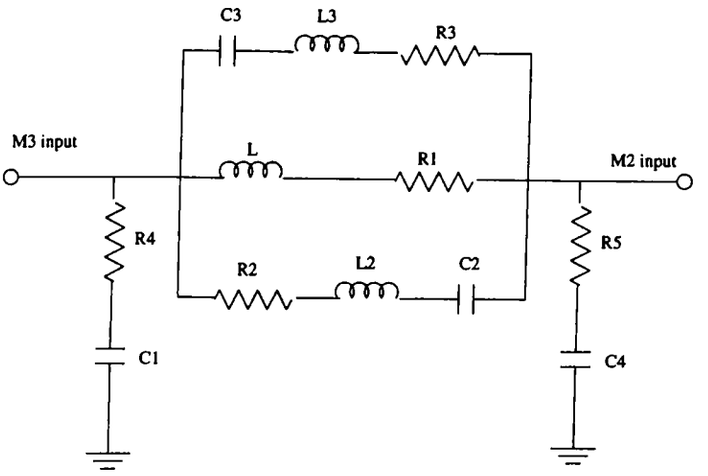

Figure 4.17: Stacked spiral equivalent circuit

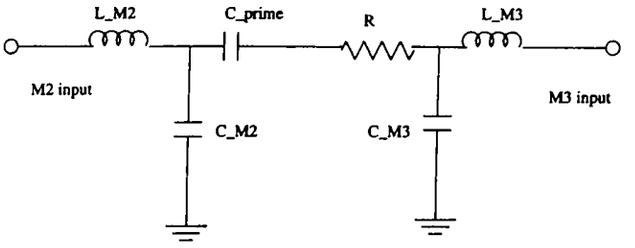

Figure 4.18: Overlay capacitor equivalent circuit

remove the polyimide from the capacitor. The area of the polyimide via defines the prime capacitance value. The same model is used as in the case of the polyimide capacitors (Fig. 4.18). The main differences are:
-Silicon-nitride capacitor exhibits symmetric RF behavior, so the M2 and M3 parasitics are the same.
-The loss element R is negligible compared to the loss of the polyimide capacitor.

4.7 Nonlinear Design

Large signal analysis is necessary to observe the steady state oscillations. However under that condition the bias must be included to simulate the oscillator. By using the voltage-current curves (Fig. 3.4) obtained by LIBRA, the bias resistor, R_s, is found as about 28Ω for the drain current of $I_d = I_{dss}/2$. However, by considering the series choke inductor's loss resistance which is about 6Ω for 5.8nH prime inductance, the bias resistor is chosen as 22Ω.

The nonlinear analysis were carried out by using harmonic balance techniques (Appendix A) in LIBRA. The most important element for oscillation simulations in LIBRA is the oscillator test element (OSCTEST) (Appendix B). This element allows you to inject an AC voltage, at the fundamental frequency, into the feedback loop of the oscillator circuit and determine the oscillation frequency, the output power, and the output spectrum. The element was developed so that it does not affect the natural response of the circuit under simulation.

4.7.1 Nonlinear Design For Capacitive Feedback Topology

The schematic representation of a VCO is shown in Fig.4.19 for nonlinear simulations. Here, the varactor circuit is realized by a $4 * 75$ FET (drain and source grounded), a coupling capacitor and choke inductors. The steady state oscillation frequency is found as follows:
- Tune the varactor by applying a specific tuning voltage
- Increase the amplitude of the injected signal until the magnitude of R (the ratio of the voltage extracted from the feedback loop to that of the voltage used to stimulate the feedback loop) is unity and the angle of R is zero, meaning that the steady state conditions are reached at the oscillation frequency. The nonlinear simulation file is given in section C.3 (Appendix C), as an example.

For the positive tuning voltages corresponding to higher capacitance values for which the negative resistance at the input port is maximum in magnitude, the harmonic contents especially the second harmonic level is very high, just 3-4dB below the carrier. In other words, the output waveform is highly distorted as shown in Fig.4.20. The reason of such distortions is that:
The drain current is simply expressed as,

$$I_d = I_{dss}(1 - \frac{V_{gs}}{V_p})^2 \tag{4.5}$$

and V_{gs} is composed of DC and AC terms,

$$V_{gs} = V_{GS0} + Acoswt \tag{4.6}$$

and,

$$I_d = I_{dss}(1 - 2\frac{V_{gs}}{V_p} + \frac{V_{gs}^2}{V_p^2}) \tag{4.7}$$

$$I_d = I_{d0} + i_d \tag{4.8}$$

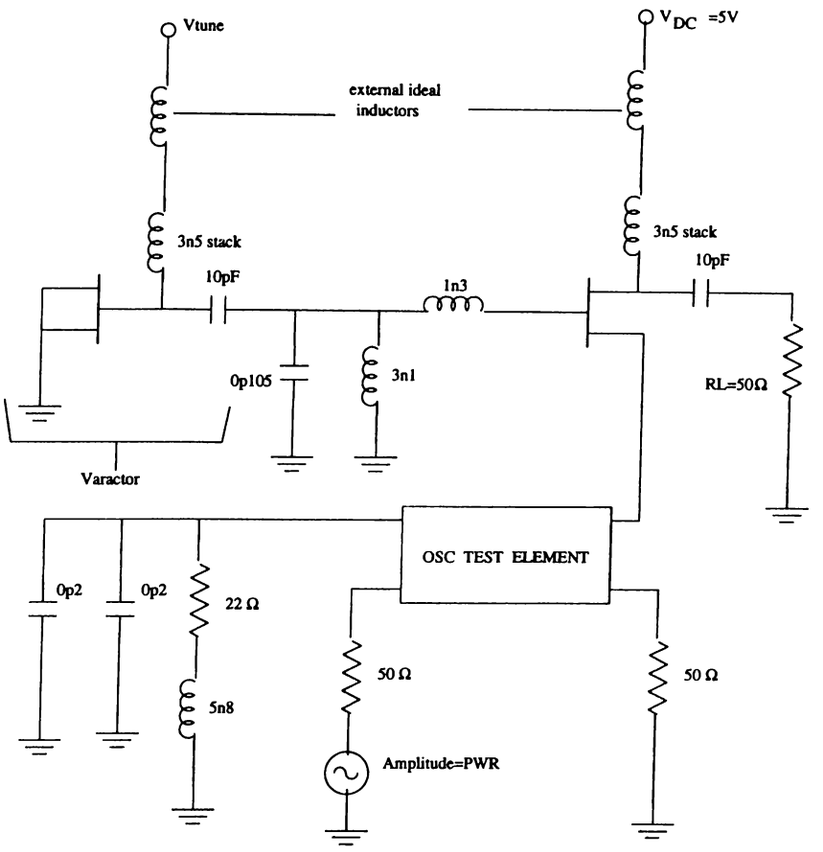

Figure 4.19: Schematic representation of a VCO prepared for nonlinear simulation

$$I_{d0} = I_{dss}(1 - \frac{2}{V_p}V_{GS0} + \frac{1}{V_p^2}V_{GS0}^2 + \frac{1}{4V_p^2}A^2) \tag{4.9}$$

$$i_d = I_{dss}(-\frac{2A}{V_p}coswt + \frac{2V_{GS0}A}{V_p^2}coswt + \frac{A^2}{4V_p^2}cos2wt) \tag{4.10}$$

The third term of the last expression (Eq. 4.10) represents the second harmonic distortion of the drain current. Increasing the negative resistance, the RF signal rises-up, resulting a second harmonic distortion.

However, Curtice Cubic model have been used in LIBRA for nonlinear simulations, hence the current expression relating the drain current to the input voltage is in cubic form (Eq. 3.1). The coefficient A2 which is responsible for the quadratic term, also causes the second harmonic distortion.

In order to kill the harmonic oscillations, a harmonic filter, such as low-pass filter(LPF) or band-pass filter(BPF) can be used. A BPF not only suppresses the harmonic oscillations but also overcome the low frequency oscillations caused by undesired resonances in the circuit. In addition, it is not necessary to suppress the harmonics so much by the filter. Since the filter is highly

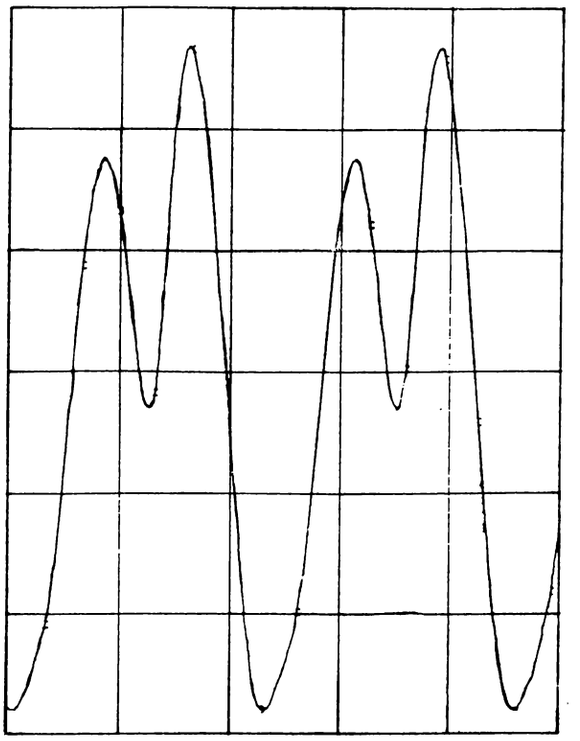

Figure 4.20: Distorted output waveform

reflective for the harmonics, the reflected power is regained and transferred to the fundamental harmonic. This process compensates the insertion loss of the filter, and the harmonic suppression increases as if there exist a higher order of filter. The filter elements are optimized to maximize the output power, the bandwidth, and to fit the oscillation band to the desired point.

Two VCOs with BPFs are given in Fig.4.21, and their oscillation frequencies, fundamental and second harmonic power levels for certain tuning voltages are tabulated in Table 4.4. The S-parameters of the filters in 50Ω system with GEC components are shown in Figures 4.22 and 4.23, respectively.

Although GEC library does not bring limitations on capacitors, inductor values can not be chosen arbitrarily. An inductor element must be one of the GEC defined element which have discrete inductance values (unless one uses a nonstandart inductor by rounding the transmission lines). Thus, the circuits are designed with these inductors. 3.5nH stacked spirals were used as the choke inductors. Therefore, a small area is occupied, compared to 3.6nH spiral inductors. In addition, the low frequency oscillations are killed because of low quality factor of stacked inductors. Since silicon-nitride capacitors are not available up to 1.3pF, polyimide capacitors are used as the feedback capacitors.

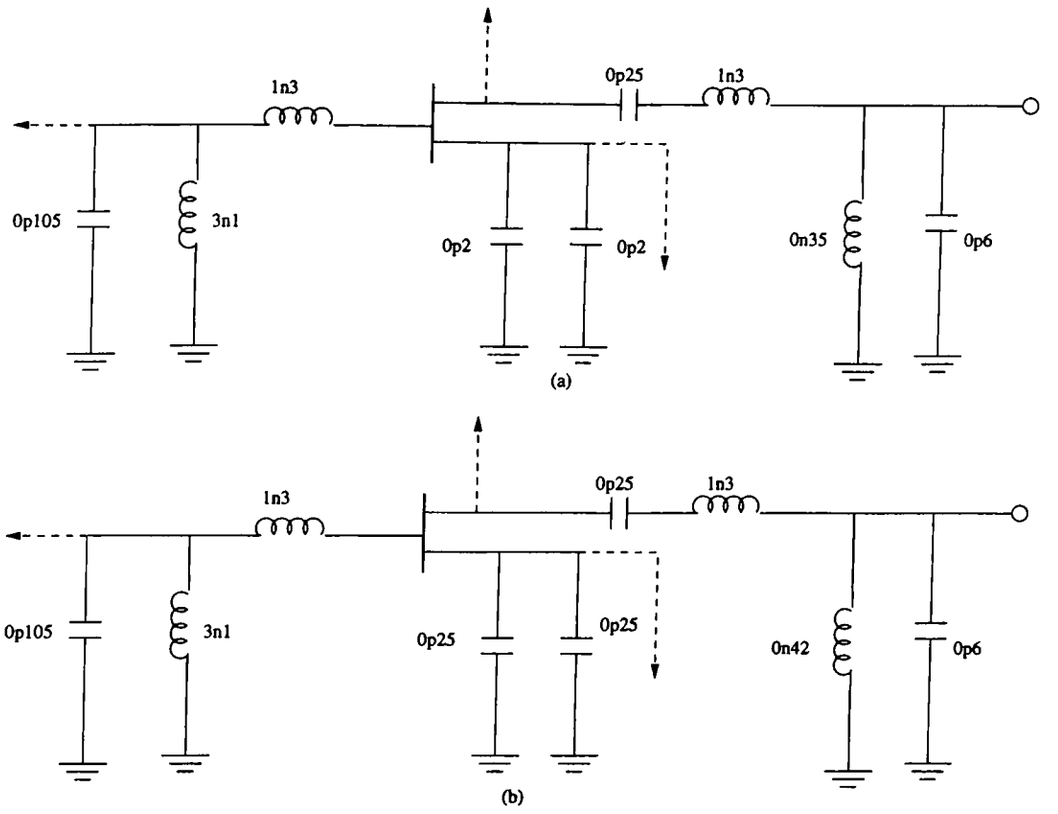

Figure 4.21: Two capacitive feedback VCOs with BPFs

$V_{tune}(V)$	$f_0(GHz)$	$P_f(dBm)$	$P_2(dBm)$
1	8.74	10.7	-20.12
0	9.54	10.35	-23
-2	10.16	13.36	-38.7
-10	10.58	13.77	-41
1	8.53	11.77	-17.3
0	9.47	10.51	-21.0
-2	10.11	13.5	-31.5
-10	10.52	14.0	-37.77

Table 4.4: The oscillation performances of the VCOs given in Figures 4.21.a and 4.21.b, respectively

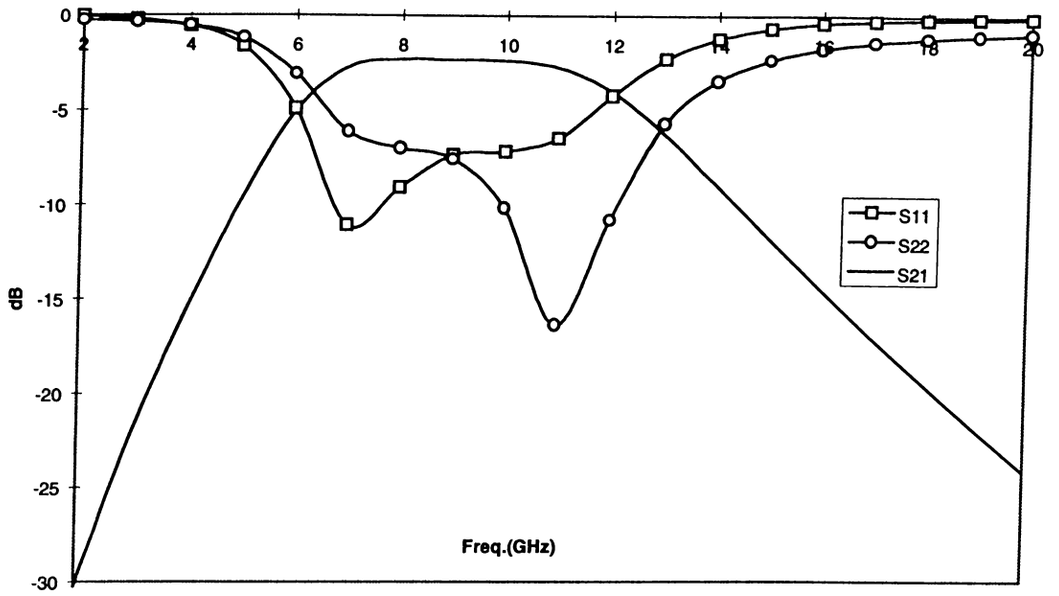

Figure 4.22: Filter response of the circuit in Fig. 4.21.a

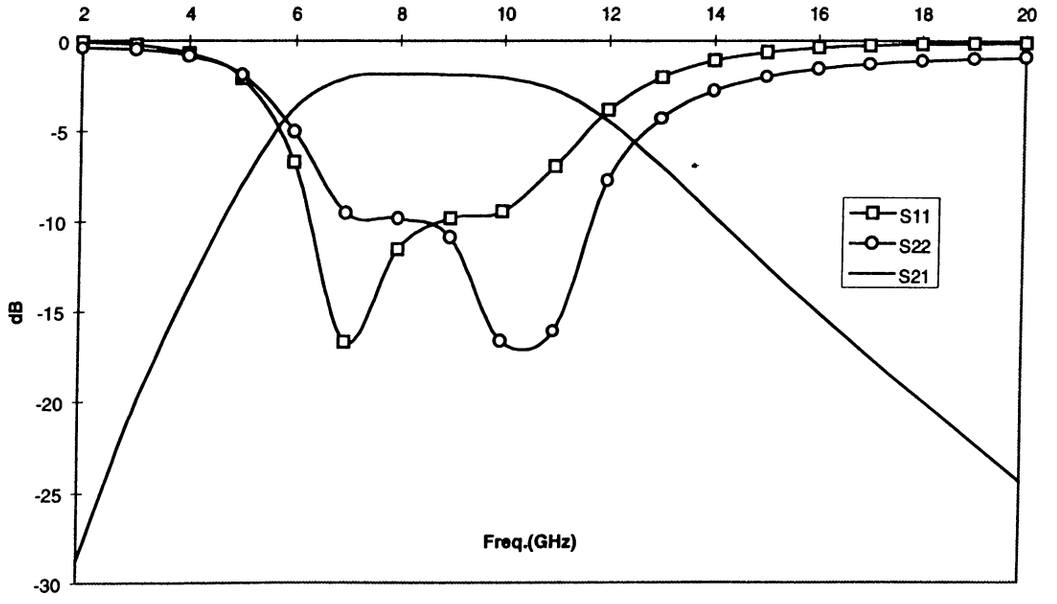

Figure 4.23: Filter response of the circuit in Fig. 4.21.b

4.7.2 Nonlinear Design For Inductive Feedback Topology

The simulation is done in a similar manner as in the case of the capacitive feedback topology, by taking into account seven harmonics of the oscillation frequency (Fig. 4.24).

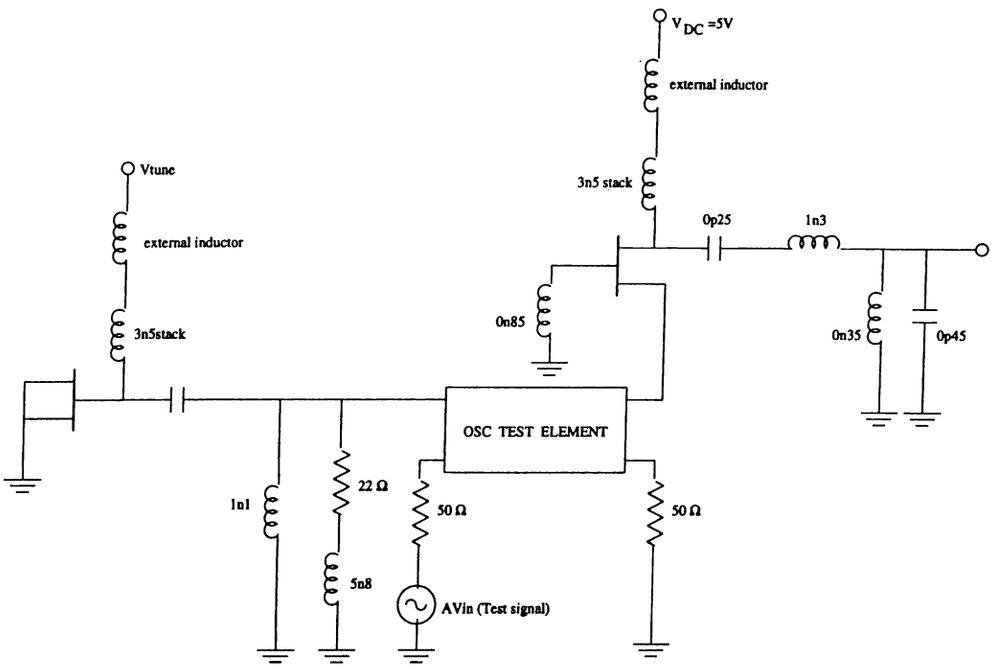

Figure 4.24: The schematic representation of the VCO prepared for LIBRA

This topology is very sensitive to parasitic elements, and for the low oscillation frequencies multiple resonances occur near the high end of the oscillation band. In order to overcome this problem, the tuning ratio of the varactor has been reduced by using a 1.5pF coupling capacitor instead of 10pF with a small sacrifice of the bandwidth. Even for the reduced tuning ratio, the circuit has a bandwidth of 3.24 GHz ranging from 9.41 GHz to 12.65 GHz. The simulation results for certain tuning voltages are tabulated in Table 4.5 .

$V_{tune}(V)$	$f_0(GHz)$	$P_f(dBm)$	$P_2(dBm)$
1	9.41	13.81	-19.04
0	10.26	14.18	-19.33
-10	12.65	10.79	-36.9

Table 4.5: The oscillation performance of the VCO given in Fig. 4.24

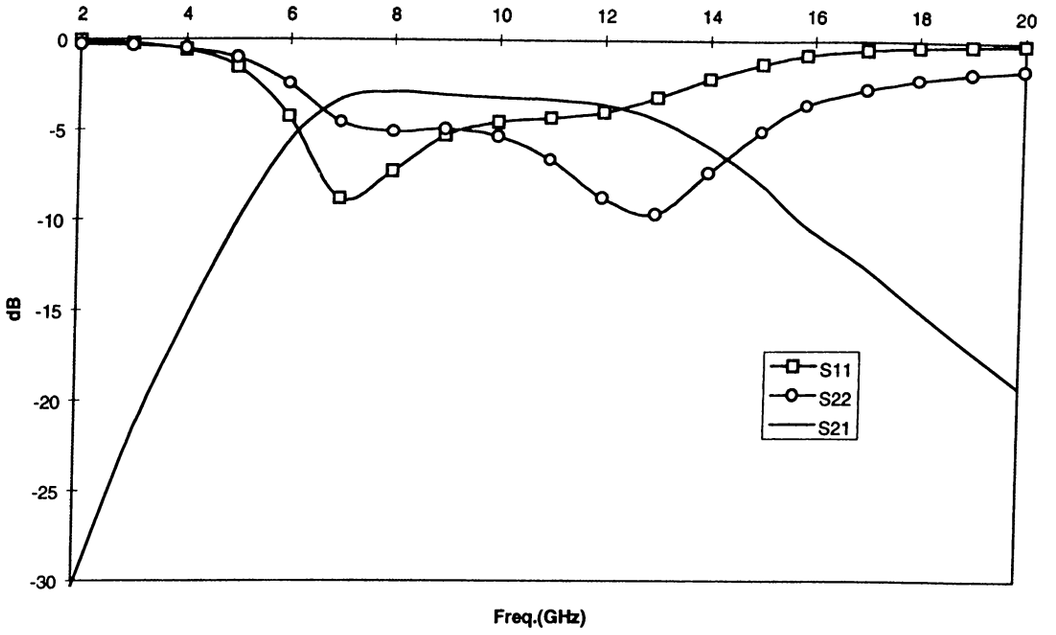

Figure 4.25: The filter response of the common-gate VCO

The filter is a second order band-pass filter and optimized with the VCO itself (Fig. 4.25). Notice that the return loss does not exceed 10 dB in order to increase the output power, whereas this is not the case for an amplifier circuit.

4.8 Analysis of The Finished Layouts

All the analysis mentioned so far, are carried out by considering parasitics of lumped elements. However some extra elements must be taken into account after the layout design. These elements, such as transmission lines for connections, pads for DC biasing and RF input or output, and via holes for grounding, etc., are required to realize the circuits physically.

The layouts of the three VCO were designed on a single chip by using the F20 library in CADENCE's layout tool. The overall the chip area including the border is about $3mm^2$. The design steps to finish the layout can be illustrated by a flowchart (Fig. 4.26).

Because of the layout limitations, the lumped elements were tuned and some transmission lines were included. The overall layout was minimized while preserving the design specs. In order to increase the reduced output power resulting from the losses of the transmission lines, the source bias resistor were reduced to 20Ω for the first two VCOs. The series loss resistance of transmission

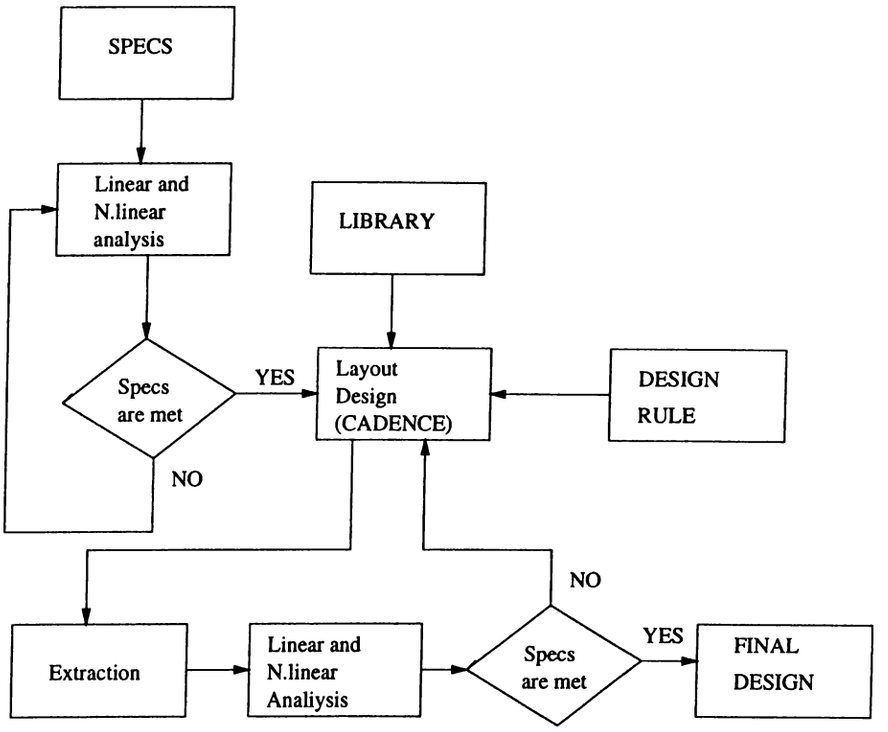

Figure 4.26: Design flowchart

lines with different lengths and widths are tabulated in Table 4.6. The bias resistors are the nichrome resistors which are more appropriate for small values and more linear than the mesa resistors. The schematic representation of the final designs (Appendix C) are shown in Figures 4.27, 4.28,and 4.29.

If the layout is finished for a design, the circuit is reanalyzed with the new circuit parameters extracted from the layout. The new circuit parameters mean the modified elements, via holes, bond pads, transmission lines, bends, etc,. A via hole is modeled as a .02nH inductor and a series .2Ω resistor to the ground, whereas .048pF shunt capacitor represents a bond pad for the simulation. In order to simulate transmission lines in M2 and M3 layers, different polynomials are given for the each layer. Although the characteristic impedance is just a function of the width of the line under consideration and it is non-dispersive over the F20 frequency range, the effective dielectric constants varies with frequency. For detailed information GEC Design Manual can be investigated.

The large signal simulations were carried out on the final VCO circuits. In order to find start-up oscillation conditions a small AC voltage (.001V) is applied in the large signal simulations. Outputs obtained from the large simulations are given in Table 4.7,8,and 9. See Appendix C for further informations about the performances of the final designs.

$Length(\mu m)$	R_{loss}@$3.5GHz(\Omega)$	R_{loss}@$8GHz(\Omega)$	R_{loss}@$10GHz(\Omega)$
100	.168	.209	.227
200	.336	.419	.457
400	.674	.849	.935
600	1.016	1.305	1.457
800	1.363	1.801	2.053
1000	1.718	2.356	2.765
1200	2.082	2.995	3.656
1400	2.459	3.754	4.828
1600	2.849	4.683	6.459
2000	3.684	7.402	12.784
100	.093	.121	.134
200	.186	.243	.269
400	.373	.493	.550
600	.562	.759	.86
800	.755	1.051	1.217
1000	.952	1.38	1.65
1200	1.155	1.762	2.2
1400	1.364	2.223	2.942
1600	1.583	2.795	4.0
2000	2.052	4.524	8.34

Table 4.6: The losses of the transmission lines in the M3 metalization layer with $12\mu m$ and $24\mu m$ track-widths, respectively

$V_{tune}(V)$	$f_{start}(GHz)$	$f_0(GHz)$	Output Power (dBm)
.5	9.75	8.88	10.9
0	10.0	9.48	13.64
-1	10.2	9.94	14.13
-2	10.3	10.09	14.26
-3	10.35	10.17	14.34
-4	10.38	10.23	14.37
-5	10.40	10.27	14.40
-6	10.42	10.30	14.39
-7	10.45	10.33	14.37
-8	10.47	10.35	14.36
-9	10.49	10.37	14.35
-10	10.5	10.40	14.34

Table 4.7: The oscillation performance of the first VCO

$V_{tune}(V)$	$f_{start}(GHz)$	$f_0(GHz)$	Output Power (dBm)
.5	9.56	8.71	9.95
0	9.82	9.32	13.14
-1	10.04	9.78	14.13
-2	10.14	9.93	14.26
-3	10.19	10.01	14.37
-4	10.21	10.07	14.41
-5	10.24	10.11	14.44
-6	10.26	10.14	14.46
-7	10.29	10.17	14.47
-8	10.31	10.19	14.47
-9	10.33	10.21	14.46
-10	10.35	10.23	14.46

Table 4.8: The oscillation performance of the second VCO

$V_{tune}(V)$	$f_{start}(GHz)$	$f_0(GHz)$	Output Power (dBm)
1.0	9.34	8.965	13.22
0	10.46	10.44	12.77
-1	11.0	11.10	12.04
-2	11.23	11.41	11.44
-3	11.42	11.6	11.06
-4	11.59	11.73	10.65
-5	11.71	11.82	10.42
-6	11.8	11.92	10.14
-7	11.84	11.98	9.98
-8	11.95	12.04	9.80
-9	12.02	12.10	9.61
-10	12.05	12.14	9.45

Table 4.9: The oscillation performance of the third VCO

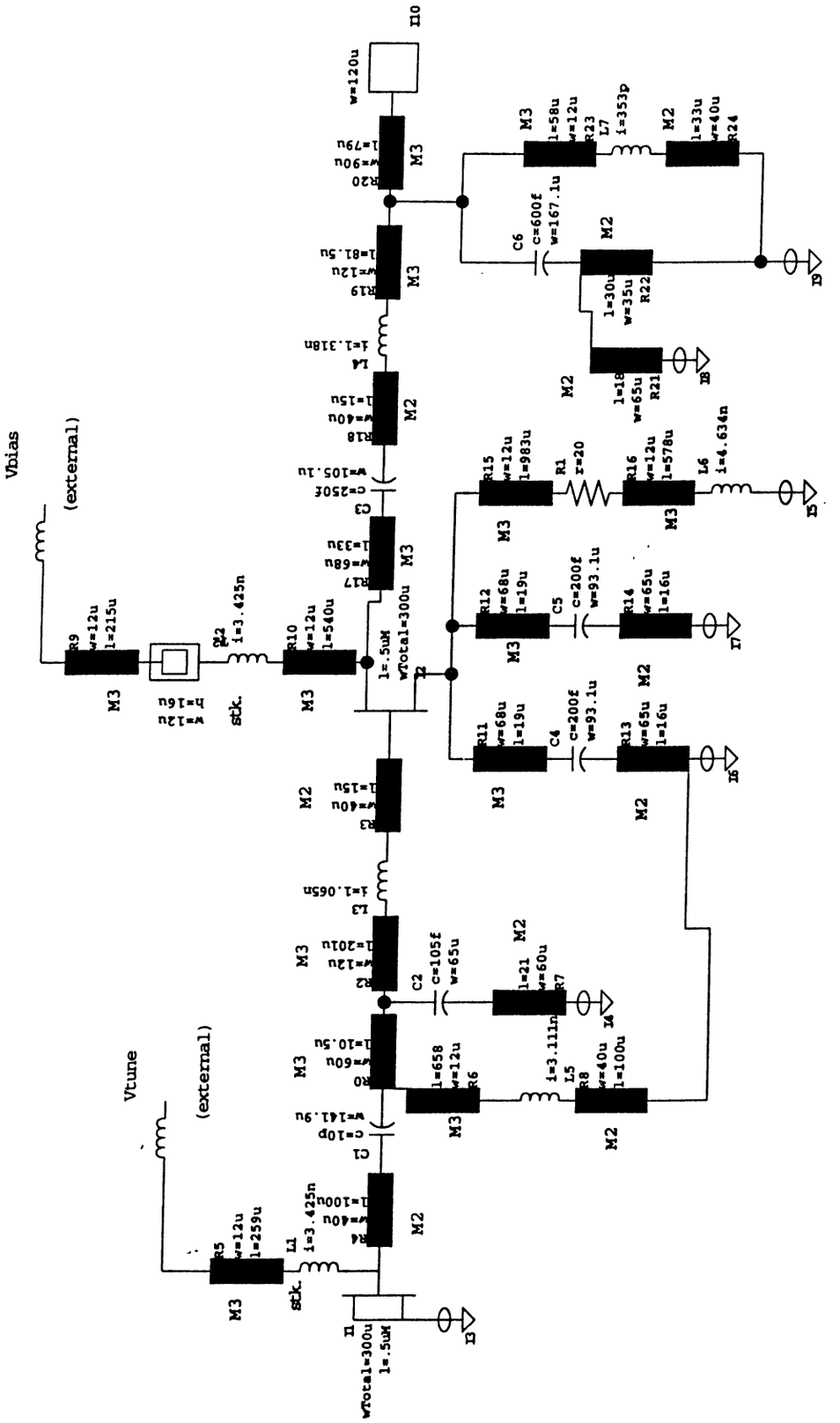

Figure 4.27: The first VCO's schematic representation

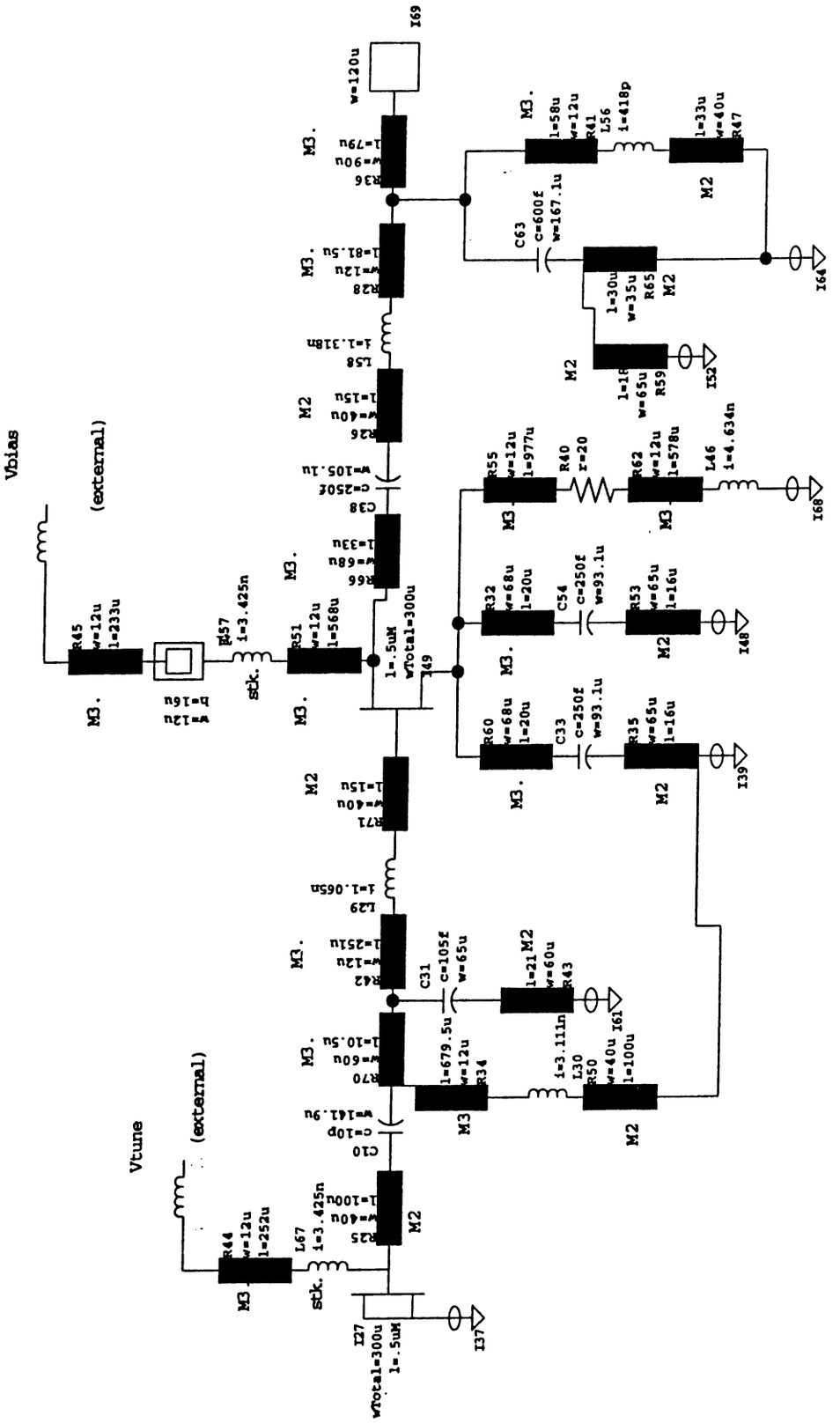

Figure 4.28: The second VCO's schematic representation

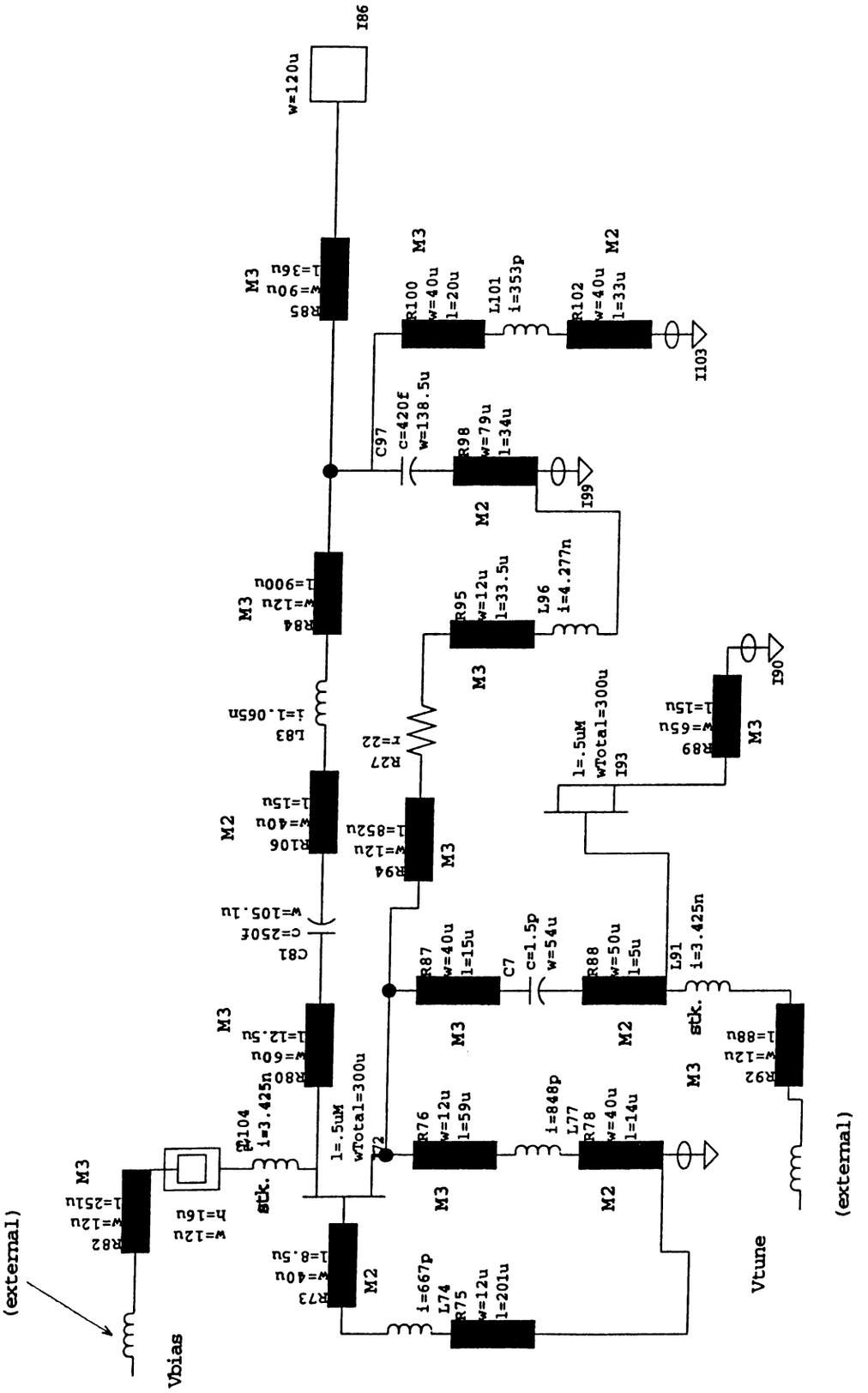

Figure 4.29: The third VCO's schematic representation

Chapter 5

CONCLUSION

In this work, three VCOs were designed using MMIC technology and sent for fabrication. Firstly, the design topologies and the design procedure were selected. According to this procedure, the small signal simulations were carried out by using TOUCHSTONE, as the first step. Then, using the harmonic balance utility of LIBRA, the nonlinear simulations were carried out. CADENCE was the unique tool for preparing the layouts.

After fabrication some important performances such as, power variation, tuning linearity, harmonic suppression of the VCOs will be measured.

In order to advance in the MMIC VCO design, double varactor and switching mode VCOs may be implemented for wideband applications. The buffered structures may be considered to improve the isolation and the output power.

Appendix A

HARMONIC BALANCE ANALYSIS

The CAD of linear microwave circuits can be considered a well-settled matter, as is shown by the extensive technical literature on this subject, and by the commercial availability of powerful general-purpose CAD programs. On the other hand, general problem of nonlinear circuit problems still exist.

A nonlinear circuit can be solved in three ways: fully in time domain or in frequency domain or a combination of these two methods can be applied.

The SPICE operates fully in the time domain. The drawbacks of SPICE are: (1) the lack of an optimizer; (2) dispersive transmission lines and discontinuities, tee junctions (distributed elements) can not be analyzed; and (3) the slow execution speed related to the time-domain approach.

If a circuit is weakly nonlinear, it can be analyzed via relatively straight forward techniques, such as power series or Volterra series. In Volterra series simulation, the actual computation time is somewhat independent of the values of the components used in a circuit. However once the number of harmonics goes up, Volterra series expansion also becomes very time consuming. Volterra series has the limitation that the degree of nonlinearity must be mild.

The harmonic balance method is a hybrid time and frequency domain approach that combines a time domain nonlinear device model with the lumped and distributed linear elements defined in the frequency domain. It is an iterative technique seeking to match the frequency components of the current in a set of the branches joining the nonlinear and linear parts of the circuit.

The important utility in the harmonic balance method is to take advantage of linear programs such as, S.COMPACT, TOUCHSTONE which handle all the microwave components accurately. The microstrip and stripline discontinuities are of greatest interest. This calculation is done in the frequency domain and thus is fast and efficient. An interface is required which transfers the information to the nonlinear portion of the program, which uses the harmonic balance method, being computed in the time domain.

A general equivalent circuit that describes many types of nonlinear microwave components is depicted in Fig. A.1.

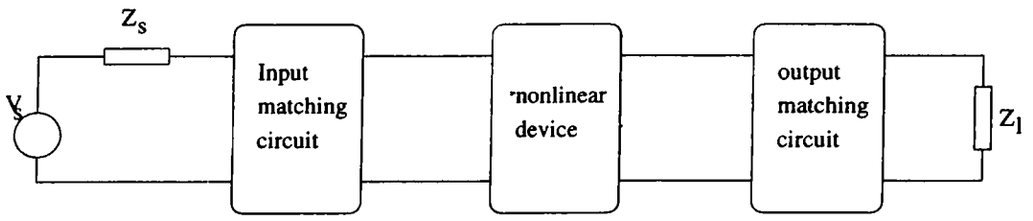

Figure A.1: A typical nonlinear circuit block diagram

The circuit consist of a nonlinear solid-state device that is connected to a load and a source of large signal excitation. Fig. A.2 shows the seperation between the frequency-domain and time-domain portions.

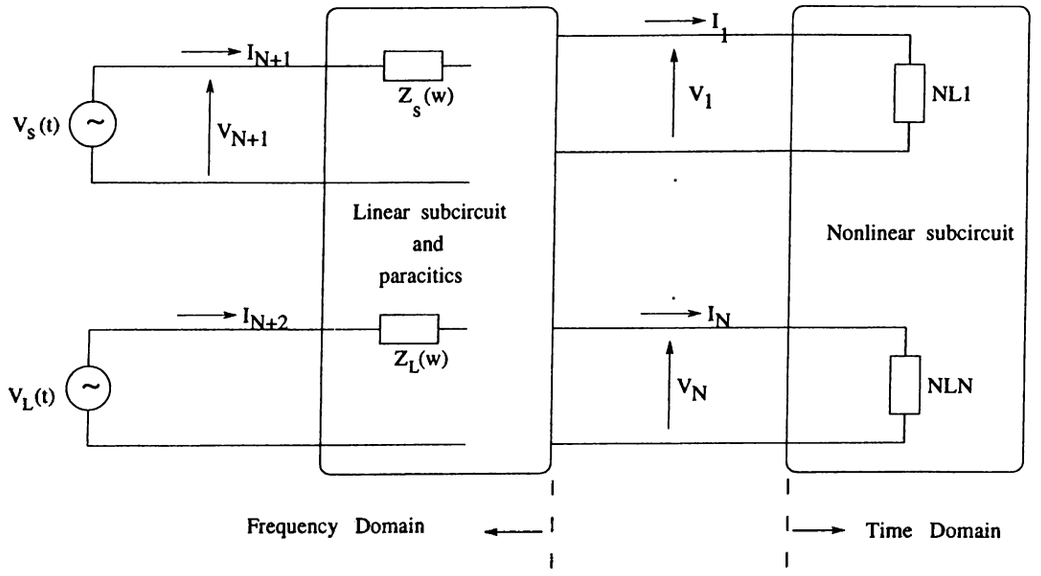

Figure A.2: Partitioned nonlinear circuit

In the analysis, the frequency domain is passed through only once; the admittance matrix of the linear subnetwork is computed and stored for subsequent use. In the time domain, the state-variable harmonics are first used

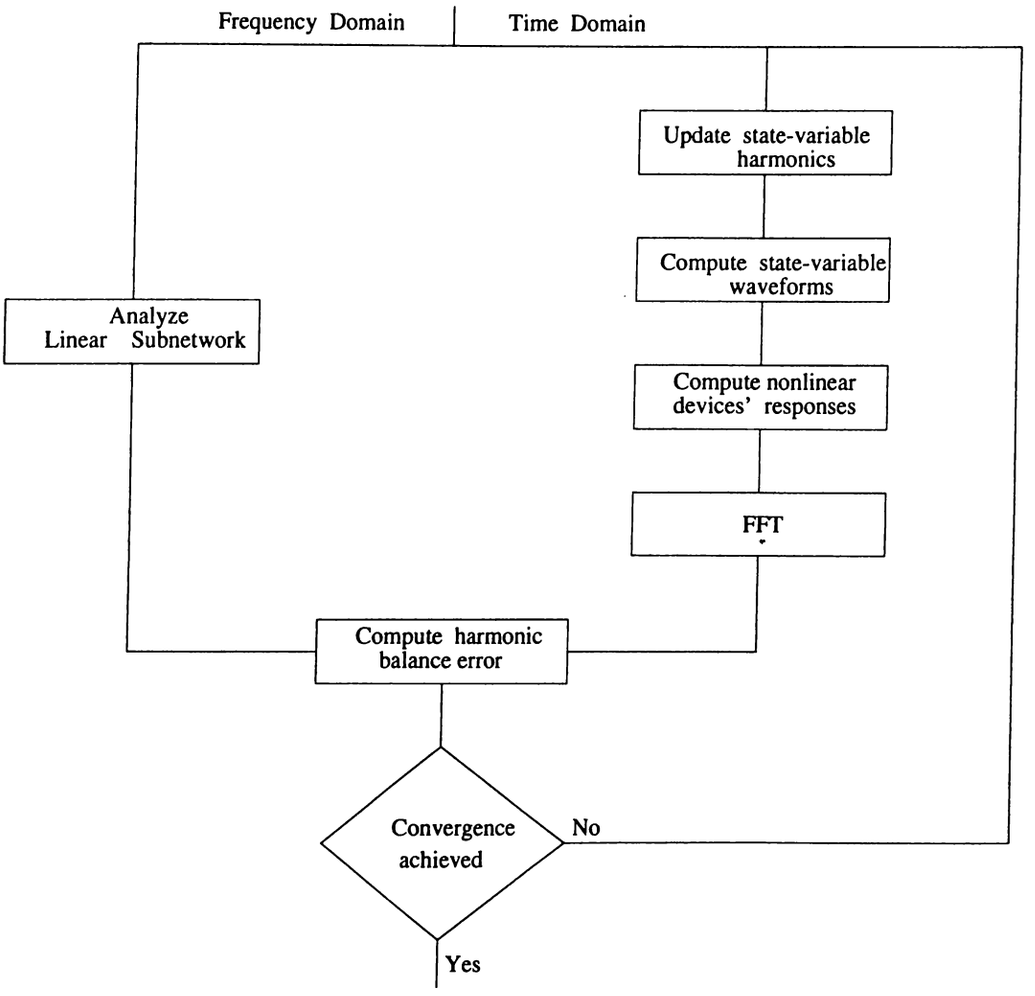

Figure A.3: Flowchart of harmonic balance analysis

to compute the corresponding time-domain waveforms, and these are fed to nonlinear device equipment to produce the time-domain device port voltages and currents. Voltage and current harmonics are described by one-or two-dimensional fast Fourier transforms (FFTs) for the cases of single-tone and two-tone excitation, respectively.

The voltage harmonics are used to generate linear current harmonics via the linear subnetwork admittance matrix. The two sets of current harmonics are finally compared to produce individual harmonic balance errors and a combined harmonic balance error to be used in a convergence test. All the harmonic balance analysis can be expressed by a flowchart (Fig. A.3).

Appendix B

VCO CIRCUIT SIMULATION USING TOUCHSTONE AND LIBRA

B.1 Linear Simulations

The linear simulation is carried out by just observing the input impedance and the gain plots of the circuit under consideration. If $Im[Z] = 0$, $Re[Z] < 0$ and a considerable gain is obtained by optimization tool of TOUCHSTONE , the frequency at which these conditions are satisfied, is nothing but the start-up oscillation frequency.

B.2 Oscillator Test (OSCTEST) Element

This element is symbolled as in Fig. B.1, and the syntax is:

```
      OSCTEST   n1 n2 n3 n4
where parameters,
      n1, n2 = input and output nodes;
      n3 = node for injecting the test signal;
      n4 = node for sampling the returned test signal.
```

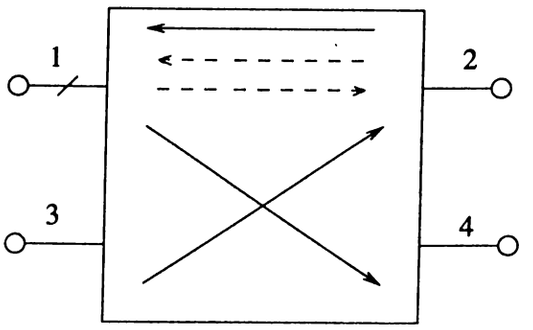

Figure B.1: Symbol of OSCTEST element

The OSCTEST element is used to analyze oscillator circuits using harmonic balance algorithm. It provides a path for injecting a test signal into an oscillator circuit for stimulating oscillations. The specialized directional coupler has zero electrical length and is invisible to normal circuit simulation. It allows injection of a fundamental frequency test signal, blocks the fundamental frequency flow in the feedback path, and monitors the signal returned by the feedback path relative to the test signal.

The fundamental frequency test source and the source resistor should be connected at node 3 and the fundamental frequency signal returned by the feedback path should be measured at node 4 by connecting a sampling resistor at node 4. Nodes 1 and 2 are used to connect the OSCTEST element in the feedback path.

The scattering matrix of OSCTEST at the fundamental frequency is different from its scattering matrix at all the harmonics (including DC). All ports of OSCTEST are matched at all frequencies. Both scattering matrices of OSCTEST are pure real. The scattering matrix at the fundamental frequency is as follows:

$$[S_{fundamental}] = \begin{pmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix}$$

and at all other frequencies:

$$[S_{harmonic}] = \begin{pmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix}$$

In other words, transmission between certain nodes of OSCTEST depends upon whether the frequency is the fundamental oscillation frequency or one of the harmonics (including DC).

Only the fundamental frequency is transmitted from node 3 and node 2. All frequencies are transmitted from node 2 to node 1 and from node 1 to node 4. All frequencies, except the fundamental frequency, are transmitted from node 1 to node 2. All other transmission coefficients are zero.

Oscillator analysis using the OSCTEST element assumes a single-tone excitation. If the OSCTEST element is used with multi-tone excitation, the results are unpredictable.

The S-parameters of the OSCTEST element are referred to the reference resistance Z_0. It is important that the source and sampling resistances used with the OSCTEST elements are the same as Z_0 for accurate oscillator analysis.

B.3 Nonlinear Measurements

In order to find the steady state oscillation frequencies and to get the information about the spectrum, the nonlinear measurements are necessary. This is achieved by modifying the linear circuit file for nonlinear measurements. The use of the PWR parameter in the VAR block is a trick that allows optimization of the AC voltage source, which will be injected into the feedback loop of the circuit.

The CIRCUIT BLOCK is modified to insert the OSCTEST element into the source feedback loop. The first part of OSCTEST should be connected to the circuit side of the device, the second port is connected to the device, the third and fourth ports are the signal input and output, respectively, and are connected to the loads in the SOURCE block which is used for harmonic balance, DC or DCTR simulation.

Modify the SOURCE block as follows:

```
SOURCE
    OSC1  VS_DVDD  20 0 DC^VD
    OSC1  IND  40 20 L=10
    OSC1  VS_DD10D 10 0 DC^VB
```

```
OSC1  IND 10 100 L=10
OSC1  VS_AVIN  51 0 AMP^PWR  F^F1
OSC1  RES_RIN 50 51 R=50
OSC1  RES_RFB 60 0  R=50
OSC1 RES_RLOAD 400 0 R=50
```

VIN and RIN represent the AC voltage source used as the injection signal. This signal is fed into OSCTEST port 3. The RFB resistor terminates the fourth port of OSCTEST and is used to measure the feedback signal. The load resistor is used to terminate the output of the oscillator and is used in making power measurements, and it is not used in linear analysis.

Add the OUTVAR and OUTEQN blocks. The new blocks added after the SOURCE block are as follows:

```
OUTVAR
   VIN = OSC1 VFC 50 0 H1=1
   VFB = OSC1 VFC 60 0 H1=1
OUTEQN
    R = VFB/VIN
```

where,
VFC: a frequency selective complex voltage measurement at the indicated node.
H1=1: the indication that the fundamental frequency is being measured.
VIN: a measurement of the stimulating signal.
R: the ratio of the voltage extracted from the feedback loop to that of the voltage used to stimulate the feedback loop. It is this ratio's magnitude and angle that indicate when the condition for oscillation exists.

The OUT block is modified as follows to provide tabular and graphical display of the desired measurements:

```
OUT
   OUTEQN  MAG[R]  SCN
   OUTEQN  ANG[R]  SCN
   OUTEQN  MAG[R]  GR2
   OUTEQN  ANG[R]  GR2

   OSC1    PT_POSC  400  0  R=RES_RLOAD  H1=1  SCN
```

```
OSC1    PS_POSC  400  0  R=RES_RLOAD        SCN
OSC1    PS_POSC  400  0  R=RES_RLOAD        GR3
OSC1    V_OUT    400                       GR4
```

MAG[R] and ANG[R] provide the primary data to determine if the condition for oscillation exists. The total output power PT, output spectrum PS, and output voltage V, are also provided.

Since the nonlinear analysis uses the harmonic balance technique, we must specify the number of harmonics, NH, to include in the simulation.To determine the nonlinear frequency band and NH, the following three steps are used, providing the accurate simulations.

1. To find the approximate frequency of oscillation:

Setting the NH=3 reduces the simulation time and allows you to find a small band surrounding the actual oscillation frequency.

Use the nonlinear simulation, then display the appropriate grids to find the frequencies where the ANG[R] goes from + to - angle.

If the MAG[R] at these frequencies is > 1.0 then the amplitude of VIN will have to be increased to find the actual frequency.

In certain types of oscillations, the phase remains relatively constant as VIN varied; while in other types, the phase change significantly. Frequencies that bracket the actual oscillation frequency are selected and phase change with VIN is assumed.

2. To adjust VIN: The value of VIN is adjusted while viewing GR2 and performing 'RF Sweep' in the split screen mode. VIN is changed until the MAG[R] is <1.03.

Once this condition is achieved, NH is set to improve the accuracy of the measurement.

3. To determine NH: The narrow band has been found, and MAG[R] is sufficiently small, determine how many harmonics should be included in the simulation for accurate results. The value selected for NH is determined by the amount of distortion in the output waveform. Before setting on the number of harmonics, a higher harmonic case must be examined whether significant distortion is present or not.

Appendix C

SIMULATION FILES, RESULTS and FINISHED LAYOUTS

The results were obtained from the TOUCHSTONE and the LIBRA by carrying out the linear and nonlinear simulations. The section C.1 shows a simulation file for LIBRA to simulate the varactor circuit at constant frequency, 10 GHz for different tuning voltages. A TOUCHSTONE simulation file for the linear analysis is shown in section C-2. The varactor loss resistance were assumed as 3.0 ohm, constant value. Table C-1 shows how one can find the start-up oscillation frequency, in a tabular manner. As an example of nonlinear simulations, a LIBRA file is given in section C-3.

Figures C.1, C.2 and C.5, C.6 illustrate how the steady state oscillations are reached while increasing the injected signal level for 0.5 V and -10 V tuning voltages. The output waveforms and the harmonic contents are depicted in Figures C.3, C.4 and C.7, C.8.

Some performances of the each VCO are given in a triple groups of figures extending from C.9 to C.17.

Figures C.18, C.19, C.20 show the layouts of the first, the second and the third VCOs, respectively. The overall layout of the chip is given in Fig C.21. All the layouts were drawn by using CADENCE (Artist).

C.1 Varactor Simulation File

The varactor capacitance and the series resistance are found by simply taking the ratio of the voltage across the gate and the source to the current flowing into the gate. The capacitance and the resistance values are found in pF and Ω by compiling the following LIBRA simulation file:

```
DIM
RES OH
COND /OH
IND NH
CAP PF
LNG UM
TIME PS
ANG DEG
VOL V
CUR MA
PWR DBM

VAR
PWR=.1
VB=.65

CKT

cap 1 0 c=.048
def1p 1 pad

ind 1 2 l=.02
res 2 0 r=.2
def1p 1 gvia

ind 1 3 l=3.425
res 3 4 r=9.53
cap 1 8 c=.0376
ind 8 9 l=.96
res 9 4 r=15
res 1 6 r=2.754
ind 6 7 l=.948
```

```
cap 7 4 c=6.115e-3
res 1 2 r=30
cap 2 0 c=.035
res 4 5 r=30
cap 5 0 c=.042
def2p 1 4 3n5stack

ind 1 2 l=20.41e-3
cap 2 4 c=10
ind 4 5 l=20.41e-3
cap 2 0 c=25.275e-3
cap 4 0 c=25.275e-3
def2p 1 5 10psi

GAASFET_AGEC 10 11 12 [MODEL=GEC4*75]
IND 1 10 L=.02
IND 11 2 L=.015
IND 12 3 L=.007
DEF3P 1 2 3 GSFET

10PSI 10 1
GSFET 1 5 5
GVIA 5
DEF2P 10 1 VRC

MODEL
GEC4*75 GAS MODEL=2 VTO=-3.5 AO=54.84E-3 A1=.049 A2=.00865 A3=-1.24E-3
BETA=.0331 GAMMA=2.314 RDSO=1567.4 VDSDC=5 VDSO=5 CGSO=.372P VBI=.776
FC=.296 RIN=3.91 RF=430 N=1.54 IS=1.42E-10 VBR=17 RG=1.2 RS=2.4 RD=3.25
CDS=.058P TAU=2.8P CGD=.029P

SOURCE
VRC VS_DDIOD 11 0  DC^VB
VRC IND 1 11 L=10
VRC VS_AVIN 30 0 AMP^PWR  F^F1
VRC RES_RIN 30 10 R=50

FREQ
NH=8
!SWEEP 7 13 1
```

```
STEP 10

OUTVAR
VIN=VRC VFC 10 0 H1=1
IIN=VRC IFC_IIN RES_RIN H1=1
VR=VRC RE[VFC] 10 0 H1=1
VI=VRC IM[VFC] 10 0 H1=1
IR=VRC RE[IFC]_IIN RES_RIN H1=1
II=VRC IM[IFC]_IIN RES_RIN H1=1

OUTEQN
ZIN=VIN/IIN*1000
R=(VR*IR+VI*II)/(IR*IR+II*II)*1000
C=-1/((VI*IR-VR*II)/((IR*IR+II*II)*100))/2/PI/F1/1000

OUT
OUTEQN RE[R] SCN
OUTEQN RE[C] SCN

GRID
HBCTL
RELTOL=1E-8
OPT
YIELD
TOL
```

C.2 Small Signal Simulation

The small signal simulation file of the circuit shown in Fig.4.8 and it's tabulated oscillation conditions for 2.0pF and 0.2pF varactor capacitances are given below:

```
DIM
FREQ GHZ
RES OH
IND NH
CAP PF
```

```
LNG UM
TIME PS

!VAR

CKT

IND 1 2 L=28.57E-3
RES 2 3 R=1.6
CAP 3 4 C=.275
RES 4 5 R=3.25
RES 5 6 R=2.38
IND 6 7 L=15.75E-3
CAP 3 8 C=.0272
RES 8 5 R=270
RES 8 9 R=1.2
IND 9 10 L=17.7E-3
VCCS 3 8 4 5 M=35.2E-3 A=0 R1=1E7 R2=1E7 F=0 T=2.83
DEF3P 1 10 7 GSLFET

GSLFET 10 11 12
IND 1 10 L=.02
IND 11 2 L=.015
IND 12 3 L=.007
DEF3P 1 2 3 GSFET

ind 1 2 l=3.11
res 2 3 r=3.9
cap 1 3 c=22.32e-3
cap 1 0 c=46.66e-3
cap 3 0 c=35.4e-3
def2p 1 3 3n1plan

ind 1 2 l=1.318
res 2 3 r=2.26
cap 1 3 c=17.6e-3
cap 1 0 c=26.2e-3
cap 3 0 c=24.75e-3
def2p 1 3 1n3plan
```

```
ind 1 2 l=3.437e-3
cap 2 3 c=.2
res 3 4 r=5.956
ind 4 5 l=22.29e-3
cap 2 0 c=24e-3
cap 4 0 c=4.652e-3
def2p 1 5 0p2pl

ind 1 2 l=18.148e-3
cap 2 4 c=8.024
ind 4 5 l=18.14e-3
cap 2 0 c=22.56e-3
cap 4 0 c=22.56e-3
def2p 1 5  8p0si

GSFET 1 2 3
0P2PL 0 3
0P2PL 0 3
1N3PLAN 10 1
3N1PLAN 10 0
CAP 10 11 C=2
RES 11 12 R=3
8P0SI 2 20
DEF2P 12 20 0

OUT
0 DB[S21] GR2
0 RE[Z1] GR1
0 IM[Z1] GR1A

FREQ
SWEEP 8 10.5 .5

GRID
RANGE 8 10.5 .5
GR1 -300 0 20
GR1A -200 300 20
GR2 -5 15 2.5
OPT
```

FREQ.(GHz)	DB[S21]	RE[Z1]	IM[Z1]	
8	12.019	-33.002	-24.95	
8.5	12.283	-26.316	-13.39	
9	11.389	-21.573	-2.571	Oscillation
9.5	9.81	-18.059	7.924	frequency
10	8.054	-15.36	18.475	
10.5	6.358	-13.222	29.454	
11	4.785	-11.474	41.264	
11.5	3.339	-9.996	54.388	
12	2.005	-8.689	69.458	
12.5	.765	-7.456	87.37	
13	-.397	-6.174	109.484	
8	.348	-33.002	-114.475	
8.5	.935	-26.316	-97.648	
9	1.715	-21.573	-82.148	
9.5	2.696	-18.059	-67.465	
10	3.886	-15.36	-53.145	
10.5	5.226	-13.222	-38.755	
11	6.695	-11.474	-23.845	
11.5	7.719	-9.996	-7.89	Oscillation
12	7.597	-8.689	9.775	frequency
12.5	6.179	-7.456	30.074	
13	4.152	-6.174	54.392	

Table C.1: Start-up oscillation frequencies for Cv=2.0pF and 0.2pF, respectively

C.3 Large Signal Simulation

The following lines are the large signal simulation file written in LIBRA for the initial design shown in Fig. 4.19.

```
DIM
RES OH
COND /OH
IND NH
CAP PF
LNG UM
TIME PS
ANG DEG
VOL V
```

```
CUR MA
PWR DBM

VAR
PWR=.1
VB=.65

CKT

ind 1 3 l=3.425
res 3 4 r=9.53
cap 1 8 c=.0376
ind 8 9 l=.96
res 9 4 r=15
res 1 6 r=2.754
ind 6 7 l=.948
cap 7 4 c=6.115e-3
res 1 2 r=30
cap 2 0 c=.035
res 4 5 r=30
cap 5 0 c=.042
def2p 1 4 3n5stack

ind 1 2 l=1.32
res 2 3 r=2.26
cap 1 0 c=.025
cap 3 0 c=.026
cap 1 3 c=.018
def2p 1 3 1n3plan

ind 1 2 l=3.11
res 2 3 r=3.91
cap 1 0 c=.035
cap 3 0 c=.047
cap 1 3 c=.022
def2p 1 3 3n1plan

ind 1 2 l=5.863
res 2 3 r=6.03
cap 1 0 c=70.53e-3
```

```
 cap 3 0 c=48.1e-3
 cap 1 3 c=26.28e-3
 def2p 1 3 5n8plan

 ind 1 2 l=2.29e-3
 cap 2 3 c=.105
 res 3 4 r=13.181
 cap 2 0 c=15.7e-3
 cap 4 0 c=3.833e-3
 ind 4 5 l=13.9e-3
 def2p 1 5 0p105pl

 ind 1 2 l=3.437e-3
 cap 2 3 c=.2
 res 3 4 r=5.956
 cap 2 0 c=24e-3
 cap 4 0 c=4.652e-3
 ind 4 5 l=22.29e-3
 def2p 1 5 0p2pl

 ind 1 2 l=20.41e-3
 cap 2 4 c=10
 ind 4 5 l=20.41e-3
 cap 2 0 c=25.275e-3
 cap 4 0 c=25.275e-3
 def2p 1 5 10psi

GAASFET_AGEC 10 11 12 [MODEL=GEC4*75]
IND 1 10 L=.02
IND 11 2 L=.015
IND 12 3 L=.007
DEF3P 1 2 3 GSFET

GSFET 1 0 0
10PSI 1 2
DEF2P 1 2 VARACTOR

GSFET 3 4 5
10PSI 4 400
1N3PLAN 2 3
```

```
 3N1PLAN 3 0
 0P105PL 0 3
 RES 6 7 R=22
 5N8PLAN 7 0
 0P2PL 0 6
 0P2PL 0 6
 VARACTOR 1 2
 3N5STACK 100 1
 3N5STACK 4 40
 DEF1P 400 OSC1

 MODEL
 GEC4*75 GAS MODEL=2 VTO=-3.5 AO=54.84E-3 A1=.049 A2=.00865 A3=-1.24E-3
 BETA=.0331 GAMMA=2.314 RDSO=1567.4 VDSDC=5 VDSO=5 CGSO=.372P VBI=.776
 FC=.296 RIN=3.91 RF=430 N=1.54 IS=1.42E-10 VBR=17 RG=1.2 RS=2.4 RD=3.25
 CDS=.058P TAU=2.8P CGD=.029P

 SOURCE
 OSC1 VS_DVDD 20 0  DC=5
 OSC1 IND 40 20 L=10
 OSC1 VS_DDIOD 10 0  DC^VB
 OSC1 VS_AVIN 51 0 AMP^PWR  F^F1
 OSC1 RES_RIN 50 51 R=50
 OSC1 RES_RFB 60 0  R=50
 OSC1 RES_RLOAD 400 0 R=50

 FREQ
 NH=7
 SWEEP 10.37 10.42 .01
 !STEP 10.4

 OUTVAR
 VIN=OSC1 VFC 50 0 H1=1
 VFB=OSC1 VFC 60 0 H1=1

 OUTEQN
 R=VFB/VIN

 OUT
 OUTEQN MAG[R] SCN
```

```
 OUTEQN ANG[R] SCN
 OUTEQN MAG[R] GR2
 OUTEQN ANG[R] GR2A
 OSC1 PF_POSC 400 0 R=RES_RLOAD H1=1 SCN
 OSC1 PS_POSC 400 0 R=RES_RLOAD SCN
 OSC1 PS_POSC 400 0 R=RES_RLOAD GR3
 OSC1 V_VOUT 400 0 GR4

 GRID
 FREQ 10.37 10.42 .01
 GR2 0 2 1
 GR2A -50 50 5
 FREQ 0 80 10
 GR3 -80 20 5
 TIME 0 250 50
 GR4 -2 2 .5

 HBCNTL
 RELTOL=1E-8

 OPT
 YIELD
 TOL
```

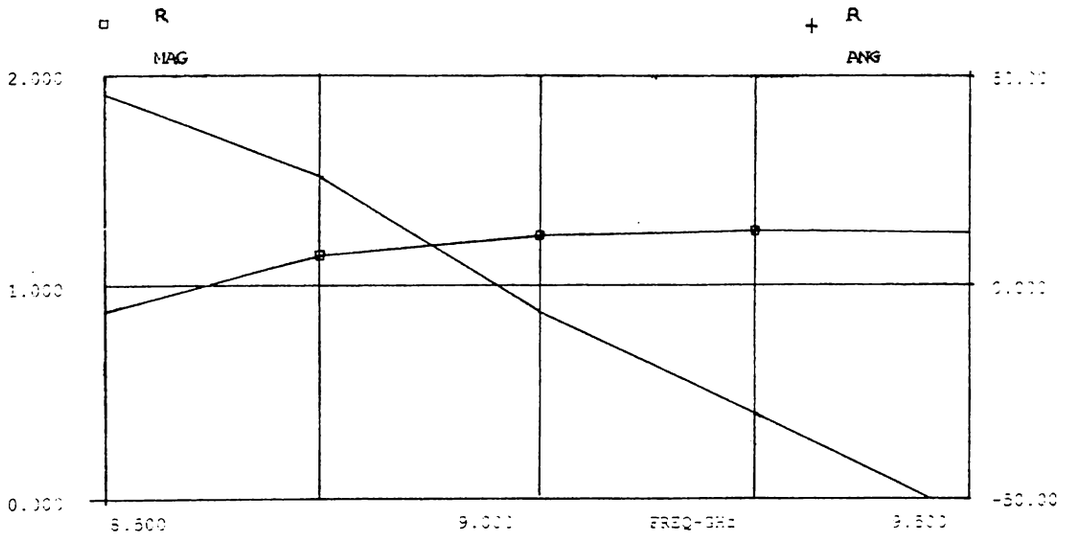

Figure C.1: LIBRA simulation graphic for V_{tune}=.5V, PWR=AVIN=1.5V, NH=3 (first VCO)

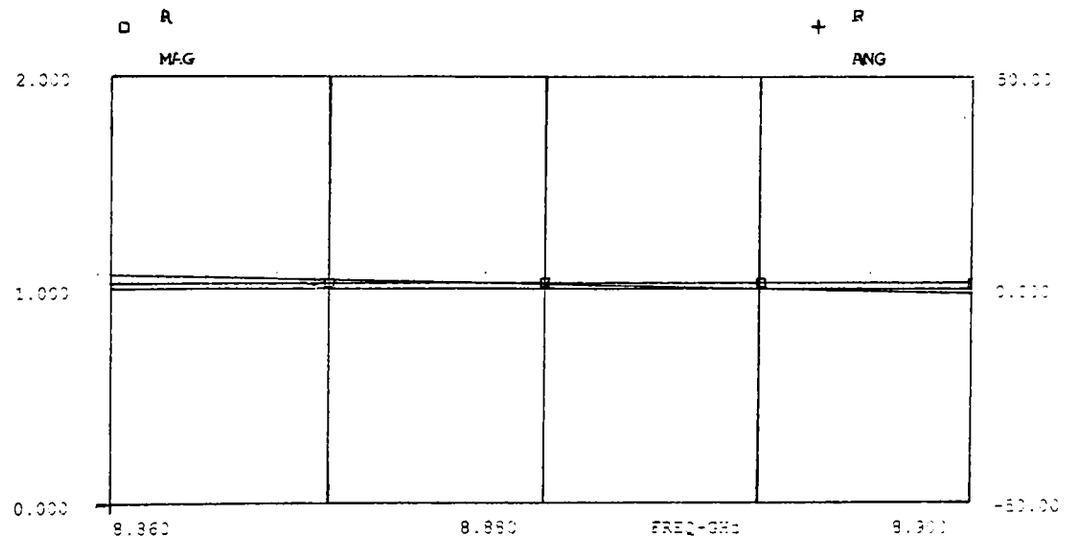

Figure C.2: LIBRA simulation graphic for V_{tune}=.5V, PWR=AVIN=1.8V, NH=7, f_{osc}=8.88GHz (first VCO)

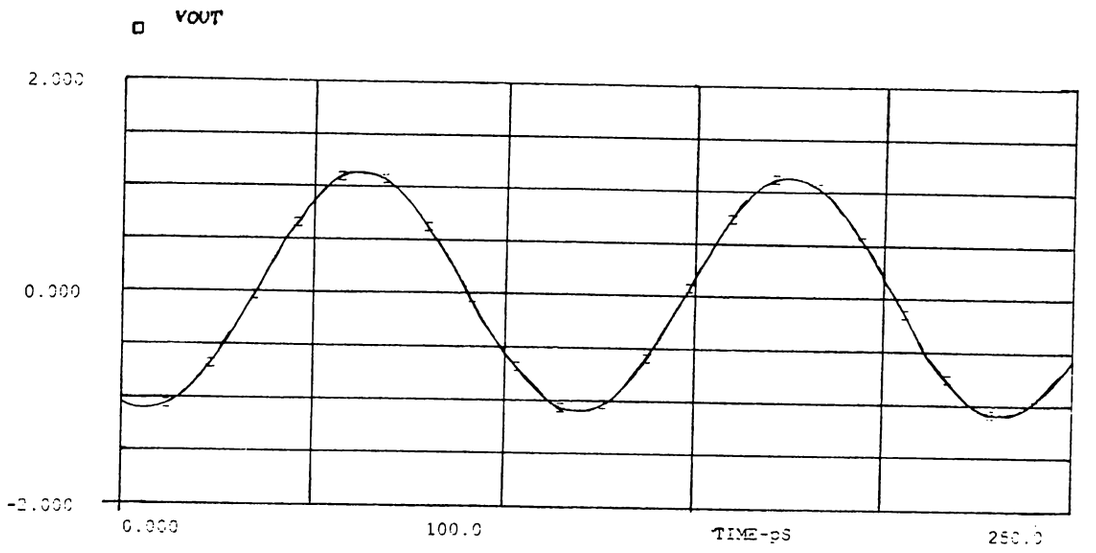

Figure C.3: Output waveform @ 8.88GHz

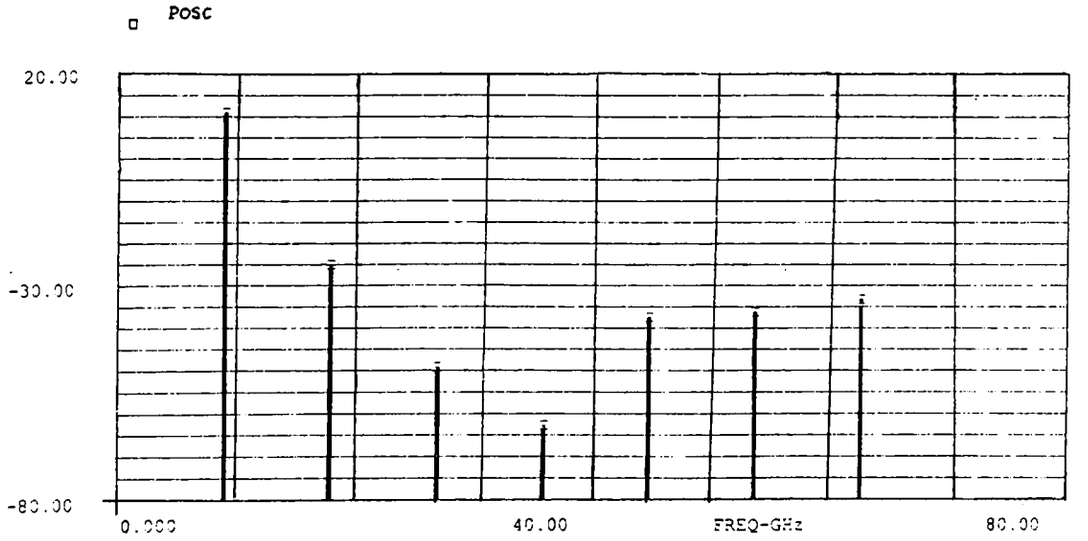

Figure C.4: Harmonic content of the output waveform when V_{tune}=.5V

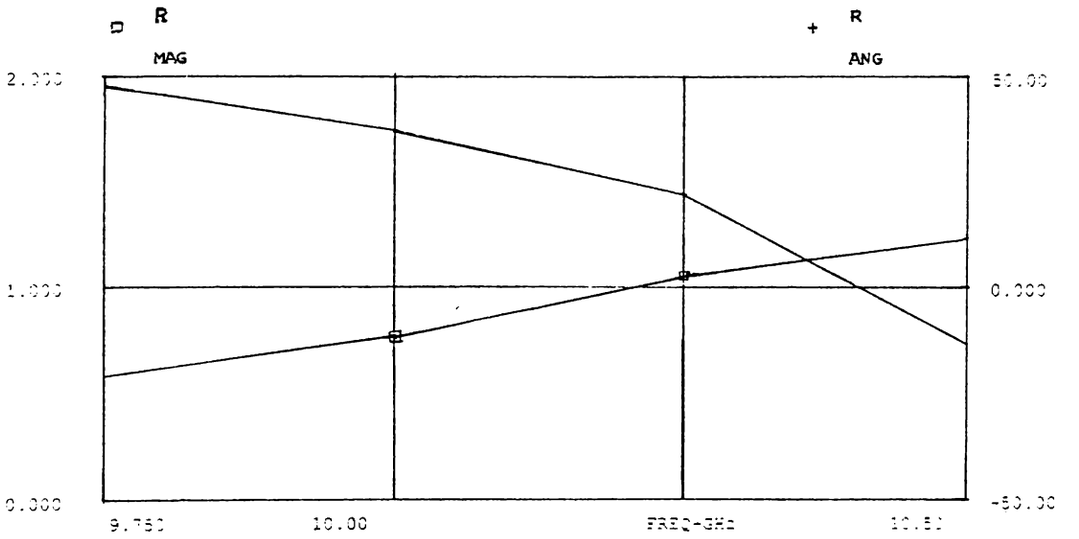

Figure C.5: LIBRA simulation graphic for V_{tune}=-10V, PWR=AVIN=1V, NH=3 (first VCO)

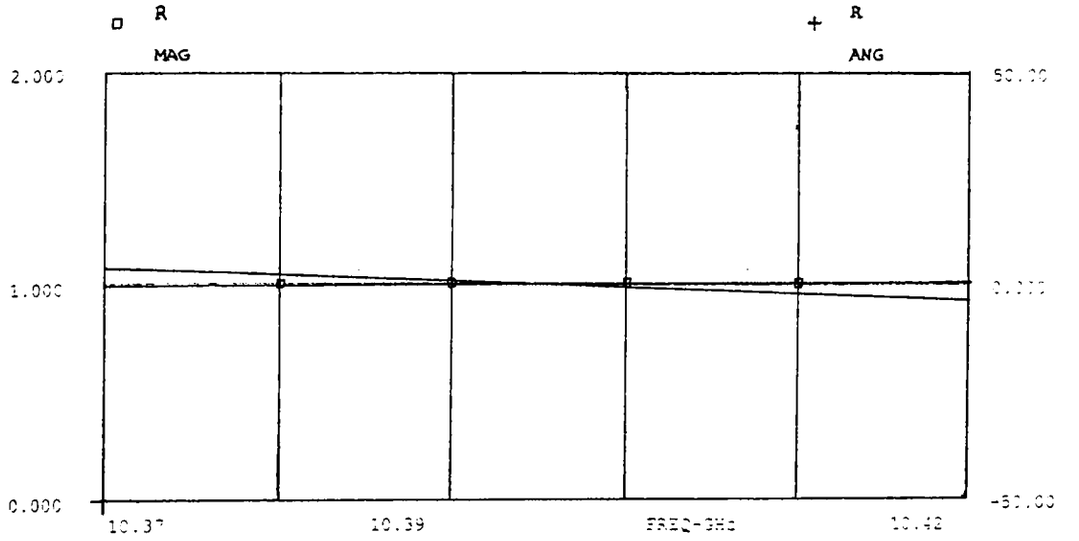

Figure C.6: LIBRA simulation graphic for V_{tune}=-10V, PWR=AVIN=1.23V, NH=7, f_{osc}=10.395GHz (first VCO)

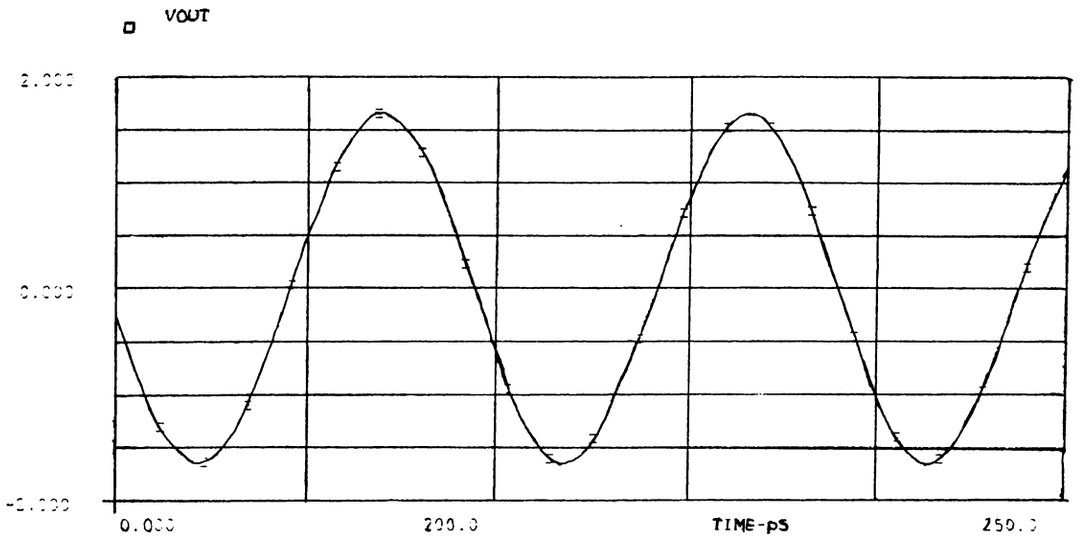

Figure C.7: Output waveform @ 10.395GHz

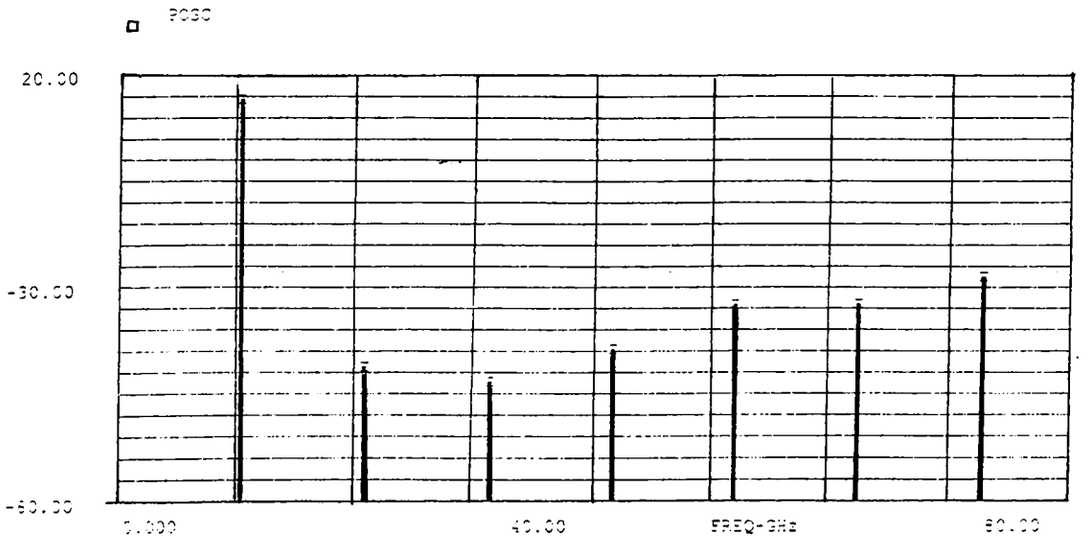

Figure C.8: Harmonic content of the output waveform when V_{tune}=-10V

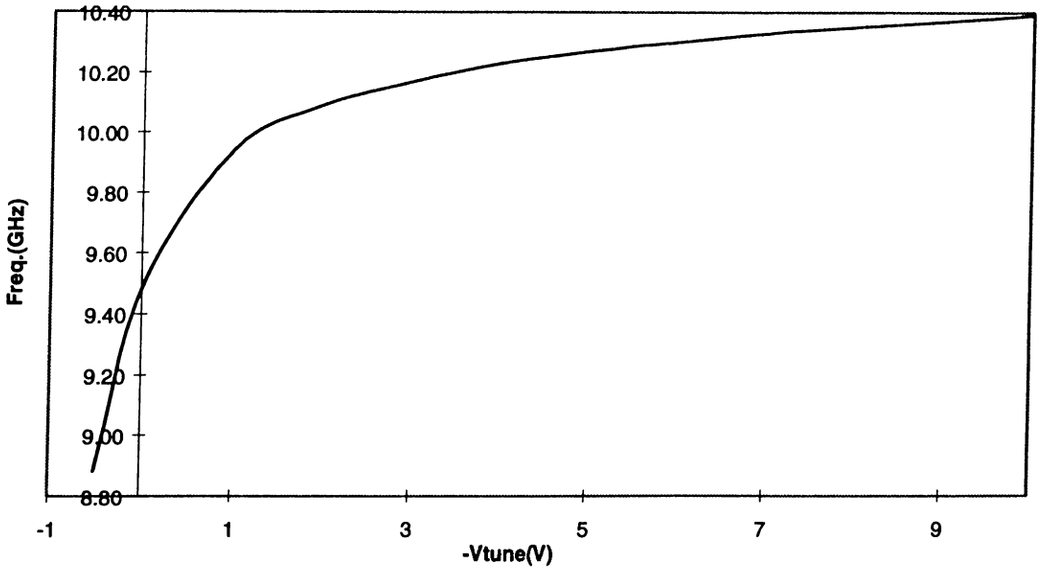

Figure C.9: Tuning linearity of the first VCO

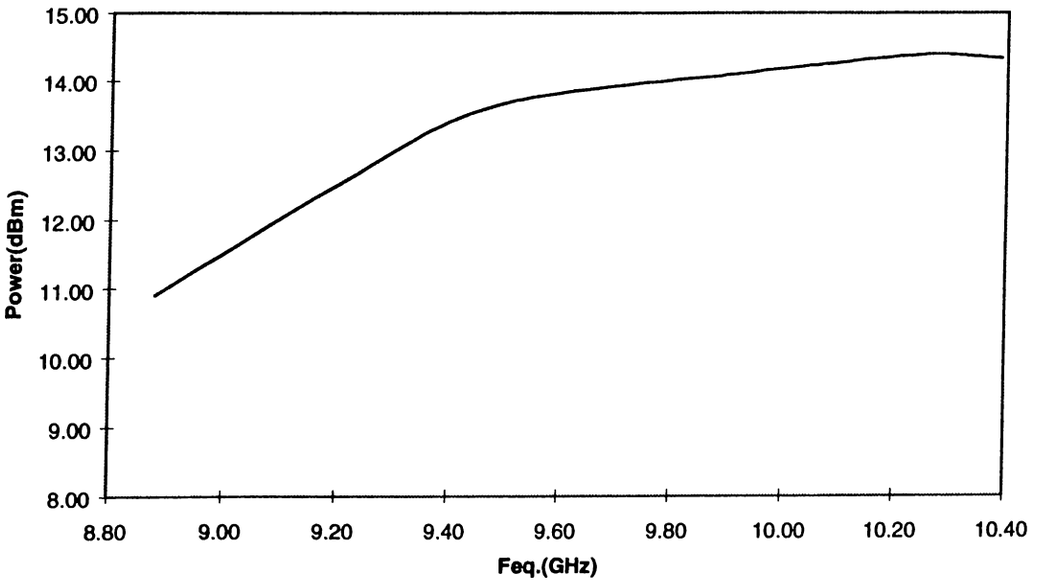

Figure C.10: Power variation of the first VCO

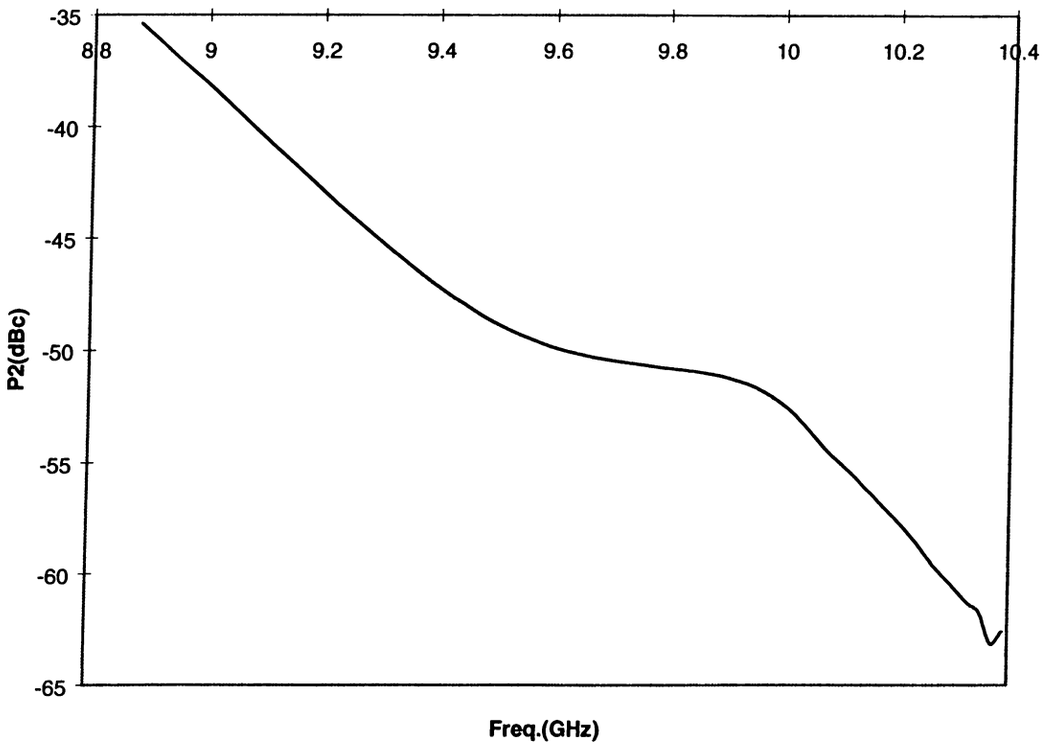

Figure C.11: Second harmonic suppression versus the oscillation frequency for the first VCO

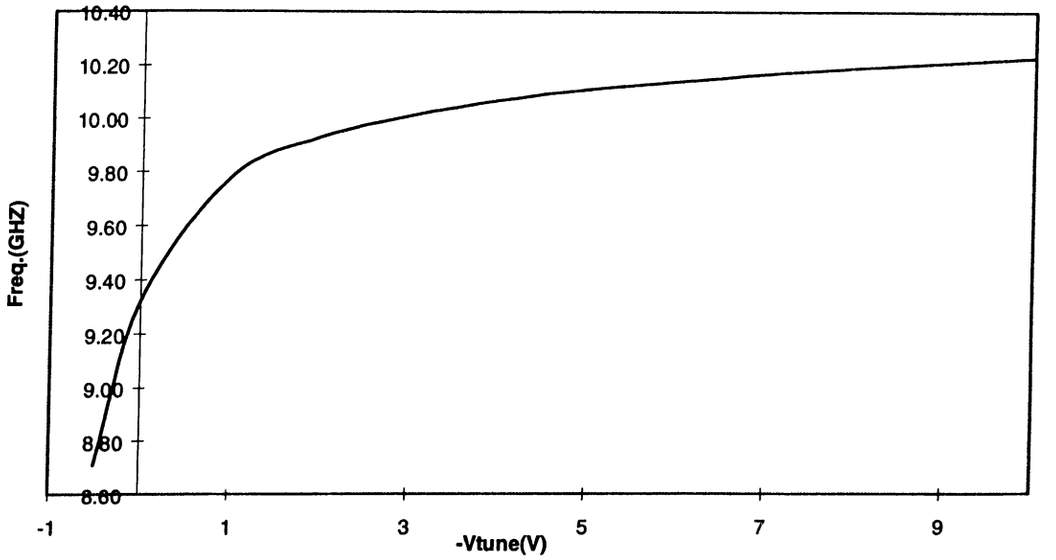

Figure C.12: Tuning linearity of the second VCO

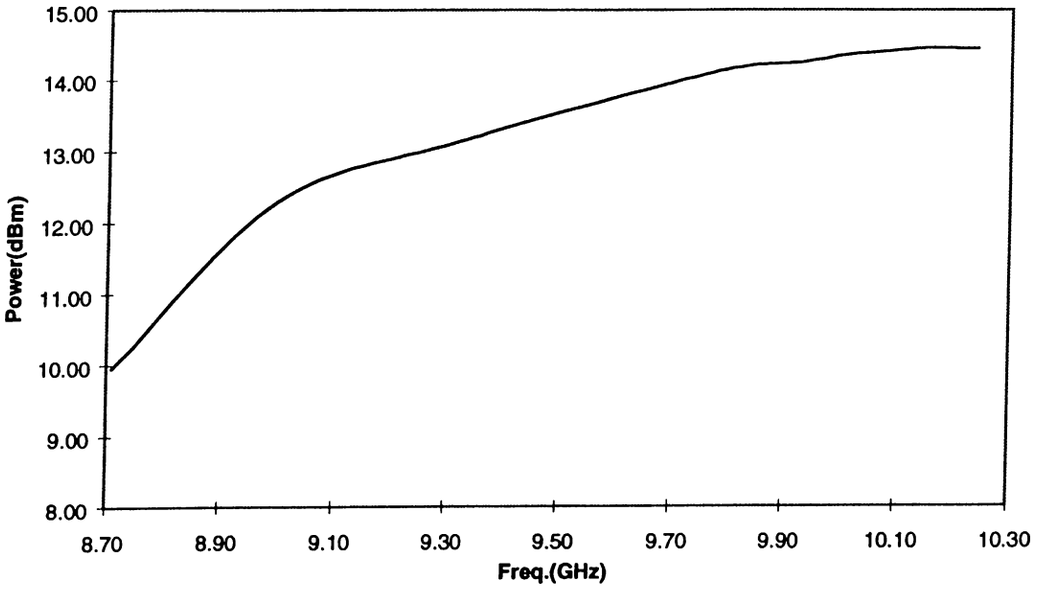

Figure C.13: Power variation of the second VCO

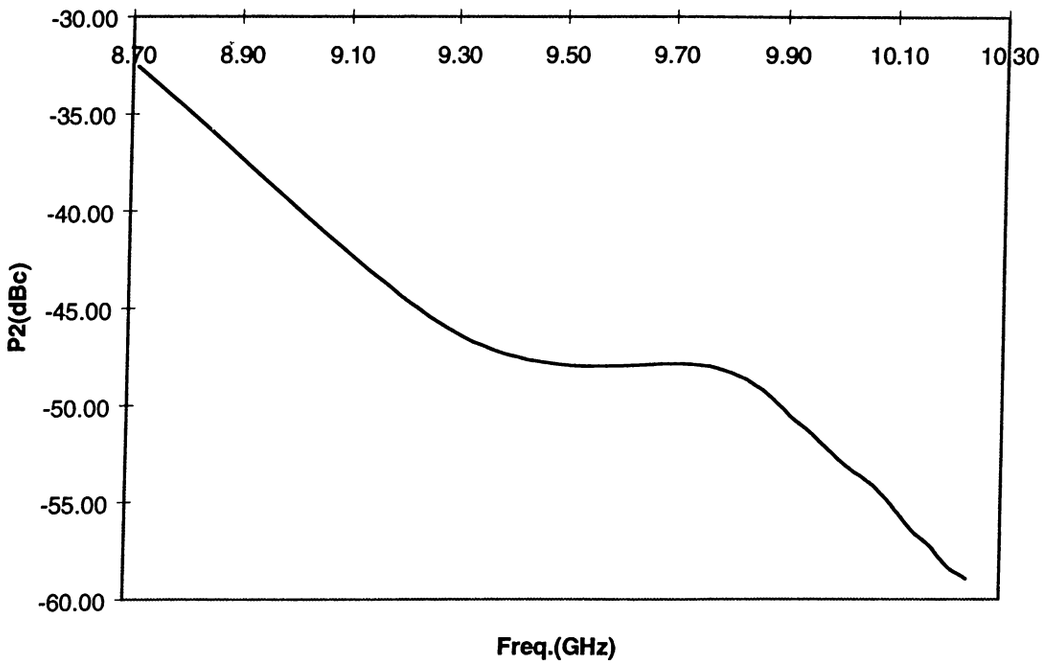

Figure C.14: Second harmonic suppression versus the oscillation frequency for the second VCO

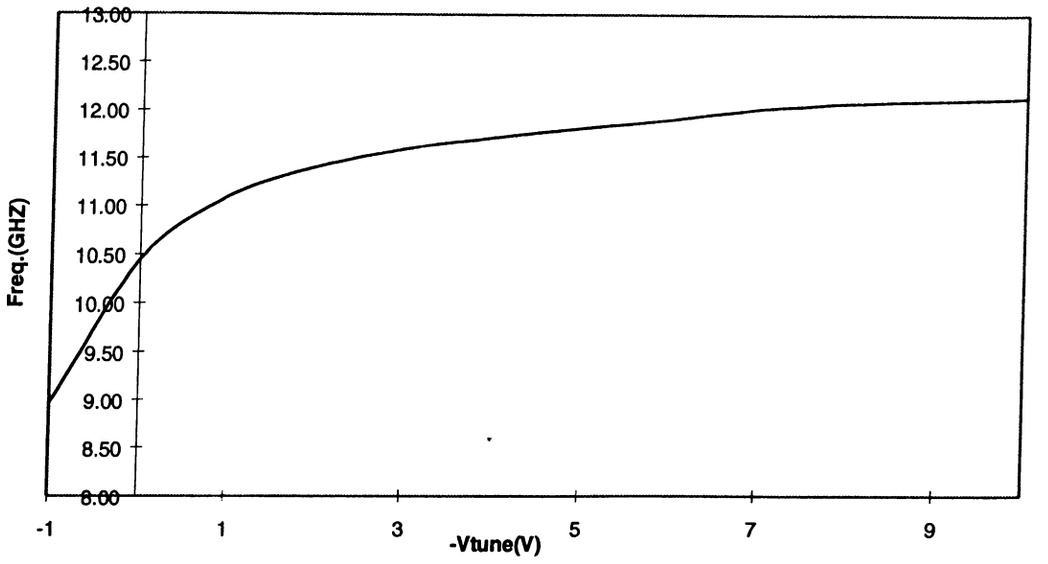

Figure C.15: Tuning linearity of the third VCO

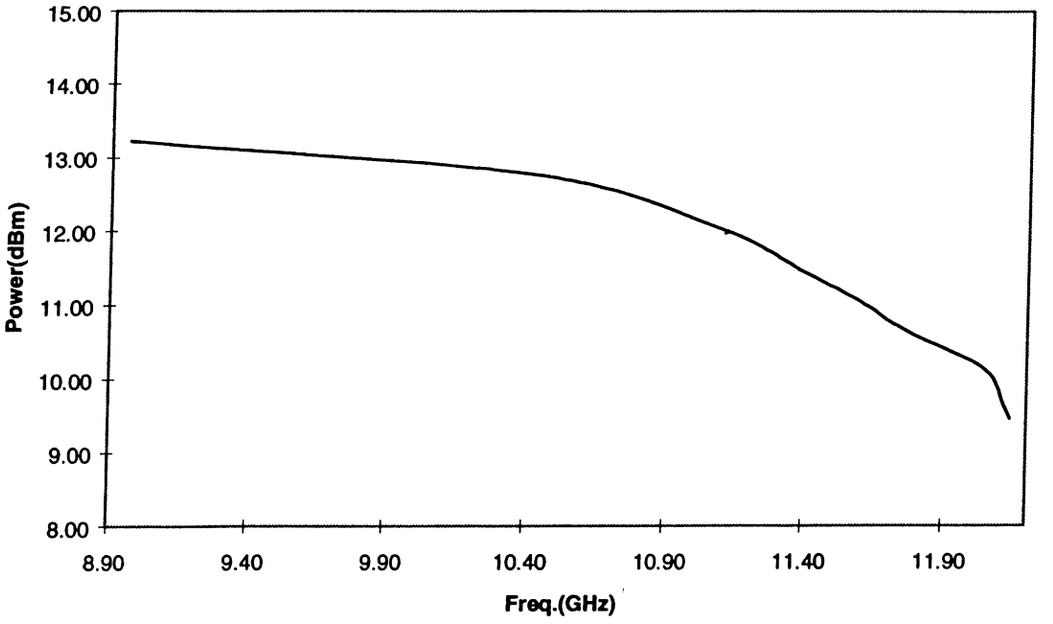

Figure C.16: Power variation of the third VCO

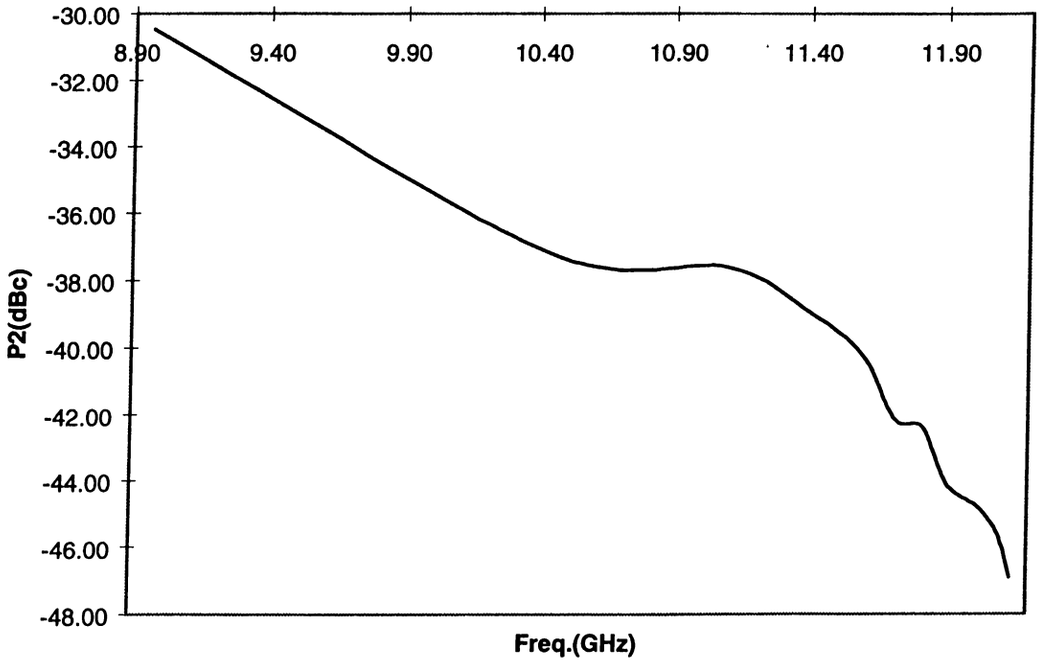

Figure C.17: Second harmonic suppression versus the oscillation frequency for the third VCO

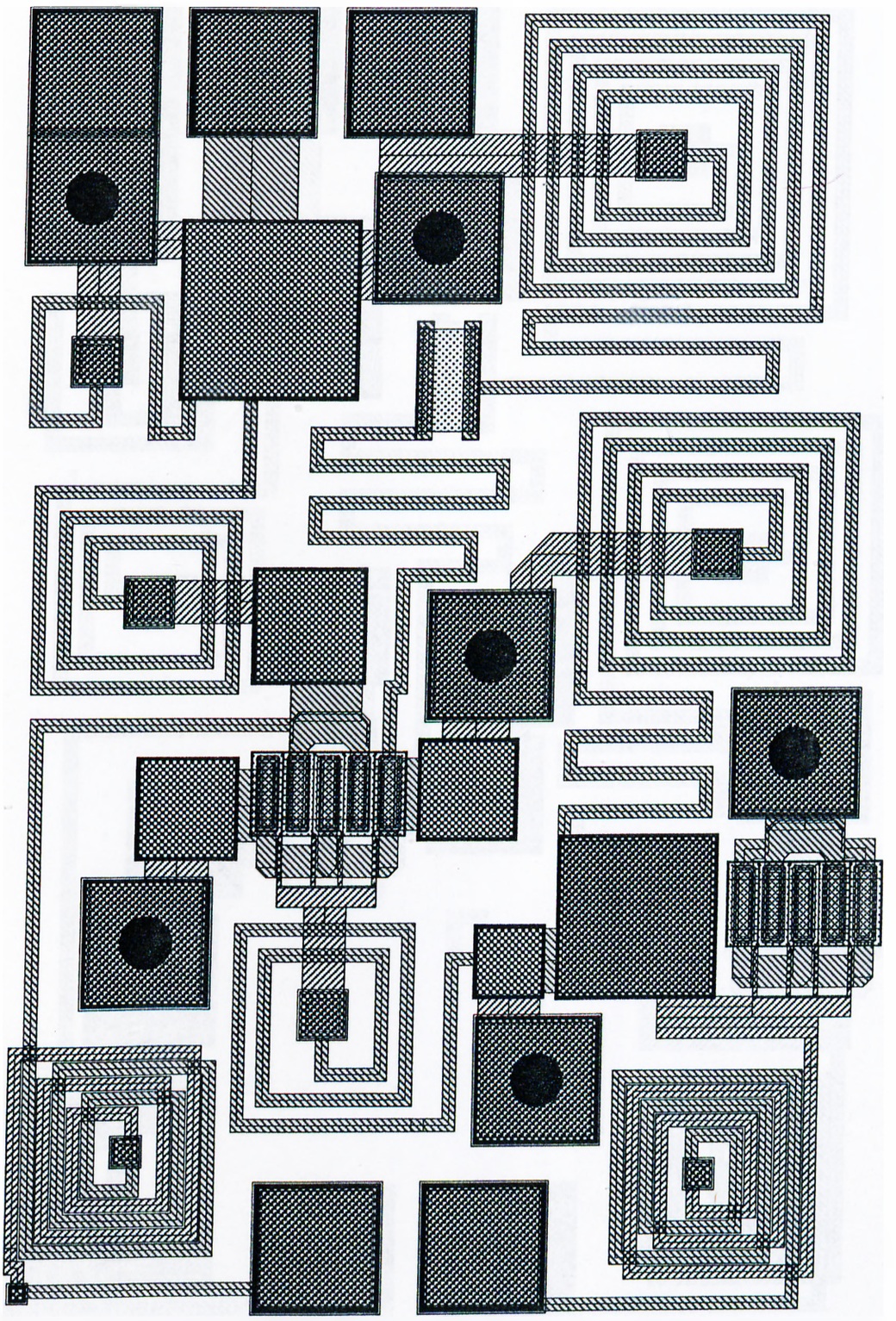

Figure C.18: Finished layout of the first VCO

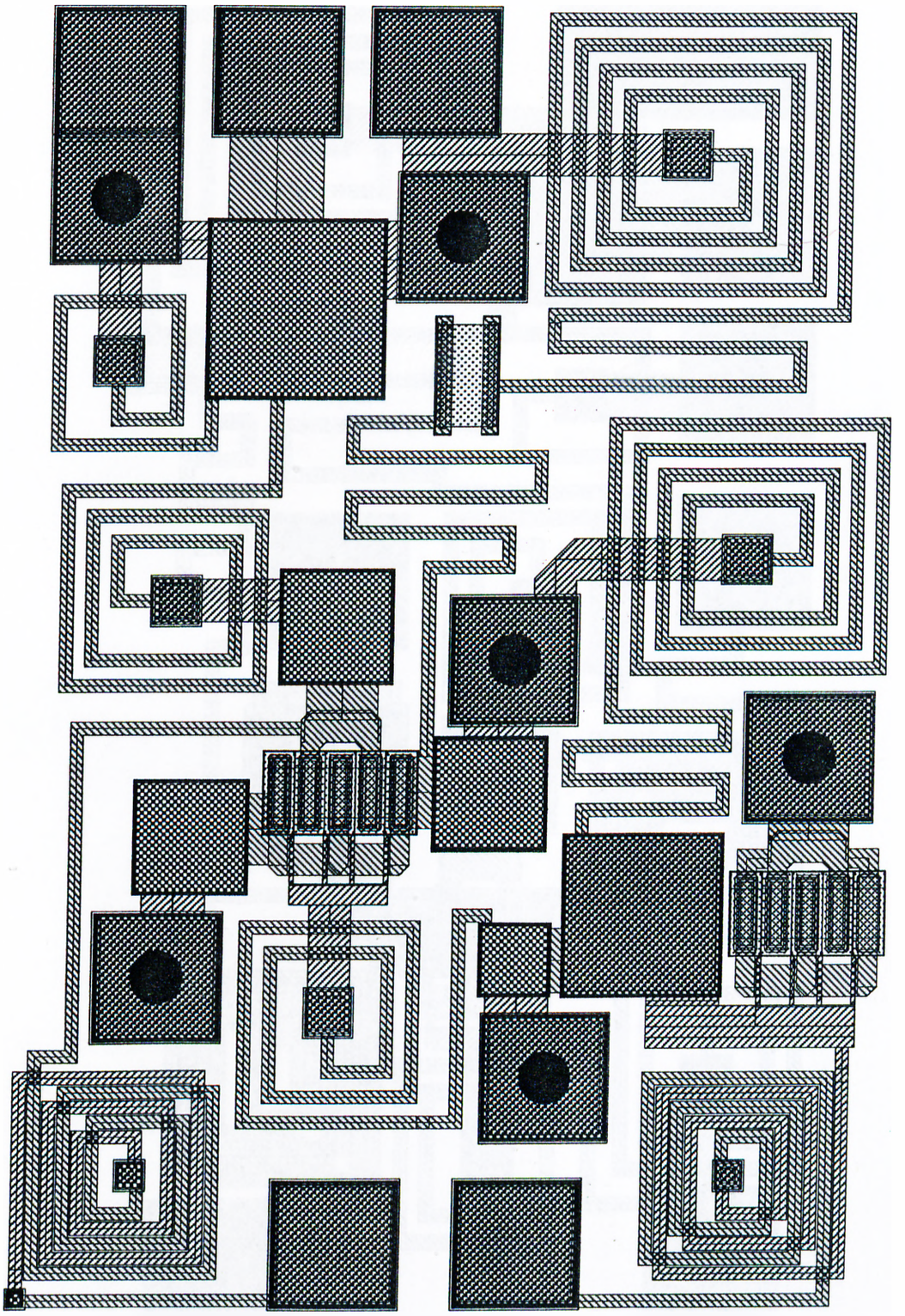

Figure C.19: Finished layout of the second VCO

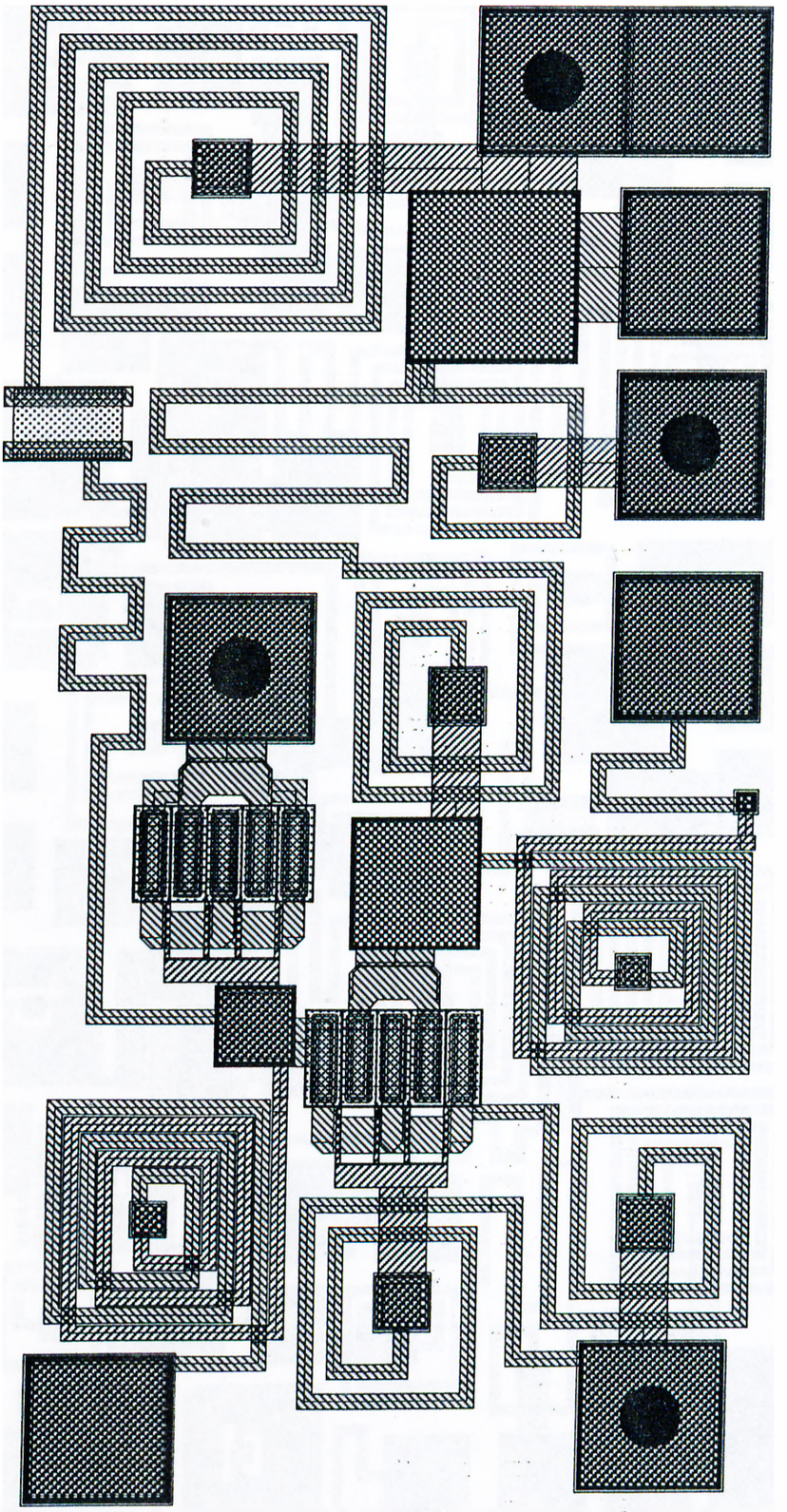

Figure C.20: Finished layout of the third VCO

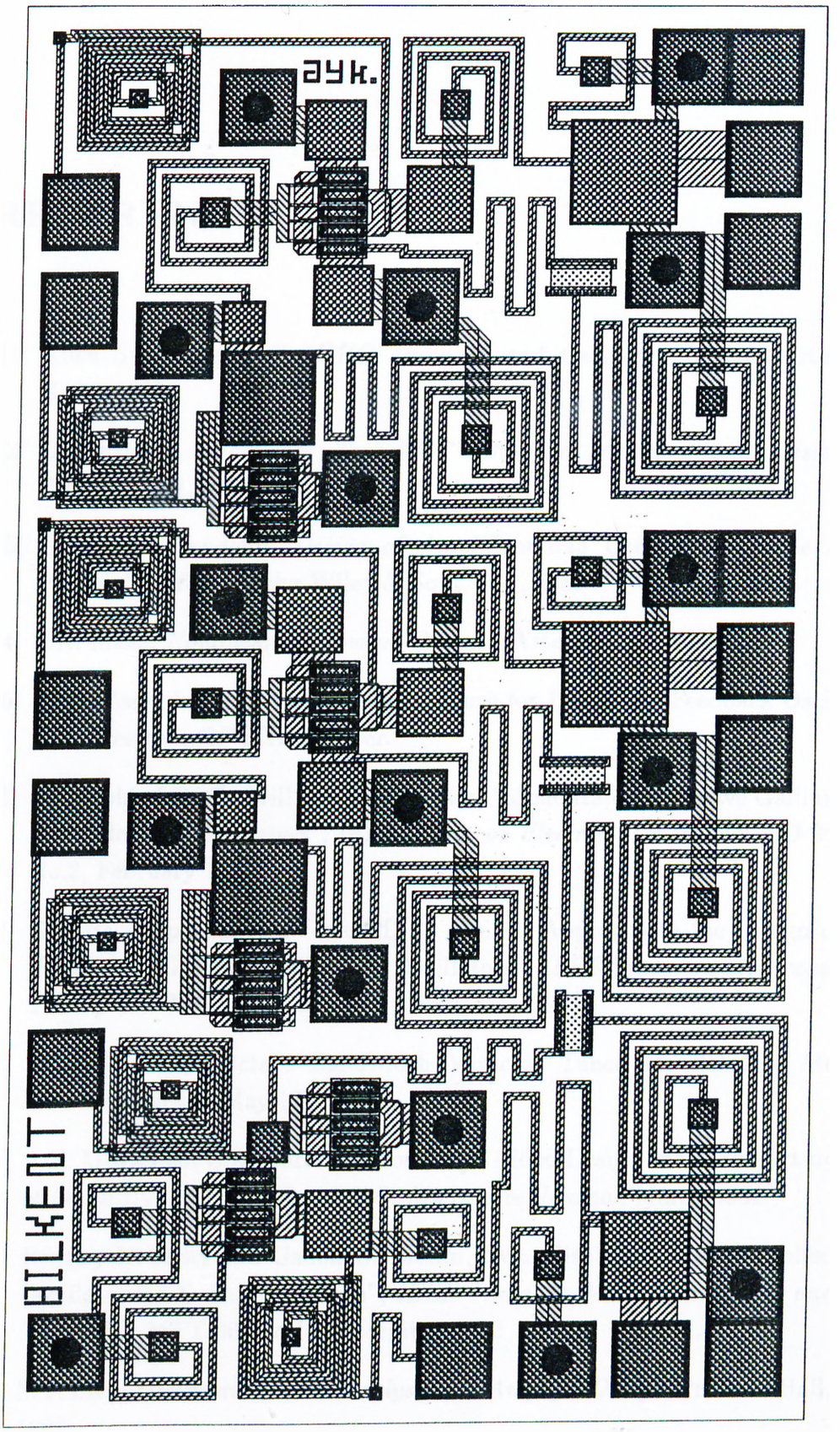

Figure C.21: Finished layout of the chip

REFERENCES

[1] Allen Sweet, *MIC & MMIC Amplifier and Oscillator Design*, Artech House,1990

[2] G.Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, Prentice-Hall, Inc., 1984

[3] George D. Vendelin, *Design of Amplifiers and Oscillators by the S-Parameter Method*,John Wiley & Sons, Inc., 1982

[4] S.A. Maas, *Nonlinear Microwave Circuits*, Artech House,1988

[5] E.C. Westenhover " A General Procedure for Low Noise Feedback Oscillator Design", *RF-EXPO* Paper.

[6] J.S. Joshi, J.R. Cockrill and J.A. Turner, "Monolithic Microwave Gallium Arsenide FET Oscillators", *IEEE Trans. on Electron Devices*, Vol. ED-28, No.2, February 1981

[7] G.R Basawapatna, R.B Stancliff, "A Unified Approach to the Design of Wideband Microwave Solid-state Oscillators", *IEEE Trans. on Microwave Theory and Tech.* , Vol. MTT-27, No.5, May 1979

[8] John Kitchen, "Octave Bandwidth Varactor Tuned Oscillators", *Microwave Journal*, May 1987

[9] A.E. Moysenko, C.A. Barratt, "Computer Aided Design and Manufacture of GaAs Hyperabrupt Varactors", *Microwave Journal*, March 1982

[10] Bentley N. Scott and Gailon E. Brehm, "Monolithic Voltage Controlled Oscillator for X- and Ku-Bands", *IEEE Trans. on Microwave Theory and Tech.*, Vol. MTT-30, No.12, December 1982

[11] S.Y. Liao, *Microwave Circuit Analysis and AmplifierDesign*, Prentice-Hall, 1987

[12] Minoru Maeda, Katsuhiro Kimura, Hiroshi Kodera, "Design and Performance of X-Band Oscillators with GaAs Schottky-Gate Field-Effect Transistors", *IEEE Trans. on Microwave Theory and Tech.* , Vol. MTT-23, No.8, August 1975

[13] Kenneth M. Johnson, "Large Signal GaAs MESFET Oscillator Design", *IEEE Trans. on Microwave Theory and Tech.* , Vol. MTT-27, No.3, March 1979

[14] John W. Boyles, "The Oscillator as a Reflection Amplifier:an Intiutive Approach to Oscillator Design", *Microwave Journal*, June 1986

[15] K. Kurokawa , "Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits ", *The Bell System Technical Journal*, July-August, 1969

[16] Chao-Ren Chang, Michael B. Steer, Scott Martin and Ellias Reese, "Computer Aided Analysis of Free-runing Microwave Oscillators", *IEEE Trans. on Microwave Theory and Tech.* , Vol.39, No.10, October 1991

[17] Günter Braun and Heinz Lindermeier, "Transistor Oscillators with Impedance Noise Matching", *IEEE Trans. on Microwave Theory and Tech.* , Vol.39, No.9, September 1991

[18] Walter Wagner, "Oscillator Design by Device Line Measurement", *Microwave Journal*, February 1979

[19] Tohru Takada, KiyoyukiYokoyama, Masao Ida and Tsuneta Sudo, "A MESFET Variable-capacitance for GaAs Integrated Circuit Simulation", *IEEE Trans. on Microwave Theory and Tech.* ,Vol.MTT-30, No.5, May 1982

[20] Steve Hamilton, "Microwave Oscillator Circuits", *Microwave Journal*, April 1978

[21] Cüneyt Birdir, " Design of Microwave Voltage Controlled Oscillators Using MMIC Technology",*M.S.Thesis, Electrical and Electronics Engineering of METU*, August 1994

[22] Ferit Öztürk, "2-40 GHz High Performance MMIC SPDT Switches", *M.S.Thesis, Electrical and Electronics Engineering of BILKENT University*, September 1993

[23] Fatih Üstüner, "Design of Front-end LNA, T/R Switch and Power Amplifier of DECT Woreless Communication System",*M.S.Thesis, Electrical and Electronics Engineering of METU*, September 1994

[24] Muharrem Kara, "A Large Signal Technique for Designing Voltage Controlled Transistor Oscillators with Optimum Power Output",*M.S.Thesis, Electrical and Electronics Engineering of METU*,September 1991

[25] Neil Sclater, *Gallium Arsenide IC Technology*, TPR,1988

[26] GEC-Marconi Materials Technology, GaAs Product Handbook,1994

[27] GaAs IC Foundry Design Guide Process F20/14, GEC Marconi, 1994

[28] H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET", *Bell System Technologies Journal*, March 1979

[29] Hakan Erdeĝirmenci, "The Definitions and Measurements of the VCO Parameters",*M.S.Thesis, Electrical and Eloctronics Engineering of METU*,September 1987