LOW-VOLTAGE CURRENT-MODE CMOS FILTER STRUCTURE FOR HIGH FREQUENCY APPLICATIONS

A THESIS
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
AND THE INSTITUTE OF ENGINEERING AND SCIENCES
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

By
Aydın İlker Karşılayan
July 1995

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Aydın İlker Karşılayan tarafından bağışlanmıştır

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc. Prof. Dr. Mehmet Ali Tan(Supervisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah Atalar

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Hayrettin Köymen

Approved for the Institute of Engineering and Sciences:

Prof. Dr. Mehmet Baray
Director of Institute of Engineering and Sciences

ABSTRACT

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Aydın İlker Karşılayan
M.S. in Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Mehmet Ali Tan
July 1995

In this thesis, a new method for the design of tunable current-mode CMOS filters is presented. The proposed structure is suitable for low-voltage (3V) and high frequency applications. Basic building blocks are differential damped integrator and differential damped differentiator, which have tunable corner frequencies. Using first order building blocks and applying feedback techniques, biquadratic sections of low-pass, high-pass and band-pass filters are generated. Higher order filters are implemented by using cascaded biquad synthesis. Filters are tuned by means of two control voltages, from 50% to 130% of their corner frequencies. HSPICE simulations show that filter implementation up to $0.5GHz$ is possible for 2.4μ CMOS technology. The available frequency range can be increased using a better technology such as 0.7μ CMOS. Layouts for two test chips are generated using CADENCE full-custom design environment for 0.7μ and 2.4μ CMOS processes.

Keywords : Filter, low-voltage, current-mode.

ÖZET

YÜKSEK FREKANS UYGULAMALARI İÇİN DÜŞÜK GERİLİMLİ AKIM MODU CMOS SÜZGEÇ YAPISI

Aydın İlker Karşılayan
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
Tez Yöneticisi: Dr. Mehmet Ali Tan
Temmuz 1995

Bu tezde, ayarlanabilir akım modu CMOS süzgeç tasarımı için yeni bir metod sunulmuştur. Önerilen yapı, düşük gerilim ve yüksek frekans uygulamaları için uygundur. Temel yapı blokları, köşe frekansları ayarlanabilen sönümlü fark integral alıcı ile sönümlü fark türev alıcıdır. Birinci derece yapı bloklarını kullanarak ve geri besleme teknikleri uygulayarak, alçak-geçiren, yüksek-geçiren ve band-geçiren ikinci derece süzgeç blokları oluşturulmuştur. Daha yüksek dereceli süzgeçler, ikinci dereceden süzgeçlerin ardarda bağlanması ile gerçekleştirilmiştir. Süzgeçler iki kontrol gerilimi yoluyla köşe frekanslarının %50'sinden %130'una kadar ayarlanabilmektedir. HSPICE simulasyonları göstermektedir ki, 2.4μ CMOS teknolojisi ile $0.5GHz$'e kadar süzgeçlerin gerçekleştirilmesi mümkündür. Kullanılabilir frekans bandı, 0.7μ gibi daha iyi bir teknoloji kullanılarak arttırılabilinir. CADENCE'ın 0.7μ ve 2.4μ CMOS tasarım ortamları kullanılarak iki test yongasının yerleşim planları üretilmiştir.

Anahtar Kelimeler : Süzgeç, düşük gerilim, akım modu.

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Chapter 1

INTRODUCTION

Continuous time analog filters are one of the main blocks that make the link between analog and digital circuitry, hence realization of these filters in integrated form allows very large scale integration of mixed mode analog-digital systems [1]. Today, the place for continuous time filters is rather well established, and in fact they are inevitable for several applications such as video signal processing, antialiasing filtering, magnetic disk-drive read-channel systems, telephony circuits and line equalizers for computer networks, to name a few [2], [3].

Among other filter types, switched capacitor filters and digital filters are being widely used in integrated form at moderate frequencies [4]. Since they are very accurate, no tuning mechanism is needed [1]. However, at the VHF range, clock feedthrough problem makes the operation of SC filters impossible [3]. Digital filters, even though operating at that frequencies, are power hungry. Another point is that sampled-data filters (including SC and digital filters) need an antialiasing continuous time filter to band-limit the input signal. Due to the sampling, high frequency noise can be aliased on to the base band, increasing the noise level and hence reducing the filter dynamic range [1]. Continuous time filtering avoids the aliasing effect, however, precision of these filters is in the order of 30-50%, which comes out to be the major disadvantage of continuous time filters. In order to correct filter characteristics, on-chip tuning circuitry

is required [1], [3], [5], [6].

With the increasing clock frequency and reliability considerations, digital CMOS processes are driven to low power supply voltages, as evidenced by the emerging 3V standard [7]. Using low-voltage digital CMOS technologies, design of voltage-mode filters becomes considerably difficult due to linearity and dynamic range limitations [8]. Furthermore, due to high impedance nodes in voltage-mode circuits, parasitic capacitances are effective at high frequencies.

Current-mode signal processing, in which primary signal medium is current rather than voltage, allows highly linear circuits with wide dynamic range operating at high frequencies and low-supply voltages [7], [8]. Due to low impedance nodes in current-mode circuits, voltage swing becomes so small that linear operation is satisfied even for low supply voltages. In addition, the effect of parasitic inductances is less severe than the effect of parasitic capacitances in voltage-mode circuits [8]. Furthermore, current domain operations such as addition and multiplication by a constant are simpler than their voltage-mode analogue [9].

Several current-mode filters have been reported in the literature [7], [8], [10], [11]. In most filters, main building block is an integrator, which ideally has to have infinite DC gain. The method proposed in this thesis uses damped integrator and damped differentiator to implement higher order filters by cascading and applying feedback techniques. The advantage of using damped blocks is that they are more realistic and easier to implement since every integrator is damped due to finite DC gain. In addition, they absorb the effect of parasitics such that the resulting transfer function remains unchanged with a slight change of parameters, which can be corrected by tuning. The filter blocks are suitable for low-voltage applications and tunable for the purpose of correcting the fabrication tolerances and environmental changes.

Implementation and simulation of filters have been carried out by using CADENCE and HSPICE software packages. For the simulation part, MIETEC 2.0μ double-metal, double-poly CMOS technology is used. In fact, this is a shrunken 3μ technology. During mask generation, layout is shrunk with a scaling factor of 0.8. The procedure followed is that layout is generated in 3μ technology with a minimum gate-witdh of 3μ, and then shrunk to 2.4μ

during fabrication. In the thesis, dimensions of the transistors are given in 3μ technology, as in the original layout, but the simulations include the shrinking effect. Layouts for the filters have been drawn using CADENCE full custom design kit, and then the parasitic routing capacitances have been extracted, which has been used in post-layout simulation.

Chapter 2

BASIC BUILDING BLOCKS

The main building block for the proposed filter structure is a current mirror, which has a tunable input conductance, g_m. Figure 2.1 shows the basic structure. The transistors M_{n1},M_{n2},M_{p1} and M_{p2} constitute the current mirror whereas M_{cn1},M_{cn2},M_{cp1} and M_{cp2} are used to tune the conductances by means of the two control voltages V_{cn} and V_{cp}. Low-supply voltage characteristics of the circuit comes from the fact that only two transistors exist from supply to ground rail, which enables the circuit operate even at 2 volts.

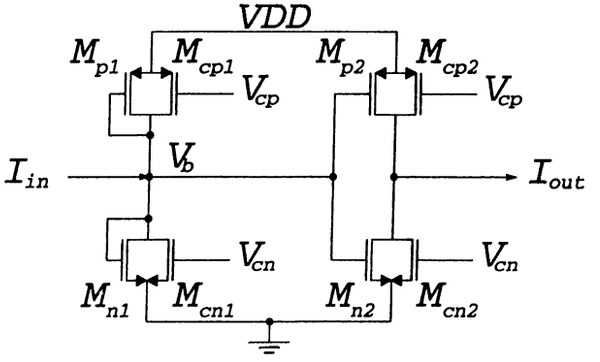

Figure 2.1: g_m-tunable current mirror.

Throughout this chapter, we will assume that the tuning transistors M_{cn1},M_{cn2},M_{cp1} and M_{cp2} are in cut-off, correspondingly $V_{cp} = V_{dd}$ and $V_{cn} = 0$. Therefore our analysis for this chapter will include their only parasitic effects,

and we will concentrate on the current mirror. Tuning mechanism and the effect of tuning transistors will be explained in Chapter 3.

To analyze the circuit behaviour, first we assume that p type transistors M_{p1} and M_{p2} are matched, and n type transistors M_{n1} and M_{n2} are matched as well. As clear from Fig. 2.1, the two transistors M_{n1} and M_{p1} are in saturation since $V_{gs} = V_{ds}$ for both. In addition, V_{gs} of M_{p2} is equal to that of M_{p1}, and since they are matched, M_{p2} is also in saturation. The same argument can be applied to the transistors M_{n1} and M_{n2}. Having four transistors in saturation, and neglecting output conductances and parasitic capacitances, small signal equivalent circuit can be obtained as in Fig. 2.2.

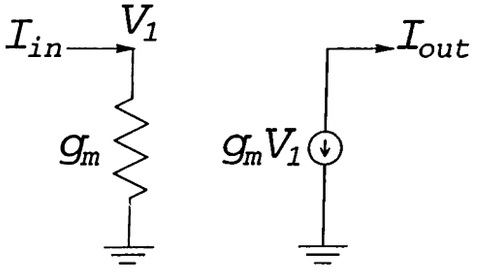

Figure 2.2: Small signal model of current mirror.

Applying KCL at the input and output nodes yields

$$I_{in} = g_m V_1 \tag{2.1}$$

$$I_{out} = -g_m V_1 \tag{2.2}$$

resulting in

$$I_{out} = -I_{in} \tag{2.3}$$

where

$$g_m = g_{mp} + g_{mn} \tag{2.4}$$

$$g_{mp} = \beta_p(V_{dd} - V_b + V_{tp}) \tag{2.5}$$

$$g_{mn} = \beta_n(V_b - V_{tn}) \tag{2.6}$$

Including the effect of output conductances and parasitic capacitances, the small signal equivalent circuit becomes as in Fig. 2.3. The circuit can be simplified by combining parallel capacitances and conductances, as shown in Fig. 2.4.

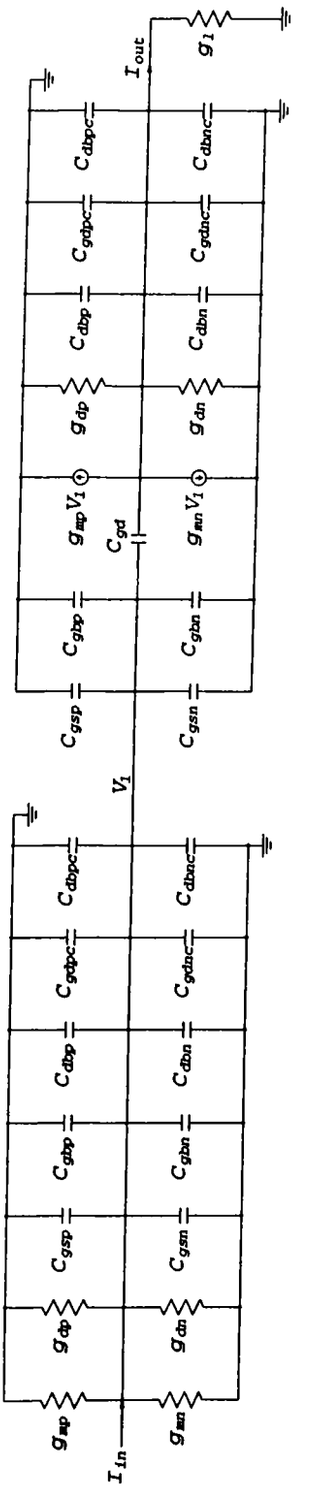

Figure 2.3: Small signal model of current mirror including parasitics.

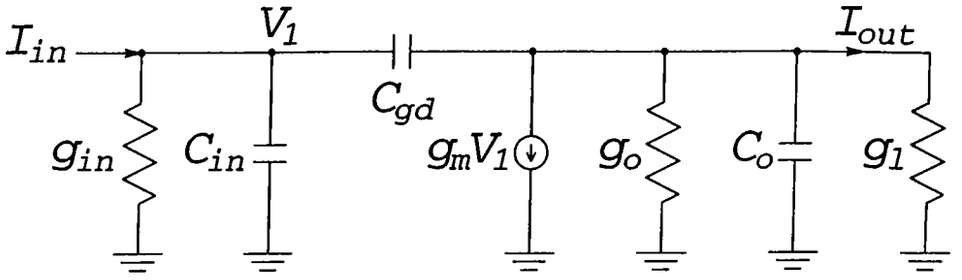

Figure 2.4: Simplified small signal model of current mirror.

KCL at the input and output nodes now yields

$$g_{in}V_1 + sC_{in}V_1 + sC_{gd}(V_1 - V_2) - I_{in} = 0 \tag{2.7}$$

$$sC_{gd}(V_2 - V_1) + g_m V_1 + g_o V_2 + sC_o V_2 + g_l V_2 = 0 \tag{2.8}$$

substituting $I_{out} = g_l V_2$ and rearranging the terms,

$$\frac{I_{out}}{I_{in}} = H(s) = \frac{-g_l(g_m - sC_{gd})}{[sC_{ieq} + g_{in}][sC_{oeq} + g_{oeq}] + sC_{gd}(g_m - sC_{gd})} \tag{2.9}$$

where

$$\begin{aligned}
C_{gd} &= C_{gdp} + C_{gdn} && (2.10)\\
C_{ieq} &= C_{gd} + C_{in} && (2.11)\\
C_{in} &= 2C_{gsp} + 2C_{gsn} + 2C_{gbp} + 2C_{gbn} + && (2.12)\\
&\quad C_{dbp} + C_{dbpc} + C_{dbn} + C_{dbnc} + C_{gdpc} + C_{gdnc} && (2.13)\\
C_{oeq} &= C_{gd} + C_o && (2.14)\\
C_o &= C_{dbp} + C_{dbpc} + C_{dbn} + C_{dbnc} + C_{gdpc} + C_{gdnc} && (2.15)\\
g_{oeq} &= g_o + g_l && (2.16)\\
g_o &= g_{dp} + g_{dn} && (2.17)\\
g_{in} &= g_m + g_{dp} + g_{dn} && (2.18)
\end{aligned}$$

It is clear from Fig. 2.3 that most of the parasitic capacitances appear in parallel at the input stage, between input node and ground. The output conductances of the transistors are added to g_m, resulting in an increased input conductance g_{in}. First parasitic pole is located approximately at g_{in}/C_{ieq} and the second pole occurs approximately at g_{oeq}/C_{oeq}. The capacitance between

C_{gdp}	$1.44fF$
C_{gdpc}	$8.399fF$
C_{gdn}	$2.263fF$
C_{gdnc}	$0.6034fF$
C_{gsp}	$6.161fF$
C_{gspc}	$8.399fF$
C_{gsn}	$17.55fF$
C_{gsnc}	$0.6034fF$
C_{gbp}	$8.872fF$
C_{gbn}	$22.18FF$
C_{dbp}	$6.745fF$
C_{dbpc}	$33.95fF$
C_{dbn}	$10.85fF$
C_{dbnc}	$3.798fF$
g_{mp}	$37.57\mu(1/\Omega)$
g_{mn}	$91.6\mu(1/\Omega)$
g_{dp}	$0.8375\mu(1/\Omega)$
g_{dn}	$0.7658\mu(1/\Omega)$

Table 2.1: Parameters obtained from HSPICE

input and output nodes, C_{gd}, yields a zero at g_m/C_{gd}. Besides directly being added to input and output capacitances, C_{gd} causes a slight shift in two poles due to the additive term $sC_{gd}(g_m - sC_{gd})$ in the denominator of $H(s)$.

The circuit in Fig. 2.1 is simulated using MIETEC 2.0μ technology and the parameters obtained from HSPICE simulations are shown in table 2.1. Using this table, coefficients of the transfer function $H(s)$ given in Eq. 2.9 are calculated as shown in table 2.2. The output conductance g_l is chosen to be equal to g_{in} since it is the admittance seen when an identical block is cascaded.

C_{gd}	$3.703fF$
C_{ieq}	$177.5744fF$
C_{oeq}	$68.0484fF$
g_m	$129.17\mu(1/\Omega)$
g_{in}	$130.7733\mu(1/\Omega)$
g_l	$130.7733\mu(1/\Omega)$
g_{oeq}	$132.3766\mu(1/\Omega)$

Table 2.2: Calculated parameters

Substituting the calculated parameters into $H(s)$ given in Eq. 2.9 magnitude of $H(s)$ is plotted in Fig. 2.5. The first parasitic pole is located at $736.44MHz$, whereas the second pole occurs at $1.95GHz$. Zero of the transfer function is located at $34.9GHz$.

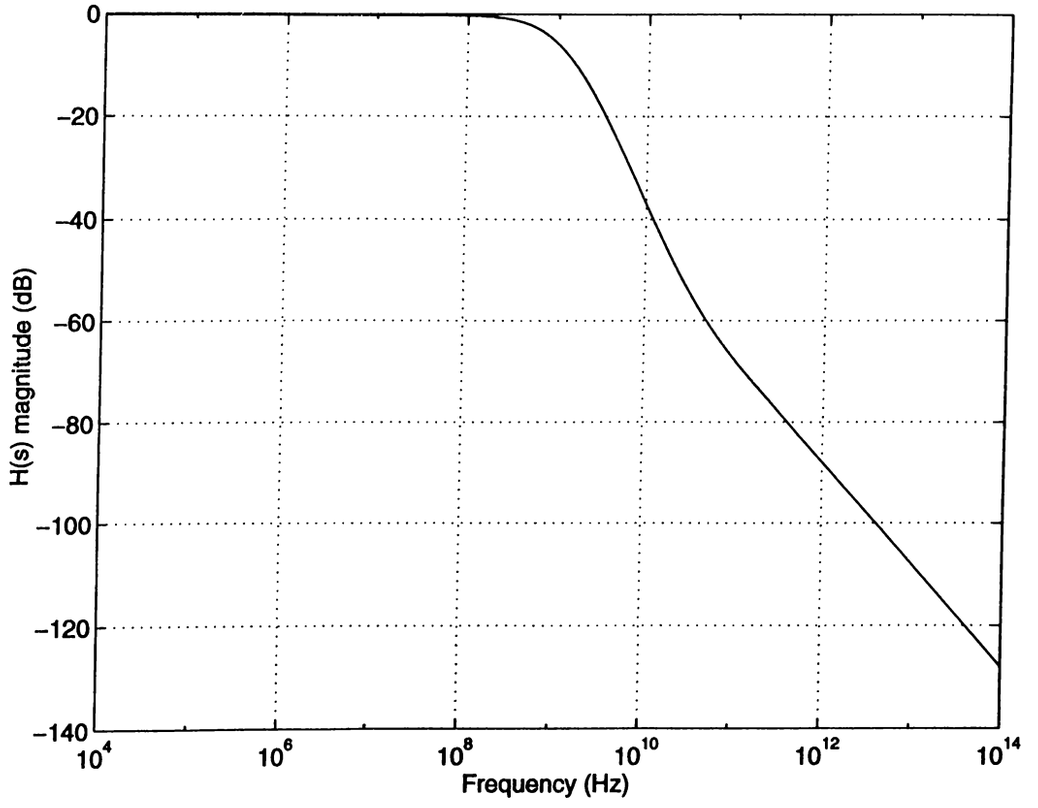

Figure 2.5: Magnitude plot of $H(s)$

In the denominator of $H(s)$, the additive term $sC_{gd}(g_m - sC_{gd})$ does not add an extra pole, but slightly shifts the transfer function. In order to show this effect, let us define the following function

$$H'(s) = \frac{-g_l(g_m - sC_{gd})}{[sC_{ieq} + g_{in}][sC_{oeq} + g_{oeq}]} \tag{2.19}$$

Magnitude plot of the error function $\epsilon(s) = [H(s) - H'(s)]$ is plotted in Fig. 2.6. Note that, magnitude of the error caused by the additive term $sC_{gd}(g_m - sC_{gd})$ is below $-40dB$. Therefore, ignoring this term, we can say that parasitic capacitances and conductances yield 2 poles and a zero, where only the first pole is below gigahertz range.

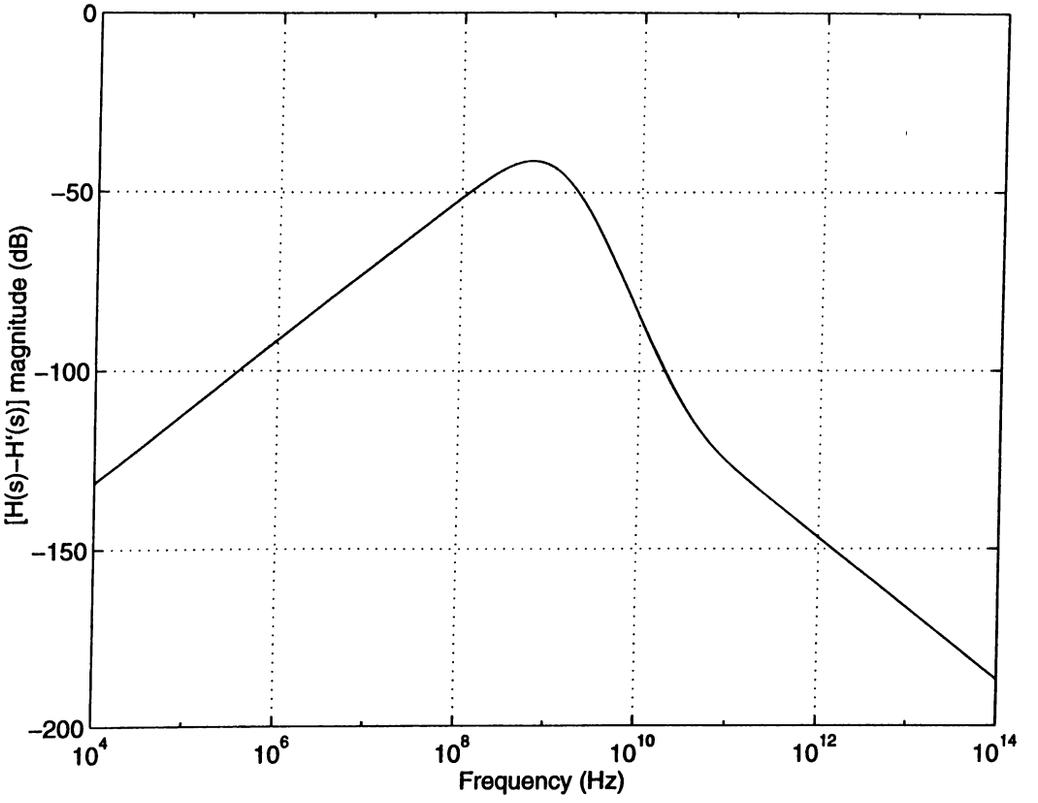

Figure 2.6: Magnitude plot of $\epsilon(s) = [H(s) - H'(s)]$

Up to this point, we have analyzed the current mirror with one output stage. Unlike voltage mode circuits, only one circuit block can be connected to the output stage of the current mirror. Therefore, multiple output stages are required for current multiplication and feedback implementation. For the given current mirror structure, this is simply achieved by connecting an inverter together with its tuning transistors to the input node. The configuration is shown in Fig. 2.7. Each output current branch is called a *current replica.*

In order to use in filter implementation, damped integrator and damped differentiator blocks are constructed using the current mirror and capacitors.

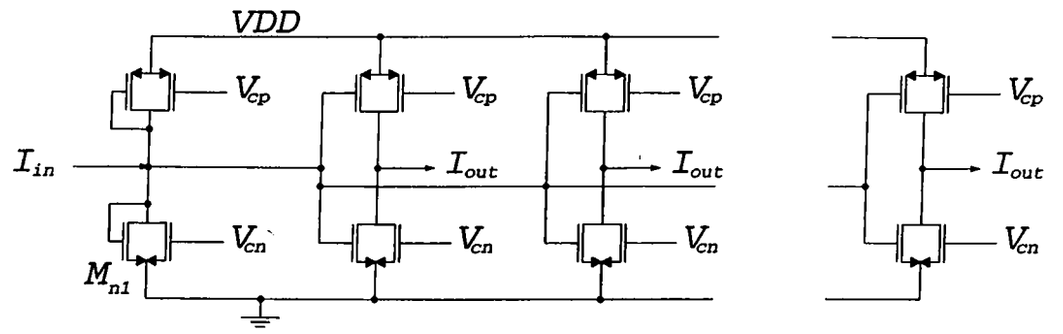

Figure 2.7: Current multiplication

2.1 Damped Integrator

Damped integrator is the basic building block for the construction of low-pass biquadratic filters as well as band-pass biquads. Characteristic function for a damped integrator is given as follows

$$H(s) = \frac{a}{s+a} \tag{2.20}$$

where a is the dominant pole of the circuit. If a capacitor C_a is connected between the input node of the current mirror and ground, small signal equivalent model for the resulting circuit becomes as in Fig. 2.8

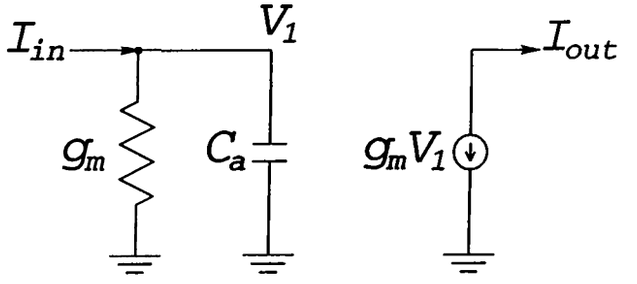

Figure 2.8: Small signal model of damped integrator.

KCL at the input and output nodes yields

$$I_{in} = (sC_a + g_m)V_1 \tag{2.21}$$

$$I_{out} = -g_m V_1 \tag{2.22}$$

resulting in

$$\frac{I_{out}}{I_{in}} = -\frac{g_m/C_a}{s + g_m/C_a} \tag{2.23}$$

Further analysis including parasitic capacitances and output conductances yields the same small signal model as in Fig. 2.4, where C_{ieq} is replaced by $C_{ieq} + C_a$. Since the input conductance is also increased to g_{in}, the dominant pole is shifted to $g_{in}/(C_a + C_{ieq})$. The non-dominant pole is still the same as the second parasitic pole of the current mirror, located at g_{oeq}/C_{oeq}. Previously, it is calculated as $1.95GHz$, which is located very far from the dominant pole. Consequently, below gigahertz range parasitics do not have a significant effect on the transfer function other than a slight shift of the dominant pole. Correction of this shift is possible by tuning, which will be discussed in the next chapter. Therefore, the proposed structure is very suitable for high frequency filter design.

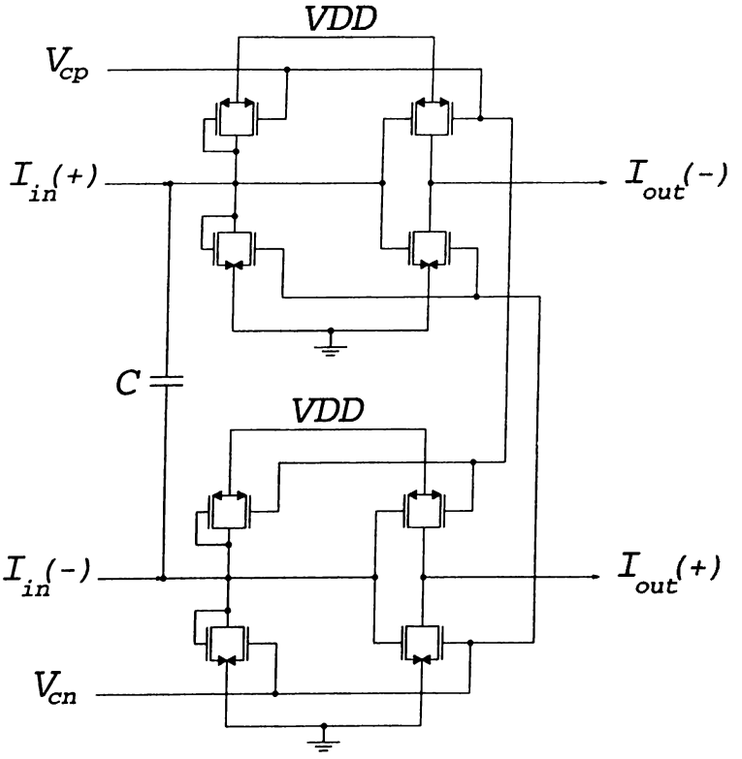

Figure 2.9: Differential configuration.

In order to obtain better noise characteristics and wider dynamic range, a fully differential block is needed. This is achieved by connecting two basic blocks as shown in Fig. 2.9. Besides providing both positive and negative output currents for feedback implementation, the differential configuration requires half the capacitance used for the non-differential block for the same

cutoff frequency, which means that area of the capacitors are reduced by a factor of 2.

2.2 Damped Differentiator

Damped differentiator is the basic building block for the design of high-pass biquadratic filters. Also, it can be used in the design of band-pass biquads. Characteristic function of a damped differentiator is given as follows

$$H(s) = \frac{s}{s+a} \tag{2.24}$$

where a is the dominant pole. For the design of damped differentiator, the input capacitor is placed between the input node of the current mirror and another conductance (g_m) block as in Fig. 2.10.

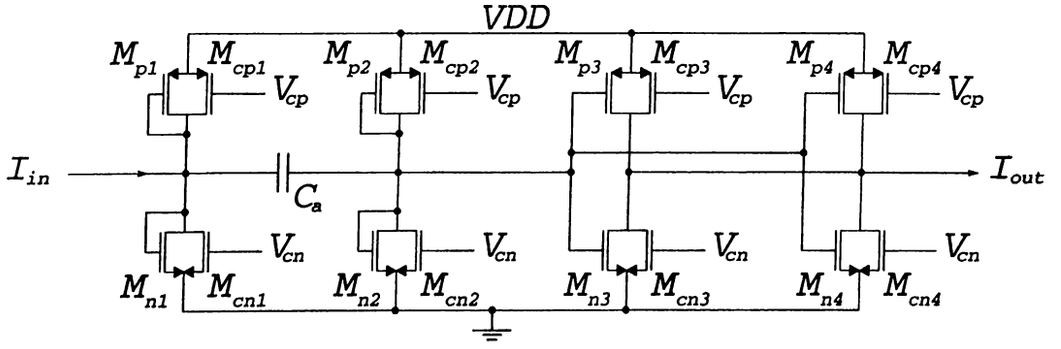

Figure 2.10: Schematic of damped differentiator.

Neglecting the effect of parasitics, the small signal model is obtained as shown in Fig. 2.11.

Writing the node equations

$$V_x = I_{in}\frac{1}{g_m + \frac{1}{1/sC+1/gm}} \tag{2.25}$$

$$= I_{in}\frac{1}{g_m + \frac{g_m sC}{g_m+sC}} \tag{2.26}$$

$$= I_{in}\frac{g_m + sC}{g_m(2sC + g_m)} \tag{2.27}$$

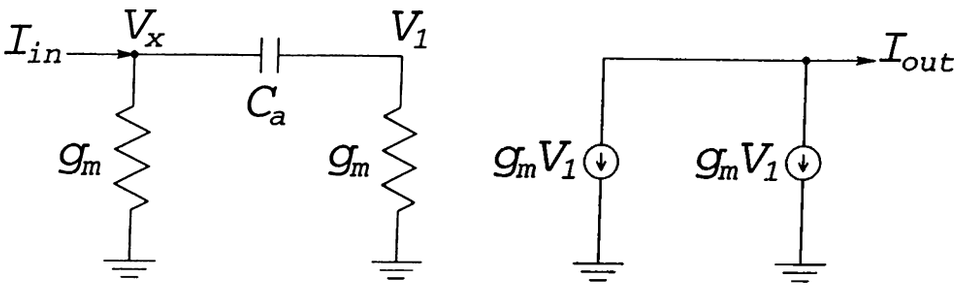

Figure 2.11: Small signal model of damped differentiator.

$$V_1 = V_x \frac{1/g_m}{1/g_m + 1/sC} \tag{2.28}$$

$$= I_{in} \frac{g_m + sC}{g_m(2sC + g_m)} \frac{sC}{(g_m + sC)} \tag{2.29}$$

$$= I_{in} \frac{sC}{g_m(2sC + g_m)} \tag{2.30}$$

$$I_{out} = -2V_1 g_m \tag{2.31}$$

$$= -\frac{2sC}{2sC + g_m} \tag{2.32}$$

resulting in,

$$\frac{I_{out}}{I_{in}} = -\frac{s}{s + \frac{g_m}{2C}} \tag{2.33}$$

Detailed analysis shows that parasitic capacitances at the input node are not absorbed in the input capacitance C_a, unlike the low-pass case. Furthermore, extra g_m block at the input stage adds new parasitics to the circuit. Output conductance of the block is also increased as well as output capacitance, since another current replica is added to get unity high frequency gain. Because of all these factors, high-pass filter design is restricted to lower frequencies than in low-pass case. However, the parasitic pole is still beyond some hundreds of megahertz frequency, and filters can be designed within the low VHF range.

Again for noise immunity and feedback implementation, differential block is needed for the damped differentiator. The differential configuration is obtained by just adding another differentiator block with negative input current.

As mentioned in the introduction, in all simulations throughout this thesis

MIETEC 2μ technology is used. The main limitation is that extracted parasitic capacitance values can be as large as $1pF$, which is important at high frequencies. If the parasitics are not small compared to input capacitance, the error in the transfer function may be beyond tuning limits. To avoid this, for the same corner frequency, g_m can be made larger with larger input capacitance so that parasitics have less effect. However, large g_m means increasing W/L ratios, together with parasitics. Besides, chip area increases. Therefore, increasing g_m is not a good solution. Using a better technology, such as 0.7μ brings the frequency range beyond $0.5GHz$.

Chapter 3

TUNING

The transfer function of a filter varies considerably due to process variations, temperature effects and aging. The resulting variation in component values and parameters can be as high as 30% of the desired ones. In addition, change of parameters for each transistor is not the same. Therefore, tuning is necessary for continuous time filters in order to correct these errors.

In the proposed structure, tuning is achieved by changing the bias voltage V_b, by either sinking or supplying a constant DC current to the input and output nodes. The input stage of the current mirror is redrawn in Fig. 3.1. The bias voltage V_b can be calculated using the following relation

$$V_b = \frac{\sqrt{\beta_p}(V_{dd} + V_{tp}) + \sqrt{\beta_n}V_{tn}}{\sqrt{\beta_p} + \sqrt{\beta_n}} \tag{3.1}$$

For $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$, V_b is equal to $V_{dd}/2$. For $\beta_n > \beta_p$, V_b is less than $V_{dd}/2$, and vice versa. Typically, treshold voltage of a MOS transistor is 1 volt for n-types, and -1 volt for p-types. Hence V_b voltage is confined between $V_{dd} - 1 = 2V$ and $1V$, including the voltage swing caused by the input current.

To explain the tuning mechanism, first let us explain how g_m changes for varying V_b, and then continue with the control mechanism of V_b.

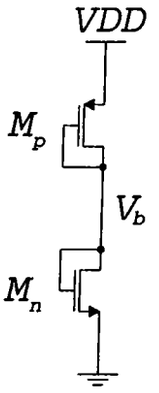

Figure 3.1: Input stage of the current mirror.

Writing the g_m relation as given in Eq. 2.4,

$$g_m = \beta_p(V_{dd} - V_b + V_{tp}) + \beta_n(V_b - V_{tn}) \tag{3.2}$$

rearranging the terms, we have

$$g_m = [\beta_p(V_{dd} + V_{tp}) - \beta_n V_{tn}] + V_b(\beta_n - \beta_p) \tag{3.3}$$

The first term in Eq. 3.3, which is square-bracketed, is independent of V_b and determined by ratios of the n and p transistors. The second term is the key point for the tuning mechanism. Since variation of the V_b voltage is 1 volts for the best case, maximum variation of g_m is $(\beta_n - \beta_p)$. For a MOS transistor, the transconductance parameter β is given as

$$\beta = \frac{W}{L}\mu C_{ox} \tag{3.4}$$

Typically, μ_n is 2.5-3 times greater than μ_p, while the oxide thickness C_{ox} is the same for both. Therefore, for equal sized transistors, β_n is readily greater than β_p. Keeping the size of p-type transistors minimum, $(\beta_n - \beta_p)$ factor can be increased by choosing a wider n-type transistor for the current mirror. As a result, the tuning range can be increased by just using wider n transistors. The other way is also possible, that is to keep the size of n transistors minimum and using wider p-type transistor. However, to obtain the same tuning range, p transistors should be much larger, resulting in more chip area. In the analysis, we will use the first approach and have minimum-sized p transistors ensuring that $\beta_n > \beta_p$. Looking at Eq. 2.4 more closely, it is obvious that a raise in V_b

causes g_m to increase, which we call *up-tuning*. Also, *down-tuning* is achieved by decreasing V_b together with g_m.

Even though increasing W/L ratio of the n transistors also increase the tuning range, it has a negative effect on the input signal swing, which is another bottleneck in low-voltage circuits. Maximum input swing is obtained when the bias voltage V_b is equal to $V_{dd}/2$. As discussed earlier, this condition is met when $\beta_n = \beta_p$, resulting in zero tuning range for $V_{tn} = -V_{tp}$. Having $\beta_n > \beta_p$ the tuning range increases together with decreasing V_b and decreasing input swing. Therefore, there is a trade-off between input signal swing and the tuning range of the current mirror. Besides, the tuning is not symmetrical when V_b is different from $V_{dd}/2$. For our case, down-tuning range is less than up-tuning range. For low-pass filter case, this is more preferrable than the reverse condition, since most of the parasitic capacitances are absorbed in the input capacitor of the filter block, decreasing the corner frequency or shifting it *down*.

So far, we have discussed the effect of V_b on g_m, but we did not mention how V_b is changed. We will now analyze the up-tuning and down-tuning mechanisms separately. It should be noted that, when down-tuning mechanism is active, up-tuning is off, and vice versa.

3.1 Down-Tuning

As stated earlier, down-tuning is achieved by decreasing the bias voltage V_b. This is simply carried out by sinking a constant DC current from the input and the output nodes. Since the gate-to-source voltages for the output transistors are the same as those of input ones, bias voltage at the output node is the same as the input bias voltage, V_b, if the same DC current is sunk from that node. Therefore, our analysis will only include the input stage, and extend it to output stage using matched transistors.

Figure 3.2 shows the down-tuning mechanism at the input stage. The transistor M_{cn} is controlled by V_{cn} voltage and it is operated either in cut-off

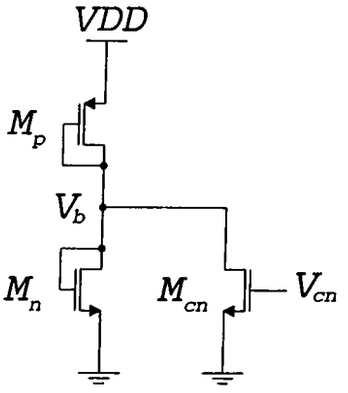

Figure 3.2: Input stage for down-tuning.

or in saturation region.

Assuming that M_{cn} is in saturation, KCL at the input node yields the following equation

$$I_{dn} = \frac{\beta_p}{2}(V_{dd} - V_b + V_{tp})^2 - \frac{\beta_n}{2}(V_b - V_{tn})^2 \tag{3.5}$$

where I_{dn} is the constant DC current given as

$$I_{dn} = \frac{\beta_{cn}}{2}(V_{cn} - V_{tn})^2 \tag{3.6}$$

In Eq. 3.6, β_{cn} is the transconductance parameter of the transistor M_{cn}. In order to obtain maximum tuning range, the ratios of the tuning transistor (W_{cn} and L_{cn}) should be chosen appropriately so that V_b voltage can be adjusted down to V_{tn}, and no less than that value since the transistor M_n cease to conduct below that voltage. In Fig. 3.3, V_{ds} and $(V_{gs} - V_{tn})$ for varying V_{cn} is plotted for the transistor M_{cn}. Length of the transistor is chosen as 3μ, which is the minimum for the technology used.

In the figure, minimum attainable V_b values, which is equal to V_{ds}, is determined by the intersection point of V_{ds} and $V_{gs} - V_{tn}$ curves. Below that point, the tuning transistor M_{cn} operates in the linear region. The point is going down, as the width W_{cn} is increased. However, V_b is already limited by the treshold voltage V_{tn}, and additional input swing. Therefore, choosing a ratio which allows V_b to decrease down to 0.6 volts has no meaning other than waste of chip area since it requires wider transistor. In Fig. 3.3, $W_{cn} = 4\mu$ seems to be the most appropriate one, and it is chosen for further simulations. If the

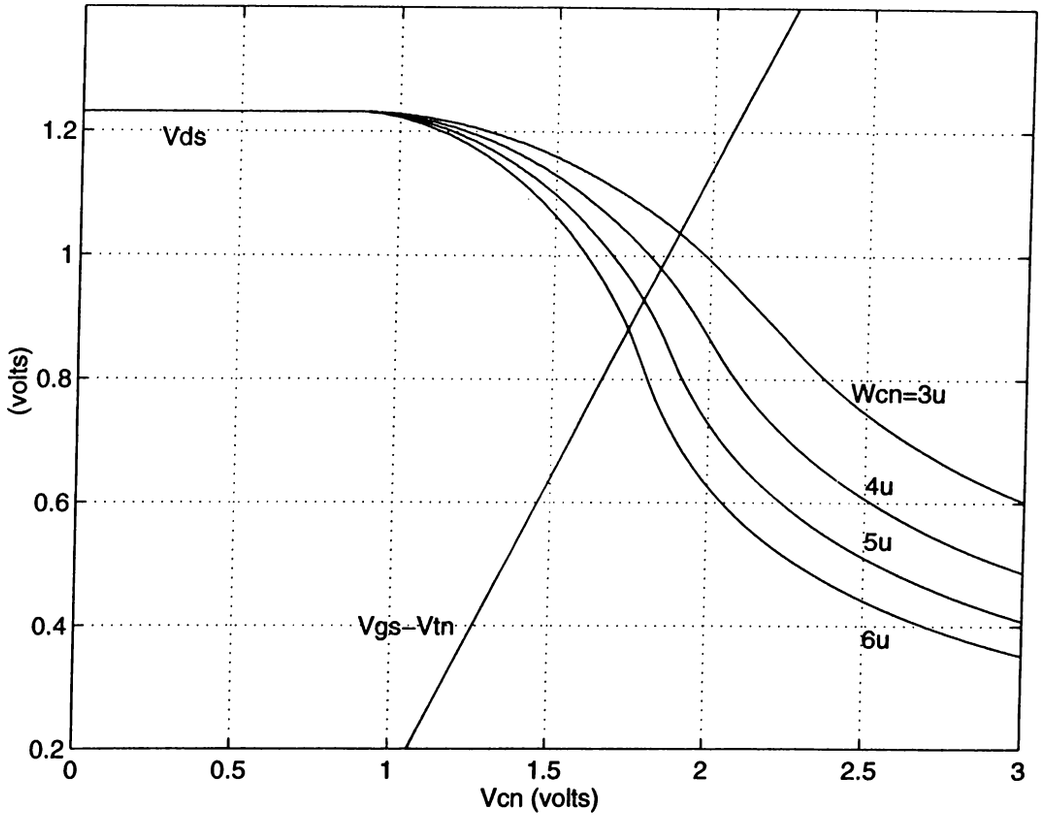

Figure 3.3: Effect of V_{cn} for several W_{cn}.

quiscent V_b voltage for $V_{cn} = 0$ had been higher, a wider transistor may have been chosen.

Going back to the basic block given in Fig. 2.1, with M_{cp1} and M_{cp2} are off and the rest in saturation, the small signal model for the circuit is the same as in Fig. 2.4, with the difference in g_{in} and g_{out} as in the following

$$g_{in} = g_m + g_{dp} + g_{dn} + g_{dcn} \tag{3.7}$$

$$g_o = g_{dp} + g_{dn} + g_{dcn} \tag{3.8}$$

Resulting in the same transfer function as in Eq. 2.9, the tuning transistors increase the input and the output conductances by a small amount, which is considered as the non-ideal effect of the tuning mechanism. Neglecting this effect, g_m decreases considerably, also decreasing the corner frequency. Figure 3.4 shows g_m versus V_{cn} plot within the valid range.

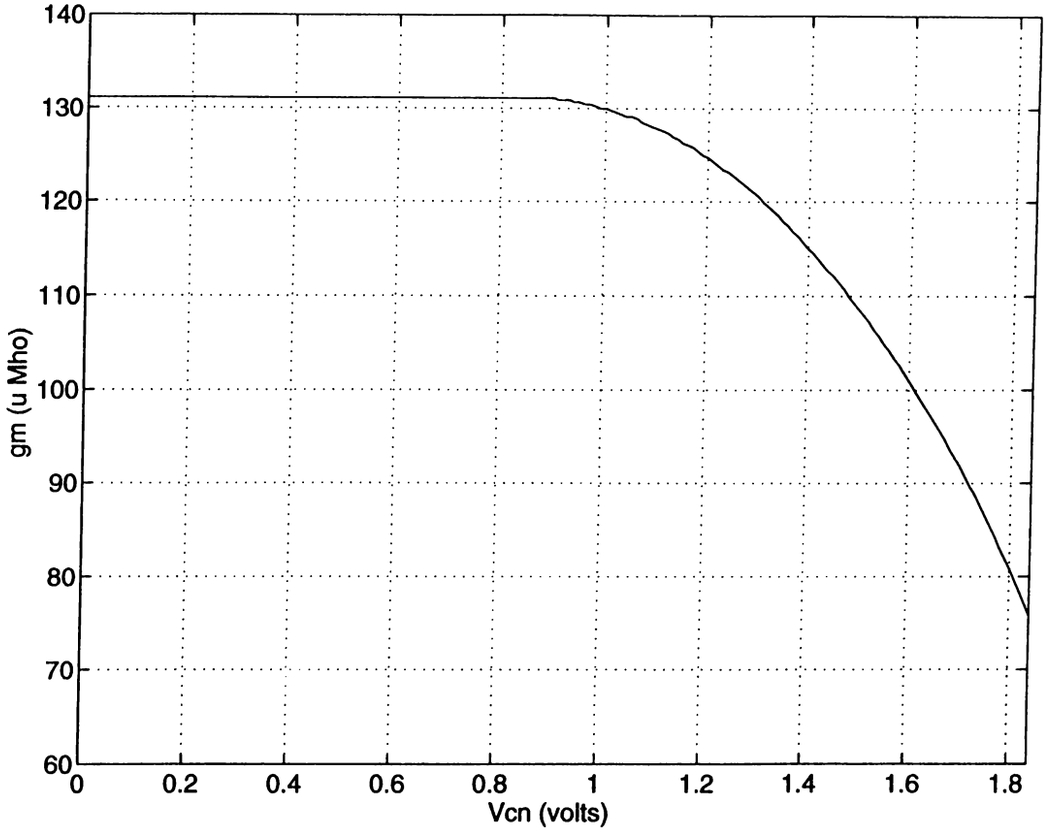

Figure 3.4: g_m versus V_{cn}.

Input conductance of the current mirror is determined by the (W/L) ratios of the transistors M_{n1} and M_{p1}. In an ideal current mode circuit, input conductance is equal to infinity, therefore the voltage swing is zero. Due to finite conductance of input stage, a small voltage swing occurs, which also limits the maximum input signal level. Having g_{in} as the input conductance, $(V_b + \frac{I_{in}}{g_{in}})$ should be above V_{tn} and below $3 - V_{tp}$. Since V_b is controlled by means of V_{cn}, maximum input swing also depends on V_{cn}, which is plotted in Fig. 3.5.

As it is clear from the figure, a linear relationship is observed between I_{out} and I_{in} when $I_{in} < 50\mu A$. This range can be increased by using wider transistors for the mirror.

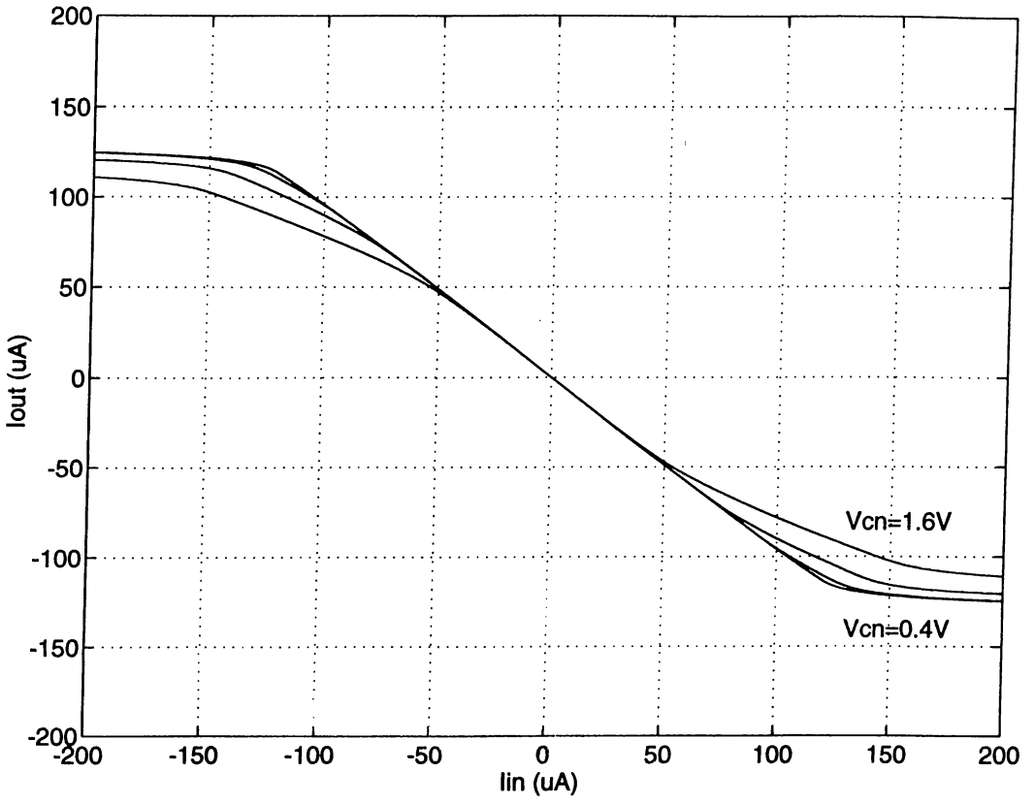

Figure 3.5: I_{out} versus I_{in}

3.2 Up-Tuning

A similar analysis follows for the up-tuning of the current mirror. As in down-tuning case, the input stage as shown in Fig. 3.6 is analyzed. In the figure, the transistor M_{cp} is used to supply a DC current to the input node. The current is controlled by V_{cp} voltage, which also keeps the transistor either in cut-off or in saturation.

Again assuming saturation for the transistor M_{cp}, KCL at the input node yields,

$$I_{dp} = \frac{\beta_n}{2}(V_b - V_{tn})^2 - \frac{\beta_p}{2}(V_{dd} - V_b + V_{tp})^2 \tag{3.9}$$

where I_{dp} is the current supplied to the node and given as

$$I_{dp} = \frac{\beta_{cp}}{2}(V_{dd} - V_{cp} + V_{tp})^2 \tag{3.10}$$

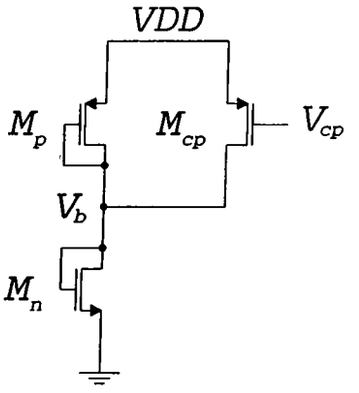

Figure 3.6: Input stage for up-tuning.

This time, the bias voltage V_b is increased, and the amount of increase depends on V_{cp} and β_{cp}. The upper limit for V_b is equal to $(V_{dd} - V_{tp})$, including a positive swing caused by input current. In Fig. 3.7, $|V_{ds}|$ and $(|V_{gs}| + V_{tp})$ curves for the transistor M_{cp} is depicted for several W_{cp} values, where L_{cp} is chosen as 3μ, which is the minimum length.

Minimum $|V_{gs}|$ values are the intersection points of the curves $(|V_{gs}| + V_{tp})$ and $|V_{ds}|$. V_{cp} is valid to the right of that point, where the transistor is not in linear region. To locate this intersection point at the optimum value, which is $V_{dd} - V_{tp}$, width of the transistor, W_{cp}, is chosen as 35μ. Further increasing the width causes V_b to rise over 2V within the valid range of V_{cp}, where M_p gets into cut-off region.

The small signal model for the up-tuned circuit, in which M_{cn1} and M_{cn2} are off and others are in saturation, is the same as in Fig. 2.4. The parameters g_{in} and g_{out} also change as in the following

$$g_{in} = g_m + g_{dp} + g_{dn} + g_{dcp} \tag{3.11}$$

$$g_o = g_{dp} + g_{dn} + g_{dcp} \tag{3.12}$$

Therefore, the transfer function of the current mirror is still the same as in Eq. 2.9 with minor differences in parameters. As shown in Fig. 3.8, value of g_m increases more than twice within the valid range of V_{cp}, which means that the corner frequency can be tuned up more than twice the original one.

Dynamic range of the current mirror, i.e. maximum allowable input current

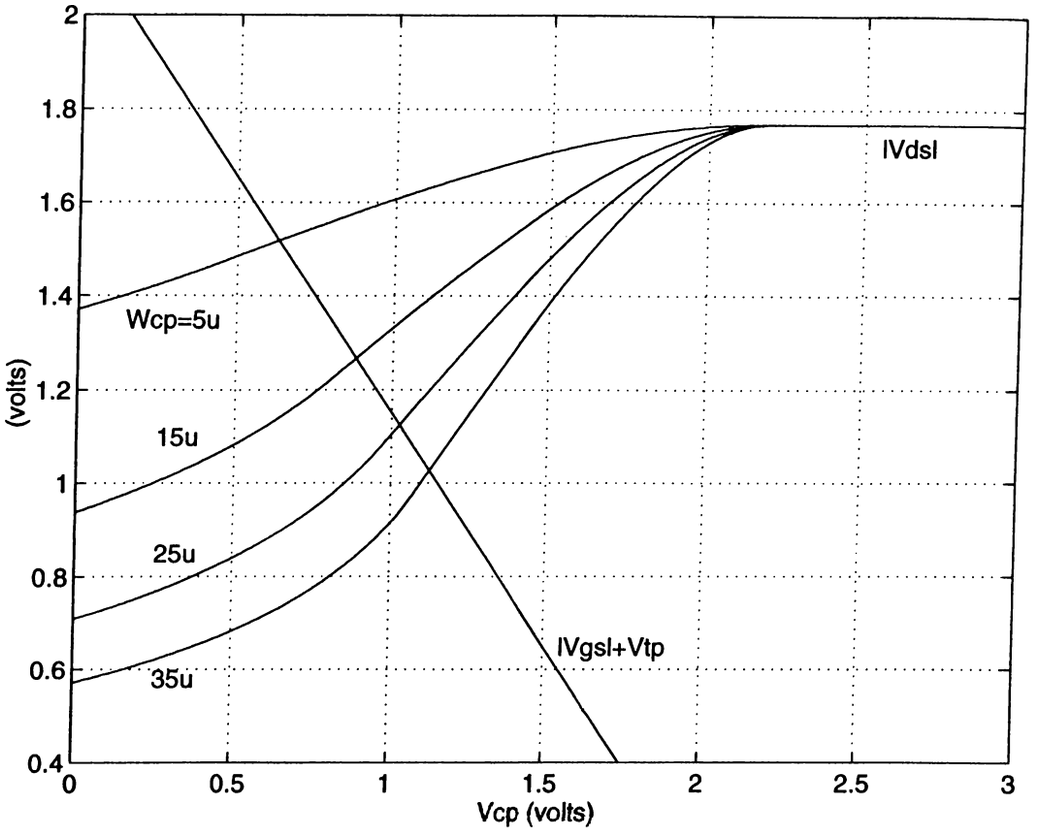

Figure 3.7: Effect of V_{cp} for several W_{cp}.

amplitude also depends on the control voltage V_{cp}. In Fig. 3.9, I_{out} versus I_{in} plots for several V_{cp} voltages are shown. For this case, a linear relationship is observed between I_{in} and I_{out} when $I_{in} < 50\mu A$.

Having the results of both up and down tuning, we will now compare them. Because of the difference in transconductance of the mirror transistors, up and down tuning ranges are not equal. As we discussed earlier, it is better to have wider up-tuning range, considering the effect of parasitics.

Frequency characteristics and up-down tuning curves of the damped integrator obtained from HSPICE simulations are depicted in Fig. 3.10. Due to finite output impedances of transistors and other non-ideal effects, a slight decrease in the passband occurs when the filter is tuned.

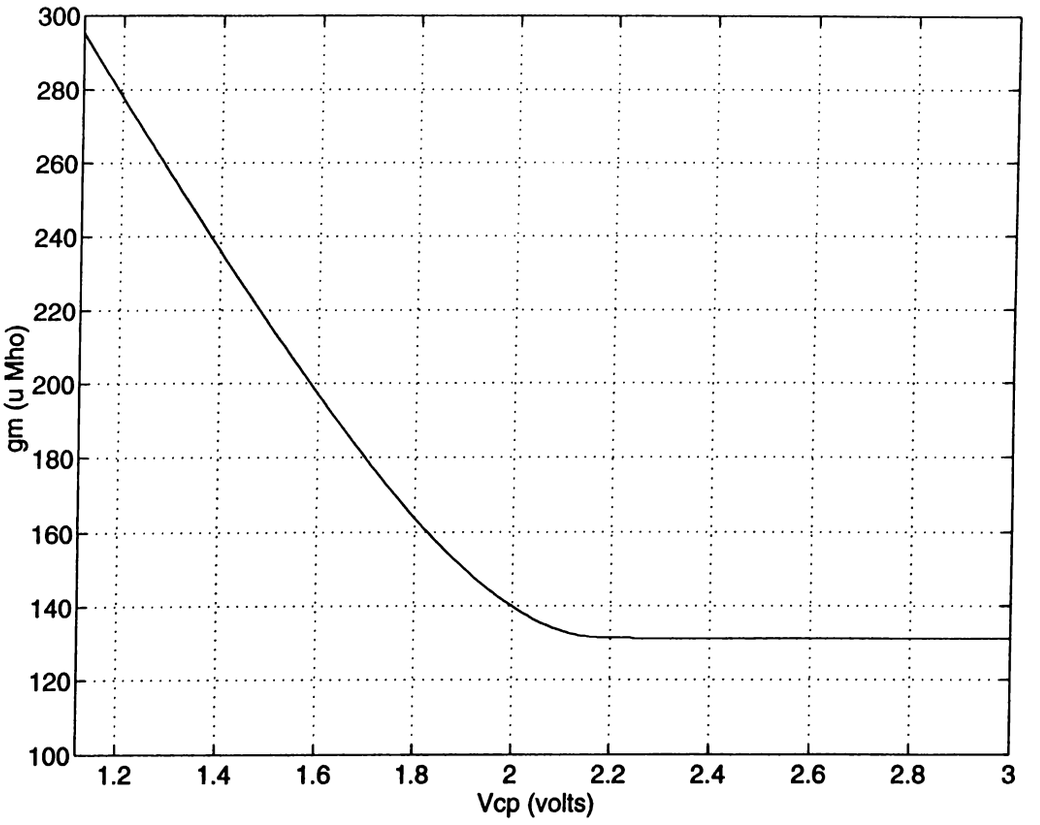

Figure 3.8: g_m versus V_{cp}.

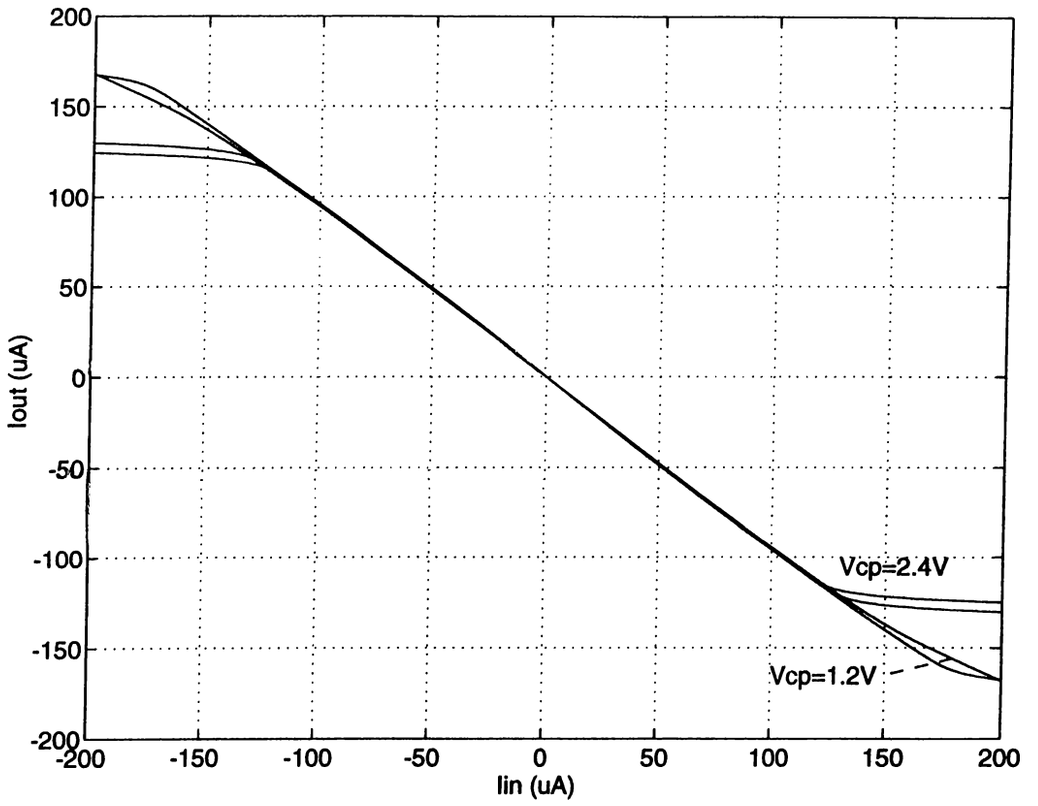

Figure 3.9: V_{cp} versus V_1.

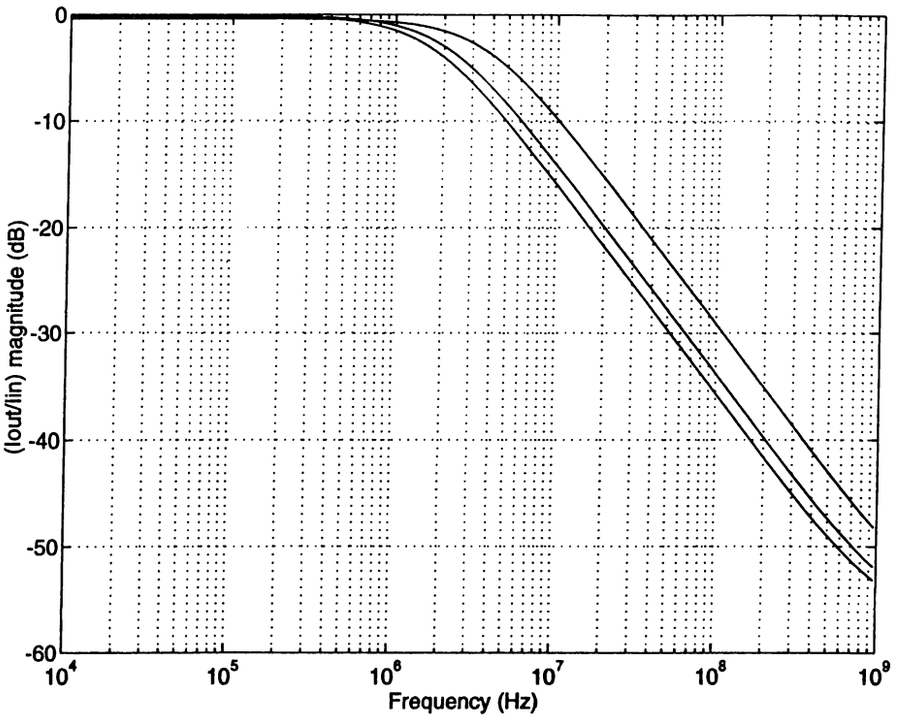

Figure 3.10: Frequency characteristics and tuning curves of the damped integrator.

Chapter 4

IMPLEMENTATION OF FILTER BLOCKS

Realization of filters is carried out by using cascaded biquad synthesis, in which a filter transfer function is decomposed in a cascade of multiple damped integrator and damped differentiator blocks. In Chapter 2, basic building blocks were constructed. In this chapter, biquads of low-pass, high-pass and band-pass functions will be synthesized.

In most general form, a biquad can be represented as

$$H(s) = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{4.1}$$

Depending on the coefficients k_2, k_1 and k_0, all types of biquads can be obtained [4], [12]. Instead of implementing the function in Eq. 4.1 in general circuit form, we will treat all filter types separately.

4.1 Low-pass Biquad Design

A low-pass biquadratic filter is characterized by the transfer function

$$H(s) = \frac{K_0\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.2}$$

In Eq. 4.2, K_0 is the DC gain, Q is the quality factor, and ω_0 is the resonant frequency of the filter. For Q values less than $1/\sqrt{2}$, the magnitude plot has no peak. The case where $Q = 1/\sqrt{2}$ is referred to as the *maximally flat magnitude.* For $Q > 1/\sqrt{2}$, the peak occurs at the frequency ω_0.

Two different approaches for the implementation of the transfer function in Eq. 4.2 are presented in this section. The first approach, the Low-Q biquad, is suitable for filters having low-Q factors. In fact, there is no exact boundary between low and high quality factors. In our analysis, we will treat low quality factor as being less than or equal to 1. The second approach, namely high-Q biquad, can be used in implementation of filters of high-Q factors, as well as low-Q ones.

4.1.1 Low-pass Low-Q Biquad

The first approach for implementation of a biquad is suitable for low-Q designs. The filter is composed of two differential damped integrators which are used in cascade form. Applying a negative feedback from the output to the input, generation of complex poles is achieved. The signal-flow graph of the biquadratic filter is drawn in Fig. 4.1.

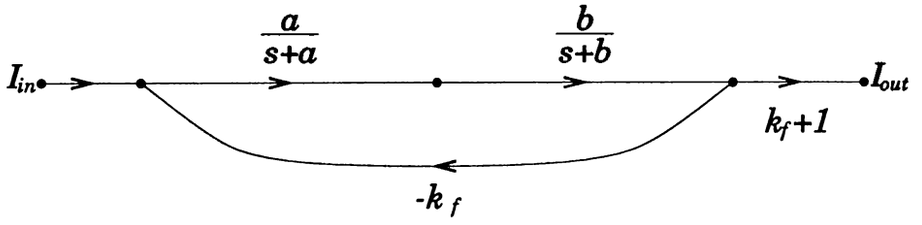

Figure 4.1: Signal-flow graph of low-pass low-Q biquad.

Transfer function of the filter structure in Fig. 4.1 is given as follows

$$\frac{I_{out}}{I_{in}} = \frac{ab(k_f + 1)}{s^2 + (a + b)s + ab(k_f + 1)} \tag{4.3}$$

where a and b are g_m/C values for each damped integrator.

Now, let us find the relationship between Q-factor and the feedback coefficient k_f. Without loss of generality, we can choose $\omega_0 = 1$ in order to simplify the equations. Then the denominator of the low-pass biquad becomes $s^2 + s/Q + 1$. Equating this to the denominator of Eq. 4.3 yields

$$a + b = 1/Q \tag{4.4}$$

$$ab(k_f + 1) = 1 \tag{4.5}$$

resulting in

$$a^2 - \frac{a}{Q} + \frac{1}{k_f + 1} = 0 \tag{4.6}$$

for a to be real, $\Delta \geq 0$

$$\Delta = \frac{1}{Q^2} - \frac{4}{k_f + 1} \geq 0 \tag{4.7}$$

$$k_f \geq 4Q^2 - 1 \tag{4.8}$$

Consequently, it is clear from Eq. 4.8 that for high-Q filters, feedback coefficient k_f, and hence number of current replicas at the output stage becomes very large. This increases non-ideal and parasitic effects considerably as well as the chip area. Furthermore, connecting a large number of output stages in parallel causes the output impedance to decrease, which ideally should be infinity. However, the block can be used in the design of low-Q biquads such as second order Butterworth filter with a Q-factor of $1/\sqrt{2}$.

Implementation of the low-Q biquad using MOS transistors is given as in Fig. 4.2. The numbers k_f and $k_f + 1$ represent the number of current replicas, i.e. number of output stages connected in parallel. The two capacitors, C_1 and C_2 determine filter coefficients. The frequency characteristics and the tuning curves of a second order low-pass Butterworth filter obtained from HSPICE simulations are shown in Fig. 4.3.

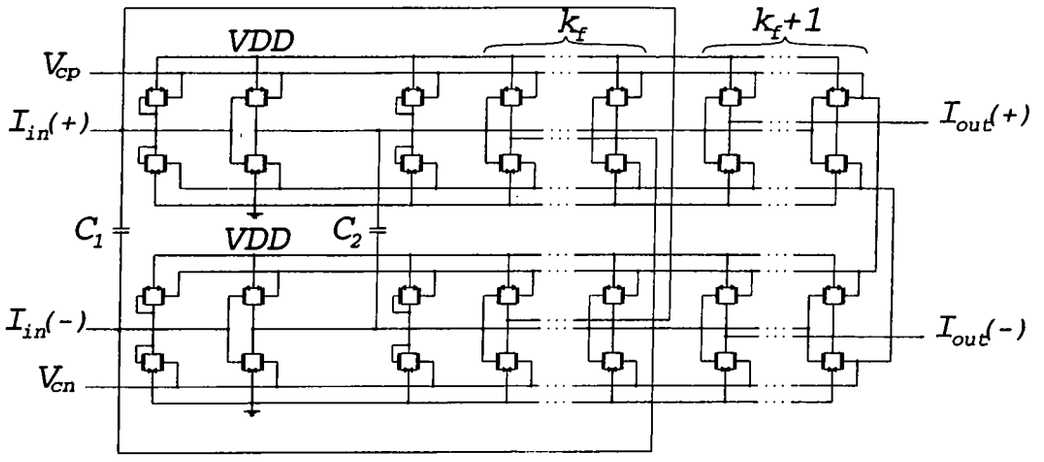

Figure 4.2: Schematic of low-pass low-Q biquad with MOS transistors.

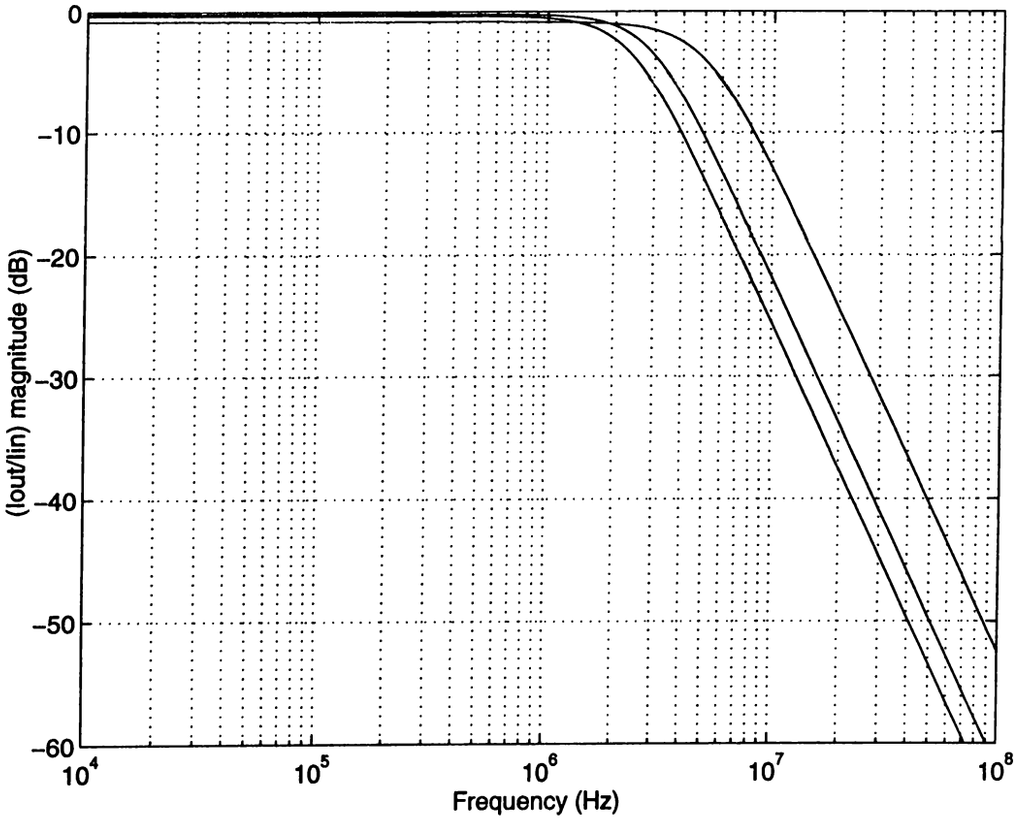

Figure 4.3: Second order Butterworth filter obtained by using the approach suitable for low-Q applications.

4.1.2 Low-pass High-Q Biquad

The second low-pass biquad structure proposed is aimed to have high-Q with minimum number of transistors. With the existing damped integrator block, which has a transfer function $a/(s+a)$, high-Q biquad construction is not practical. Figure 4.4 shows the new first order building block. Originally, it is the same structure as in Fig. 2.1 with a capacitor from the input node to ground, except for a feedback current of $-2I_{out}$ which is fed to the input node.

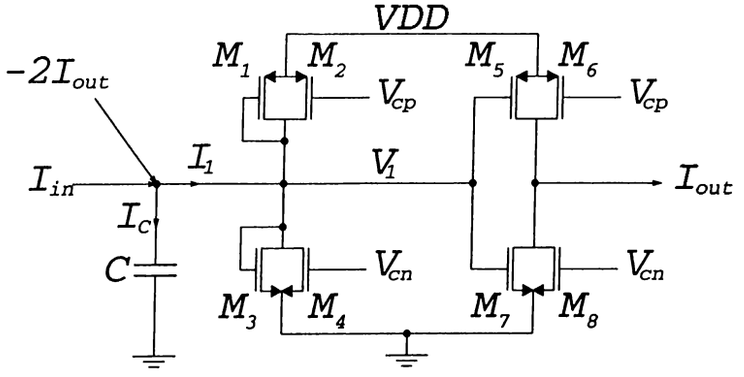

Figure 4.4: Basic building block for low-pass high-Q biquad.

The simplified small signal model is the same as in Fig. 2.2, with the input current as $I_{in} - 2I_{out}$. KCL at the input and output nodes yields

$$I_{in} - 2I_{out} = (sC_a + g_m)V_1 \tag{4.9}$$

$$I_{out} = -g_m V_1 \tag{4.10}$$

resulting in

$$\frac{I_{out}}{I_{in}} = -\frac{g_m/C_a}{s - g_m/C_a} \tag{4.11}$$

Hence the first order block with a transfer function $a/(s-a)$ can be realized. Implementation of the fully differential block is shown in Fig. 4.5.

The block itself has an unstable behaviour due to the pole on the right hand side of s-plane. In order to obtain a stable biquad, this block is combined with the previous one, as in Fig. 4.6. The transfer function of this structure is given as

$$\frac{I_{out}}{I_{in}} = \frac{ab}{s^2 + (a-b)s + ab} \tag{4.12}$$

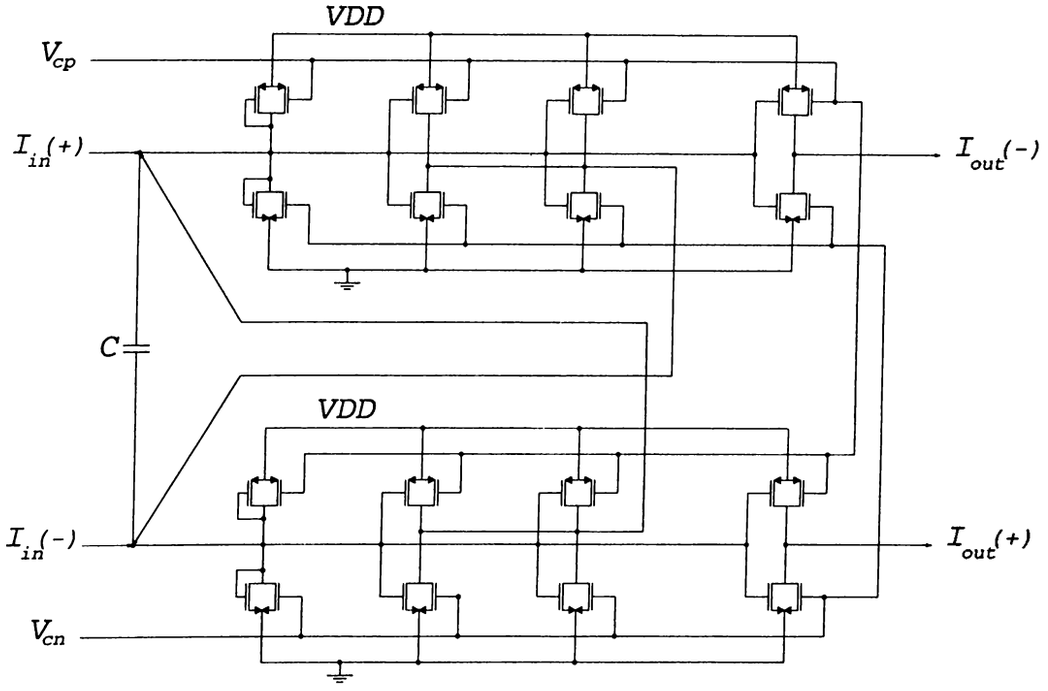

Figure 4.5: Differential configuration.

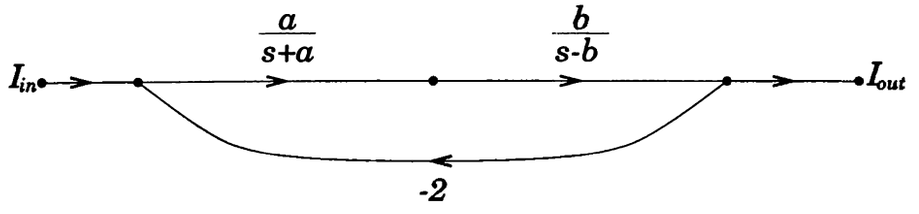

Figure 4.6: Signal-flow graph of low-pass high-Q biquad.

Using Eq. 4.12, high-Q filters can be easily implemented. The biquad is stable as long as $(a - b) > 0$. For high-Q filters, $(a - b)$ becomes very small and with the effect of parasitics it can be negative. This error is eliminated by tuning each first order blocks separately. Since the dc gain of the block is 1, no extra current replicas are needed at the output stage.

Implementation of the biquad using MOS transistors is given in Fig. 4.7. Using this schematics and only changing capacitances, a wide range of filters can be implemented. Frequency characteristics and the tuning curves of a second order Butterworth filter obtained from HSPICE simulations is depicted in Fig. 4.8.

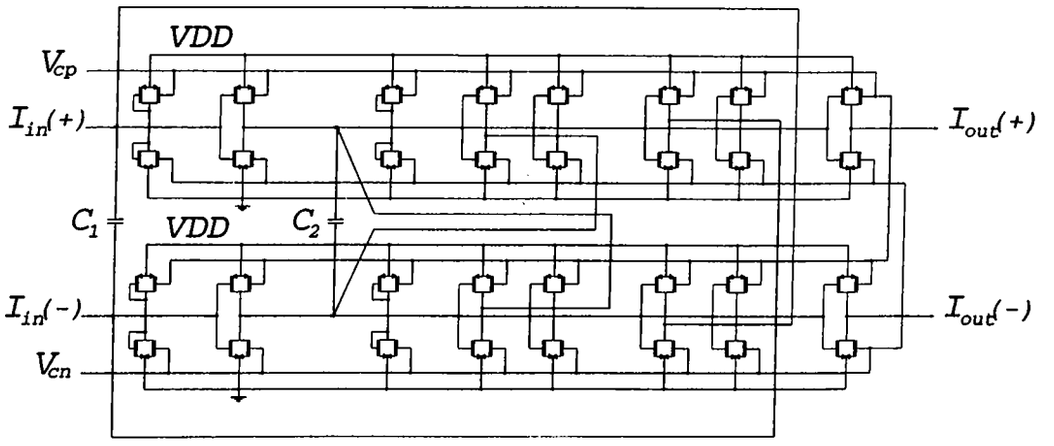

Figure 4.7: Schematic of low-pass high-Q biquad with MOS transistors.

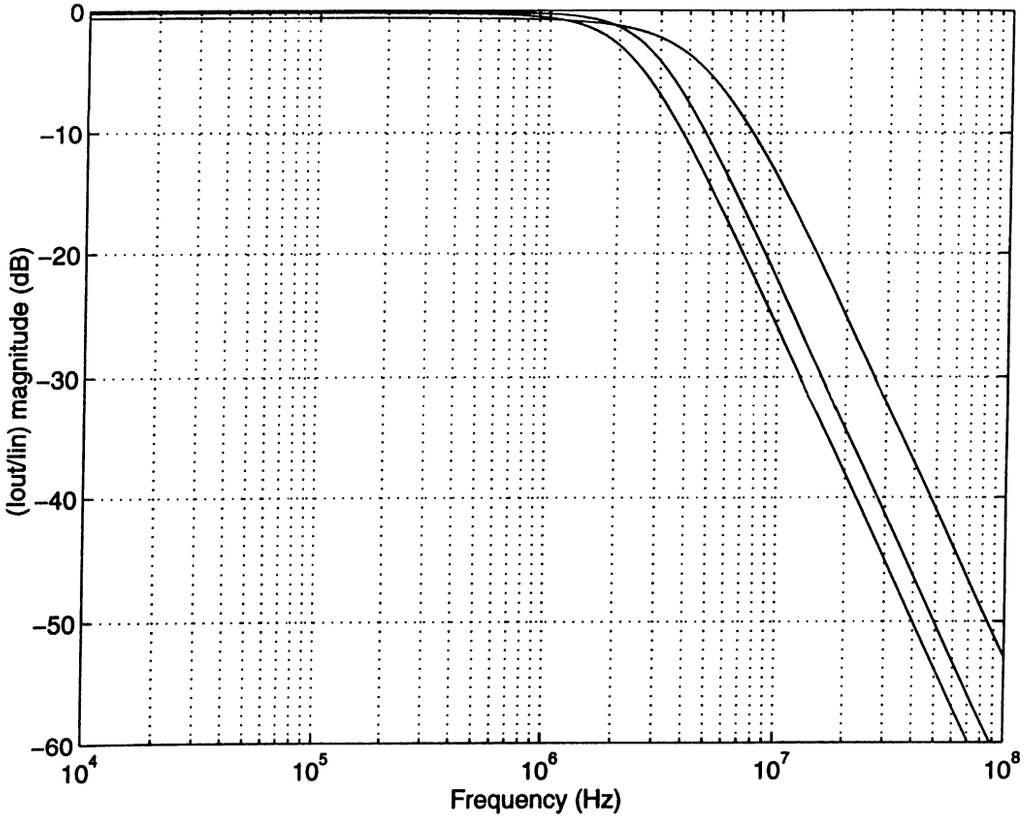

Figure 4.8: Second order Butterworth filter obtained using high-Q biquad structure.

4.2 High-pass Biquad Design

Characteristic equation for a high-pass biquad is given as follows

$$H(s) = \frac{K_0 s^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.13}$$

As in the low-pass case, two approaches for the design of high-pass biquads are presented. The first one is the Low-Q biquad, suitable for low-Q applications and the second one is high-Q biquad.

4.2.1 High-pass Low-Q Biquad

High-pass low-Q biquad includes two damped differentiator blocks in cascade form. The signal flow graph for the biquad structure is shown in Fig. 4.9. As in the low-pass case, the numbers k_f and $k_f + 1$ represent the number of current replicas.

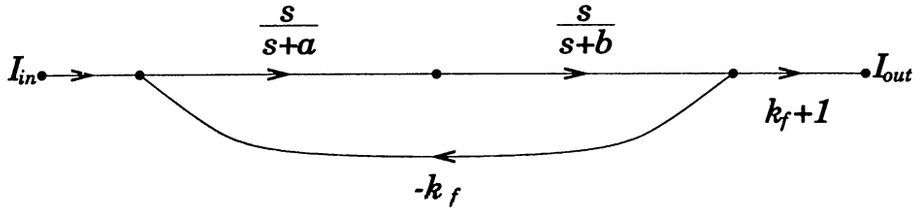

Figure 4.9: Signal-flow graph of high-pass low-Q biquad.

Transfer function of the biquad in Fig. 4.9 is

$$\frac{I_{out}}{I_{in}} = \frac{s^2}{s^2 + \frac{a+b}{k_f+1}s + \frac{ab}{k_f+1}} \tag{4.14}$$

where a and b corresponds to $g_m/2C$ values for each first damped differentiator.

Quality factor of the biquad again depends on the feedback factor k_f. For simplicty, let $\omega_0 = 1$, then

$$\frac{ab}{k_f + 1} = 1 \tag{4.15}$$

$$\frac{a+b}{k_f + 1} = \frac{1}{Q} \tag{4.16}$$

rearranging the terms,

$$a^2 + \frac{k_f + 1}{Q} a + (k_f + 1) = 0 \tag{4.17}$$

for a to be a real number, $\Delta \geq 0$,

$$\frac{(k_f + 1)^2}{Q^2} - 4(k_f + 1) \geq 0 \tag{4.18}$$

$$k_f \geq 4Q^2 - 1 \tag{4.19}$$

Clearly, for high Q values, k_f increases drastically, making biquad design impractical due to the reasons discussed in the low-pass case.

4.2.2 High-pass High-Q Biquad

In order to obtain high-Q biquad, again a first order high-pass block which has a transfer function $s/(s-a)$ is needed. Similar to low-pass case, a positive current of $-2I_{out}$ is fed to the input node of the damped differentiator given in Fig. 2.10. With an input current of $(I_{in} - 2I_{out})$, resulting small signal model is the same as in Fig. 2.11. Using Eq. 2.33 transfer function for the new block is found as

$$s(I_{in} - 2I_{out}) = -I_{out}(s + \frac{g_m}{2C}) \tag{4.20}$$

$$I_{in}s = I_{out}(s - \frac{g_m}{2C}) \tag{4.21}$$

rearranging,

$$\frac{I_{out}}{I_{in}} = \frac{s}{s - \frac{g_m}{2C}} \tag{4.22}$$

Note that the minus sign does not appear in the transfer function. Since $s/(s-a)$ type first order block is obtained, flow graph for the high-Q biquad can be drawn as in Fig. 4.10.

Transfer function of the filter in Fig. 4.10 is found as

$$\frac{I_{out}}{I_{in}} = \frac{s^2}{s^2 + (b-a)s + ab} \tag{4.23}$$

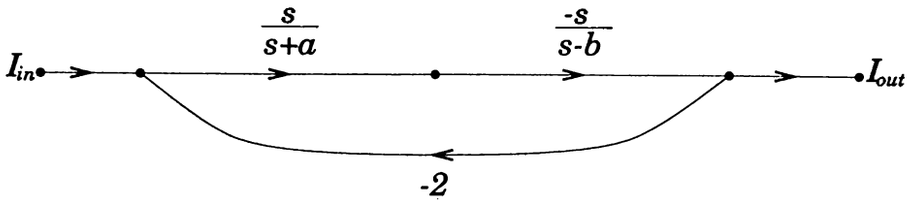

Figure 4.10: Signal-flow graph of high-pass high-Q biquad.

4.3 Band-pass Biquad

Band-pass second order function is given as

$$H_{BP}(s) = \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.24}$$

The first approach in band-pass biquad design is suitable for moderate-Q filters, which have a quality factor up to 3. Biquads are realized by using either two damped integrators, or a damped integrator and a damped differentiator block. Signal flow graphs for the two methods are shown in Figs. 4.11 and 4.12.

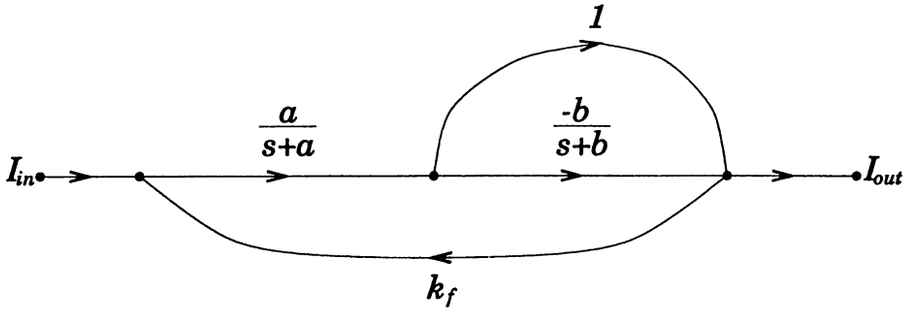

Figure 4.11: Signal-flow graph of band-pass biquad using two damped integrators.

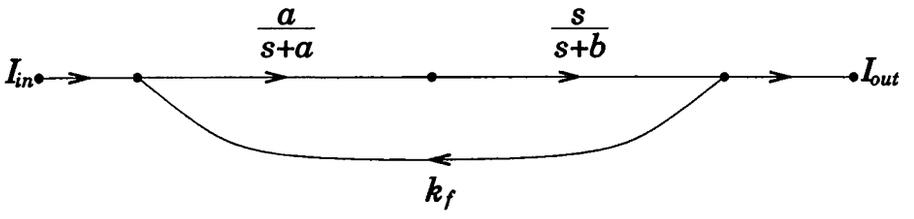

Figure 4.12: Signal-flow graph of band-pass biquad using a damped integrator and a damped differentiator.

Transfer functions corresponding to the two signal flow graphs are the same and given as

$$H(s) = \frac{as}{s^2 + (b - (k_f - 1)a)s + ab} \tag{4.25}$$

In order to have unity pass-band gain,

$$a = b - (k_f - 1)a \tag{4.26}$$

Simplifying, we obtain $b = k_f a$. Quality factor of the biquad is then calculated as follows

$$\frac{\omega_0}{Q} = a \tag{4.27}$$

$$\omega_0 = \sqrt{ab} = a\sqrt{k_f} \tag{4.28}$$

$$Q = \sqrt{k_f} \tag{4.29}$$

Therefore, in both methods the quality factor is equal to $\sqrt{k_f}$, which means that only moderate-Q filters can be implemented. Since k_f is the number of feedback current replicas, construction of high-Q filters (such as 10) is not practical. Besides, for unity DC gain, b is equal to $k_f a$, which is difficult to implement for high k_f values due to parasitic effects. The second structure is more preferrable since it requires approximately half the number of transistors used in the first one for the same k_f.

The second approach allows high-Q band-pass biquad design, by using a damped integrator and a first order section with a transfer function $b/(s - b)$. The corresponding signal flow graph is shown in Fig. 4.13.

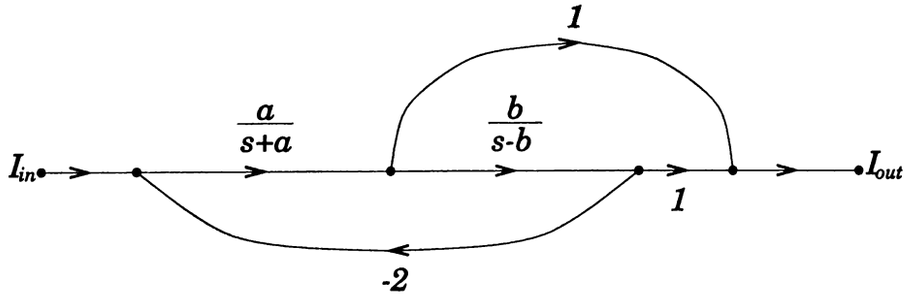

Figure 4.13: Signal-flow graph of band-pass biquad for high Q-factor

The transfer function of the biquad in Fig. 4.13 is

$$\frac{I_{out}}{I_{in}} = \frac{as}{s^2 + (a-b)s + ab} \tag{4.30}$$

Choosing $\omega_0 = 1$ for simplicity, the quality factor Q and the pass-band gain A are calculated as follows

$$a - b = \frac{1}{Q} \tag{4.31}$$

$$ab = 1 \tag{4.32}$$

$$Q = \frac{1}{a-b} = \frac{a}{a^2 - 1} \tag{4.33}$$

$$A = aQ = \frac{a^2}{a^2 - 1} \tag{4.34}$$

Rearranging the terms the following relationship is obtained between A and Q.

$$A = \frac{1 + \sqrt{4Q^2 + 1}}{2} \tag{4.35}$$

Clearly, for high Q values, the passband gain A is approximately equal to Q, whereas A approaches unity as Q goes to zero.

The transfer function given in Eq. 4.30 can also be obtained by combining a damped differentiator and a first order high-pass section of $s/(s-b)$ in a similar manner.

Chapter 5

EXPERIMENTAL RESULTS

Measurement of the filter characteristics in high-frequency range requires special precautions. The proposed filter topology is current-mode whereas all measurement devices operate in voltage-mode. Therefore, a test circuit should be designed in order to obtain the transfer function of the circuit accurately. Figure 5.1 shows the experimental setup.

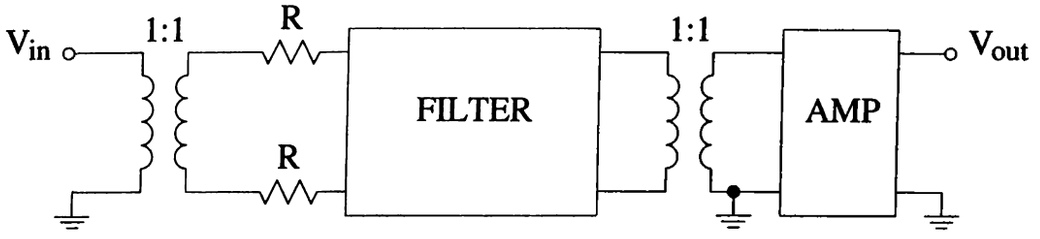

Figure 5.1: Test circuit.

Since each filter block has differential input current, a transformer is connected to the input stage in order to convert single-ended input to differential one. At the output stage, another transformer converts the differential output current to single-ended. Input impedance of the network analyzer, which measures V_{out} voltage, is equal to 50Ω. Without an amplifier at the output of the filter, the pass-band voltage gain (V_{out}/V_{in}) is measured as $-46dB$, as the input impedance of the filter is approximately $10k\Omega$. For this case, it is impossible to measure the filter characteristics correctly because of the noise

level of network analyzer and capacitive coupling through the circuit board, which severely deteriorates the transfer function. Therefore, an RF amplifier is necessary to compensate the loss caused by 50Ω output load. Magnitude and phase response of the amplifier is given in Figs. 5.2 and 5.3, respectively.

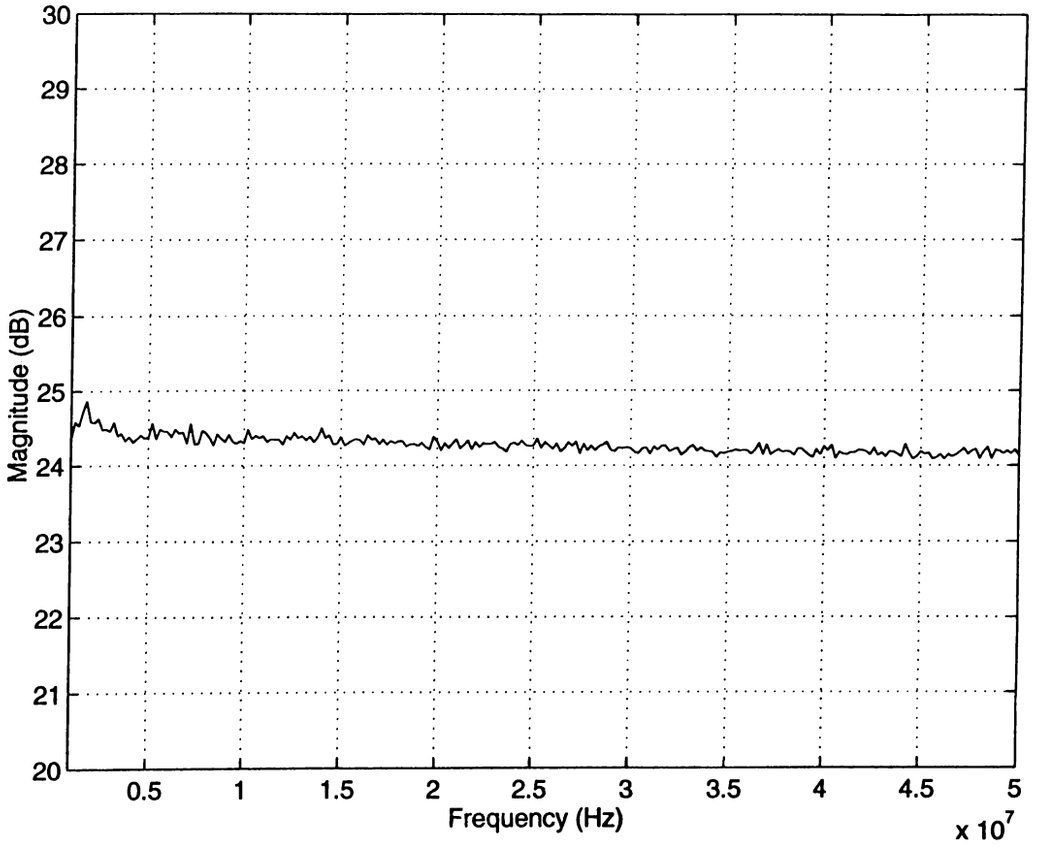

Figure 5.2: Magnitude response of the amplifier.

Using the test setup in Fig. 5.1, two Butterworth filters were tested. The amplifier has approximately $24.5dB$ gain, which is not sufficient to compensate the loss caused by impedance mismatch. Nevertheless, it enables us to obtain the filter characteristics. The band-pass gain is normalized to $0dB$ for magnitude plots. Figure 5.4 and 5.5 shows the magnitude and phase response of seventh order low-pass Butterworth filter with $4MHz$ cutoff frequency, respectively. The magnitude plot shows that the measured cutoff frequency is approximately $5.3MHz$. The shift in corner frequency can also be observed in the phase plot.

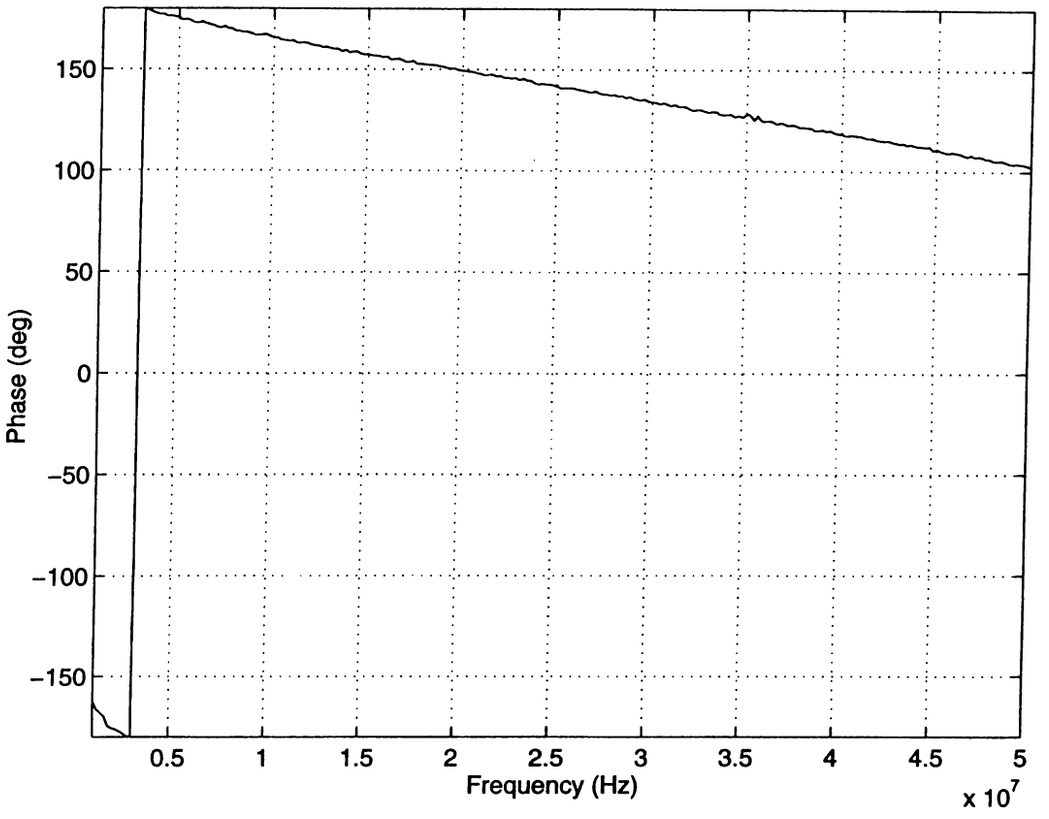

Figure 5.3: Phase response of the amplifier.

The second filter block tested is seventh order low-pass Butterworth filter with $10.7MHz$ cutoff frequency. Magnitude and phase plots are given in Figs. 5.6 and 5.7. Cutoff frequency is measured as approximately $12MHz$. The shift in filter response is due to fabrication tolerances, as well as parasitic effects caused by experimental setup.

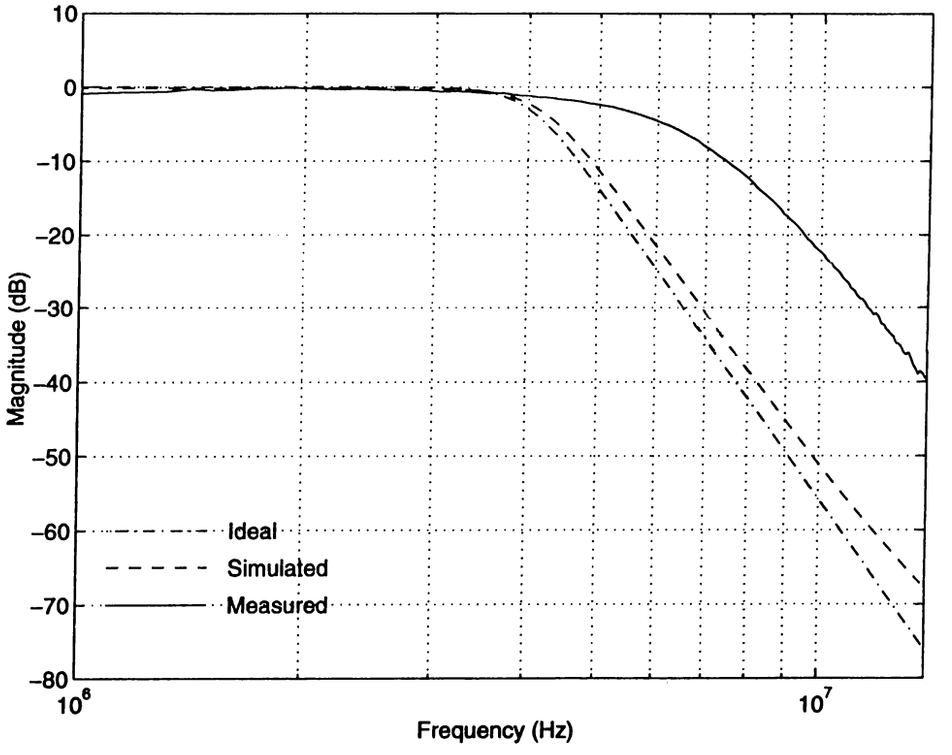

Figure 5.4: Magnitude response of seventh order low-pass Butterworth filter with $4MHz$ cutoff frequency.

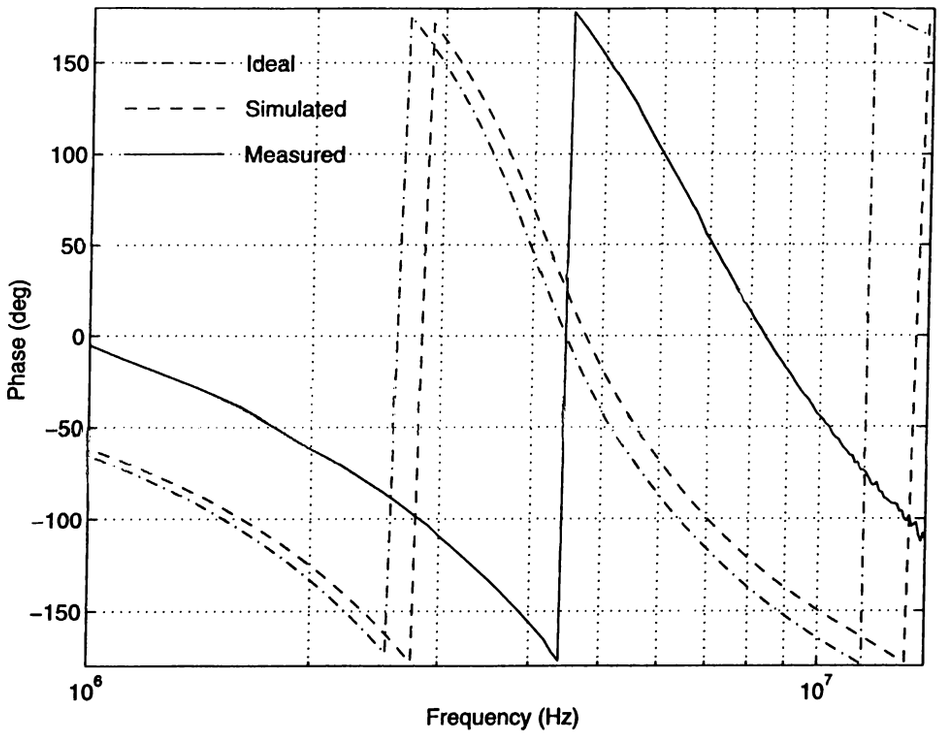

Figure 5.5: Phase response of seventh order low-pass Butterworth filter with $4MHz$ cutoff frequency.

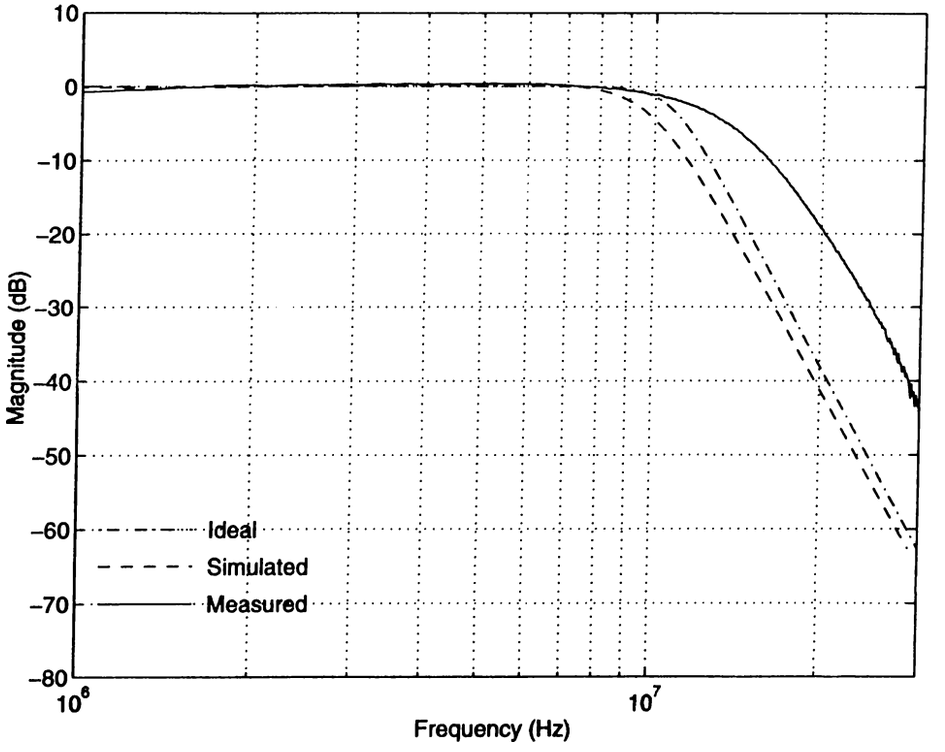

Figure 5.6: Magnitude response of seventh order low-pass Butterworth filter with $10.7MHz$ cutoff frequency.

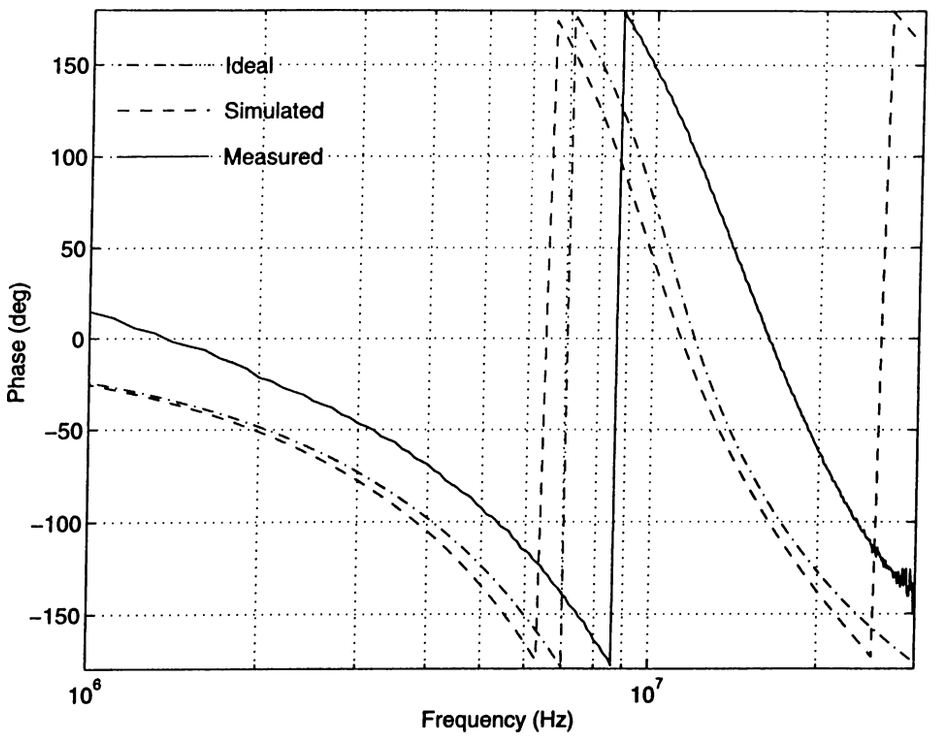

Figure 5.7: Phase response of seventh order low-pass Butterworth filter with $10.7MHz$ cutoff frequency.

Chapter 6

CONCLUSION

A new current-mode differential filter structure is proposed. The filter structure is suitable for low supply voltages and high frequency applications. In order to correct fabrication tolerances and parasitic effects, a tuning mechanism is introduced. By using two control voltages, filters can be tuned down to 50%, and up to 130% of their corner frequencies. Automatic tuning can be implemented using one of the schemes in the literature [6], [13]–[17].

Implementation of low-pass, high-pass and band-pass filters are demonstrated in the thesis. Among them, the most suitable for high frequency applications is low-pass filters, in which parasitics are absorbed in the input capacitance and do not deteriorate the transfer function below gigahertz range. For high-pass filters, the effects of parasitics are more severe, causing parasitic poles within several hundreds of megahertz range. Nevertheless, biquads having high-Q factors can be obtained for both high-pass and low-pass functions. For band-pass filters, moderate-Q biquads are implemented using two methods. In addition, high-Q biquads can be realized using another approach. However, pass-band gain is not equal to unity, and it becomes nearly the same as Q for high-Q values.

As long as HSPICE simulation results are concerned, the proposed topology allows the design of filters beyond $0.5GHz$ frequency. The available frequency

range depends on the technology used. However, at high frequencies, HSPICE analysis may not be valid.

Higher order filters are synthesized by cascading multiples of biquadratic and first order sections. Two test chips including several filter blocks have been designed. The first one includes a current mirror, a first order low-pass block, three Butterworth biquads and two Chebyshev biquads. The first chip has been submitted for fabrication to the MIETEC Alcatel 0.7μ MPW run on December 1994. The second chip contains three of seventh order Butterworth filters and four band-pass biquads with different resonant frequencies and Q-factors. This chip has been submitted to the MIETEC Alcatel 2.0μ MPW run on March 1995.

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APPENDIX A

LAYOUTS

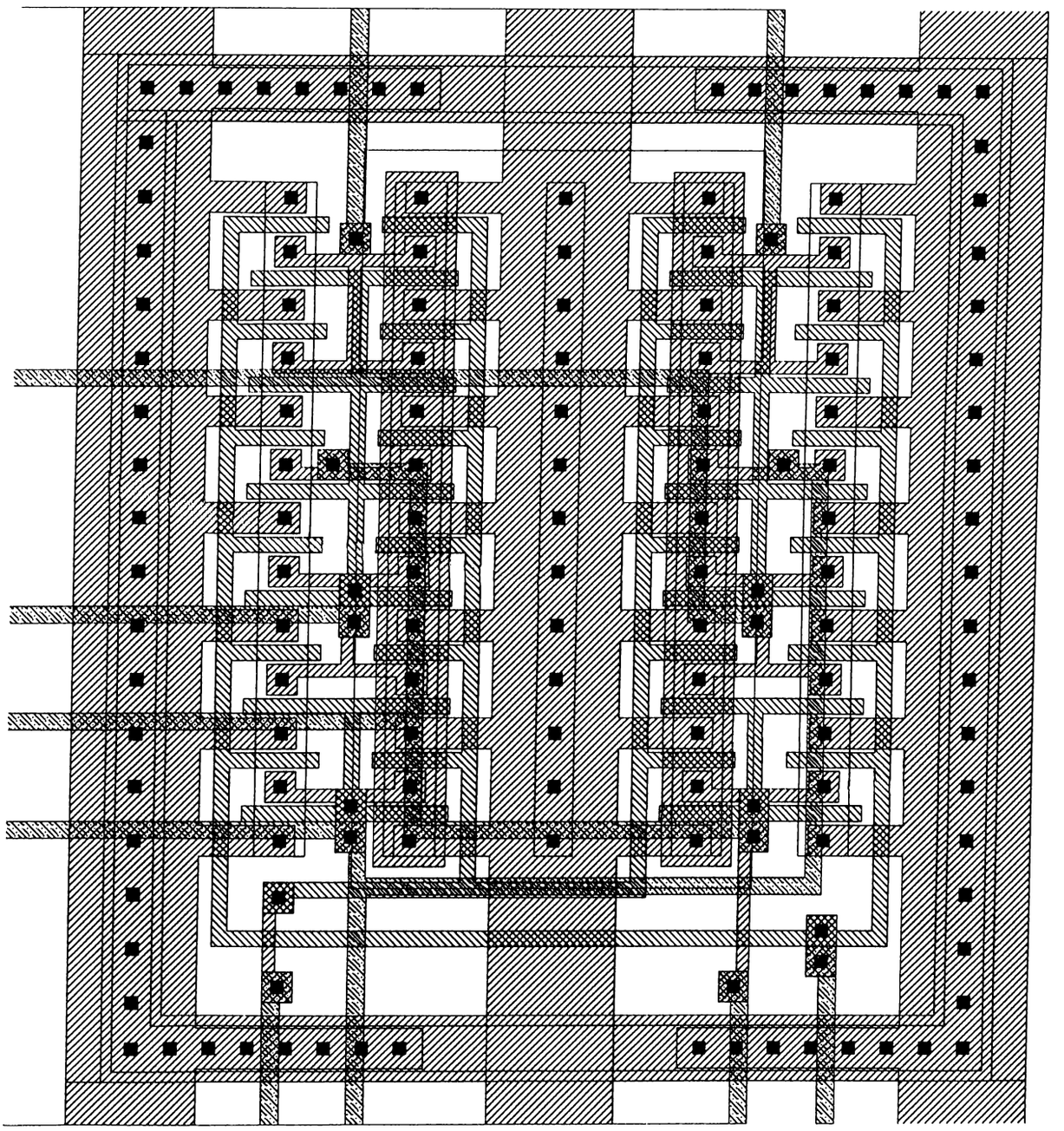

Figure A.1: Layout of the low-pass low-Q biquad (MIETEC 0.7μ).

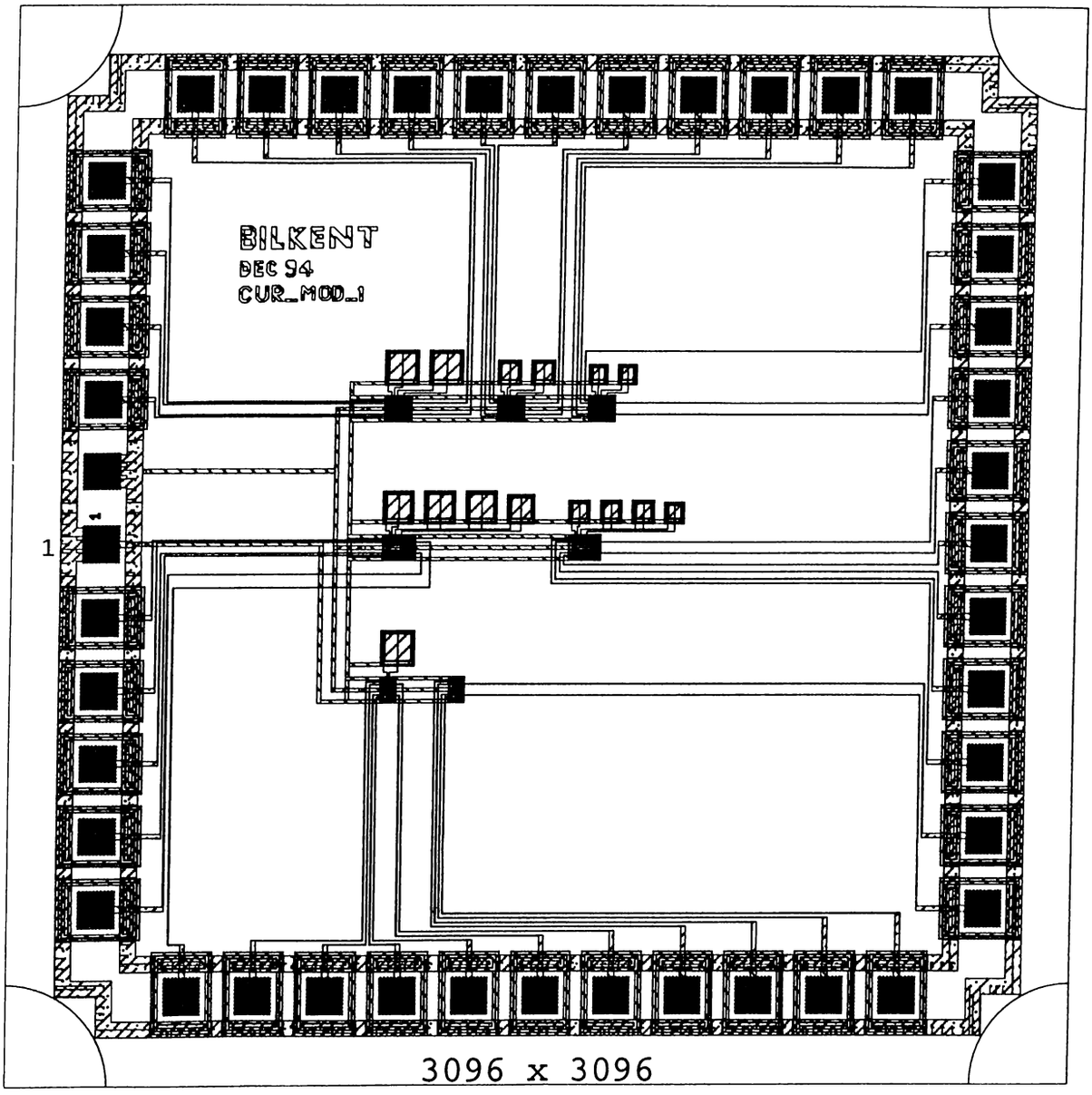

Figure A.2: Layout of the first test chip (MIETEC 0.7μ).

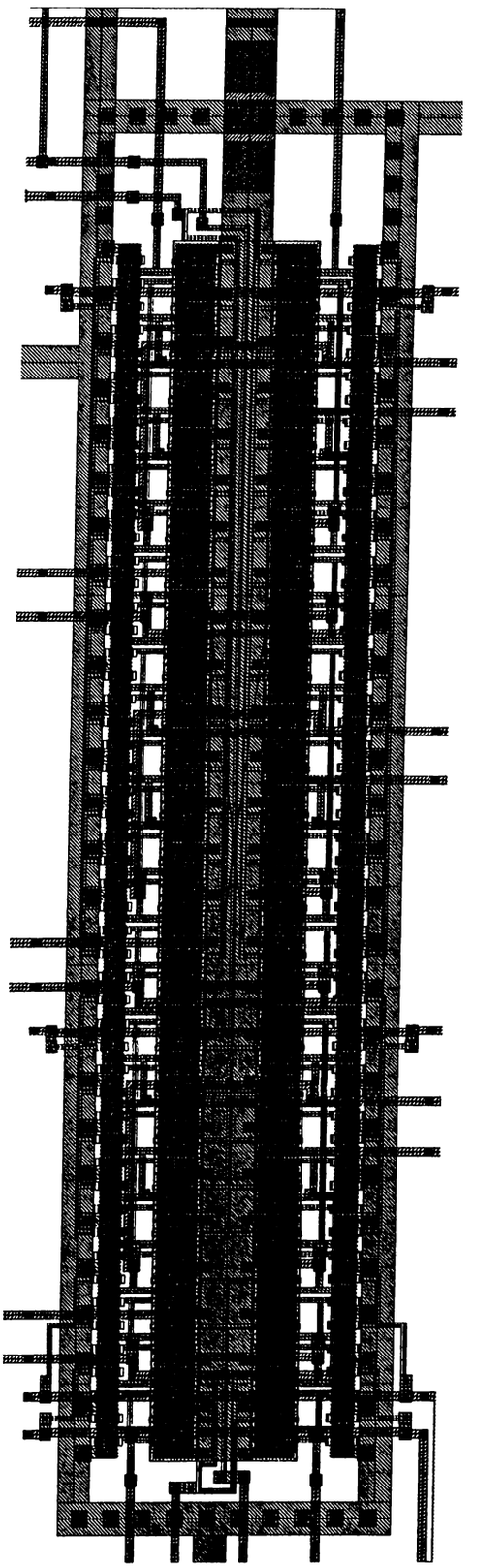

Figure A.3: Layout of 7th order Butterworth low-pass filter (MIETEC 2.0μ).

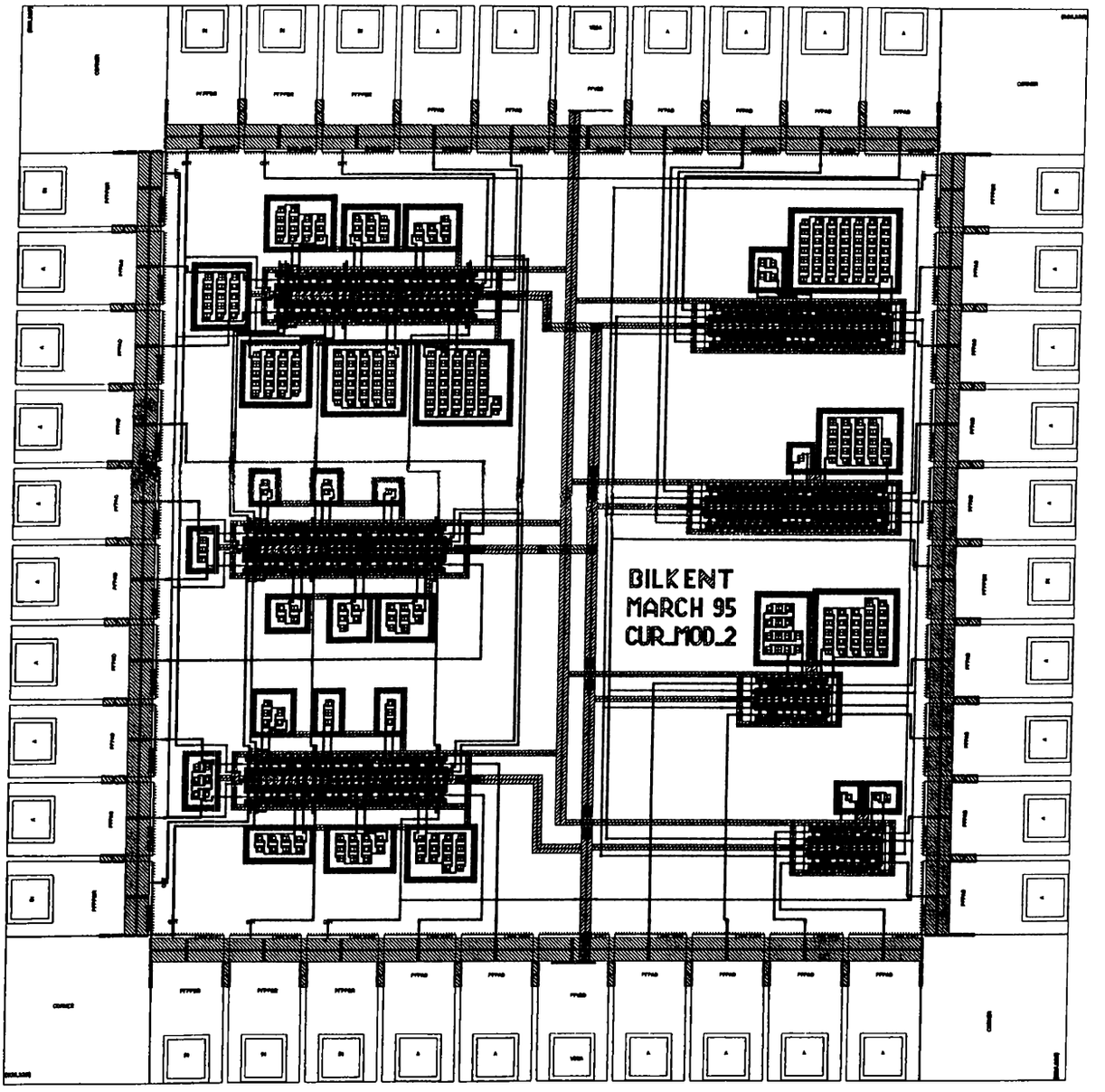

Figure A.4: Layout of the second test chip (MIETEC 2.0μ).