INFLUENCE OF DEPOSITION CONDITIONS ON CHARGE-TRAPPING BASED NONVOLATILE MEMORIES

A THESIS
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FOR THE DEGREE OF
MASTER OF SCIENCE

By
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August, 2014

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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August, 2014

Until recently, memories have been a critical bottleneck for the computer industry. Many research based (revolutionary) devices are in the research arena, however, technical concerns such as integration with the current semiconductor manufacturing processes and the feasibility prevent them from being mainstream. In contrast, charge trapping based memories are the evolutionary improvement to the currently ubiquitous floating gate (FG) based nonvolatile memory. This is predominantly due to their superior scalability and reduced leakage compared to FG based memories.

This work attempts to investigate the influence of the deposition condition on charge trapping based non-volatile memories for two different gate stacks. The first one involves ZnO as the charge trap layer. This single-step grown ALD has the advantage of having low contamination and manufacturing simplicity. The second type of device uses $Ge_2Sb_2Te_5$ as a charge trap memory. The nature of the defect states is different in the two materials, and hence the variation of the trap density with temperature.

Keywords: charge trapping, nonvolatile memories, ZnO, $Ge_2Sb_2Te_5$.

ÖZET

UÇUCU OLMAYAN BELLEKLERDE BÜYÜTME KOŞULLARININ YÜK-TUZAKLAMAYA ETKISI

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Yakın zamana kadar, elektronik bellekler bilgisayar endüstrisinin vazgeçilmez bir öğesini oluşturmaktadır. Bu alanda yapılan çok sayıda akademik çalışma olsa dahi, günümüz yarıiletken teknolojisine entegre edebilme, fabrikasyon ve üretim teknolojileri gibi teknik konular yanı sıra ekonomik fizibilite halen büyük bir engel oluşturmaktadır. Buna karşın, yük-tuzaklamaya dayalı bellekler günümüz teknolojisine yenilikçi bir bakış açısı getirmekte, önemli bir alternatif sunmaktadır. Çünkü ölçeklenebilir olması ve düşük güç tüketimi ile günümüz teknolojisine üstünlük sağladığı düşünülmektedir.

Bu çalışma kapsamında iki farklı yapı için büyütme koşullarının, uçucu olmayan belleklerde yük tuzaklamaya olan etkileri incelenmektedir. İlk yapıda, yük tuzaklama katmanı olarak Çinko Oksit (ZnO) kullanılmıştır. Atomik Katman Kaplama yöntemi ile kapı dieletriği ve yük tuzaklama katmanı tek bir büyütme basamağında yapılmış, bu sayede fabrikasyon kolaylığı sağlanmış ve çevresel kirlilik minimize edilmiştir. İkinci yapıda ise, Germanyum Antimon Telluryum ($Ge_2Sb_2Te_5$) alaşımı yük tuzaklayıcı katman olarak seçilmiştir. İki yapıda kristal kusurlarının sebepleri incelenmiş ve farklı sıcaklıklarla yapılan büyütmelerle kristal kusurlarının yoğunluklarındaki değişimler gözlemlenmiştir.

Anahtar sözcükler: Yük-Tuzaklama, Uçucu Olmayan bellekler, ZnO, $Ge_2Sb_2Te_5$
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Chapter 1

Introduction

1.1 (Semiconductor and) Memory Trends

Over the last few decades, the semiconductor industry has experienced a continuous miniaturization. As portrayed in the now-known-as 'Moore's Law'[6], the density of components on an integrated circuit doubles every 24 months (18 months were proposed originally). While this opened a new era for technology in our lives, it brought along a significant number of challenges. These challenges were not only limited by the fundamental physics underlying them (e.g. quantum effects), but also due to technical and economic concerns surrounding them.

The transistor was invented in 1947 (Bardeen, Britain, Shockley), but the concept of Floating Gate Memory came in 1967 by S.M. Sze [7]. In the years to follow, both underwent aggressive miniaturization, which was thought to be the reins of Moore's law, it soon became evident that something else was needed. Novel materials and structures soon got more attention from the engineers and scientists, and became a bandwagon for the electronic industry (for a good reason given the ever-growing challenges).

1.2 Context and Scope of Research

The research in the field of charge trapping (CT) memory itself is quite diversified. There are groups working on optimizing the charge trap material - its properties, parameters, etc. - and then there are groups working on improving the dielectrics. The former research also includes researchers trying to improve by using multi layers (or to extend the properties and obtain multi-level cells).

This thesis is limited to traditional charge trap memories. Two types of devices have been fabricated; one with ZnO as the charge trap material and the second one employs a chalcogenide - $Ge_2Sb_2Te_5$ - as the charge trap material. The effect of temperature of the ZnO layer in the former, whereas the effect of growth temperature of the dielectric in the latter is studied.

1.3 Organization of the Thesis

Chapter 1 (current) describes the trend of the semiconductor and memory industry. Chapter 2 starts with general memory requirements, the physical principles underlying the memory devices. While the fundamentals remain the same, the key differences between the two families of non-volatile memory - Floating Gate and Charge Trap Memory are presented. The chapter ends with a brief description of some competing technologies.

Chapter 3 mentions the experimental details. The principle of operation behind fabrication equipments as well as the characterization of the devices covers a significant portion of the chapter. Precautions and requirements for the electrical characterization is also presented. Chapter 4 presents the results of the fabrication and a discussion follows. Chapter 5 sums up the thesis by summarizing the gist of the work with an emphasis on the understanding of the physics of the materials involved and concludes by providing an outlook on upcoming memory improvements in the field of charge trap memories.

Chapter 2

Memory: Principles and Literature Review

2.1 Nonvolatile Memory Requirements

The past few decades has seen different memory technologies emerging - SRAM, Flash (NAND and NOR), DRAM just to name a few. Each has its own pros and cons. However, there are a few general features that ought to be consistent across all types of technologies.

- scalability of the technology
- device speed
- integration density
- endurance
- low device variability
- low power consumption and leakage
- low noise margin
- minimal interference

2.2 Floating Gate Memory

2.2.1 Principle

The FG memory is a simple extension of the traditional MOS/MOSFET structure. Its operating principle is very simple - change of the threshold voltage of a transistor.

The floating gate is effectively disconnected from the terminals because it is surrounded by dielectrics which prevent flow of current; hence the term floating. Charge from the substrate tunnels to the floating gate and changes the effective capacitance seen by the substrate and the top gate. The change in the threshold voltage is related to the amount of trapped charge, albeit in a complicated way depending on the distribution of the charge.

2.2.2 Structure

The FG Memory consists of a number of layers.

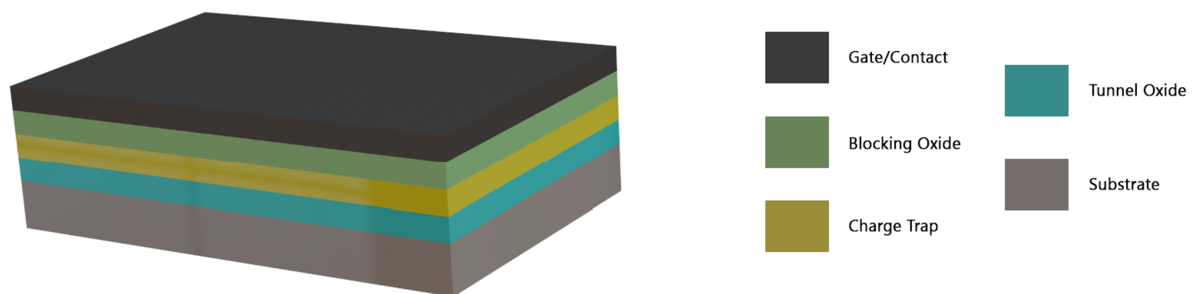

Figure 2.1: A floating gate (MOSCAP) structure

- Blocking Oxide
  - It prevents diffusion of electrons trapped in storage layer to the gate (during retention) as well as hole injection from the gate to storage layer.

    - It prevents electron injection from the gate to the storage layer (during erase). This is known as the back-current.

- Storage Layer
    - It stores charge which leads to an increase in the threshold voltage.

- Tunnel Oxide
    - It acts as the typical dielectric of a MOSFET.
    - It prevents electron from going back to substrate. This is the source of leakage current.

2.2.3 Requirements

The characteristics of each of the layer in a typical FG device are stated below.

- Tunnel Oxide
    - It should have a low trap density in order to reduce leakage.
    - It should be (relatively) thinner for a higher E_{TL} and a higher program/erase speed.

- Storage Layer
    - It should have a high trap[1] density in order to store charge
    - It should have a high dielectric constant. This will reduce the EOT, and hence will have a higher electric field

- Blocking Oxide

[1]There is a trade-off between trap depth and performance:
Shallow traps $\Longleftrightarrow$ Fast erasure $\Longleftrightarrow$ Poor retention
Deep traps $\Longleftrightarrow$ Limited erase performance $\Longleftrightarrow$ Good retention

- It should have very low charge trapping in order to prevent the degradation of the device.
- It needs to have a **high dielectric constant** in order to have a small **E**ffective **O**xide **T**hickness (EOT)

$$E_{tun} = \frac{V_G - V_{FB}}{EOT} \tag{2.1}$$

$$EOT = \left[\frac{k_{SiO_2}}{k_{HK}}\right] t_{HK} \tag{2.2}$$

  A small EOT is needed in order to have a high electric field, which is needed for fast write operation
- A higher conduction band offset to prevent charge diffusion from storage layer to gate. This implies a **high band gap**

However, there seems a major hurdle in this regard, since there is an inverse relation between band gap and dielectric constant [1], and finding a material with both of the properties is not easy.

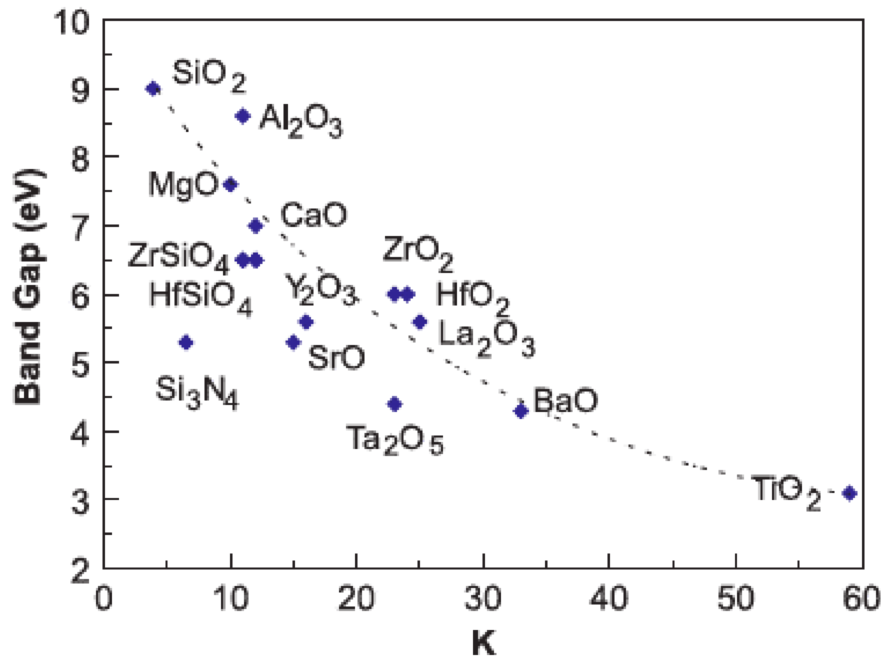

Figure 2.2: Relation between band gap and dielectric constant, from [1]

2.2.4 Tunneling Mechanism

Tunneling refers to the flow of objects through barriers which is classically forbidden. Although the exact solution requires solving the Schrödinger's equation, there are several approximations (e.g. WKB approximation) that can be used to calculate the probability of tunneling.

The physics aside, there are several regimes of tunneling that can influence the probability of tunneling. These regimes are defined based on the applied bias and the resulting electric field and have been modeled and simplified. Fig 2.3 shows these regions. The abbreviations are listed in Table 2.1

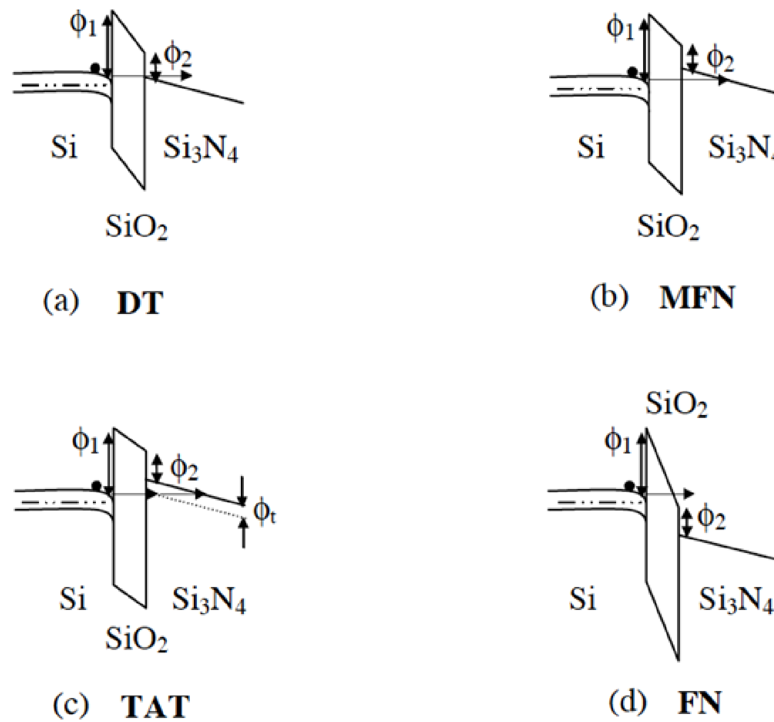

Figure 2.3: Various tunneling regimes

DT	Direct Tunneling
MFN	Modified Fowler-Nordheim Tunneling
TAT	Trap-Assisted Tunneling
FN	Fowler-Nordheim Tunneling

Table 2.1: Abbreviations for Fig 2.3

The tunneling regime affects the reliability of the devices has a direct consequence on other device parameters.

2.2.5 Limitation

One of the main disadvantages of the FG memory is that the FG has a continuous distribution of states. So any defect will lead to the escape of many - if not all - of the stored charges

2.3 Charge Trapping Memory

A charge trapping memory - taking the concept of the FG memory - moves one step further. The floating gate is replaced by a layer which contains a high number of trap density. The underlying physics is essentially the same - change of threshold voltage due to tunneling of charges.

2.3.1 Comparison with the FG Memory

A comparison [8] for FG Memory and CT memories is given in Fig 2.4.

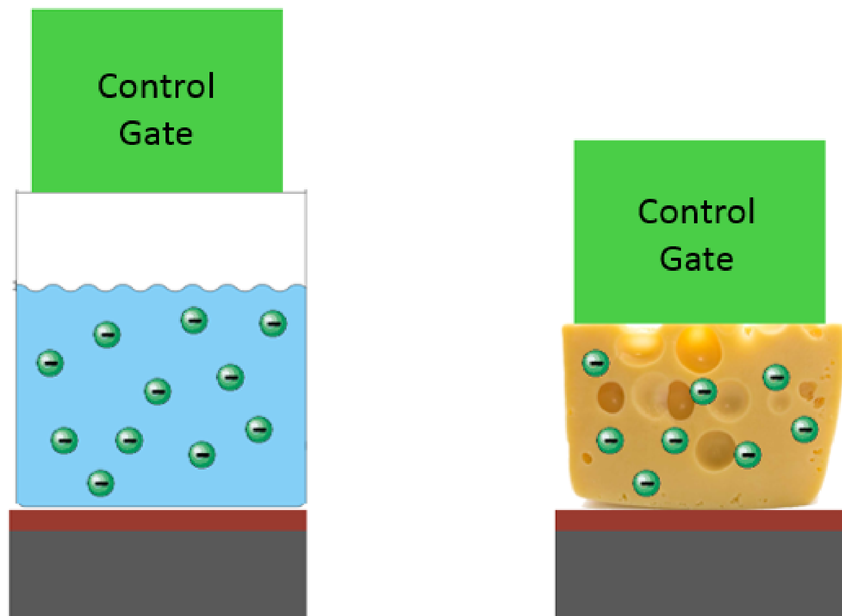

Figure 2.4: Water and cheese analogy for FG and CT memories, respectively

In essence, it highlights the fact that while carriers in a floating gate can move around, in a CT memory, they are not free to move. This means that CT memories are less prone to defects and would not significantly affect the trapped carriers in other neighboring regions.

A slightly technical comparison of the Charge Trap Memory with the Floating Gate Memory is presented below in Table 2.2.

Floating Gate	Charge Trap
Uses a floating gate to store charge.	Uses a charge trapping (CT) layer to store charge
Use Fowler-Nordheim Tunneling for charge injection from substrate	Uses different mechanisms for charge injection (MFN, etc.)
Only uses electrons for device operation can have thicker tunnel oxide, fast erase, better retention etc	Both electrons and holes are used for device operation
Continuous distribution of charges more prone to single defects	Discrete trapped charges immune to defects

Table 2.2: A comparison between FG and CT memories

2.4 Alternate Memories

There are other memory devices under research and development.

- One of these is the **Resistive Memory** [9], in which a change in the physical state in the material leads to a change in resistance. Many materials have been utilized including ZnO [10], TiO_2 [11].

- Another one is the **FeRAM**, or the **Ferrorelectric RAM** [12]. Information is stored in the form of polarization state not as stored charge. Certain crystalline materials polarize spontaneously under the influence of electric field, and remain polarized even after the field has been removed.

  This state change can be used as a memory element. Because current devices use high power to program memory, many people see FeRAM as a strong candidate for ultra-low power memory application. The main challenge associated with FeRAM is its integration with Silicon based technology which lies at the heart of our current semiconductor industry. Some

examples of FeRAM include lead-zirconate-titanate ($Pb[Zr,Ti]O_3$, PZT) [13] with a write time around 100ns and good endurance.

- An **MRAM** [14] uses a magnetic-tunnel junction (MTJ) as the memory element, and a transistor. Each MTJ consists of two ferromagnetic materials separated by a thin insulating layer (that acts as a tunnel barrier). The effective resistance of MTJ changes depending on the alignment of the magnetic moment of the two layers. The magnitude of tunneling current indicates whether a 0 or 1 was stored. Integration with the Si technology is still a key issue.

- A Phase Change Memory, **PCM** [15], uses the phase of a given material to store data. The material - generally a chalcogenide[2] - can exist in either the crystalline or the amorphous phase. While the former has a low resistance and corresponds to a logic 1, the latter typically exhibits resistance three orders of magnitude greater and corresponds to a logic 0. Such materials undergo fast and stable transitions.

[2] a chalcogenide is a compound consisting of at least one element (excluding O) of Group 6A (16) e.g. S, Se, Te

Chapter 3

Experimental Methods: Fabrication and Characterization

This chapter provides an overview of the method of fabrication and electrical characterization of the memory devices. Two types of devices were fabricated. One involves ZnO as the charge trap layer and the other involves $Ge_2Sb_2Te_5$ as a charge trap layer.

3.1 Fabrication

All CT memories were based on the MOSCAP structure. The process essentially uses no lithography steps.

The following steps were carried out in the given sequence.

- Cleaning
- Tunnel Oxide Deposition (ALD)
- Charge Trap Layer Deposition (Sputter/ALD)
- Blocking Oxide Deposition (ALD)
- Gate Deposition (Thermal Evaporator)

A visual summary is presented in Figure 3.1

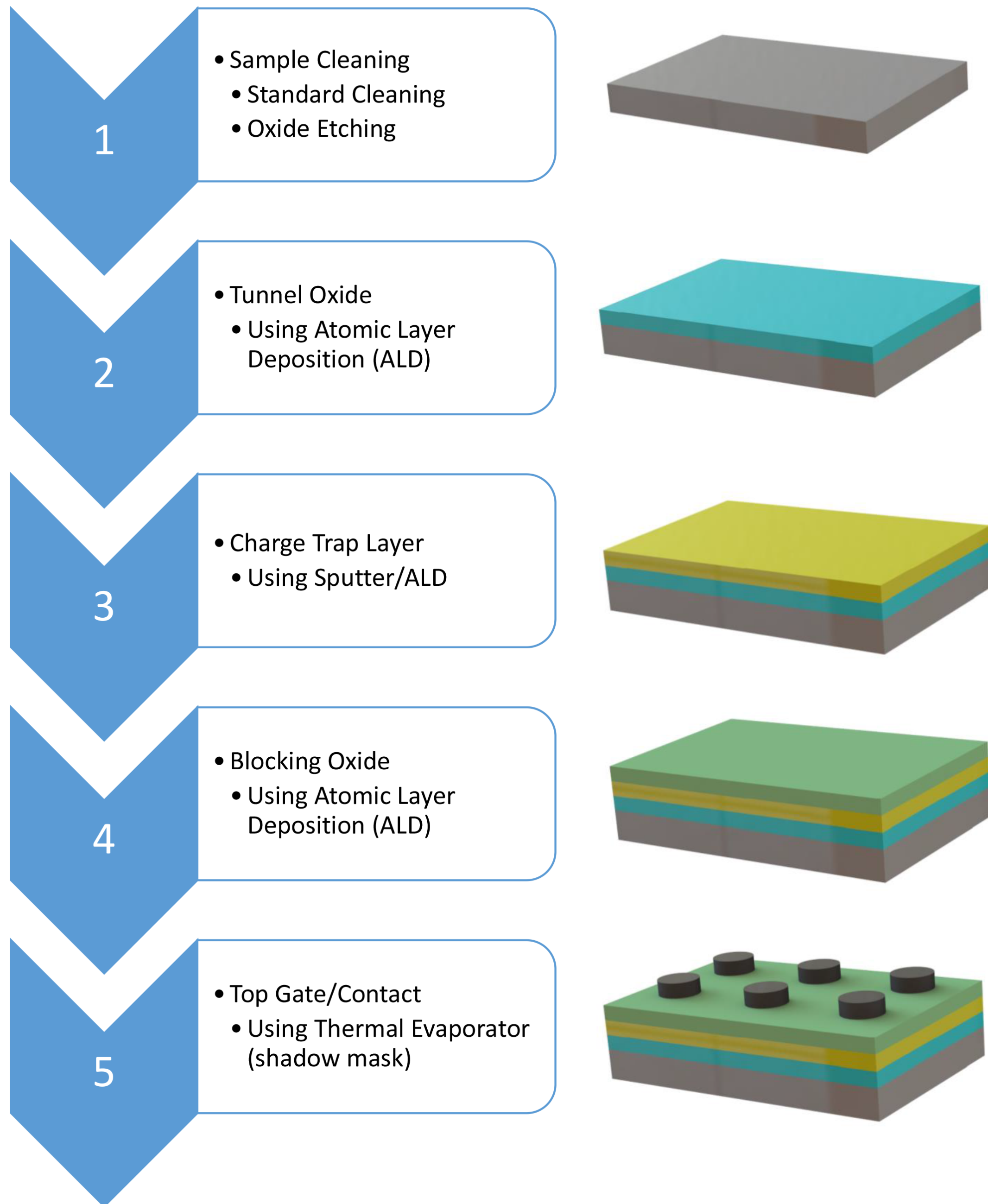

Figure 3.1: Process flow

3.1.1 Cleaning

Highly doped p-type Si substrate[1] was cleaned by sonicating in acetone, isopropanol, and DI water for 15 minutes each sequentially. The acetone removes any organic contaminants. Isopropanol is used because acetone doesn't mix uniformly with water This was followed by a 10-minute immersion in piranha solution (80% H_2SO_4; 20 % H_2O_2) This oxidizes the metallic contaminants. A 1-min dip in BOE (Buffered Oxide Etch) was done in order to remove the native SiO_2 as well as residual (metal) oxides.

3.1.2 Atomic Layer Deposition

Atomic Layer Deposition is a 'Chemical Vapor Deposition' (CVD) technique which uses sequential, self-limiting chemical reactions in order to make layers. CVD involves one or more gases which react to form a film. One of the major ways that ALD differs from conventional CVD is that in the latter, the precursors coexist in space and time [16] whereas in ALD, they are introduced sequentially.

It has many benefits including, but not limited to

- High uniformity
- Smooth surfaces
- Minimum defect and pinholes
- Insensitivity to dust

However, the precursors do have some requirements which need to be fulfilled, for instance

- the precursors must have sufficient volatility
- there must be no thermal decomposition
- precursors shouldn't etch underlying films

[1]Boron doped with resistivity 0.01-0.02 Ωcm and orientation (111)

The process involves two precursors, and two reactions take place.

- Reaction 1: $AX + S_{sub} \rightarrow A{\cdot}S_{sub} + X_{res}$
- Reaction 2: $BY + A{\cdot}S_{sub} \rightarrow BA{\cdot}S_{sub} + Y_{res}$

Here, AX and BY refer to the two precursors, S_{sub} indicates the substrate, and X_{res} and Y_{res} refer to the residual products from the reaction.

A typical ALD cycle is shown in fig 3.2

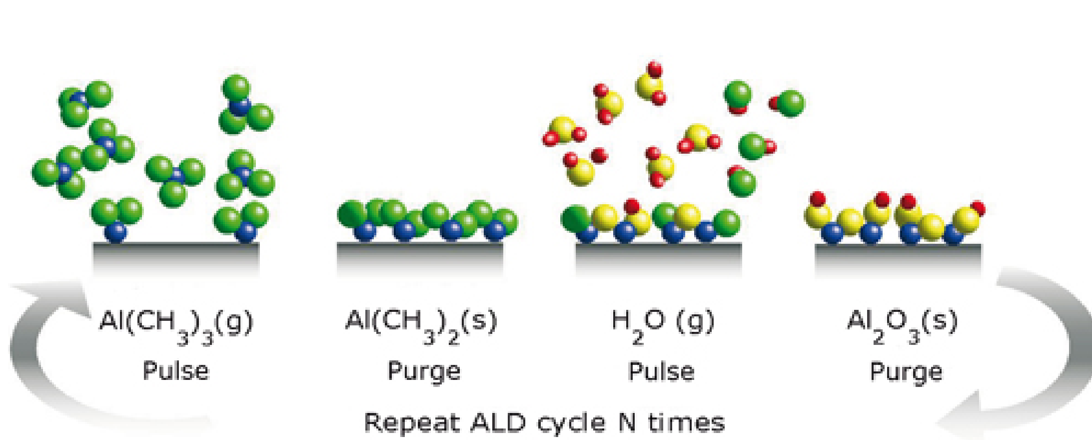

Figure 3.2: Typical ALD cycle, from [2]

The four stages are

- Precursor 1 is introduced to carry out the first reaction
- A purge time is allocated to remove the unused precursor and the residual formed in the first reaction
- Precursor 2 is introduced to carry out the second reaction
- A purge time is allocated to remove the unused precursor and the residual formed in the second reaction

For the deposition of alumina, the two cycles are as follows

- Reaction 1: $OH{\cdot}Si + Al_2(CH_3)_3 \rightarrow AlO(CH_3)_2{\cdot}Si + CH_4$

- Reaction 2: $AlO(CH_3)_2{\cdot}Si + 2H_2O \rightarrow AlO(OH)_2 + 2CH_4$

Atomic Layer Deposition was used for the deposition of the oxides - both the tunnel oxide and the blocking oxide as well as the ZnO charge trap layer. The equipment used was Savannah S100 ALD reactor from the Cambridge Nanotech Inc.

Table 3.1 mentions the precursors used for the deposition of Al_2O_3 and ZnO

	Precursor 1	Precursor 2
Al_2O_3	Trimethylaluminum ($Al_2(CH_3)_6$)	H_2O
ZnO	Diethylzinc ($(C_2H_5)_2Zn$)	H_2O

Table 3.1: Precursors for ALD of Al_2O_3 and ZnO

The dielectrics were deposited at 200°C. The ZnO CT layer was deposited at three different temperatures; 80°C, 200°C, and 250°C. The results are mentioned in Chapter 4.

The ZnO based stack consists of a 5nm tunnel oxide, a 2nm trap layer, and a 10nm blocking oxide. All steps were done in a single step.

For our devices, using ALD has an additional benefit that it minimizes the contamination during fabrication since the tunnel oxide, charge trap layer, and the blocking oxide all are deposited in a single step.

3.1.3 Thermal Evaporation

The thermal evaporation method is part of a deposition technique called 'PVD' and is used to deposit material by evaporating it to the substrate. This involves

passing high currents through a metallic strip known as a 'boat' in which pellets of the material to be deposited are placed. The boat must be able to withstand high amounts of current and is thus made of elements such as tungsten (W) or Molybdenum (Mo).

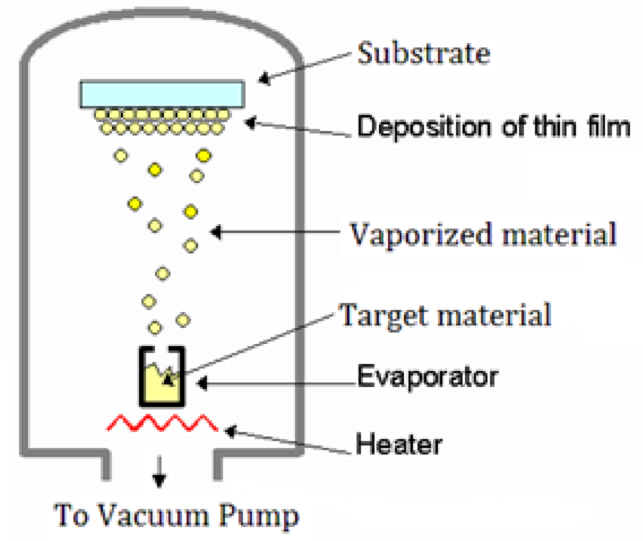

Figure 3.3: A thermal evaporation process[3]

The Al top contact was deposited using thermal evaporation. The instrument used was a Vaksis 'PVD Vapor 3S Thermal'. All depositions were done at a base pressure of $5 * 10^{-6}$ Pa. The metal contact was 100nm thick.

3.1.4 Sputter

Sputtering is another PVD technique used to deposit films. Unlike thermal evaporator where the source has to be heated, in sputtering the source is bombarded by energetic particles - Ar+ ions - and the desired material is physically ejected from the source. The plasma directs those particles towards the source.

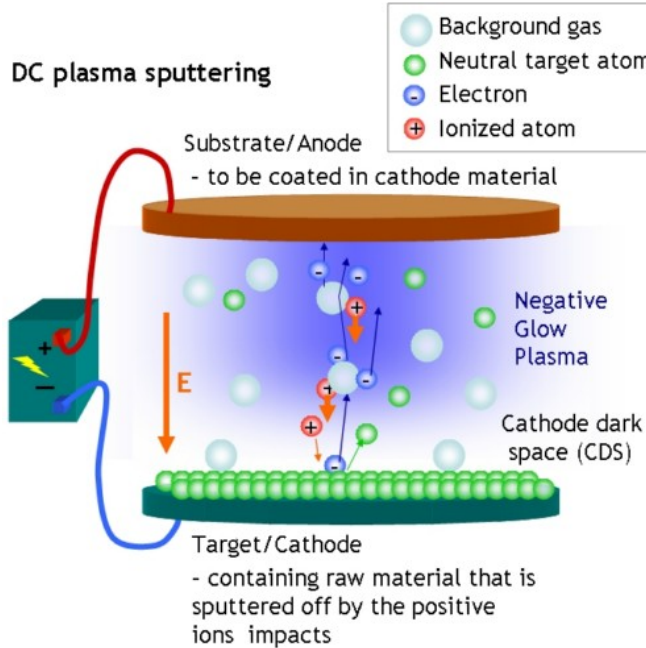

Figure 3.4: A typical sputtering process[4]

Sputtering was used to deposit the GST225 CT layer. The depositions were done at a base pressure of $5 * 10^{-6}$ Pa

3.2 Electrical Characterization

In order to investigate the effect of trapped charges on the threshold voltage, quasi-static capacitance-voltage measurements (CV) measurements were conducted using Keithley 4200-SCS.

The bottom substrate (Si) acted as the bulk as well as the bottom contact. In order to reduce the resistance, the back was scratched with a diamond scriber prior to the measurements.

A small AC signal (20mV) was superimposed on the sweeping DC bias. All measurements were high capacitance measurements done at 1 MHz. Different DC sweep ranges were used in order to investigate the effect on the hysteresis

behavior of the memory cells.

Accurate measurements require three adjustments

- Open compensation
- Short compensation
- Cable compensation

For low capacitances, the open compensation is more critical since smaller capacitances correspond to large impedances. For larger capacitances, the short compensation is more important. In either case, the cable compensation remains an important adjustment to be made.

Frequencies greater than 1Mhz are more sensitive to errors due to phase shifts as the signal propagates through the cables. This needs to be taken care of since phase shifts is the quantity that is being measured to determine the capacitance.

The measurement involves applying an initial bias (presoak value) for a given time (hold time). This is followed by a set of measurement and delay intervals (sweep delay). The values of these can be crucial parameters.

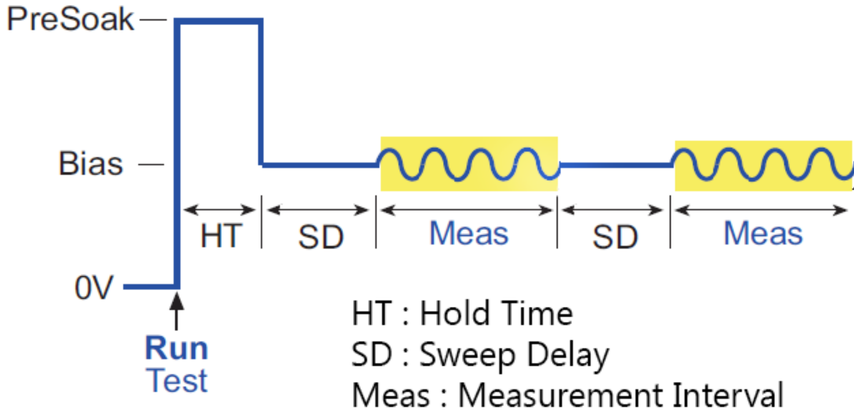

Figure 3.5: Hold delay and sweep times

When starting the sweep test, the MOSCAP can be initialized in any one of the two states; accumulation or depletion. Starting with the accumulation region

may lead to a more noisier measurement and often results in deep depletion while moving to the deletion region.

By starting in the inversion region, we can use the presoak voltage (which is equal to the initial bias voltage in order to prevent sudden peak while the measurement starts and allow the device to settle) and the hold time in order to allow a sufficient time for the minority carriers to be generated. The hold time should be sufficiently large to allow the device to recover from the deep depletion region to the inversion region. In this way, a smaller sweep delay can be used because these minority carriers recombine relatively quickly, and can reduce the measurement time. Illuminating the substrates to light can also help to reduce the hold time. Note that the hold time only applies to the start of the sweep.

Chapter 4

Results and Discussions

4.1 Results

4.1.1 Effect of Bias Sweep Range on ΔVt for ZnO Based CT Memories

Figures 4.1 to 4.3 show the results for the change in the threshold voltage for different ranges of sweep voltages. All sweeps were symmetric; the maximum applied positive voltage was equal to the minimum applied negative voltage.

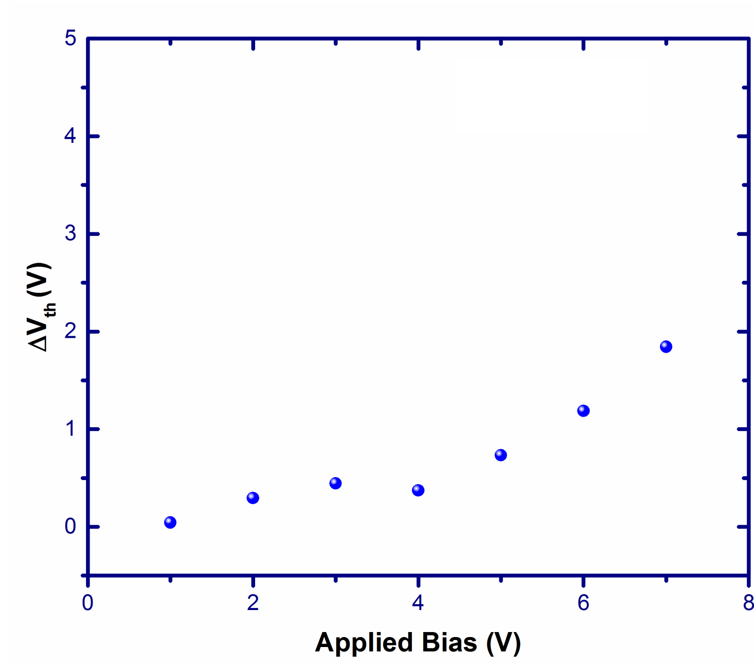

Figure 4.1: ΔV_{FB} for ZnO-based CT memories at 80°C

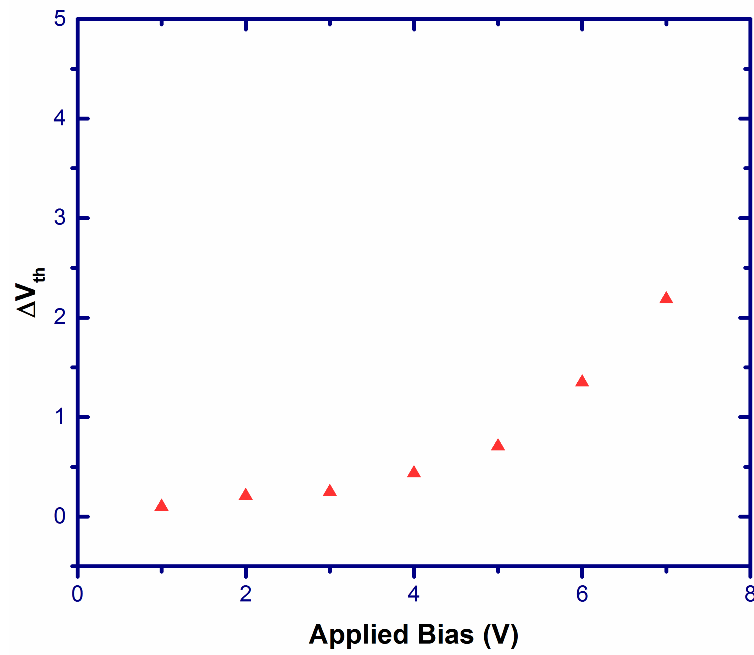

Figure 4.2: ΔV_{FB} for ZnO-based CT memories at 200°C

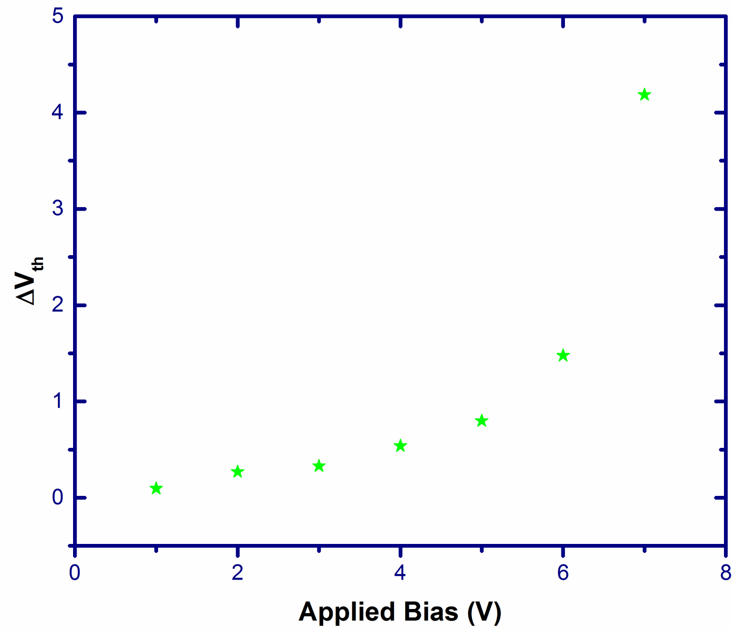

Figure 4.3: ΔV_{FB} for ZnO-based CT memories at 250°C

It can be seen that, with a few exceptions for smaller bias, ZnO deposited at higher temperature leads to a greater shift in the threshold voltage. This implies that at higher growth temperature, the ZnO layer has more stored carriers than those deposited at lower temperature. This explains the larger shift in the bias. Moreover, the change in the threshold bias for consecutive values of applied bias also increases.

4.1.2 Effect of Hold Time on CV curves for ZnO Based CT Memories

For a relatively small bias voltage, CV sweeps were performed[1] for different values of sweep delays. The results are shown in Figures 4.4 to 4.6

[1]with the same hold time

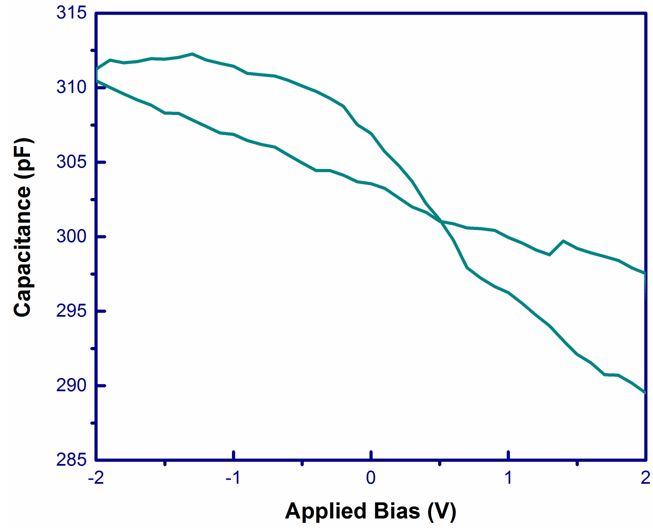

Figure 4.4: CV curve with sweep delay of 1s

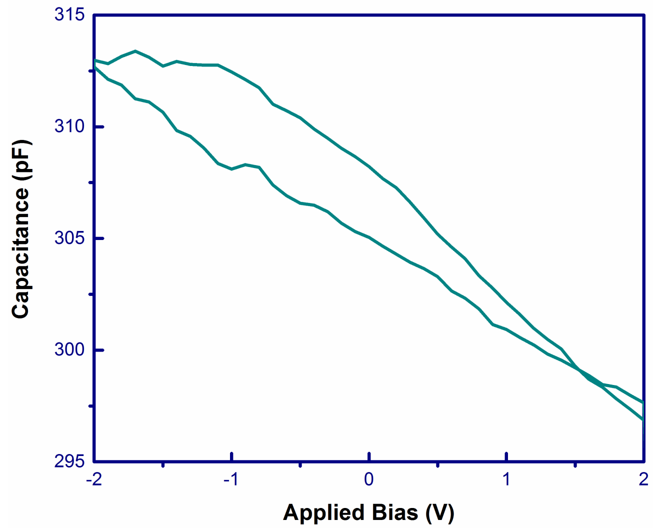

Figure 4.5: CV curve with sweep delay of 0.5s

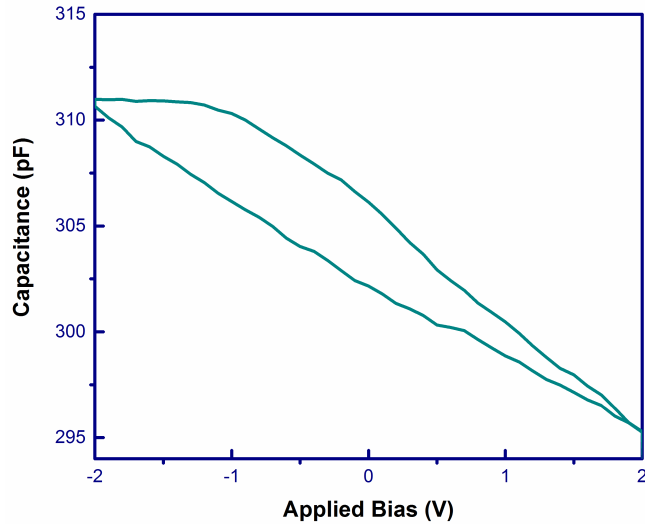

Figure 4.6: CV curve with sweep delay of 0.3s

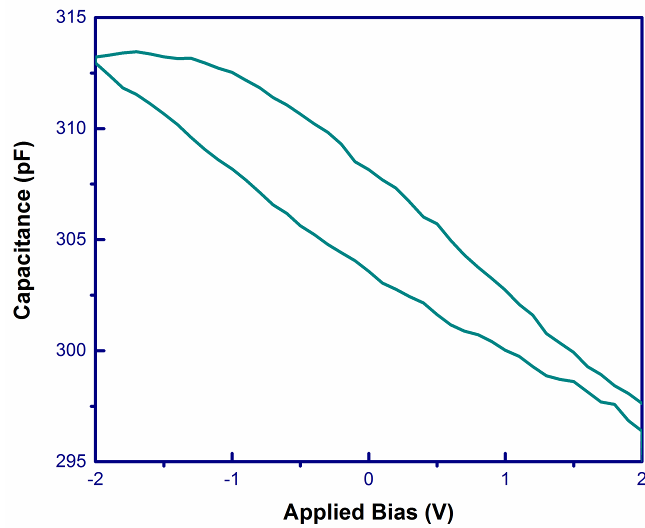

Figure 4.7: CV curve with sweep delay of 0.2s

What it essentially shows is that having the right sweep delay - not small or large is required for a proper CV sweep. Deviating from this range makes the measurements noisier and error-prone. It turns out that the optimal delay is 0.3s, which can be seen from Fig. 4.6.

4.1.3 Effect of Growth Temperature of Tunneling Oxide for GST Based CT Memories

Figures 4.8 and 4.9 show the result for the GST based CT memories whose tunneling oxide is deposited at 150°C and 200°C respectively.

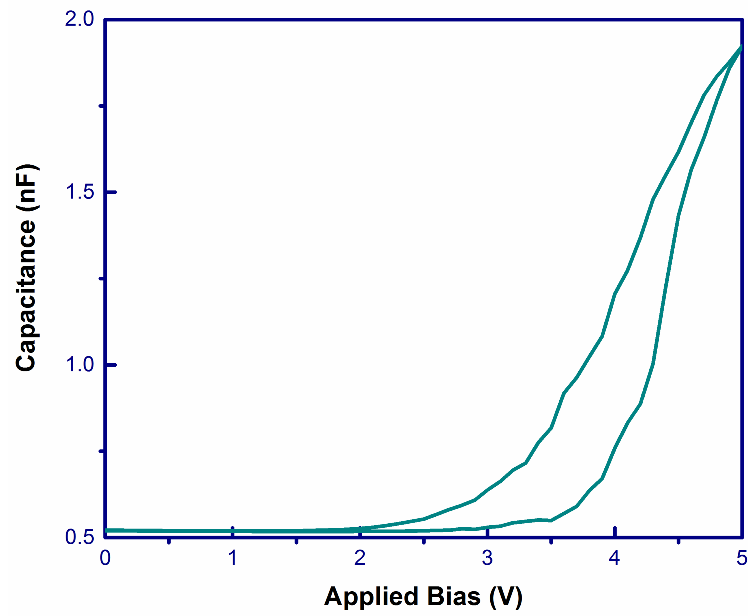

Figure 4.8: GST based CT memories - 150°C

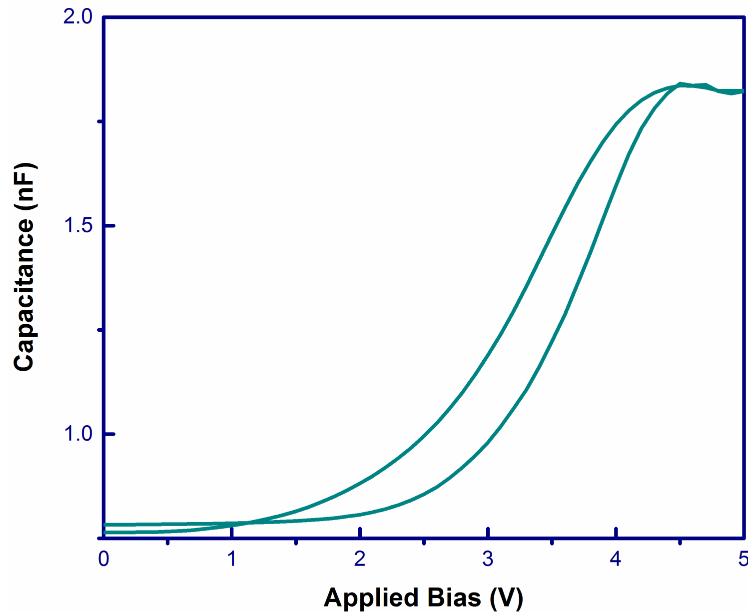

Figure 4.9: GST based CT memories - 200°C

4.2 Discussion

4.2.1 ZnO Based CT Memories

Before attempting to explain the observed behavior, it is important to understand the characteristics of the ZnO layer in the first place. It contains zinc interstitials and oxygen vacancies [17]. These defects lead to charge localization and can act as electron traps. The same defects also contribute to conductivity[2] and have been used not only in thin-film transistors [19], but also in phototransistors (PTFTs) [20].

In [19] and [21], it has been shown that ZnO films deposited at high temperature has a greater conductivity. Given the fact that the conductivity arises due to the natural 'doping' caused by the vacancies, it was expected - and demonstrated - that increasing the growth temperature increases the trap density.

[2]ZnO behaves as an n-type conductor; such conductivity is knows as residual conductivity [18]

For the bias range of (-7,7)V, the total trapped charges can be estimated using the capacitive coupling model.

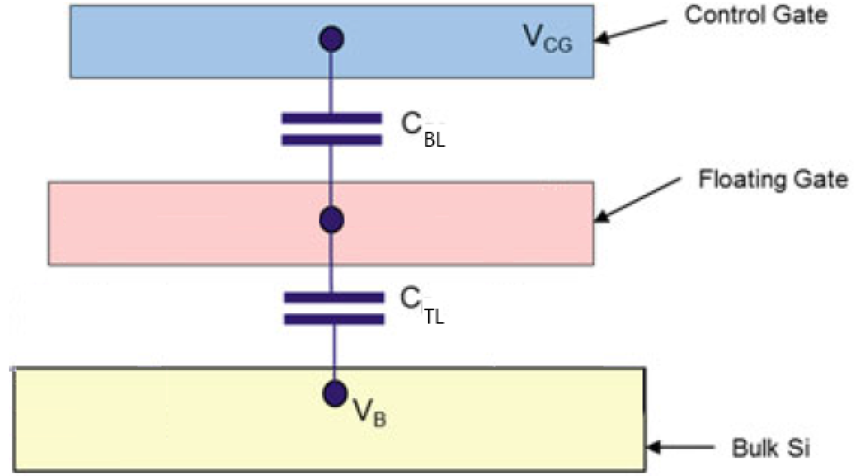

Figure 4.10: A capacitive coupling model for MOSCAP CT memory

Using this model, one can use the formulae [16]

$$C_G = \frac{C_{bl} * C_{tl}}{C_{bl} + C_{tl}} \tag{4.1}$$

and

$$\Delta V_T = \frac{Q_t}{C_{tl}} \tag{4.2}$$

whereas

$$C_{tl} = \frac{\epsilon_r \epsilon_0}{t_{tl}} \tag{4.3}$$

Here, $\epsilon_r = 9.5$ (for Alumina) and t_{tl} is 5nm.

Plugging in the numbers, we get the following value for the trapped charged density

Deposition Temperature (°C)	ΔV_t (V)	Trapped Charge Density(* 10^{17} cm^{-2})
80	1.844	1.9379
200	2.1842	2.2955
250	4.1856	4.3988

Table 4.1: Trapped charge density for ZnO based CT using capacitive coupling model

The results in Table 4.1 can be seen graphically in Fig. 4.11 and 4.12

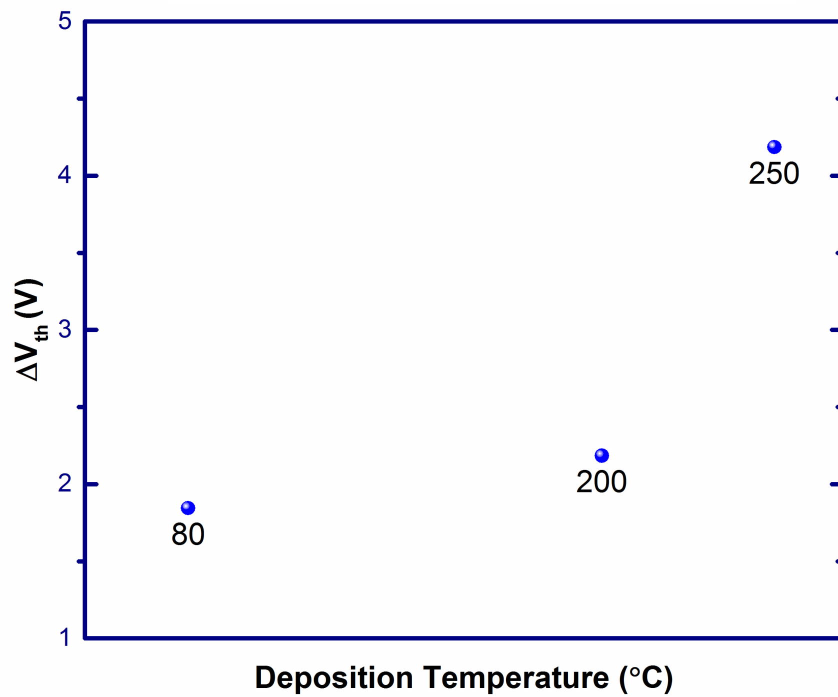

Figure 4.11: Variation of threshold voltage shift for ZnO based CT memory

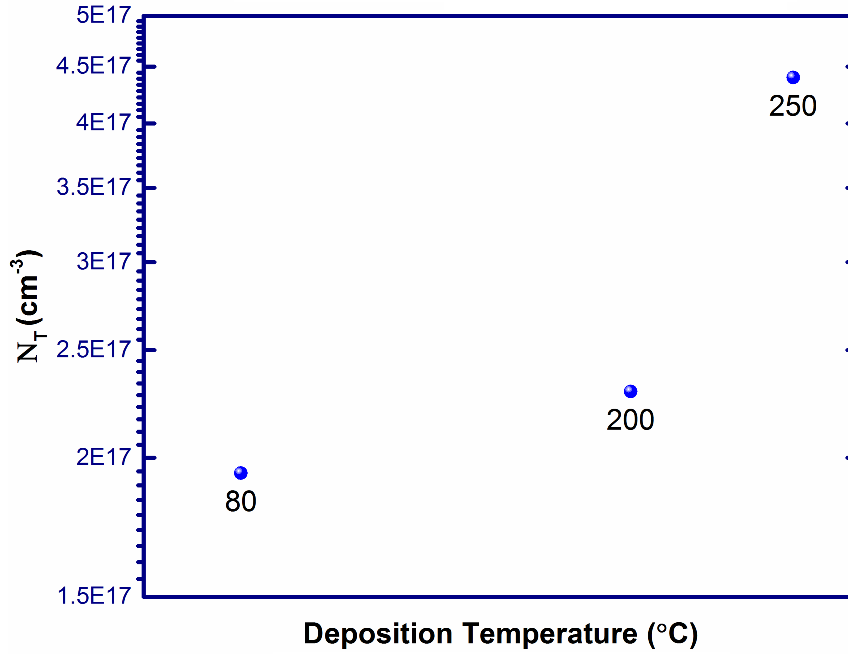

Figure 4.12: Variation of trapped charge density for ZnO based CT memory

4.2.2 GST Based CT Memories

Using the same capacitive coupling model, we can extract the trapped charge density for GST based CT memories.

Deposition Temperature (°C)	ΔV_t (V)	Trapped Charge Density(* 10^{16} cm^{-2})
150	0.5940	2.0809
200	0.4084	1.4307

Table 4.2: Trapped charge density for $Ge_2Sb_2Te_5$ based CT using capacitive coupling model

The results in Table 4.2 can be seen graphically in Fig. 4.13 and 4.14

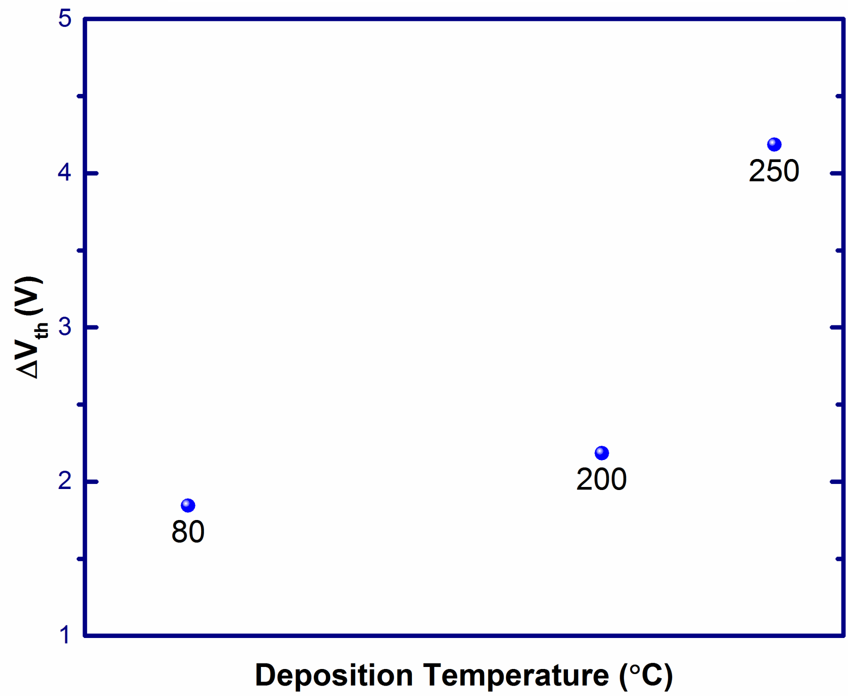

Figure 4.13: Variation of threshold voltage shift for GST based CT memory

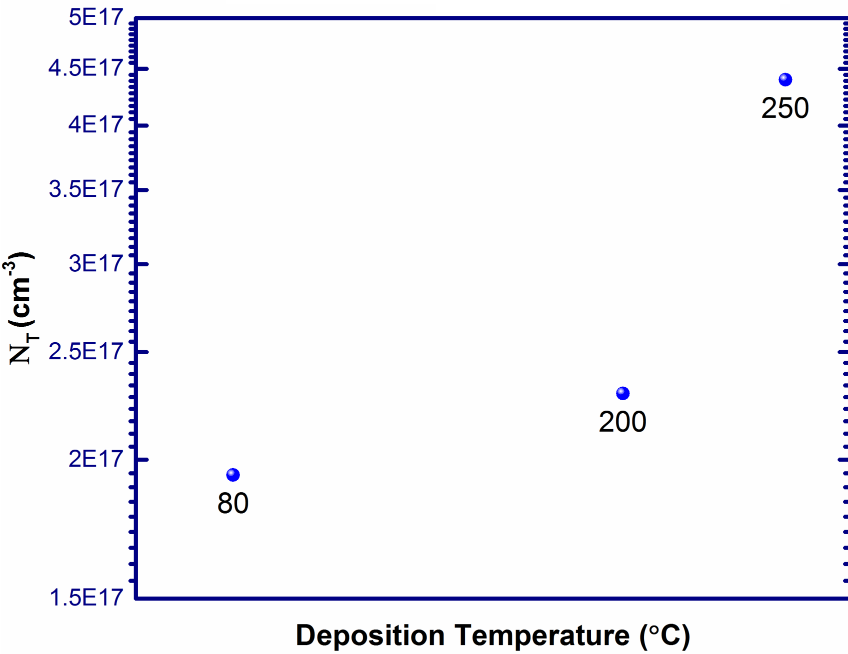

Figure 4.14: Variation of trapped charge density for GST based CT memory

It shows that as the temperature at which the tunneling oxide is deposited is lowered, the trapped charge density increases. The reason can be traced to the nature of the CT layer. GST essentially is an amorphous material which lacks a long-range order. It has many states inside the forbidden energy gap, which gives rise to localized states. These defects can act as donor or acceptor [22]. However, above a certain temperature, GST rapidly crystallizes and these defect states are reduced. However, even below this crystallization temperature, GST crystallizes slowly and this feature is evident in our observation that at a higher temperature (200°C), the threshold shift is lesser than that observed at the lower temperature (150°C).

Chapter 5

Conclusion And Outlook

5.1 Conclusion

ZnO based CT memories were fabricated at different growth temperatures. Varying the temperature changes the effective number of trap states due to zinc interstitials and oxygen vacancies present in the ZnO layer. This change is exploited to 'write' data by changing the threshold voltage of the CV structure. Increasing the temperature increases the number of states and hence the change in the threshold voltage is higher. This means that more charges are stored and could provide better retention (which is a parameter of the stored charges).

The story is different for the GST based CT memories. Increasing the deposition temperature of the blocking oxide affects the underlying CT layer and crystallizes it slightly more, leading to a lower threshold shift.

5.2 Outlook

Despite all the advancements and their pervasiveness, Flash and CT memories still face a major hurdle - the long programming/erasing time. Still a significant

number of challenges remain. Researchers are addressing such issues by proposing even more changes to the structure in order to improve the characteristics. Their physics remains in research and is still being studied.

One of these changes is the use of nanocrystals. It has been shown by many, including [23], [24], that nanocrystals can provide a good memory window. One of the key issues with nanocrystals is their relatively smaller gate-control-ratio. This means that the retention might not be as good as expected. Another issue is the uniformity while 'depositing' the nanocrystals. Current methods use spin-coating or drop-casting which leads to a non-uniform distribution of particles over the surface and can lead to device variability. The precise control of the volume of these nanoparticles itself is a concern, which can affect the trapping behavior. The exact underlining principle of such devices is still under debate. At the nanoscale, there are several other factors contributing to the device performance. Of these, Coulomb blockade is one. Another observed behavior is the strong electrostatic coupling with neighboring dielectric. These issues make it harder to model device behavior and to predict the characteristics.

3D Flash Memory [25] is another topic. A significant number of challenges exist regarding the fabrication of such devices. Cooling such devices is an issue, and researchers are engineering a way around.

In order to overcome the shortcoming due to the bandgap-dielectric relation, band engineering [26] is being utilized. This involves replacing the dielectric(s) - the tunneling oxide, or the blocking oxide - with a pair (or more) layers such that one of them has a higher dielectric constant in order to increase the effective field whereas the other layer has a larger band gap in order to prevent unnecessary flow of electrons

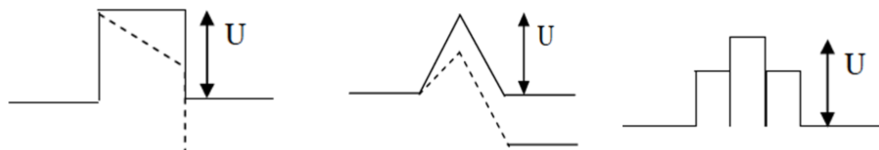

Figure 5.1: Layered barrier approach for CT memories, from [5]

For such layered barriers, the electric field across the effective barrier will have a stronger influence on the lowering of the barrier, thus making tunneling more effective.

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