View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Bilkent University Institutional Repository

GRAPHENE BASED HIGH FREQUENCY ELECTRONICS

A DISSERTATION SUBMITTED TO

THE DEPARTMENT OF PHYSICS

AND THE INSTITUTE OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Erçağ Pinçe

August, 2010

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Asst.Prof. Dr. Coşkun Kocabaş

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Prof. Dr. Atilla Aydınlı

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Prof. Dr. Recai Ellialtıoğlu

Approved for the Institute of Engineering and Science:

____

Prof. Dr. Levent Onural

Director of the Institute

ABSTRACT

GRAPHENE BASED HIGH FREQUENCY ELECTRONICS

Erçağ Pinçe

MSc. in Physics

Supervisor: Asst.Prof. Dr. Coşkun Kocabaş

August, 2010

Recent advances in chemical vapor deposition of graphene on large area substrates stimulate a significant research effort in order to search for new applications of graphene in the field of unusual electronics such as macroelectronics. The primary aim of this work is to use single layer of graphene for applications of high frequency electronics. This thesis consists of both theoretical and experimental studies of graphene transistors for the use of radio frequency electronics. We have grown graphene layer using chemical vapor deposition technique on large area copper substrates. The grown graphene layers are then transferred onto dielectric substrates for the fabrication of graphene transistors. The theoretical part of the thesis is focused on the understanding the performance limits of the graphene transistor for high frequency operation. We investigate the intrinsic high frequency performance of graphene field effect transistors using a self consistent transport model. The self-consistent transport model is based on a nonuniversal diffusive transport that is governed by the charged impurity scattering. The output and transfer characteristics of graphene field effect transistors are characterized as a function of impurity concentration and dielectric constant of the gate insulator. These experimental and theoretical studies shape the basis of our research on the graphene based radio frequency electronics.

Keywords: Graphene, RF, High Frequency Electronics, CVD

ÖZET

Erçağ Pinçe

GRAFEN TABANLI YÜKSEK FREKANS ELEKTRONİĞİ

Fizik Yüksek Lisansı

Tez Yöneticisi: Yard.Doç. Coşkun Kocabaş

Ağustos, 2010

Geniş alanlı alttaşlar üzerine kimyasal buhardan biriktirme tekniği ile elde edilir olması nedeniyle son gelişmeler Grafin'in makroelektronik gibi alışalagelmedik elektronik uygulamalarındaki araştırmaları gözle görülür biçimde hareketlendirdi. Bu çalışmanın öncelikli amacı tek tabakalı Grafin'in yüksek frekans elektroniğinde kullanılmasıdır. Bu tez radio frekans elektroniğinde kullanılacak Grafin transistörlerin kuramsal ve deneysel çalışmasını içermektedir. Geniş alanlı bakır alttaşlar üzerinde kimyasal buhar biriktirme tekniğiyle Grafin tabakası büyütüldü. Daha sonra bu tabakaları, Grafin transistör yapmak üzere dielektrik yüzeylere aktardık. Tezin kuramsal bölümü Grafin transistörün yüksek frekans elektroniğindeki performans limitlerini anlamak üzerine yoğunlaşmıştır. Bu bölümde,"Kendi içerisinde tutarlı" bir taşınım teorisi kullanılarak Grafin tabanlı alan etkili transistörlerin kendine özgü yüksek frekans başarımları incelendi. "Kendi içerisinde tutarlı" taşınım modeli, alttaş yüzeyinde oluşan yük safsızlığı saçılması tarafından belirlenen, evrensel nitelikte olmayan yaygın taşınım modeli ile açıklanır. Grafin tabanlı alan etkili transistörlerin çıkış ve transfer karakteristikleri, giriş yalıtkanının safsızlık konsantrasyonunun ve dielekrik sabitinin bir fonksiyonu olarak karakterize edildi. Yukarıda görülen deneysel ve teorik çalışmalar Grafin tabanlı radyo frekansı elektroniği alanındaki araştırmamızın temelini oluşturmuştur.

Anahtar sözcükler: Grafin,yüksek frekans elektroniği,RF,kimyasal buharı biriktirme

Acknowledgement

First, I would like to express my deepest gratitude to Asst. Prof. Dr. Coşkun Kocabaş. His caring attitude and constructive critics has been always helpful to me throughout my research period. Without him this work would not have existed.

I would present my gratitude to Prof. Dr. Atilla Aydınlı and Prof. Dr. Recai Ellialtıoğlu for their judgments and helpful critics as the Master's Thesis committee.

I would like to thank all Kocabaş research group members and our collaborators Gökçe Küçükayan and Asst. Prof. Dr. Erman Bengü for their help and interest in our research.

I wish to thank Prof. Dr. Ali Ulvi Yılmazer for encouraging me to stay within the borders of science and helped me to simply adore Physics. I am grateful to him for every lesson he gave me.

I would present all my great wishes to Melahat Gediz and Gediz Family for supporting me throughout my entire higher educational career. Also, I would like to thank to my father for the financial support.

I would like to thank my friend Ertuğrul Karademir for heart-to-heart talks and cheerful chats during the entire four semester of hard work. We endured hard times together with Ertuğrul and it has been a privilege for me to have a friend like him by my side.

Also, I want to thank Can Siyako, Serkan Ataç, Itır Çakır, Özge Yurtsevenler Düzdağ and Mahmut Horasan for being supportive and tender during harsh times of my life. It has been a very nice feeling for me to feel somebody watching my back.

I am indebted to my brother Çerağ Pinçe who was the light and the ultimate wisdom of my life whenever I was desperate and exhausted. Without him I might have made countless mistakes and he is the reason that now I am the person I ought to be.

Last but not least, I would like to thank to my "Marla Singer" Işınsu Baylam for her never-ending love. I hope we shape our future together in upcoming years.

This work is dedicated to my mother Belgin Çelebi and my grandmother Yüksel Çelebi.

Contents

1 Introduction ... 1
  1.1. The Prospects of Graphene ... 1
  1.2. Aim and Organization of the Thesis ... 3
2 Electronic Properties of Carbon Allotropes ... 5
  2.1. Diamond ... 5
  2.2. Carbon Nanotube ... 8
  2.3. Graphene ... 11
3 Synthesis of Graphene ... 16
  3.1. Deposition Methods of Graphene ... 16
  3.2. Chemical Vapor Deposition of Graphene ... 22
4 Raman Spectroscopy of Graphene ... 30
  4.1. Raman Scattering ... 30
  4.2. Raman Spectrum of CVD grown single layer graphene ... 35
5 Fabrication of Graphene Based Field Effect Transistor ... 41
  5.1. Field Effect Transistor Fabrication ... 41
  5.2. Performance of DC Field Effect Transistor ... 45
6 Investigation of High Frequency Performance of Graphene Field Effect Transistor ... 48
  6.1. Introduction ... 49
  6.2. A Self-Consistent Transport Model ... 52
  6.3. RF Device Performance ... 56
  6.4. Results and Discussion ... 59
7 Conclusions and Future Work ... 60
8 Bibliography ... 60

List of Figures

Figure 2-1.Tetrahedral diamond lattice structure of Carbon atoms (Designed in software "Balls&Sticks")... 6

Figure 2-2.The honeycomb structure rolled along Chiral vector C_h, T stands for Translation vector of hexagonal lattice. Chiral vector can be expressed as linear combination of primitive lattice vectors. In this figure $C_h= 4a_1+2a_2$. 9

Figure 2-3.Hexagonal shape of honeycomb lattice and its Brilliouin zone lattice. a_1 and a_2 are primitive lattice vectors, b_1 and b_2 are reciprocal lattice vectors. Points K and K' are called Dirac points.. 12

Figure 2-4. Energy band diagram of graphene structure. Dirac points are manifested as where upper(π) and lower energy bands coincide(π*)... 13

Figure 3-1. A schematic of electrostatic exfoliation. Graphene is exfoliated from HOPG surface with an applied bias... 18

Figure 3-2. Schematic of nanowire etching mask technique in fabrication of graphene nanoribbons with various widths. Nanowire alignment takes place in step 2 and patterns the underlying graphene sheet.By step 4, sonication clears up the patterned surface from silicon nanowires. 21

Figure 3-3. Schematic of CVD graphene growth process on copper foil. a) Methane Hydrogen and Argon gases are flowing into the chamber of furnace at ambient pressure b) Chemical decomposition of carbon atoms occur at 1000ºC, methane decompose into carbon and hydrogen gas c) carbon atoms are adsorbed on the catalyst surface and graphene islands start to grow. 24

Figure 3-4. General view of CVD system equipments. a) CVD system consisting of quartz silica tube, Protherm furnace (1), Vacuum Flange (2), Mass Flow Controllers (MFCs)(3). b) Close-up inside of the furnace. c) Close-up MFCs. All photos are courtesy of Emre Ozan Polat. 25

Figure 3-5. (a)As-grown graphene on copper surface, compare with clean copper foil surface. (b) Transferred graphene to Si/SiO_2 surface, color contrast indicates a few-layer graphene flakes. 26

Figure 3-6.The schematic of graphene transfer onto Si/SiO_2. After graphene growth on Cu, PMMA is cured onto the Cu foil and sample is put into 0.05g/mL $Fe(III)Cl_3$ solution. PMMA/Graphene composition is transferred onto Si/SiO_2 surface by applying a mechanical force onto the surface. Finally, PMMA is etched away by acetone and isopropyl alcohol. 27

Figure 3-7. Dewetting process of Cu evaporated on Si/SiO_2 surface. (a)-(b) Surface morphology after 45 mins. of CVD.(c)-(d) after 90 mins. of CVD. Finger-like pattern is becoming less dense with increasing quantity of dewet copper.............. 29

Figure 4-1. Raman scattering processes corresponding to (a) Stokes, (b) Anti-Stokes process.. 31

Figure 4-2. (a)The first order G band Raman process is depicted. Laser induces an electron hole pair and G band phonon is generated. (b) The second order double resonance (second order) G´ band Raman process Excited electron is scattered by in-plane Transverse optic phonon modes. (c)The second order double resonance (second order) D band Raman process. Momentum is conserved in both (a) and (b) type of Raman process whereas momentum is not conserved in process (c). 34

Figure 4-3. The Raman spectrum of (a) Graphene on copper foil, (b) Graphene transferred to Si/SiO_2 surface. 36

Figure 4-4. The Raman spectrum of graphene samples grown by different flow of Methane gas. Higher quality samples are yielded between 15 and 20 sccm flow of CH_4. CVD is carried on at ambient pressure. 37

Figure 4-5. The Raman spectrum shift as a function of growth temperature. As it can seen in the plot, the high quality graphene sheet growth generally occurs around 1000. 38

Figure 4-6. The Raman spectrum shift as a function of growth duration. Red,Blue and Black peaks are for 10 sccm CH_4 flow. Cyan and Orange peaks are for 40 sccm CH_4 flow at 1000°C. CVD is carried on at ambient pressure. 39

Figure 5-1. Real image photos and device schematic of the graphene DC FET. (a) Close-up to graphene based FET, Total area of patterned devices is ~3.75 cm^2. Back gate is implemented by conductive epoxy for measurement purpose (red cable embedded to upper part of device) Microscopic image of a device on the wafer is shown. Graphene layer can be recognized from the contrast between SiO_2 and graphene Device photo is courtesy of Emre Ozan Polat (b) 3D schematic of the graphene device geometry. Courtesy of Ertuğrul Karademir. 43

Figure 5-2. Fabrication process of graphene based FET. Transferred graphene to dielectric surface is patterned by photolithography. The photomask selectively transmits U.V. rays to pattern the DC device geometry. Ti and Au is evaporated onto the patterned graphene surface, then sacrificial photoresist layer is lifted off by acetone. In order to obtain graphene layer only between source and drain pads, an isolation layer is patterned by photolithography. Finally, remaining part of graphene outside the isolation area is etched away by reactive ion etching with O_2 plasma. 44

Figure 5-3. The transfer characteristics of the fabricated graphene based back gated field effect transistor. The transistor has a channel length of 8µm and channel width of 100 µm. The curve is obtained for a drain voltage of 1V. The highly doped silicon substrate is used a global gate electrode. 46

Figure 5-4. The output characteristics of the fabricated graphene based back gated field effect transistor. The transistor has a channel length of 8μm and channel width of 100 μm. The drain voltage sweep is repeated for 11 different gate voltage ranging between -90V to 90V. The highly doped silicon substrate is used a global gate electrode. 47

Figure 6-1. (a) Layout of a graphene based radio frequency transistor with a channel length Lc and channel width W. (b) The calculate the residue charges n^* as a function of charged impurity concentration n_{imp} for two different dielectric material $Hf0_2$ and $Si0_2$. (c) The conductivity of graphene layers as a function of gate voltage. The charged impurity concentration is scanned from $2x10^{11}$ cm^{-2} to $10x10^{11}$ cm^{-2} 51

Figure 6-2. (a) The transfer curves for a graphene FET with a channel length of 1 μm and channel width of 1 μm. The gate dielectric used for the calculation is 50 nm HfO2. A clear ambipolar behavior and current saturation because of contact resistance is seen on the transfer curves. The Dirac point shifts to as a function of drain voltage. (b) The output curves of the same device for the gate voltage range from 0V to 1.2V. The curves in (a) and (b) are calculated for for $n=4x10^{11}$ cm^{-2} . (c) The transfer curves for the device for different charged impurity concentrations at a drain voltage of 0.6 V. (d) Calculated maximum transconductance of the device as a function of charged impurity concentration. 55

Figure 6-3(a) The simplified small signal circuit model for of the graphene FET. Here gm is transconductance ,R_0 is output resistance, R_d is drain resistance and C_{gd} is the intrinsic gate-drain capacitance. (b)The output resistance calculated from the output curves (inset in (b)) for different impurity concentration raging from the cleanest to the dirtiest sample. (c) Two-dimensional map of small signal power gain of the device. The x and y axis represents gate and drain voltages, respectively. (d) Maximum available gain of the device as a function of charged impurity concentration. 57

to my mother and grandmother

Chapter 1

Introduction

1.1. The Prospects of Graphene

Considering the silicon based technology is reaching to its limits, every now and then a new material draw attention of the researchers and emerges to replace silicon's role in semiconductor technology[1]. Many of the candidates are eliminated and silicon is yet the most reliable semiconductor material used in the area. However, as the size of electronic devices gets smaller silicon is reaching to the scalable device limit and in near future it is widely believed that silicon can no longer support the need of high frequency electronics applications in the market. According to Moore's law number of transistors in integrated circuits double in 18 months period. By the silicon based semiconductor devices gets smaller and smaller, It is widely believed that now silicon technology is on the boundaries of fundamental limit and some problems might arise such as gate tunneling in MOSFETs[2]. Therefore, a thorough research is needed to create alternative routes to solid state device technology without any scaling problem.

In 2004, Novoselov et.al discovered a method to deposit Graphene, 2D crystal of carbon atoms arranged in hexagonal shape and observed its peculiar electrical properties[3].

Beside abrupt electrical properties of fabricated Graphene devices, Graphene layer also exhibits unusual transport phenomena[4],[5].

These intrinsic properties make graphene worthwhile for a closer inspection. Graphene is one of a solid candidate amongst the other emerging device materials for the post silicon era. The main reason for this verdict is based on fabricated graphene field effect transistors having potential for immediate applications towards RF device technology[6]'[7], showing high frequency performance[8]'[9] and high mobility, up to 23,000 $cm^2V^{-1}s^{-1}$ [10], compared with conventional CMOS devices. Furthermore, intrinsic carrier mobility values of higher than 200,000 $cm^2V^{-1}s^{-1}$ is predicted for a graphene based device[11]. Although graphene field effect transistors have lower on-off ratio compared to silicon based MOSFET and therefore lower switching capabilities, new generation graphene nanoribbons could yield promising on/off ratios (up to $\sim 10^4$) [12]. Also, new graphene growth techniques, such as chemical vapor deposition of graphene on large area substrates[13],[14] has opened up the opportunity to use RF device circuits on large displays as stretchable and foldable graphene electronics[15].

One of the most important parameter we need to investigate in graphene devices is the cut-off frequency,f_t. The cut-off frequency is the frequency at which current gain of the transistor drops to one. This means, at the cut-off frequency, the frequency response of a system is beginning to decrease. With higher cut-off frequency, the graphene devices become more suitable for use in RF applications.

Nonetheless, graphene is not the only promising carbon based material in semiconductor device technology, it has competitors: CVD Diamond and Carbon Nanotube. Diamond and carbon nanotube both have high mobilities[16], on-off ratios[17], and cut-off frequency

values[18,19,20]. Their physical and electronic properties will be discussed in subsequent chapters.

1.2. Aim and Organization of the Thesis

The aim of this thesis to show the device capability of a fabricated graphene based field effect transistor and analyze the device parameters such as mobility, transconductance, on/off ratio and other characteristics as a function of channel length.

In chapter 1, the introduction to the new graphene based device technology and latest developments in device physics of graphene is given.

Chapter 2 will address the electronic properties of 3 carbon allotropes of graphene, carbon nanotube and diamond. Their band gap structure will be briefly analyzed and the device capabilities will be discussed.

In chapter 3, we will present the synthesis of single layer graphene and its transfer techniques to a dielectric surface. This chapter will mostly concern about the fabrication of uniform and atomic thick single layer grown graphene on a substrate.

In chapter 4, Raman spectroscopy of atomic thick single layer graphene will be analyzed. We briefly discuss about Raman scattering, and the characterization of the quality of epitaxially grown graphene.

Chapter 5 summarizes the fabrication process and the electrical performance of the back-gated field effect transistor. The CVD grown graphene layers on copper foils are transferred on SiO_2 coated Si substrates.

Chapter 6 investigates the intrinsic high frequency performance of graphene field effect transistors using a self consistent transport model. The self-consistent transport model is based on a nonuniversal diffusive transport that is governed by the scattering owing to the presence of the charged impurities on the substrate. The output and transfer characteristics of graphene field effect transistors are characterized as a function of impurity concentration and dielectric constant of the gate insulator. Important high frequency device parameters have been investigated.

Chapter 7 will provide the summary of the thesis and discuss the future directions of our research on the graphene based high frequency electronics.

Chapter 2

Electronic Properties of Carbon Allotropes

2.1. Diamond

Diamond is an Carbon allotrope, standing as a crystal of the diamond lattice structure of tetrahedrally bonded sp^3 hybridized carbon atoms (see Figure 2.1) [21]. Although Natural Diamond is defined as an insulator, synthetic diamond is a wide band-gap semiconductor (E_g= 5.4 eV) and it has promising thermal and electrical properties. Basically, high pressure and high temperature values around respectively 70-80 kbar and 1400-1600 ºC is needed for the formation of natural diamond[22]. The first attempt to synthetically grow diamond was made by Bundy *et al.* in 1955 by applying the High Pressure High Temperature (HPHT) synthesis method[23]. This method is simply based on applying a high pressure on a cylinder container by a piston and raising the temperature inside the container to around 1400 ºC. HPHT synthesis might yield high quality and large area substrate of diamond but recent advances in chemical vapor deposition technique made the diamond growth process much practical and accessible. Using Hydrocarbons as carbon feedstock and surface passivator at temperatures around 2000 K at maximum, chemical reaction occurs in order to grow single or polycrystalline diamond on the substrate concerned. Generally, CH_4

(methane) or C_2H_2 (acetylene)are used as carbon feedstock in the chamber[24]. Also, it is possible to dope the diamond lattice with nitrogen or boron atom through CVD process to make N-type or P-type semiconductor device.

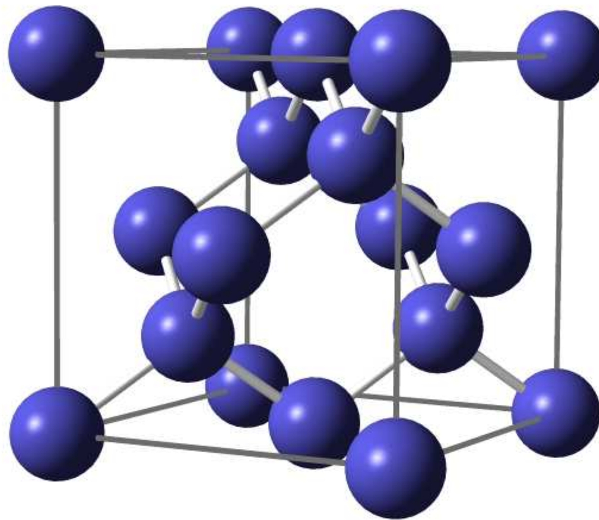


Figure 2-1.Tetrahedral diamond lattice structure of Carbon atoms (Designed in software "Balls&Sticks")

The main focus here is the measure of high end electronics performance for several base materials. Therefore, Diamond is evaluated within the framework of RF electronics. The first single crystal diamond based device in history is fabricated by Isberg *et al.* in 2002[25]. The device showed excellent high carrier mobility, respective hole and electron mobilities up to 3800 cm^2/Vs and 4500 cm^2/Vs. Also the breakdown electrical field and the thermal conductivity of diamond devices are very high values such as 10 MV/cm and 20 W/cm K. These values suggest good applicability of CVD diamond based semiconductor devices to area of high temperature and high power semiconductors among the same class of candidate semiconductor material. One of the most important physical features of diamond is its thermal conductivity. It can largely be used in RF device power management which GaN is mostly leading the area. However, the first GaN-diamond hybrid devices were fabricated in 2007, and there is still research going on in the area of thermal properties of high power devices[26].

The Presence of dangling bonds of carbon atoms on the crystal edge of diamond is a problem and are needed to be passivated from the surface in order to have a good conductance in diamond based field effect transistor. Therefore, Kawarada *et al.* manufactured diamond FET with Hydrogen surface termination[27]. By the deposition of Hydrogen to the surface using CVD, a hole channel is constructed around 10 length nm below the surface and metal contacts are evaporated at the Hydrogen terminated surface. Hence, passivated area acts as if there is a 10 nm length thick dielectric surface above the channel. Without proper Hydrogen surface termination, diamond FET cannot achieve a good RF performance[28]. The best RF performance shown up today is a cut-off frequency f_t of 45 GHz and maximum frequency f_{max} of 120 GHz which is one of the highest

frequency response for a single RF device[20]. This result indicates that diamond field effect transistors are excellent candidates for designing RF power amplifiers.

2.2. Carbon Nanotube

Rolling up the honeycomb structure to a cylinder of carbon atoms makes the 2D planar sheet of carbon into a 3D structure, namely carbon nanotube. The orientation of that graphene sheet is rolling onto itself is important by means of band gap structure of carbon nanotube. A vector is needed to describe the rolling motion of graphene sheet and it is called chiral vector (see Figure 2.2). Depending on the direction of chiral vector, rolling up graphene sheet along chiral vector might yield metallic or semiconductor carbon nanotubes[17,29]. Generally, 1/3 of yielded carbon nanotubes are metallic and 2/3 of them are semiconductors[30]. However, metallic nanotubes aligned in series might short the patterned device and can abruptly decrease device parameters such as the output resistance and the on/off ratio[31], therefore metallic nanotubes should be eliminated in order to have a good device performance. There are many chemical and physical techniques to select and eliminate metallic carbon nanotubes such as applying a breakdown electrical field and high current on the parallel aligned carbon nanotubes[32], chemical etching with gas phase hydrocarbonation reaction[33] and plasma etching by fluorine gas[34].

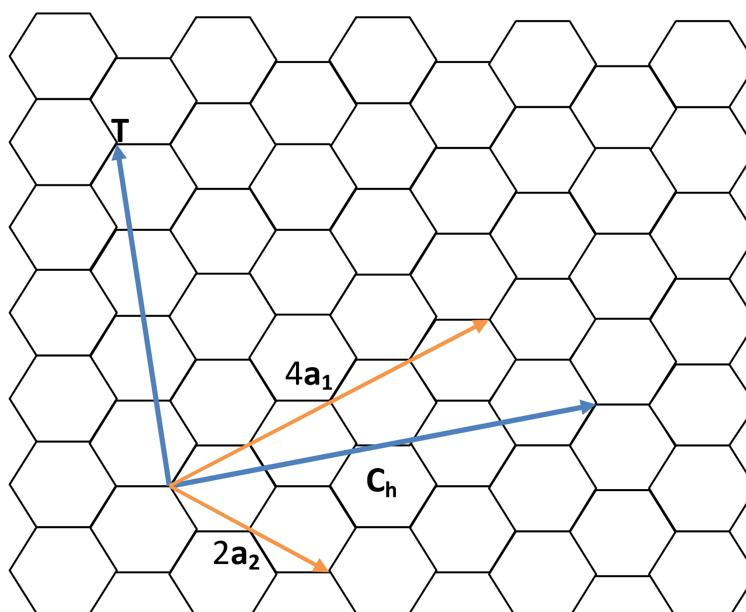


Figure 2-2.The honeycomb structure rolled along Chiral vector C_h, T stands for Translation vector of hexagonal lattice. Chiral vector can be expressed as linear combination of primitive lattice vectors. In this figure $\mathbf{C_h} = 4\mathbf{a_1} + 2\mathbf{a_2}$.

There are various numbers of carbon nanotube growth techniques[35,36], however i*n situ* growth techniques of carbon nanotubes are preferable due to the difficulties in transfer process onto an insulator substrate and the quality obtained. Hence, CVD is one of the most reliable and facile method to grow aligned carbon nanotubes. In CVD process, metal catalyst nanoparticles are placed aligned upon a substrate and various gas of carbon feedstock flows around temperature of 900-1000 ºC. Those Catalyst particles might determine the type and diameter of carbon nanotubes. Nevertheless, aligned dense nanotube array should be obtained in order to sustain a good device quality and electrical

performance. Kocabas *et al.* achieved the growth of surface guided highly aligned and dense single walled carbon nanotubes(SWNT) on quartz substrates[37]. While patterning a carbon nanotube based device with lithography, it is highly important to appropriately place carbon nanotubes right between the source and drain pads and below the gate. Otherwise, carbon nanotubes might touch a nearby device pattern and create a parasitic capacitance due to the fringing field or simply short the device. In order to have high transconductance, cut-off frequency(f_t) and maximum frequency(f_{max}), one needs to implement perfectly aligned and dense carbon nanotubes into the device geometry. Therefore, disordered and misaligned carbon nanotubes weaken the RF device performance and decrease the on/off ratio, and the mobility of carbon nanotube based devices significantly. As an example to highly parallel and dense carbon nanotube arrays, Kocabas et. al achieved to assemble SWNT based RF devices showing very high mobility up to 3000 $cm^2V^{-1}s^{-1}$ [16] and high cut-off frequency(f_t) value such as 30 GHz[18]. Furthermore, RF applications of carbon nanotube devices are explored. One group at University of California Irvine [38] succeeded to fabricate nanotube AM demodulator. A group in University of California at Berkeley[39] and another at University of Illinois Urbana Champaign[40] successfully demonstrated carbon nanotube based functioning AM radio.

To conclude, the summarized applications and device performance reflects the carbon nanotube FETs' potential to be used in RF circuit design. The challenge to grow high density aligned micrometer long carbon nanotubes still continues to enhance the device performance and hopefully a significant improvement will be seen in near future.

2.3. Graphene

Graphene is the single atom thick layer of hexagonal lattice shaped carbon atoms[3],[5, 41]. Another definition might also be written as Graphene is a 2D planar sp^2 hybridization of Carbon atoms. Since Carbon atom has 4 valence orbitals; 2s $2p_x$,$2p_y$ and $2p_z$, z showing the perpendicular direction to the x-y plane of graphene sheet, the s,p_x,p_y orbitals yield the in plane σ bond. The lateral σ bonds are strong covalent bonds which hold the honeycomb structure. However, the uncoupled p_z orbital of one carbon atoms in the sheet interacts with neighboring p_z orbitals of different carbon atoms and creates π and π* bonding along the z direction with respect to graphene sheet. Hence, each graphene sheet is bonded to each other with weak Van der Waals bonds[42]. Lumps of graphene layers, stacked one on top each other construct graphite sheet. In Figure 2.3, the lattice shape of a graphene molecule can be seen. The lattice vectors $\mathbf{a_1}$ and $\mathbf{a_2}$ are written as $\boldsymbol{a_1} = \frac{a}{2}(3, \sqrt{3})$, $\boldsymbol{a_2} = \frac{a}{2}(3, -\sqrt{3})$. These are the real space lattice vectors for hexagonal shaped carbon atoms and the reciprocal lattice vectors in the Brilliouin zone can be obtained as $\boldsymbol{b_1} = \frac{2\pi}{3a}(1, \sqrt{3})$, $\boldsymbol{b_2} = \frac{2\pi}{3a}(1, -\sqrt{3})$ (see the Figure 2.3 for vector representations). K and K' points are called Dirac points where the upper energy band (π) and lower energy band (π*) in the energy band diagram of graphene overlap (see Figure 2.4).

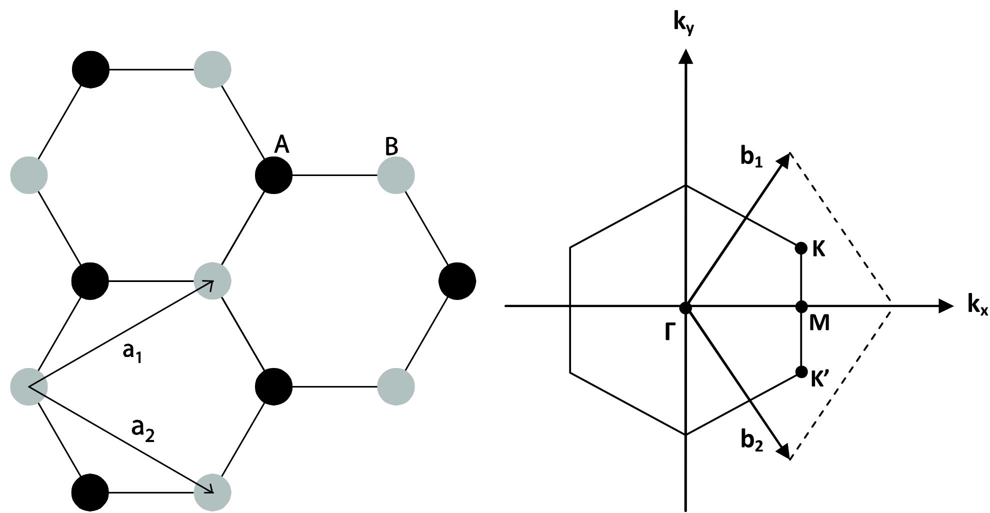


Figure 2-3.Hexagonal shape of honeycomb lattice and its Brilliouin zone lattice. a_1 and a_2 are primitive lattice vectors, b_1 and b_2 are reciprocal lattice vectors. Points K and K' are called Dirac points.

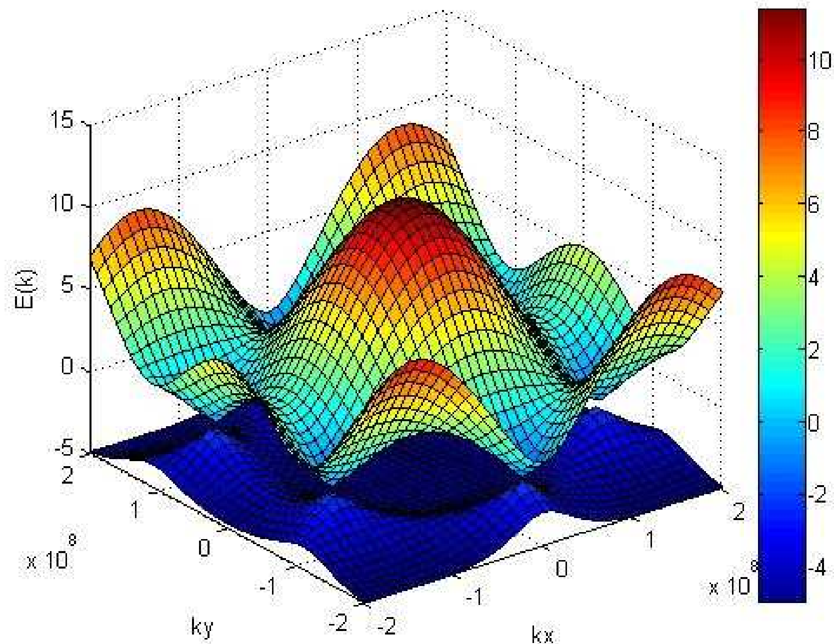


Figure 2-4. Energy band diagram of graphene structure. Dirac points are manifested as where upper($\boldsymbol{\pi}$) and lower energy bands coincide($\boldsymbol{\pi}$*).

The Fermi level is at zero conductivity point for pristine graphene, since the Fermi surface at the intersection points of π and π* band is infinitesimally thin, it would be more appropriate to name graphene other than a metallic surface. Hence, graphene is named zero band-gap semimetal. The name "Dirac" comes for the points K and K' resulting from linear energy dispersion of charge carriers behaving as massless Dirac fermions around these points. The energy dispersion for honeycomb lattice is given by

$$E_{\pm}(k_x, k_y) = \pm\gamma_0\sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}}$$

where k_x and k_y are the components of electron momentum vector **k** and γ_0 is the transfer energy between first neighbors π orbitals (also called the nearest neighbor hopping energy) which is around 2.9-3.1 eV [5, 42]. This energy dispersion formula reduces to $E = \pm\hbar v_f|k - K|$, where k is the electron momentum vector, v_f is the Fermi velocity having a value of approximately 10^6 m/s and K is the momentum vector at K point, and it resembles to the energy of a Dirac particle in relativistic field which is governed by Dirac equation. These symmetric π and π* bands provide an ambipolar device switch being symmetric around zero conductivity point which suggests an adjustable electron hole symmetry. Since, p_z state of carbon atoms in the graphene sheet is occupied by an electron, π band is filled with that electron. Thus, the points in different sides of Dirac cone (e.g. K and K' point) are interrelated by time reversal symmetry. Therefore, the six corners of reciprocal honeycomb lattice in Brillouin zone are called Dirac points and each one of them contains two Dirac cones one for hole (π* band) and one for electron state (π band).

At zero conductivity point (also suggested as neutrality point) charges carriers, both electrons and holes contribute equally to conduction and there is certain charge symmetry around zero conductivity point. Therefore, it is possible to use graphene as a flexible ambipolar device which can be switched easily from n-type to p-type, and vice versa. General point of view upon the universality of zero conductivity point on graphene is that around the minimum conductivity value of $4e^2/h\pi$ and it is independent of charge carrier concentration and therefore the transport is ballistic around these points. However, Adam et al. articulate that the universal ballistic transport can be rendered to a nonuniversal diffusive transport by adjusting the charge impurities upon the substrate[43]. By this

theory, the governing mechanism nearby Dirac point is the charge impurity scattering and it is due to the self-consistently determined induced charge carrier density. We will discuss the implication of this theory in Chapter 6.

Chapter 3

Synthesis of Graphene

3.1. Deposition Methods of Graphene

Another important issue in graphene device fabrication is creating scalable, controllable and facile growth of graphene. Scalability of growing graphene is needed for the fabrication of graphene devices over large areas. Large area means higher conduction output for devices such as photovoltaics and RF communication device. The most important aspect of graphene growth is the controllability of grown graphene layers and the challenge to obtain *in situ* single layer or bilayer graphene. Without proper control over the scalable size of graphene layer growth process, one can have graphitic structure with many layers of graphene and thus the fabricated device will show inferior performance comparing to single layer graphene based devices. Therefore, the problem of growing single layer graphene is a crucial one which nowadays researchers are still struggling to solve.

In the early days of graphene research, graphene layers were mostly obtained from kish graphite and graphite derivatives such as highly oriented pyrolytic graphite (HOPG) by using mechanical exfoliation[3]. Since, graphite is the stack of graphene layers and bonded to each other with weak van der Waals force, graphene layers can be physically detached

from the remaining graphitic structure. This process is also called ‘scotch tape’ method, after all the exfoliating is performed by sticking the tape onto the graphite and pulling it apart. Although high quality single layer graphene can be isolated by applying this technique; it does not supply the large area need of graphene for scaling graphene based devices. This technique is further improved by using SiO_2/Si based stamps[44]. These stamps are put onto the surface of graphite in order to cut a piece of graphene layer and exfoliate it. By exploiting this technique, isolated graphene can be pre-patterned for the desired device geometry or purpose. Also Polydimethylsiloxane (PDMS) and pre-patterned gold films were used for the exfoliation by other research groups[45],[46].

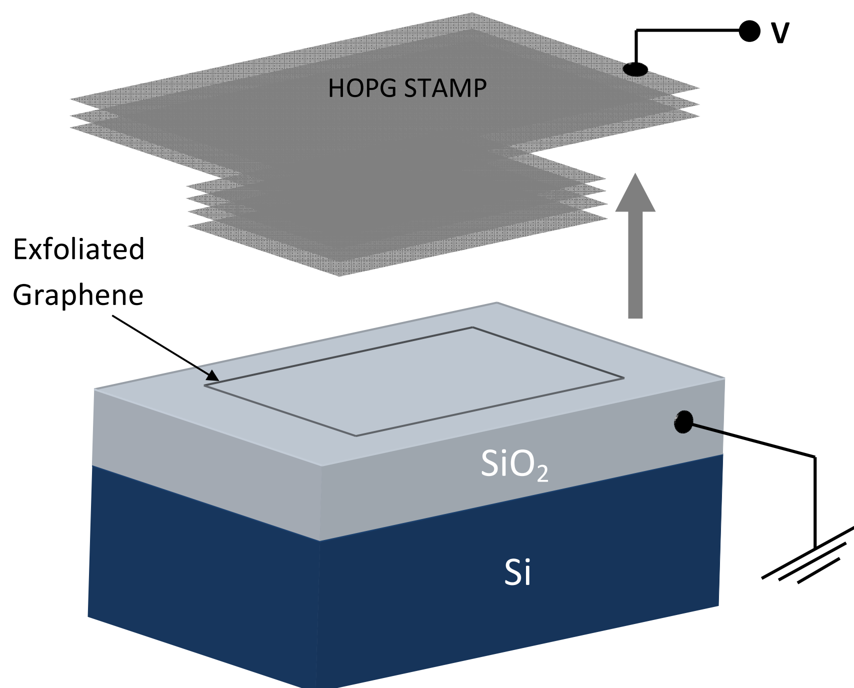


Figure 3-1. A schematic of electrostatic exfoliation. Graphene is exfoliated from HOPG surface with an applied bias.

An inspiring method was discovered by Liang et al. for exfoliation of graphene from graphite structure in 2009[47]. An explanatory schematic of the technique can be seen in Figure 3-1. A bias voltage applied between pre-patterned HOPG layer and Si/SiO_2 surface to create an electrostatic field in order to pull the pre-patterned graphene apart from HOPG and attach it onto the insulator surface. This novel technique is also called electrostatic exfoliation of graphene and it provides production of high quality few-layer graphene sheets and graphene nanoribbons up to 18 nm. Another useful exfoliation technique is liquid phase exfoliation of graphene layers. Generally in this method, the stack of graphene layers in graphitic structure are intercalated by several chemical compounds or polymers in a liquid suspension and separated into few-layers of graphene by sonication or other means of agitation. For instance, Green et al. used a density gradient ultracentrifugation in order to isolate encapsulated graphene sheets by sodium cholate[48]. They achieved to exfoliate graphene sheets and detect the number of layer by observing the buoyant density of graphene-sodium cholate suspensions. Thicker graphene layers are located near the bottom of the tube containing suspensions after density gradient ultracentrifugation treatment. This sort of exfoliation techniques provide the controllability over the number of graphene layers fabricated from HOPG or simply kish graphite. However, patterning is still an issue and is not applicable in the exfoliation process. Therefore one needs to develop a much more scalable technique to pre-pattern and put the graphene layers into the desired shapes suitable for device fabrication usage. One of the techniques that provide this kind of patterning is epitaxial growth of graphene by thermal decomposition of silicon carbide (SiC)[49],[50].

Application of the technique starts with honeycomb lattice patterning (graphitization) of carbon atoms on silicon carbide, thus epitaxial growth of graphene on top of silicon carbide template and silicon sublimation under ultrahigh vacuum. There are several drawbacks of

this technique such as the difficulty to reach ultrahigh vacuum of the order of 10^{-10} Torr at high temperatures (around 1500ºC), limitations of device geometry due to the lack of back gate and requirements of a top gate. Nevertheless, epitaxial grown graphene can be transferred to Si/SiO_2 or other substrates by using gold/polyimide films as sacrificial layer [51]. Epitaxial growth of graphene onto SiC is an unfavorable technique as a result of its harsh experimental conditions and graphene quality that it yields. There are some other creative and state-of-the-art experimental techniques to produce patterned graphene layers such as producing graphene nanomesh and unzipping carbon nanotubes [52]'[53]. Since CNTs are basically rolled up graphene sheets, it should be possible to unroll them with several chemical and physical treatments. Jiao et al. unzipped nanotubes through using PMMA layer as etching mask and etched multi walled CNTs in Argon plasma in order to obtain a several nanometer width graphene nanoribbons, furthermore transfered them onto SiO_2 substrate. Also Raman spectroscopy reveals their quality and single layer character. Graphene nanoribbon devices around 6nm wide fabricated by using the unzipping CNT technique showed promising on-off ratio up to 100 and the technique can be further improved. Another effective method to obtain graphene nanoribbons is to align silicon nanowires on top of graphene sheets and use them as etching mask to oxygen plasma[54]). In this method, silicon nanowires protect underlying graphene sheet and leave remaing part of the sheet exposed to oxygen plasma. Finally, etchant mask nanowires are detached and removed by sonication. Various sub-10 nm width graphene nanoribbons are obtained. An explanatory schematic of the technique is shown in Figure 3-2. The width of graphene nanoribbons can be controlled by the diameters of selected silicon nanowires and adjusting oxygen plasma etching rate. It can be claimed that this techniques brings an alternative to conventional lithography techniques to pattern graphene sheets.

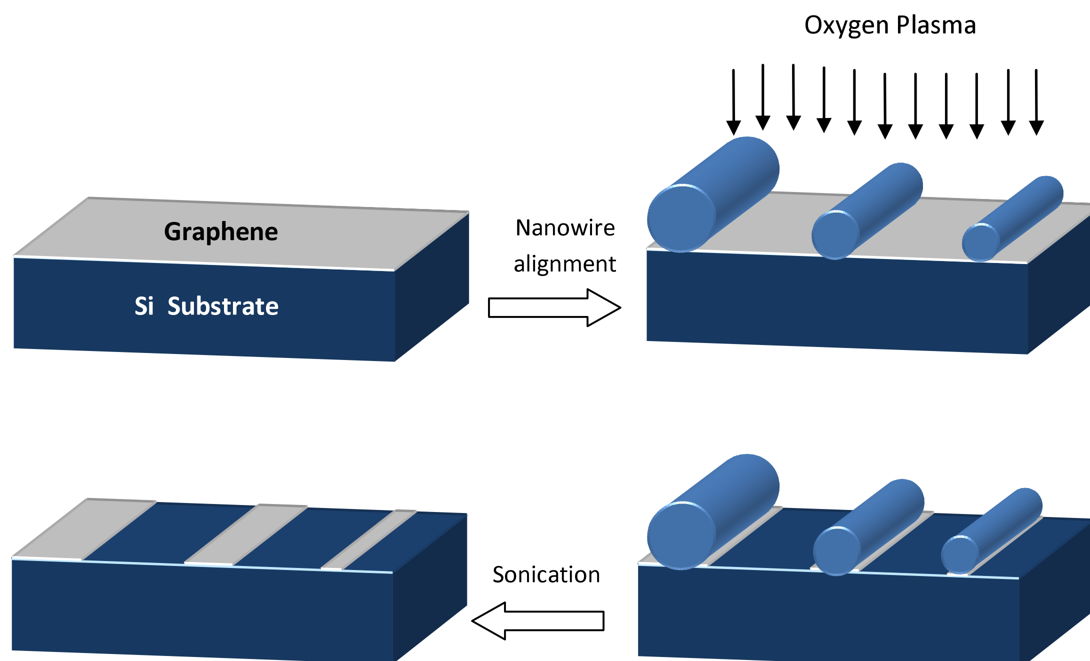


Figure 3-2. Schematic of nanowire etching mask technique in fabrication of graphene nanoribbons with various widths. Nanowire alignment takes place in step 2 and patterns the underlying graphene sheet.By step 4, sonication clears up the patterned surface from silicon nanowires.

Although thermal decomposition of SiC, mechanical, electrostatic and liquid exfoliation are effective technique to produce graphene layers, several drawbacks make them unfavorable such as lack of yielding large-area few layers graphene at high quality, applicability, controllability of the technique and pre-patterning the substrate in order to have desired, necessary patterns beforehand. Hence, epitaxial growth of graphene on a template should be provided by a more handy growth process. These requirements can be achieved by the chemical vapor deposition (CVD) and we will discuss this technique in the next section.

3.2. Chemical Vapor Deposition of Graphene

Chemical vapor deposition (CVD) of graphene is a facile and controllable epitaxial graphene synthesis method to produce large-area few layer graphene sheets. CVD is also used in carbon nanotube[18] and various nanomaterial production[55]. The process consists of high temperature containing in a hot wall furnace and generally flowing H_2 (Hydrogen), and CH_4 (Methane) or C_2H_5OH (Ethyl alcohol) under certain pressure. Gas molecules like methane and ethanol are carbon feedstock needed for graphitization over the catalyst surface. Generally, catalyst particles of CVD process are transition metals such as Ni,Cu,Co,Pt,Ir which are deposited on a wafer or simply put as large area foils or metal blocks. Resembling to the growth of Carbon Nanotubes, catalyst particles dictate the growth pattern of graphene in desired geometries determined beforehand and catalyze the chemical decomposition of carbon feedstock molecules on the surface or within the catalyst itself. Also, they play the role of support to carbon atoms during growth process. Carbon solubility of catalyst takes a crucial role in the controllability of epitaxial growth graphene layer number. General opinion upon the dynamics of carbon graphitization in catalyst metal such as Nickel during CVD process was either carbon precipitation[14] or segregation[56]. In 2009, Li et al. illuminated the growth mechanism of CVD graphene on Ni and Cu surfaces by using carbon isotope labeling in order to track down their movement during graphitization[57]. They concluded that CVD growth of graphene on Ni is a carbon segregation and precipitation process whereas growth on Cu is a process based on surface adsorption. In Ni catalyzed process, carbon atoms first diffuses in metal thin film, segregate into islands of graphene, and precipitate onto the surface, on the other hand in Cu case carbon atoms are attached to the surface to form the graphene layer and the growth process is self-terminating which limits the formation of multilayer graphene. The main reason of

self-termination of the growth process on the Cu surface is the low-carbon solubility of Cu. Once CH_4 diffuses into Cu surface, it catalytically decomposes and begins to form graphene islands. When the whole Cu surface is covered with graphene layers, catalyst particles deplete on the surface and carbon atoms cannot dissolve within Cu anymore indicating the carbon saturation and low solubility of Cu. Hence, CVD growth of graphene on Cu is named as surface catalyzed self-terminating process and therefore the thickness of graphene, the number of layers is much more controllable on large scales. Ni films have higher carbon solubility than Cu, therefore uniform graphene layers are not produced and layer thickness spatially varies on Ni surface. To control the formation monolayer graphene sheet on Ni surface, one needs to cool down the CVD process much faster in order to suppress the carbon precipitation. This method is much more difficult whereas CVD on large-area copper foils seems more reliable and physically controllable[13]. As an extreme example to CVD growth of graphene on large area Cu foil, Ahn et al. succeded to manufacture 30-inch diagonal width of rectangular monolayer graphene film by[15]. This development made the monolayer graphene production and graphene macroelectronics accessible on very large scales (e.g. large displays).

In this work, we used CVD growth technique in order to produce graphene sheets needed for graphene based field effect transistors. The process we carried on to grow uniform graphene layers is illustrated in Figure 3-3. To grow graphene layer onto Cu surface, process chamber is heated until reached to 1000 ºC while Argon and Hydrogen gases are flowing throughout the chamber at 240 sccm (cm^3 per minute) and 8 sccm respectively. The gas rate flowing into the chamber is adjusted through using mass flow controllers (MFCs) shown in Figure 3-4. Sample is annealed at 1000ºC for 10 minutes then methane is introduced to chamber at rate of 5 sccm for 10 minutes to start growth sequence. After 10 minutes of growth, sample is sharply cooled down to room temperature. During cool down

hydrogen and argon gas are flowing at rate of 8 sccm and 240 sccm respectively. The surface morphology of graphene grown on copper surface is following the pattern of low purity (%99.8) copper foils.

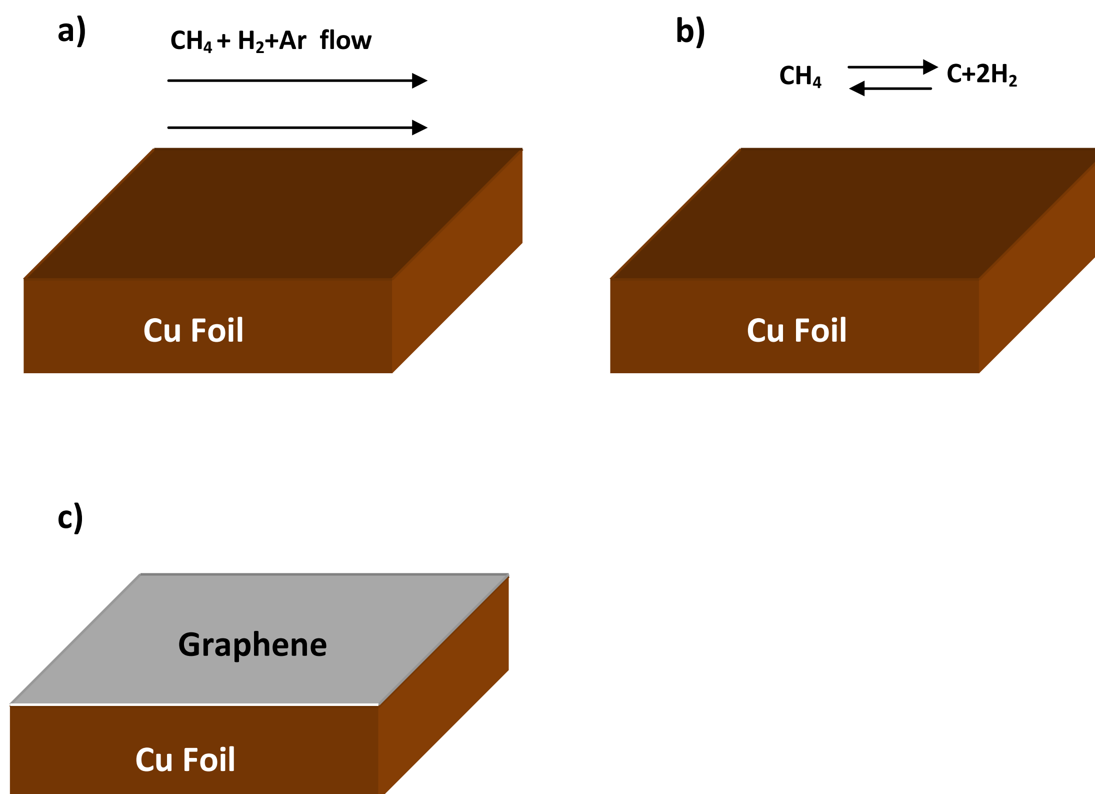


Figure 3-3. Schematic of CVD graphene growth process on copper foil. a) Methane Hydrogen and Argon gases are flowing into the chamber of furnace at ambient pressure b) Chemical decomposition of carbon atoms occur at 1000℃, methane decompose into carbon and hydrogen gas c) carbon atoms are adsorbed on the catalyst surface and graphene islands start to grow.

CVD system that we used in our laboratory is shown in Figure 3-4, Protherm furnace containing 180 cm long quartz silica tube is labeled as 1, it is able to reach up to 1100ºC temperature by a speed of 8ºC per minute. Vacuum flange is labeled as 2 and MFCs for Hydrogen, Argon and Methane is labeled as 3 in the Figure.

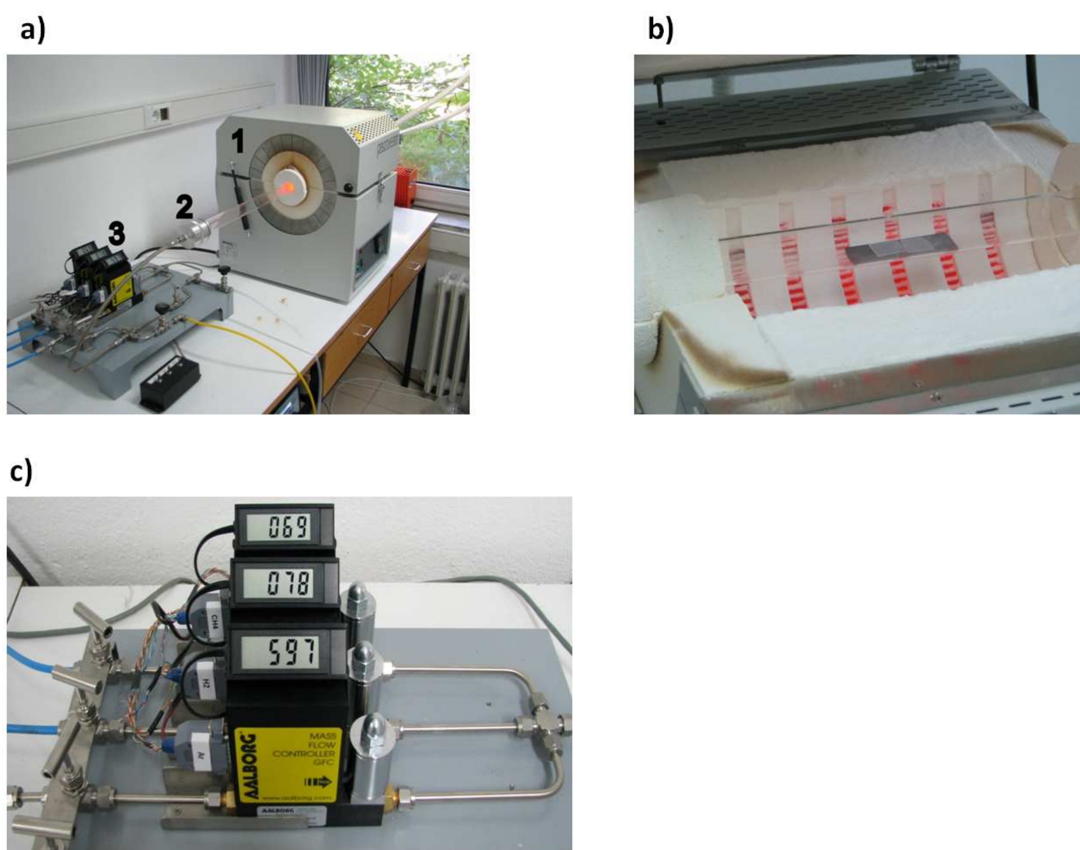


Figure 3-4. General view of CVD system equipments. a) CVD system consisting of quartz silica tube, Protherm furnace (1), Vacuum Flange (2), Mass Flow Controllers (MFCs)(3). b) Close-up inside of the furnace. c) Close-up MFCs. All photos are courtesy of Emre Ozan Polat.

CVD growth sample of graphene on top of copper surface (~1cm^2) can be seen in Figure 3-5. After growth copper surface becomes shiner than before growth process. Post treatment of the graphene sheet starts with transferring it to Si/SiO_2 surface. Polymethylmethacrylate (PMMA) solution is deposited onto of Cu/Graphene surface and cured at 120ºC for 1 minute. The process continues until PMMA properly adhere to the graphene surface. Then Cu/Graphene/PMMA is released to 0.05 g/ml Fe(III)Cl_3 solution to etch the Cu surface .After staying for ~4 hours of Cu etching, sample is pulled from the Fe(III)Cl_3 solution and rinsed in de-ionized water. Graphene/PMMA sample is then transferred to Si/SiO_2 surface.

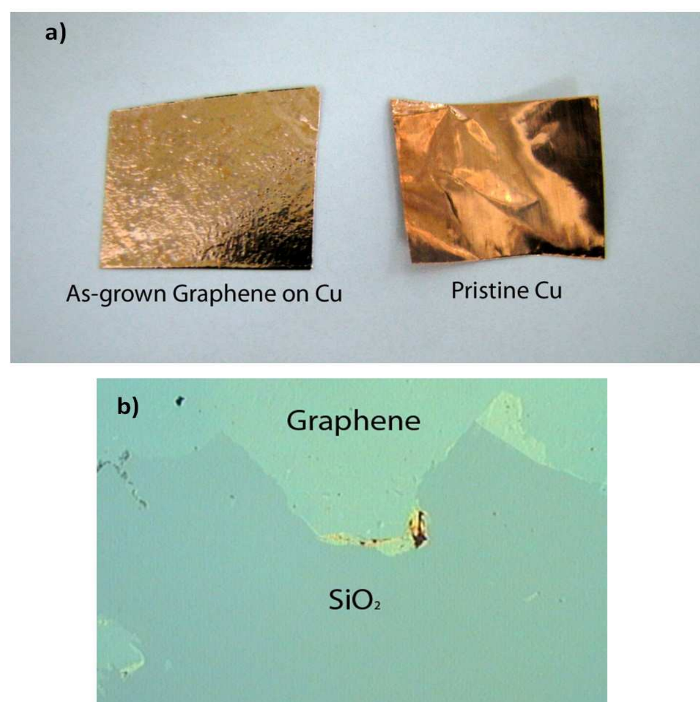


Figure 3-5. (a)As-grown graphene on copper surface, compare with clean copper foil surface. (b) Transferred graphene to Si/SiO_2 surface, color contrast indicates a few-layer graphene flakes.

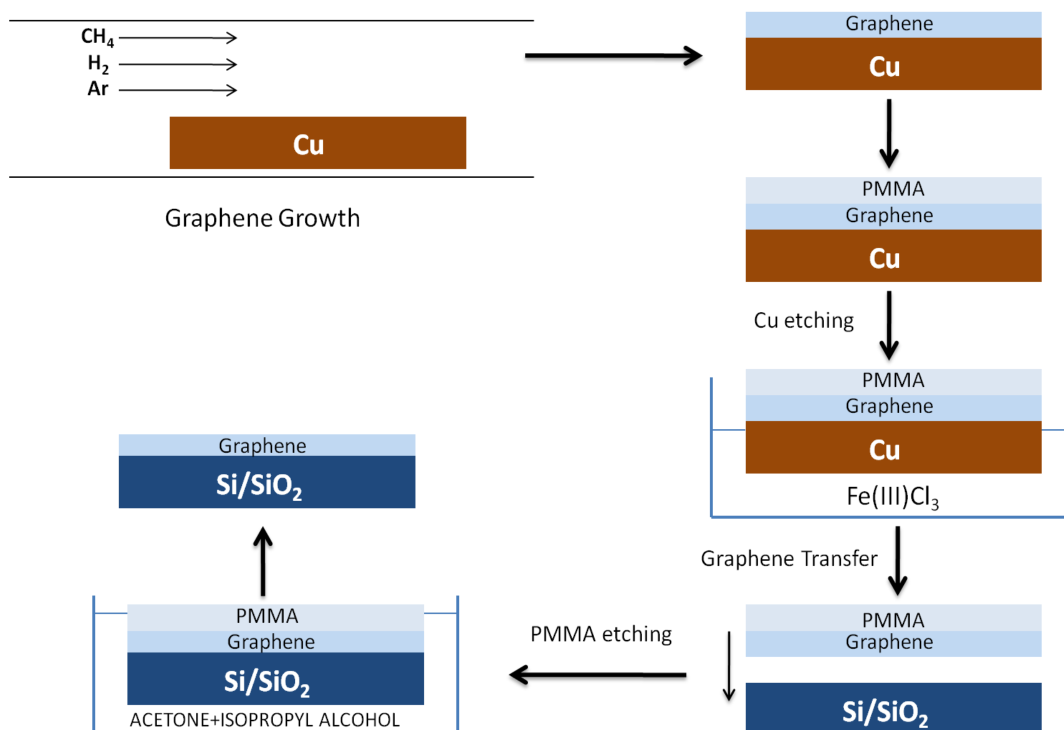


Figure 3-6.The schematic of graphene transfer onto Si/SiO_2. After graphene growth on Cu, PMMA is cured onto the Cu foil and sample is put into 0.05 g/mL Fe(III)Cl_3 solution. PMMA/Graphene composition is transferred onto Si/SiO_2 surface by applying a mechanical force onto the surface. Finally, PMMA is etched away by acetone and isopropyl alcohol.

Transfer of graphene procedure can be better comprehended by following the schematics in Figure 3-6.

SiO_2 surface is highly flat and smooth whereas surfaces of both Cu foil and as-grown graphene are rough enough to have large corrugations[58]. PMMA follow the same surface topology as well and becomes even rougher after cured at high temperatures. As a result of that large gaps are formed between graphene and SiO_2 surface causing cracks and leaks during transfer process. In order to prevent this, we followed the same procedure as Li et al. which is depositing PMMA on transferred graphene surface and curing it at 150 ºC[59]. The second PMMA treatment is needed for relaxing the underlying rough graphene sheet in order to avoid cracks due to large gaps underneath.

Graphene transfer to SiO_2 procedure might potentially damage graphene sheet due to cracks formed on graphene surface and deteriorate device performance significantly. Therefore, other methods should be investigated to eliminate transfer process and its negative effects on device operation process. According to Ismach et al. graphene can be directly grown onto SiO_2 by dewetting of deposited Cu on Si/SiO_2 surface [60]. This procedure is based on normal vacuum (100-500 mTorr) CVD growth process on Cu deposited SiO_2 surface for several hours (15-420 mins.). As a result of that, Cu dewets as a "finger-like" structure (see Figure 3-6) from SiO_2 surface and grown graphene is directly adhere to the insulator surface. However, the method needs to be improved if higher quality and less defected graphene sheet is desired to be directly transferred. Figure 3-6 shows the graphene sample for which we applied direct CVD process. The thickness of Cu layer is between 100 nm and 150 nm. One can see the evolution of the surface morphology and dewet finger-like shaped Cu surface after 30-45 mins. and 90 mins. of CVD at ambient pressure. This method basically eliminates Cu etching and graphene transfer to a dielectric

surface. Hence, Direct CVD is a promising method in graphene based device fabrication and electronic performance enhancement.

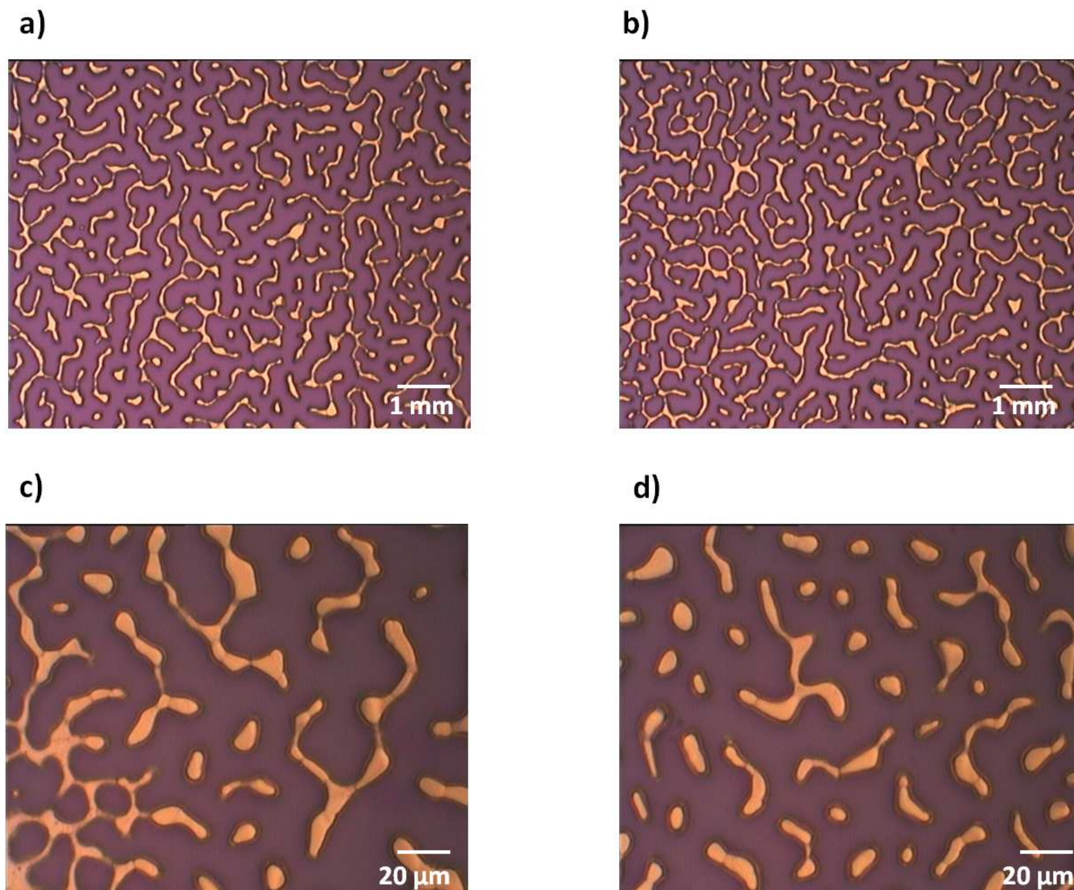


Figure 3-7. Dewetting process of Cu evaporated on Si/SiO_2 surface. (a)-(b) Surface morphology after 45 mins. of CVD. (c)-(d) after 90 mins. of CVD. Finger-like pattern is becoming less dense with increasing quantity of dewet copper.

Chapter 4

Raman Spectroscopy of Graphene

4.1. Raman Scattering

Raman scattering is basically phonon creation or annihilation [21] in a crystal structure due to inelastic scattering of a photon by that crystal. Let ω, **k** be the wave frequency and vectors of incident photons, ω´, **k´** be wave frequency and vector of the scattered photons and σ, **K** be wave frequency and vector of the created or annihilated phonon. The allowed transitions between states for the first order Raman effect are $\omega = \omega' \pm \sigma$ and $\boldsymbol{k} = \boldsymbol{k}' \pm \boldsymbol{K}$. The order of Raman process is proportional with the phonon number involved in scattering, e.g. in second order Raman process two phonons are involved in the scattering of one photon. To activate Raman scattering in a molecule, polarizability plays an important role. Strain induced electronic polarizability on a molecule activates the Raman effect on that molecule or crystal concerned. Assume that polarizability α is a function of phonon mode and can be written in a power series of phonon amplitude u:

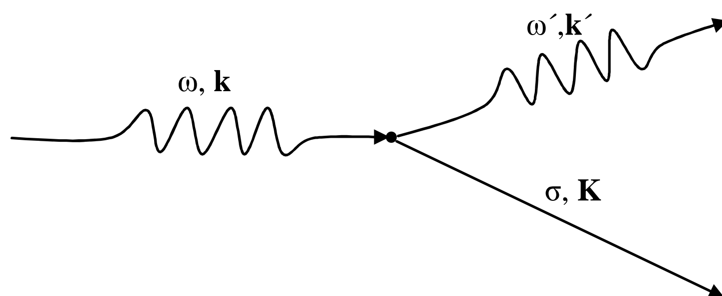
$$\propto = \propto_0 + \propto_1 u + \propto_2 u^2 + \cdots$$

Let phonon amplitude be $u(t) = u_0 \cos \sigma t$ and electric field component of the incident photon $E(t) = E_0 cos\omega t$, then the induced dipole moment of the system to the first degree is given as follows:

$P(t) = \alpha E(t)$ and therefore the induced electrical dipole moment on the first order Raman process becomes to the form. $P = (\alpha_1 u)E_0 \cos \omega t = \frac{1}{2}\alpha_1 u_0 E_0 [\cos(\omega + \sigma)t + \cos(\omega - \sigma)t]$

This equation suggests that two photons can be emitted after scattering takes place, a photon at frequency ω + σ and a photon at frequency ω - σ. The photon at ω + σ represents the Stokes line and photon at ω - σ anti-Stokes line. Stokes process corresponds to phonon creation inside the crystal by the scattering of incident photon and anti-stokes process corresponds to phonon annihilation.

a)



b)

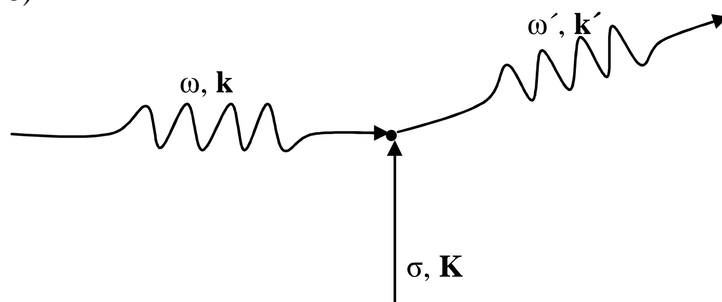


Figure 4-1. Raman scattering processes corresponding to (a) Stokes, (b) Anti-Stokes process.

In graphene lattice, stretching of C-C atoms along σ bonds create strain induced polarizability and causes to break hexagonal symmetry[61]. This polarization makes graphene surface Raman active. There are six phonon dispersion branches, 3 of them are acoustic and 3 are optic phonon branches. Depending on the direction of the C-C atoms (noted as A and B atoms in Figure 2.3), vibrations perpendicular and parallel with respect to A-B carbon atoms orientation are respectively called transverse and longitudinal phonon modes. Two out of three optic phonon modes are transverse; one corresponds to in plane and the other one to out-of-plane vibrations. Remaining one optic phonon mode corresponds to longitudinal mode. Likewise, two of the acoustic phonon modes are transverse corresponding to in- and out-of-plane vibrational phonon modes and the remaining one is longitudinal acoustic mode[62]. These dispersion curves are important for detecting Raman active modes which give rise to several Raman peaks of graphene. Especially, phonon modes in the vicinity of K symmetry point (see Figure 2.3-b) is important by means of double resonance process[61]. The significant character of atom thick layer of graphene in Raman spectroscopy is sharp Lorentzian peaks appearing at 1582 cm^{-1} and 2700 cm^{-1} so called G-band and G´-band respectively. Third peak appearing at 1350 cm^{-1} with lower intensity is called D-band addressing disorder induced Raman signals. The G-band corresponds to the in-plane transverse and longitudinal optical mode, around Γ point, therefore these are the Raman active phonon modes occurring as a first order Raman process, whereas D and G´ bands are second order Raman scattering processes involving a double resonance (DR) process. The double resonance process includes scattering of two phonon inside the boundary of the first Brillouin zone around K and K´ points which are related to each other with time reversal symmetry[62]. Basically in DR process, laser induces excitation of an electron hole pair in the circle around K point, then electron is inelastically scattered by a phonon with momentum **q**. The electron is back

scattered to the previous energy state by a phonon with momentum **–2q**. Therefore, these momentum vectors cancel out each other and electron emits a photon by recombining with the hole in previous energy state (see Figure 4-2). From kinematical point of view, in both first order and second order Raman processes energy and momentum are conserved quantities.

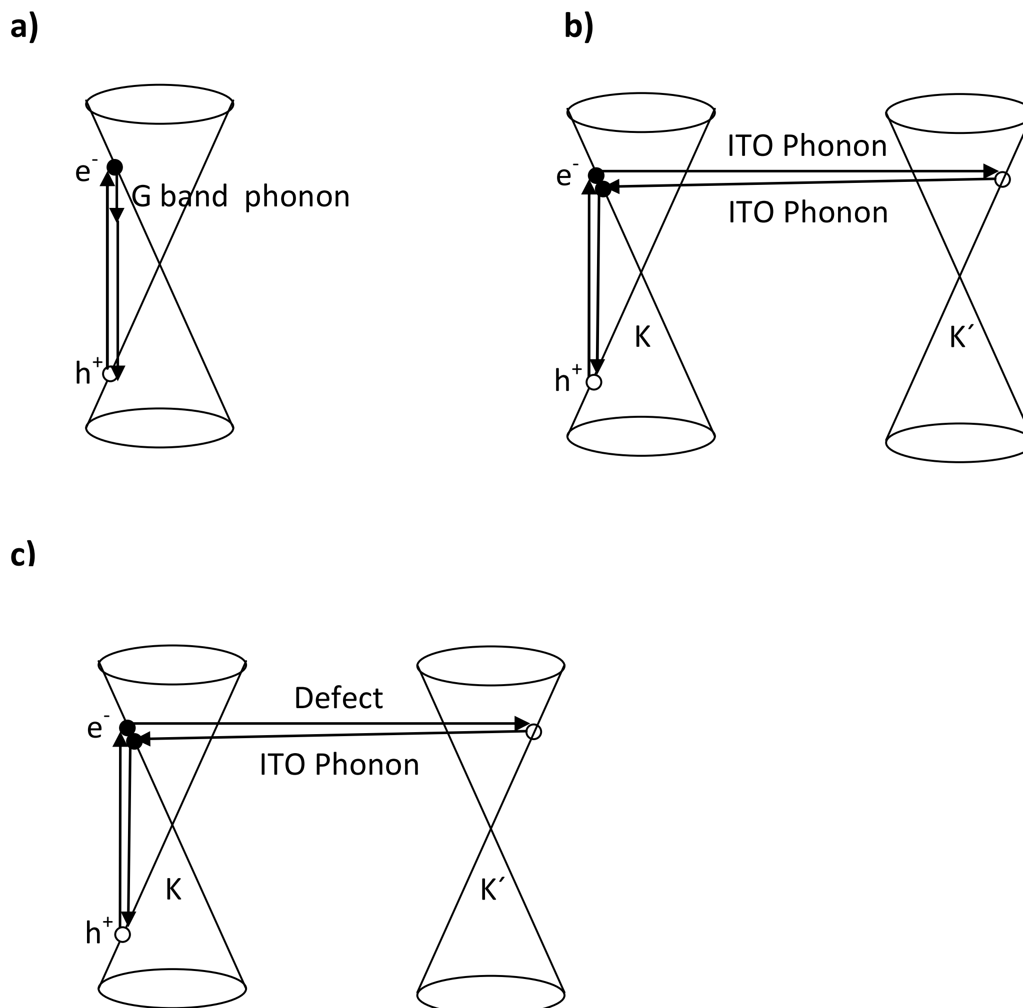


Figure 4-2. (a)The first order G band Raman process is depicted. Laser induces an electron hole pair and G band phonon is generated. (b) The second order double resonance (second order) G´ band Raman process Excited electron is scattered by in-plane Transverse optic phonon modes. (c)The second order double resonance (second order) D band Raman process. Momentum is conserved in both (a) and (b) type of Raman process whereas momentum is not conserved in process (c).

Importance of the G´-band in Raman spectrum of graphene is that the number of layers in a graphitic structure can be deduced from the full width at maximum (FWHM) of G´ band peaks which is around 24 cm^{-1}.

4.2. Raman Spectrum of CVD grown single layer graphene

D, G and G´ bands are generally characterizing graphene layer both quantitatively and qualitatively. Intensity ratio of D band over G band, I_D/I_G, shows us the general quality of graphene layer. Since D-band spots the defective part of graphene layer, the more disordered graphene structure is the more D-band Raman signal intensity will be. Therefore, I_D/I_G ratio should be minimum (preferably zero). Another important feature of graphene Raman spectroscopy is the G´ band width. It generally indicates the number of graphene layers. As the number of layers increases sharp Lorentzian peak of G´ band becomes wider and FWHM of the peak increases[63]. Some researchers articulate that the $I_G/I_{G'}$ ratio is as important as FWHM of G´ band for the judgment of number of layers, also for the quality of graphene layer and this ratio should be less than 1 in order to have a high quality graphene layer [60]. However, this point has not been clarified yet and there is no concrete background in Raman literature to explicitly prove the correlation between $I_G/I_{G'}$ ratio and quality of graphene layer.

The Raman spectrum of the graphene layer grown on thin copper foil in our CVD system can be seen in Figure 4-3. Here the Raman spectrum of the sample grown at 1000ºC with 5 sccm of methane, 8 sccm of hydrogen and 240 sccm of argon gas flow for 10 minutes at ambient pressure.

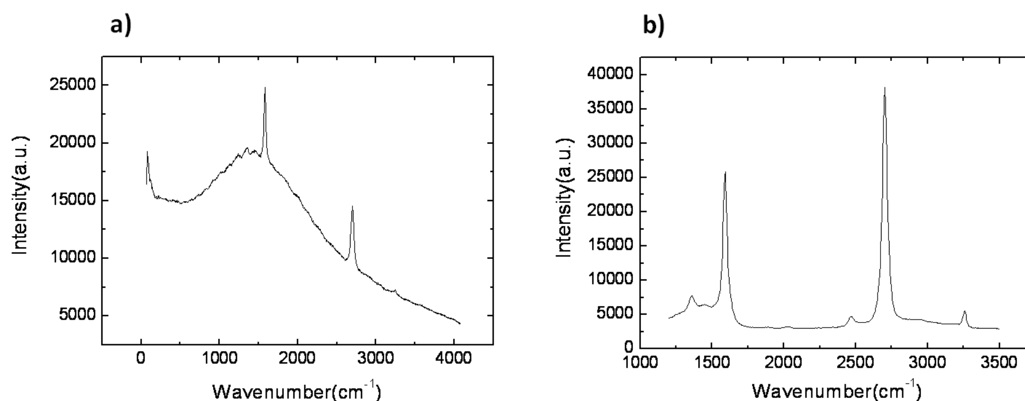


Figure 4-3. The Raman spectrum of (a) Graphene on copper foil, (b) Graphene transferred to Si/SiO_2 surface.

Here couple of distinct features of Raman spectrum of transferred graphene explicitly shows us that the graphene layer is mostly few-layer since (1) FWHM of G´ band is ~46 cm^{-1}, (2) the intensity of the G´ peak is larger than D band and (3) the spectral shape of G´ band is Lorentzian. Furthermore, $I_G/I_{G'}$ is less than 1 which is also an indication for few-layer graphene formation on the substrate concerned. Moreover, Raman spectrum shows a low I_D/I_G addressing the quality and absence of large area defects on the graphene sheet.

We have optimized the growth conditions by looking at the Raman spectra of the grown samples. The growth temperature, time and the rate of flow of methane and hydrogen plays the critical role for the optimum growth of a few layer graphene. Figure 4-4 shows the effect of flow of methane during the growth process. The growth time and temperature is kept at 5 min. and 1000 ^{o}C, respectively. The flow of CH4 is scanned from 10 sccm to 40 sccm at ambient pressure. By looking at the intensity of D band and G` band, it can be seen

that the optimum rate of flow is around 15-20 sccm. Generally, the optimum CVD growth sample is lumping around 1000 ºC where I_D/I_G is low, $I_G/I_{G'}$ and FWTH of G´ indicate lower number of graphene layers. Comparing the quality of these samples by means of CVD growth parameter opens up the possibility to fully control the CVD process parameters and obtain the optimum conditions to grow almost defect free single-layer graphene sheet. Hence, Raman spectroscopy is a good roadmap to find the optimum CVD growth parameters.

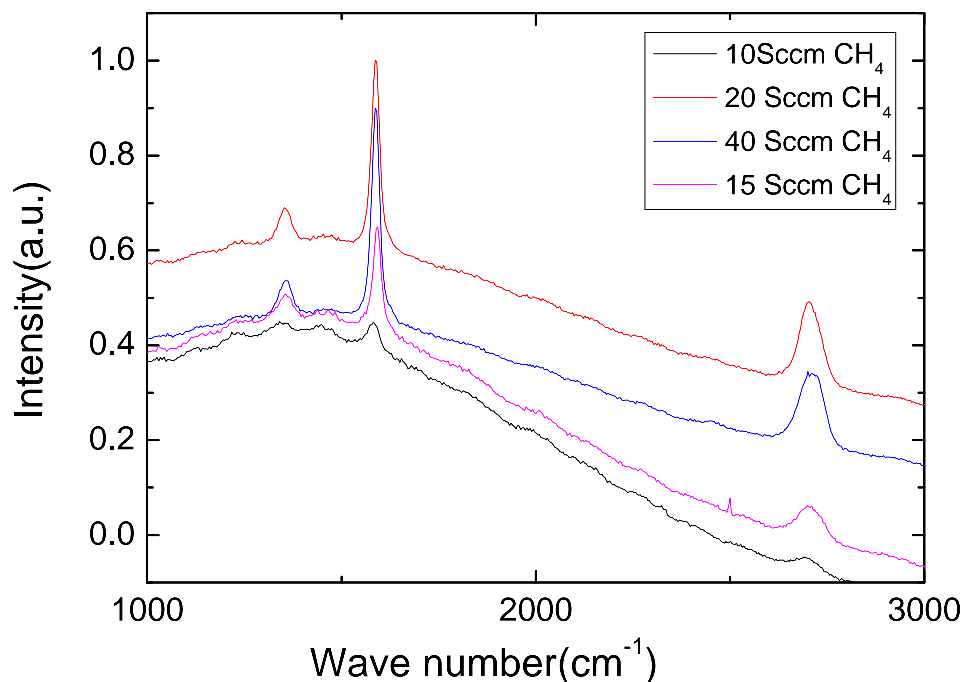


Figure 4-4. The Raman spectrum of graphene samples grown by different flow of Methane gas. Higher quality samples are yielded between 15 and 20 sccm flow of CH_4. CVD is carried on at ambient pressure.

The growth temperature is another important growth parameter. We grew graphene samples with different growth temperature. Figure 4.5 shows the Raman spectrum of the samples. The growth temperature of 1000 °C provides the lowest $I_G/I_{G'}$ ratio and lowest I_D/I_G ratio which indicates the lowest concentration of defects.

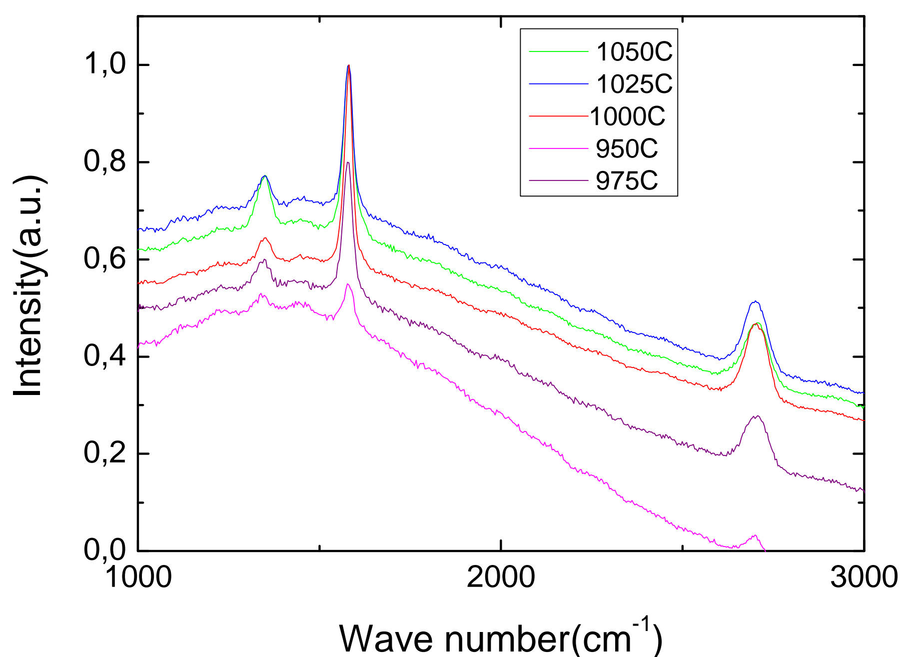


Figure 4-5. The Raman spectrum shift as a function of growth temperature. As it can seen in the plot, the high quality graphene sheet growth generally occurs around 1000 ºC.

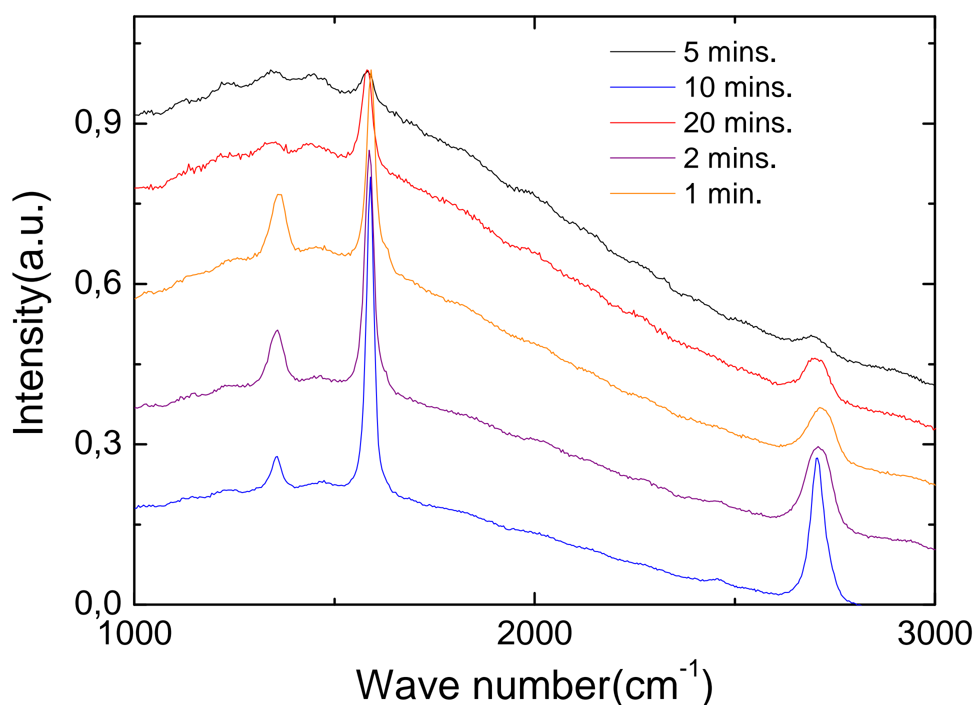


Figure 4-6. The Raman spectrum shift as a function of growth duration. Red,Blue and Black peaks are for 10 sccm CH_4 flow. Cyan and Orange peaks are for 40 sccm CH_4 flow at 1000°C. CVD is carried on at ambient pressure.

Figure 4.6 shows the effect of growth duration. The growth is start by flowing methane and stopped by termination of the flow. The growth time of 5-10 min. provides the optimum graphene samples at 1000 ^{o}C and at the ambient pressure. In all Figures 4-4, 4-5 and 4-6 it can be seen an attempt to optimize the graphene layer quality and number. The experiment which has the Raman spectrum given in Figure 4-4 is carried on for finding optimum

carbon feedstock (here, Methane) flow quantity while keeping other CVD parameters constant such as pressure at ambient, growth duration at 5 minutes and temperature at 1000ºC. Here on this point, Raman spectroscopy determines how varied and constant parameters effect defect formation and number of layers on graphene surface.

Chapter 5

Fabrication of Graphene Based Field Effect Transistor

5.1. Field Effect Transistor Fabrication

Graphene based field effect transistor fabrication starts with the transfer of graphene onto the Si/SiO_2 (see Figure3-5c). After characterization of graphene on dielectric surface, we pattern the device template (Si/SiO_2 + graphene) by conventional pholithography techniques. This process begins with photoresist coating on the template surface by AZ5214E and spinning the sample at 5000 rpm. for 50 seconds. Then, the sample is hard baked at 110ºC for 50 seconds like in most photolithographic processes. Sample is exposed to U.V. for 120 seconds in order to pattern the electrodes of the device by using DC device mask in Karl-Suss mask aligner. Photoresist residue is developed away by AZ5214E developer. As a result, source and drain pads are patterned on graphene/SiO_2. Metallization of S/D pads is performed within the box coater; Au and Ti respectively on the thickness of 50 nm and 5 nm are evaporated on the patterned surface with evaporation rate of 0.5 nm/s and 0.2 nm/s. Post-treatment of evaporated sample is lifting-off Ti/Au in acetone from the sample surface in order to complete the metallization. The isolation layer protecting the graphene layer in the device area should be patterned before reactive ion etching (RIE) of residual transferred graphene. Therefore, the isolation layer is patterned by using AZ5214E

once again, exposed to U.V. for 40 s. and developed for 2 minutes. Finally, residual graphene is etched away by RIE with 100W O_2 plasma for 1 minute. Device geometry and actual device can be seen in Figure 5-1. Source and Drain pads are coated with Ti/Au and graphene layer is located between them (see Figure 5-1b).

The probe station that we intended to measure electrical capability of the graphene DC FETs did not allow us to practically connect every micrometer scaled device on the probes for back gate bias; therefore we used conductive epoxy to connect the whole wafer containing DC FETs. Silver conductive epoxy is carried on by curing adhesive flakes at around 100ºC for 30-45 minutes. The bonded red cable to the DC device wafer can be seen in Figure 5-1a.

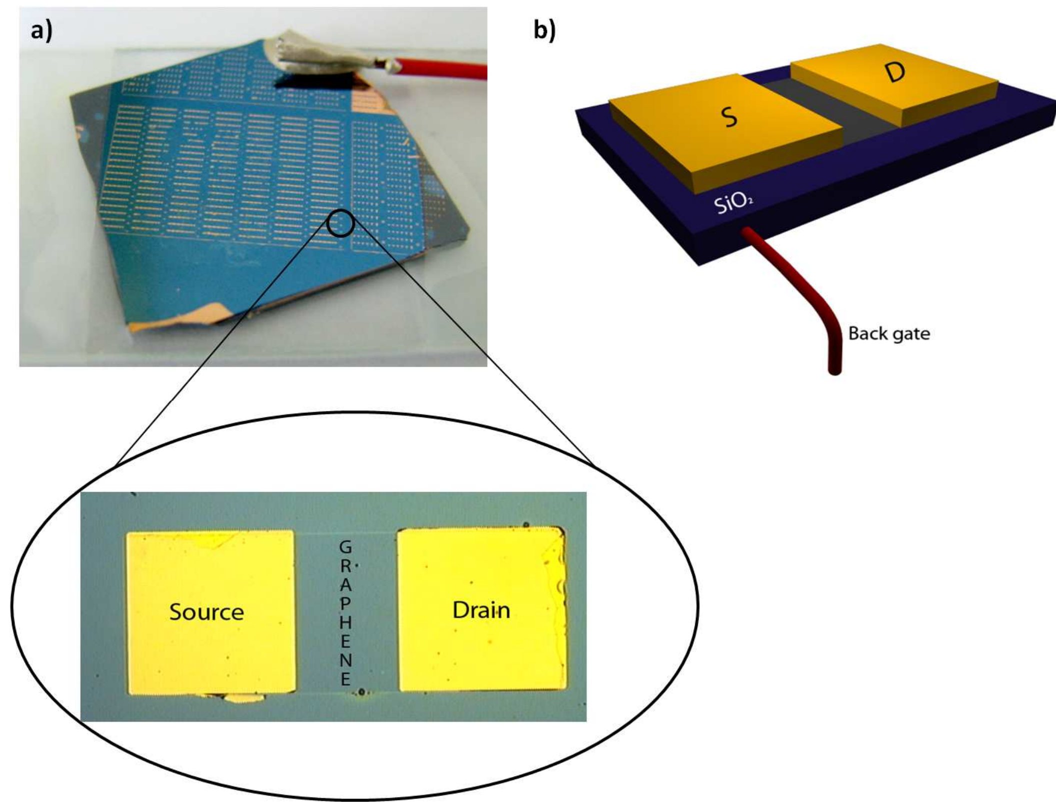


Figure 5-1. Real image photos and device schematic of the graphene DC FET. (a) Close-up to graphene based FET, Total area of patterned devices is ~3.75 cm^2. Back gate is implemented by conductive epoxy for measurement purpose (red cable embedded to upper part of device) Microscopic image of a device on the wafer is shown. Graphene layer can be recognized from the contrast between SiO_2 and graphene Device photo is courtesy of Emre Ozan Polat (b) 3D schematic of the graphene device geometry. Courtesy of Ertuğrul Karademir.

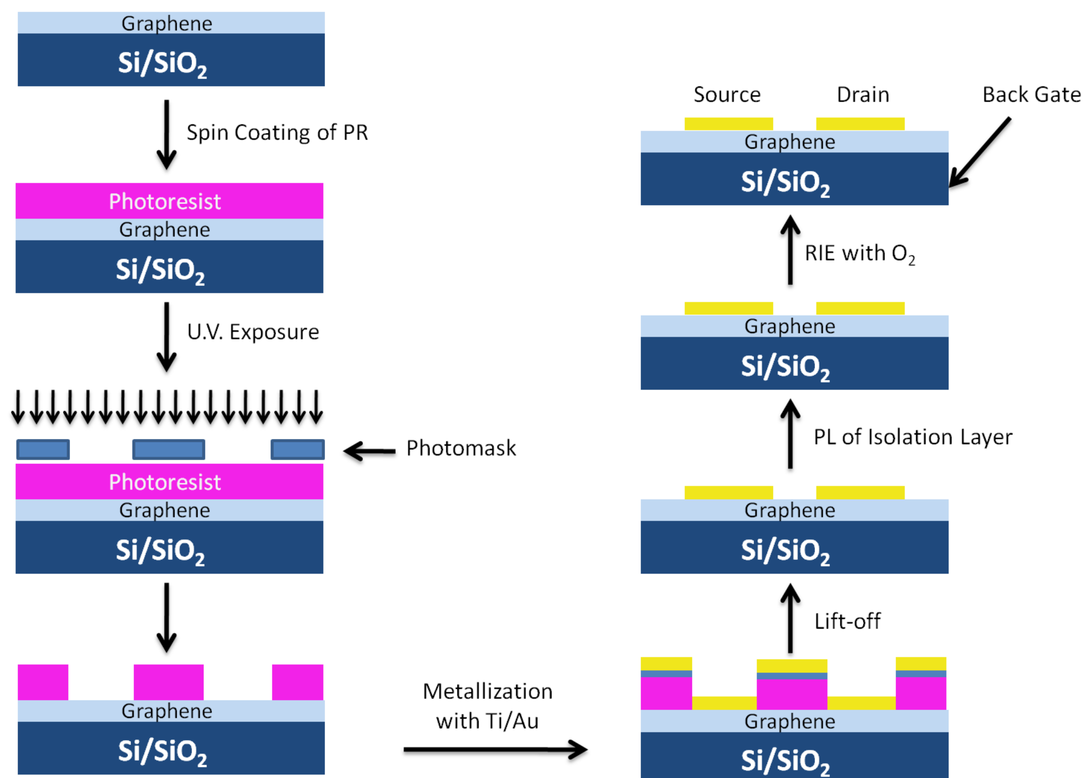


Figure 5-2. Fabrication process of graphene based FET. Transferred graphene to dielectric surface is patterned by photolithography. The photomask selectively transmits U.V. rays to pattern the DC device geometry. Ti and Au is evaporated onto the patterned graphene surface, then sacrificial photoresist layer is lifted off by acetone. In order to obtain graphene layer only between source and drain pads, an isolation layer is patterned by photolithography. Finally, remaining part of graphene outside the isolation area is etched away by reactive ion etching with O_2 plasma.

5.2. Performance of DC Field Effect Transistor

The electrical measurement of our fabricated graphene based device is performed on probe station of brand named Alessi. We used HP 4241B semiconductor parameter analyzer to measure the electrical performance of the fabricated devices. The device that we measured has channel-length of 8µm. First of all, we checked whether the device has a gate leakage. The gate current I_G vs. the gate voltage V_G characteristics of the device showed us that it has almost no gate leakage (The gate current is less than 1nA). Transfer and output characteristics of a device provide the information about the device performance and quality of the graphene layer.

The transfer curve of the device can be seen in Figure 5-2. We sweep the gate voltage from -90 V to +90 by keeping the drain bias at 1V. and source bias at 0V. The Drain current as a function of gate voltage is plotted in Figure 5-2. Drain current of 250µA is obtained at the on state and 100µA is obtained at the off state. The transfer curve shows a moderate modulation of the drain current with an I_{on}/I_{off} of around 2 which indicate that the graphene is only a few layer. Single layer graphene should provide I_{on}/I_{off} more than 3.

The output characteristics of the device are measured by sweeping the drain bias between -10V to 10 V for a constant gate voltage. We repeat the drain voltage sweep for 11 different gate bias (ranging between -90 V to 90 V) to obtain the full output characteristics. Figure 5-3 shows the measured I_dV_d curves of the device with a channel length of 8µm and channel width of 100 µm.

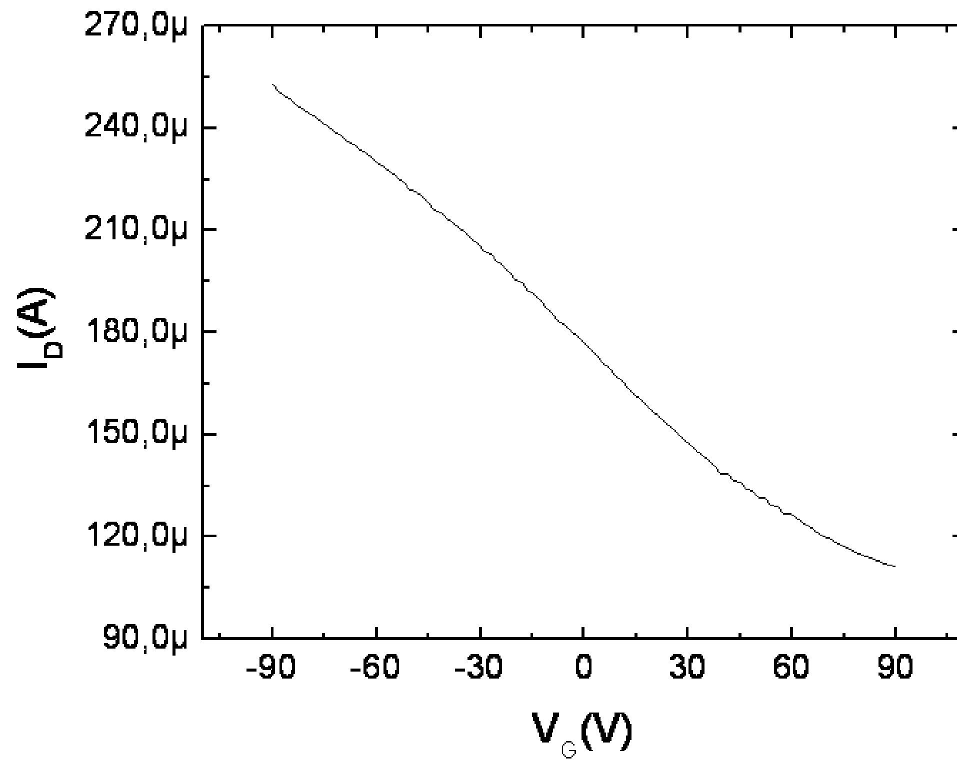


Figure 5-3. The transfer characteristics of the fabricated graphene based back gated field effect transistor. The transistor has a channel length of 8µm and channel width of 100 µm. The curve is obtained for a drain voltage of 1V. The highly doped silicon substrate is used a global gate electrode.

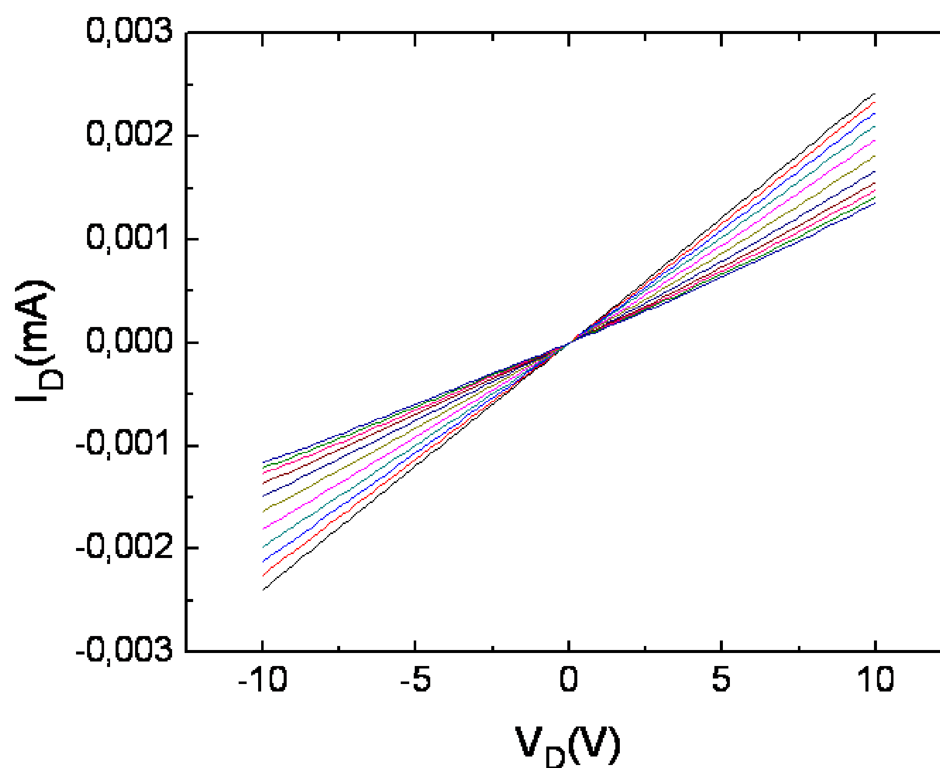


Figure 5-4. The output characteristics of the fabricated graphene based back gated field effect transistor. The transistor has a channel length of 8µm and channel width of 100 µm. The drain voltage sweep is repeated for 11 different gate voltage ranging between -90V to 90V. The highly doped silicon substrate is used a global gate electrode.

Chapter 6

Investigation of High Frequency Performance of Graphene Field Effect Transistor

This chapter will be submitted to Applied Physics Letters under the name "Investigation of High Frequency Performance of Graphene Field Effect Transistor Using a Self-Consistent Transport Model" Erçağ Pinçe, Coşkun Kocabaş.

Recent advances of chemical vapor deposition of graphene on large area substrates[13] stimulate a significant research effort searching for new applications of graphene in the field of unusual electronics such as macroelectronics[64],. Graphene can function as an effective semiconductor or a transparent conducting coating for large area displays and photovoltaic devices. Recent developments in scaling of graphene films open up new opportunities for flexible electronics. Extremely high field effect mobility of graphene together with the large area deposition process, could provide alternative solutions for the challenges of traditional organic materials. Operation at radio frequencies is one of the main challenges of the organic based field effect transistors owing to the poor field effect mobilities of organic semiconductors. Therefore radio frequency analog electronics could be an immediate high-end application of graphene.

In this chapter we provide a framework based on an analytical model for understanding the design considerations of the graphene based transistors operating at radio frequency band. Although high frequency analog electronics is a well established field for inorganic semiconducting materials, the effects of unusual transport properties of mono-atomic graphene sheets at high frequencies are widely unknown. Recent experimental studies show several demonstrations of graphene and carbon nanotube arrays for high frequency operation[65]’[8]’[40]. Cut-off frequencies of 10 GHz for carbon nanotube arrays[40]’[18]’[16] and 100 GHz for graphene[8, 9] have been achieved. Using critical design considerations, these values can be advanced by orders of magnitude. There is little in the literature that provides a simple yet quantitative model to analyze the critical design considerations of radio frequency operation of graphene based field effect transistors. This work is aiming to develop an analytical model to design a graphene based RF transistors based on diffusive transport governed by the charged impurity scattering.

6.1.Introduction

A schematic representation of a model RF transistor is shown in Figure 6-1. The transistor consists of a graphene layer printed on an insulating substrate (e.g. quartz or sapphire). The source and drain electrodes are formed on the graphene layer. A thin layer of dielectric material functions as a gate dielectric for the field effect transistor configuration. The gate electrode is formed on top of the gate dielectric. This electrode is registered with the source and drain electrodes in such a way that the parasitic capacitance and resistance are decreased.

A typical layout (common drain) of a RF transistor is more complicated than the schematic shown in the Figure because electrical measurements of these type of devices requires passive coplanar waveguide probes (ground-signal-ground configuration, GSG). The heart of RF devices however is the same with the diagram. For the model, the dielectric thickness is 50 nm and the channel length and width are 1 μm. Here, we consider the transport mechanism governed by the charged impurity scattering owing to the presence of the charged impurities on the substrate and the gate dielectric. The dielectric constant of the surrounding medium (gate dielectric and substrate) controls the effects of the impurity charges on the graphene layer. High-k dielectric materials (e.g. HfO_2) concentrate the electric field in to the dielectric material and reduce the formation of residue charges on the graphene layer. Fang et.al[66, 67] confirmed the effect of the charge screening on the charge mobility of the graphene[67]. Recent experimental results also agree with charge mobility lowering of graphene device by increasing charged impurities with potassium doping[68]. For the top gate configuration, both substrate and the gate dielectric determine the effective dielectric constant. Therefore, the substrate should have high dielectric constant or has to be coated with high-k material, such as HfO_2. A quartz wafer coated with a thin layer of HfO_2, grown by atomic layer deposition, could be a good substrate for graphene based RF transistors.

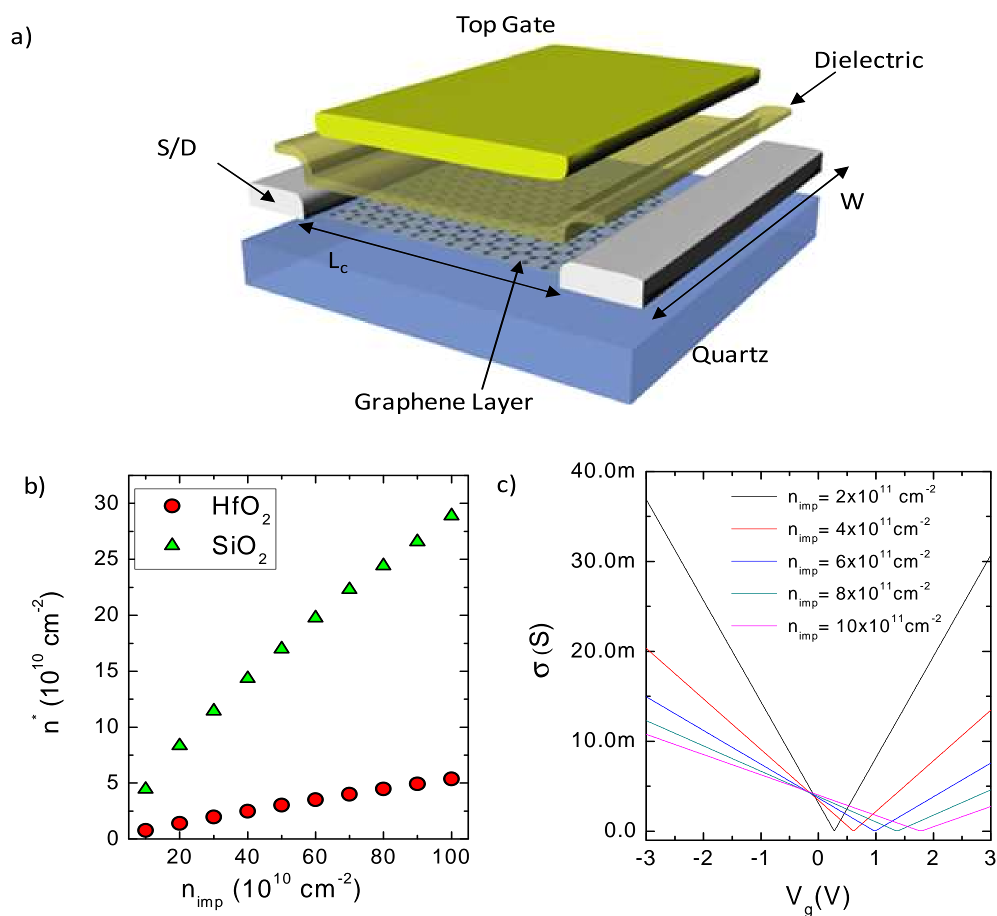


Figure 6-1. (a) Layout of a graphene based radio frequency transistor with a channel length Lc and channel width W. (b) The calculate the residue charges n^* as a function of charged impurity concentration n_{imp} for two different dielectric material $Hf0_2$ and $Si0_2$. (c) The conductivity of graphene layers as a function of gate voltage. The charged impurity concentration is scanned from $2x10^{11}$ cm^{-2} to $10x10^{11}$ cm^{-2} .

6.2. A Self-Consistent Transport Model

Here, we consider the transport mechanism governed by the charged impurity scattering owing to the presence of the charged impurities on the substrate and the gate dielectric. The dielectric constant of the surrounding medium (gate dielectric and substrate) controls the effects of the impurity charges on the graphene layer. High-k dielectric materials (e.g. HfO_2) concentrate the electric field in to the dielectric material and reduce the formation of residue charges on the graphene layer. Fang et.al[66, 67] confirmed the effect of the charge screening on the charge mobility of the graphene[67]. Recent experimental results also agree with charge mobility lowering of graphene device by increasing charged impurities with potassium doping[68]. For the top gate configuration, both substrate and the gate dielectric determine the effective dielectric constant. Therefore, the substrate should have high dielectric constant or has to be coated with high-k material, such as HfO_2. A quartz wafer coated with a thin layer of HfO_2, grown by atomic layer deposition, could be a good substrate for graphene based RF transistors. The charge transport mechanism of single layer graphene has been the focus of various theoretical and experimental studies. The unique band structure makes graphene unlike the other 2D confined electronic systems. In the present analysis of the radio frequency devices we consider a self-consistent transport model developed by S. Adam *et al.* based on a charged impurity scattering. This model explains the most of the observed electrical behavior of graphene sheets, e.g. non-universal minimum conductivity and ultrahigh mobility of suspended graphene layers. The beauty of the model is that it requires only a few empirical parameters, density of charged impurities and the distance between the impurity and graphene layer and the dielectric constant of the surrounding medium. The distance of charged impurities between graphene is effectively located around 0.1-1 nm from the graphene sheet[69]. We have analyzed the frequency

response of graphene devices in three steps. First, we have used the self consistent model[43] to calculate the residue charges n^* on the graphene layer (Fig. 6-2b). After calculating the conductivity from the residue charges, then we calculated the drain current at a given bias condition using a 2-dimensional FET model. Scanning the gate and drain bias voltages we obtained the transfer and output curves of the device. Finally using the outcome of the device model we calculate the maximum transconductance which provides the highest frequency response point. The residue charges on graphene layer n^* depends on the charge impurity concentration and the dielectric constant of the gate dielectric and the substrate. Figure 1.b shows the graph which provides the self consistent solution of the residue charge for SiO_2 and HfO_2 gate dielectrics. SiO_2 provides 6 times more residue charges on graphene layer than HfO_2 owing to the low dielectric constant. Having calculated the residue charges, we have calculated the conductivity of the graphene layer as a function of gate voltage by Equation 6-1 [43].

$$\sigma(n-\bar{n}) = \begin{cases} \frac{20e^2\, n^*}{h\, n_{imp}} & if\ n-\bar{n}>n^* \\ \frac{20e^2\, n^*}{h\, n_{imp}} & if\ n-\bar{n}>n^* \end{cases} \qquad (6\text{-}1)$$

where $\bar{n} = \frac{{n_{imp}}^2}{4n^*}$. Here the carrier concentration n on the graphene layer is used as $n = C_{ox}V_g$ where C_{ox} is the gate capacitance and V_g is the gate voltage. Figure 6-1c shows the calculated conductivity as a function of the gate voltage for impurity concentrations ranging from $2x10^{11}$ cm^{-2} to $10x10^{11}$ cm^{-2}.

For a bias point, the carrier density changes as a function of position along the graphene layer. Knowing the gate voltage dependence of the conductivity, the carrier density can be

calculated as a function of position. We have considered the constant contact resistance R_s of 1.2 kΩ between the source/drain electrodes and the graphene layer. For 2-dimensional FET, the drain current is written as [70]

$$I_d = \frac{W}{L_c}\int_0^{L_c} \sigma(x)E(x)dx = \frac{W}{L_c}\int_{V_s - R_s I_d}^{V_d - R_s I_d} \sigma(V)dV \quad (6\text{-}2)$$

Where $\sigma(x)$ is the conductivity and $E(x)$ is the electric field along the graphene layer. With a change of variable including the voltage drops at the contacts, the integral becomes a simple transcendental equation. Solving this transcendental equation using the conductivity values calculated by Eq.(6-1) provides the drain current for a given biasing condition. Figure 2a and 2b show transfer and output curves of a device with a channel length of 1 μm and channel width of 1 μm. In this calculation we have used a 50 nm HfO_2 as a gate dielectric with a dielectric constant of 16. For these calculation, the only empirical parameter that we used is impurity concentration on the dielectric and contact resistance between the electrodes and the graphene.

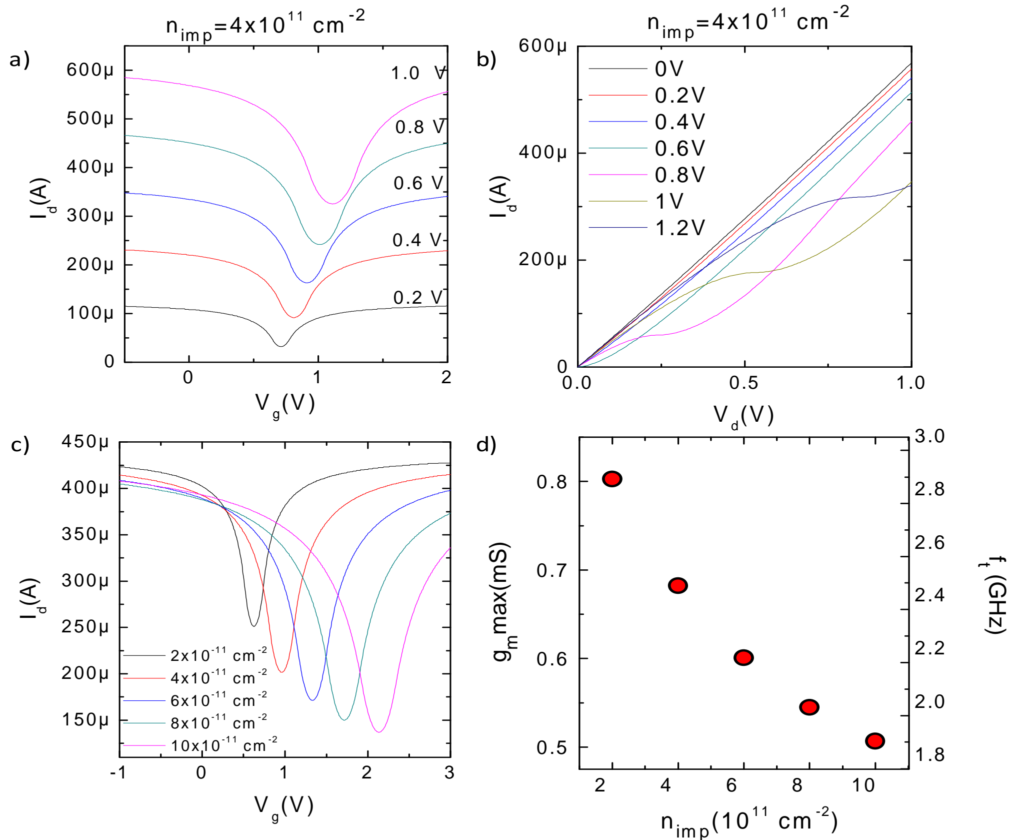


Figure 6-2**.** (a) The transfer curves for a graphene FET with a channel length of 1 μm and channel width of 1 μm. The gate dielectric used for the calculation is 50 nm HfO2. A clear ambipolar behavior and current saturation because of contact resistance is seen on the transfer curves. The Dirac point shifts to as a function of drain voltage. (b) The output curves of the same device for the gate voltage range from 0V to 1.2V. The curves in (a) and (b) are calculated for for $n=4x10^{11}$ cm^{-2} . (c) The transfer curves for the device for different charged impurity concentrations at a drain voltage of 0.6 V. (d) Calculated maximum transconductance of the device as a function of charged impurity concentration.

This framework allows us to analyze the effect of the gate dielectric material on the device performance. Figure 6-2c shows the calculated transfer curves for different charge impurity concentration. The Dirac point shifts to the higher voltages and the on/off ratio increases with increasing charge impurity concentration. The on/off ratio of the devices increases from 1.7 to 3.0 as the impurity concentration increases. Dependence of on/off ratio on the impurity concentration can be understood from the decreasing of minimum conductivity of the graphene layer as the impurity concentration increases. This behavior provides a tradeoff between transconductance and output resistance for the high frequency performance.

6.3.RF Device Performance

Cutoff frequency is defined as the frequency where the current gain is 0 dB. After cutoff frequency the drain current due to the modulation of the channel is less than the gate leakage current. Gate capacitance and the small signal transconductance of a device determine the cutoff frequency of a device as $f_t = g_m / 2\pi C_g$. Figure 6-3d shows the calculated maximum transconductance of the device and the associated cutoff frequency as function of charged impurity concentration. The parallel plate gate capacitance used for the calculation. Cleanest samples with charged impurity levels of $2\text{x}10^{11}$ have f_t around 25 GHz for 1 μm channel length. The calculated cutoff frequency decays down to 18 GHz as we increase the charged impurity concentration.

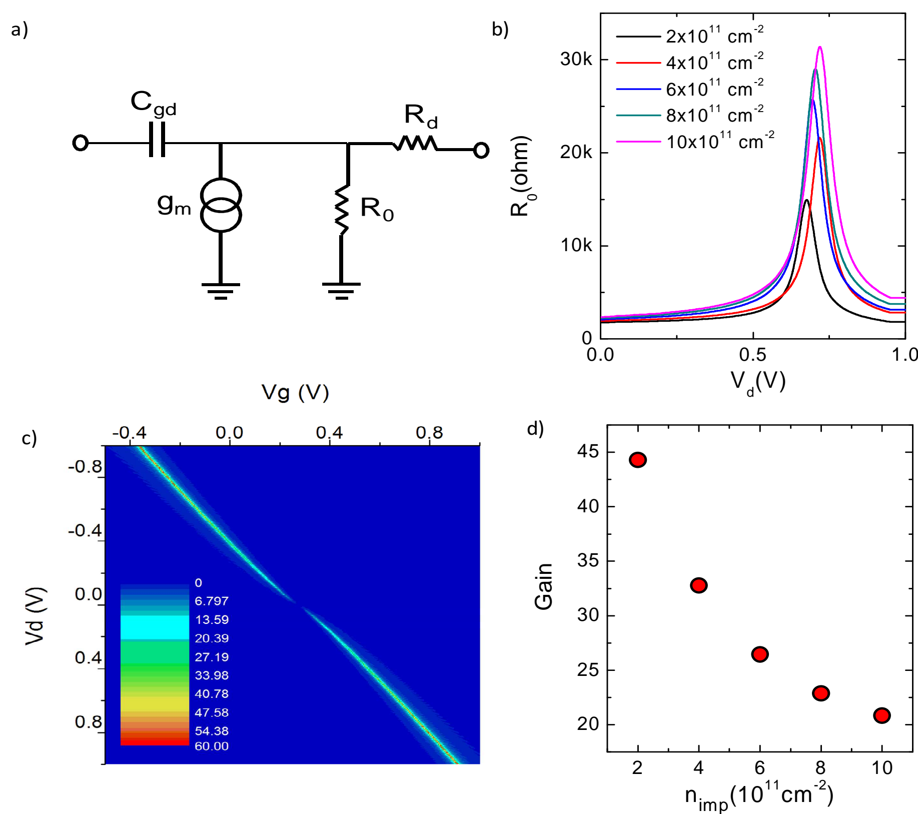


Figure 6-3(a) The simplified small signal circuit model for of the graphene FET. Here gm is transconductance ,R_0 is output resistance, R_d is drain resistance and C_{gd} is the intrinsic gate-drain capacitance. (b)The output resistance calculated from the output curves (inset in (b)) for different impurity concentration raging from the cleanest to the dirtiest sample. (c) Two-dimensional map of small signal power gain of the device. The x and y axis represents gate and drain voltages, respectively. (d) Maximum available gain of the device as a function of charged impurity concentration.

A small signal circuit model for the graphene devices is presented to understand the high frequency performance. A simplified small-signal equivalent circuit model of a graphene device is given in Figure 6-3a. C_{gd}, g_m, R_d and R_0 represent gate-drain capacitance, transconductance, drain resistance and the output resistance of the device round a bias point, respectively. We have not used the source-gate capacitance because it will be much smaller than the drain-gate capacitance at the saturation regime[18]. Graphene FETs have very small on/off ratios owing to a large minimum conductivity at the Dirac Point. This minimum conductivity limits the output resistance of the device. The output resistance, defined as $R_0 = \frac{1}{\left(\frac{\partial I_d}{\partial V_d}\right)_{V_g}}$, plays a critical role in the high frequency operation especially for the signal amplification. Figure 6-3b shows the output resistance as a function of the drain voltage. Large output resistance (~30 kΩ) can be achieved at a very narrow range of drain and gate voltages. The knowledge of output resistance and transconductance provides the power gain of the device. Power gain of a transistor used as an amplifier is another important parameter for high frequency operation. Power gain is defined as $G = g_m R_0$ where g_m is the transconductance, and R_0 is the output resistance. The highest available gain for a device with a given impurity concentration is given in Figure 4d. A gain of 45 can be achieved for the impurity concentration around $2\text{x}10^{11}\text{cm}^{-2}$.

6.4. Results and Discussion

The most striking point here is that even devices with a very poor on/off ratio can provide power gain at suitable. The results reveal that graphene transistors can be used for RF power amplifiers.

In this work we provide a simple yet quantitative framework to model the high frequency performance of graphene based field effect transistors. The model uses a self consistent charge transport mechanism based on a charge impurity scattering. The effect of contact resistance, minimum conductivity and gate dielectric is studied. Basic device considerations for analog electronic applications such as output resistance and power gain are discussed. Although graphene has very unusual device performance, radio frequency analog electronics could be an immediate high-end application of graphene.

Chapter 7

Conclusions and Future Work

In this work, we studied the chemical vapor deposition of graphene layers on copper substrates. The characterization of the grown graphene samples were performed by Raman Spectroscopy. We also developed a transfer printing technique to transfer the grown graphene layers on a dielectric substrates such as quartz. Graphene layers on dielectric substrate allowed us to fabricate field effect transistors. Graphene based back gated FETs were fabricated and their electrical performance have been characterized.

Also, we investigated high frequency limits of the graphene based devices by exploiting a self-consistent transport theory in graphene. The results showed us that graphene is very suitable for high-end applications and can be used as a RF power amplifier.

By this vision, in near future we are going to research the fabrication of graphene based high frequency operating device. Afterwards, we will research the area of graphene based devices which can fully operate in RF region and some applications will be studied.

Bibliography

1. "Emerging Research Devices," (The International Technology Roadmap for Semiconductors, 2009).
2. B.G.Streetman, *Solid State Electronic Devices* (Prentice-Hall International,Inc., New Jersey, 1995).
3. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," Science **306**, 666-669 (2004).
4. Y. B. Zhang, Y. W. Tan, H. L. Stormer, and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," Nature **438**, 201-204 (2005).
5. A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," Reviews of Modern Physics **81**, 109-162 (2009).
6. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, J. H. Ahn, P. Kim, J. Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," Nature **457**, 706-710 (2009).
7. Y. Lee, S. Bae, H. Jang, S. Jang, S. E. Zhu, S. H. Sim, Y. I. Song, B. H. Hong, and J. H. Ahn, "Wafer-Scale Synthesis and Transfer of Graphene Films," Nano Letters **10**, 490-493 (2010).
8. Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," Science **327**, 662-662 (2010).
9. Y. M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of Graphene Transistors at Gigahertz Frequencies," Nano Letters **9**, 422-426 (2009).
10. L. Liao, J. W. Bai, Y. Q. Qu, Y. C. Lin, Y. J. Li, Y. Huang, and X. F. Duan, "High-kappa oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors," Proceedings of the National Academy of Sciences of the United States of America **107**, 6711-6715 (2010).
11. S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant intrinsic carrier mobilities in graphene and its bilayer," Physical Review Letters **100** (2008).

12. X. Wang, and H. Dai, "Etching and narrowing of graphene from the edges," Nat Chem **2**, 661-665.
13. X. S. Li, W. W. Cai, J. H. An, S. Kim, J. Nah, D. X. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," Science **324**, 1312-1314 (2009).
14. A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," Nano Letters **9**, 30-35 (2009).
15. S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," Nat Nano **advance online publication**.
16. S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," Nature Nanotechnology **2**, 230-236 (2007).
17. P. Avouris, Z. H. Chen, and V. Perebeinos, "Carbon-based electronics," Nature Nanotechnology **2**, 605-615 (2007).
18. C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. N. Ho, H. S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, S. V. Rotkin, and J. A. Rogers, "High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes," Nano Letters **9**, 1937-1943 (2009).
19. L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes," Applied Physics Letters **94**, 3 (2009).
20. K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook, and S. E. Coe, "Diamond FET using high-quality polycrystalline diamond with f(T) of 45 GHz and f(max) of 120 GHz," Ieee Electron Device Letters **27**, 570-572 (2006).
21. C. Kittel, *Introduction to Solid State Physics* (John Wiley, 2005).
22. R. S. Balmer, J. R. Brandon, S. L. Clewes, H. K. Dhillon, J. M. Dodson, I. Friel, P. N. Inglis, T. D. Madgwick, M. L. Markham, T. P. Mollart, N. Perkins, G. A. Scarsbrook, D. J. Twitchen, A. J. Whitehead, J. J. Wilman, and S. M. Woollard, "Chemical vapour deposition synthetic diamond: materials, technology and applications," Journal of Physics-Condensed Matter **21**, 23 (2009).
23. F. P. Bundy, H. T. Hall, H. M. Strong, and R. H. Wentorf, "Man-Made Diamonds," Nature **176**, 51-55 (1955).

24. A. Cheesman, J. A. Smith, M. N. R. Ashfold, N. Langford, S. Wright, and G. Duxbury, "Application of a quantum cascade laser for time-resolved, in situ probing of CH4/H-2 and C2H2/H-2 gas mixtures during microwave plasma enhanced chemical vapor deposition of diamond," Journal of Physical Chemistry A **110**, 2821-2828 (2006).
25. J. Isberg, J. Hammersberg, E. Johansson, T. Wikstrom, D. J. Twitchen, A. J. Whitehead, S. E. Coe, and G. A. Scarsbrook, "High carrier mobility in single-crystal plasma-deposited diamond," Science **297**, 1670-1672 (2002).
26. J. G. Felbinger, M. V. S. Chandra, Y. Sun, L. F. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis, and F. Ejeckam, "Comparison of GaNHEMTs on diamond and SiC substrates," Ieee Electron Device Letters **28**, 948-950 (2007).
27. H. Kawarada, M. Aoki, and M. Ito, "ENHANCEMENT-MODE METAL-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS USING HOMOEPITAXIAL DIAMONDS," Applied Physics Letters **65**, 1563-1565 (1994).
28. M. Kasu, K. Ueda, Y. Yamauchi, A. Tallaire, and T. Makimoto, "Diamond-based RF power transistors: Fundamentals and applications," Diamond and Related Materials **16**, 1010-1015 (2007).
29. R. S. G. D. M.S.Dresselhaus, *Physical Properties of Carbon Nanotubes* (Imperial College Press, 1998).
30. P. G. C. P.Avouris, *The Electronic Properties of Carbon Nanotubes* (Elsevier, Amsterdam, 2008).
31. C. Rutherglen, D. Jain, and P. Burke, "Nanotube electronics for radiofrequency applications," Nature Nanotechnology **4**, 811-819 (2009).
32. P. C. Collins, M. S. Arnold, and P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," Science **292**, 706-709 (2001).
33. G. Y. Zhang, P. F. Qi, X. R. Wang, Y. R. Lu, X. L. Li, R. Tu, S. Bangsaruntip, D. Mann, L. Zhang, and H. J. Dai, "Selective etching of metallic carbon nanotubes by gas-phase reaction," Science **314**, 974-977 (2006).
34. C. M. Yang, K. H. An, J. S. Park, K. A. Park, S. C. Lim, S. H. Cho, Y. S. Lee, W. Park, C. Y. Park, and Y. H. Lee, "Preferential etching of metallic single-walled carbon nanotubes with small diameter by fluorine gas," Physical Review B **73** (2006).
35. M. Meyyappan, L. Delzeit, A. Cassell, and D. Hash, "Carbon nanotube growth by PECVD: a review," Plasma Sources Science & Technology **12**, 205-216 (2003).
36. P. J. F. Harris, "Solid state growth mechanisms for carbon nanotubes," Carbon **45**, 229-239 (2007).
37. S. J. Kang, C. Kocabas, H. S. Kim, Q. Cao, M. A. Meitl, D. Y. Khang, and J. A. Rogers, "Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic, applications," Nano Letters **7**, 3343-3348 (2007).

38. C. Rutherglen, and P. Burke, "Carbon nanotube radio," Nano Letters **7**, 3296-3299 (2007).
39. K. Jensen, J. Weldon, H. Garcia, and A. Zettl, "Nanotube radio," Nano Letters **7**, 3508-3511 (2007).
40. C. Kocabas, H. S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, S. V. Krishnaswamy, and H. Zhang, "Radio frequency analog electronics based on carbon nanotube transistors," Proceedings of the National Academy of Sciences of the United States of America **105**, 1405-1409 (2008).
41. A. K. Geim, and K. S. Novoselov, "The rise of graphene," Nature Materials **6**, 183-191 (2007).
42. S. M. M. Dubois, Z. Zanolli, X. Declerck, and J. C. Charlier, "Electronic properties and quantum transport in Graphene-based nanostructures," European Physical Journal B **72**, 1-24 (2009).
43. S. Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma, "A self-consistent theory for graphene transport," Proceedings of the National Academy of Sciences of the United States of America **104**, 18392-18397 (2007).
44. X. Liang, Z. Fu, and S. Y. Chou, "Graphene transistors fabricated via transfer-printing in device active-areas on large wafer," Nano Letters **7**, 3840-3844 (2007).
45. L. Song, L. J. Ci, W. Gao, and P. M. Ajayan, "Transfer Printing of Graphene Using Gold Film," Acs Nano **3**, 1353-1356 (2009).
46. M. J. Allen, V. C. Tung, L. Gomez, Z. Xu, L. M. Chen, K. S. Nelson, C. W. Zhou, R. B. Kaner, and Y. Yang, "Soft Transfer Printing of Chemically Converted Graphene," Advanced Materials **21**, 2098-2102 (2009).
47. X. G. Liang, A. S. P. Chang, Y. G. Zhang, B. D. Harteneck, H. Choo, D. L. Olynick, and S. Cabrini, "Electrostatic Force Assisted Exfoliation of Prepatterned Few-Layer Graphenes into Device Sites (vol 9, pg 467, 2009)," Nano Letters **9**, 919-919 (2009).
48. A. A. Green, and M. C. Hersam, "Solution Phase Production of Graphene with Controlled Thickness via Density Differentiation," Nano Letters **9**, 4031-4036 (2009).
49. C. Berger, Z. M. Song, X. B. Li, X. S. Wu, N. Brown, C. Naud, D. Mayou, T. B. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," Science **312**, 1191-1196 (2006).
50. H. Huang, W. Chen, S. Chen, and A. T. S. Wee, "Bottom-up Growth of Epitaxial Graphene on 6H-SiC(0001)," Acs Nano **2**, 2513-2518 (2008).
51. S. Unarunotai, Y. Murata, C. E. Chialvo, H. S. Kim, S. MacLaren, N. Mason, I. Petrov, and J. A. Rogers, "Transfer of graphene layers grown on SiC wafers to other

substrates and their integration into field effect transistors," Applied Physics Letters **95** (2009).

52. J. W. Bai, X. Zhong, S. Jiang, Y. Huang, and X. F. Duan, "Graphene nanomesh," Nature Nanotechnology **5**, 190-194 (2010).

53. L. Y. Jiao, L. Zhang, X. R. Wang, G. Diankov, and H. J. Dai, "Narrow graphene nanoribbons from carbon nanotubes," Nature **458**, 877-880 (2009).

54. J. W. Bai, X. F. Duan, and Y. Huang, "Rational Fabrication of Graphene Nanoribbons Using a Nanowire Etch Mask," Nano Letters **9**, 2083-2087 (2009).

55. Z. Y. Liu, V. Srot, and J. C. Yang, "Self-assembled crystalline silicon carbide Y junctions by coalescence of nucleated iron catalysts," Applied Physics Letters **96** (2010).

56. Q. K. Yu, J. Lian, S. Siriponglert, H. Li, Y. P. Chen, and S. S. Pei, "Graphene segregated on Ni surfaces and transferred to insulators," Applied Physics Letters **93** (2008).

57. X. S. Li, W. W. Cai, L. Colombo, and R. S. Ruoff, "Evolution of Graphene Growth on Ni and Cu by Carbon Isotope Labeling," Nano Letters **9**, 4268-4272 (2009).

58. M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams, "Atomic structure of graphene on SiO2," Nano Letters **7**, 1643-1648 (2007).

59. X. S. Li, Y. W. Zhu, W. W. Cai, M. Borysiak, B. Y. Han, D. Chen, R. D. Piner, L. Colombo, and R. S. Ruoff, "Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes," Nano Letters **9**, 4359-4363 (2009).

60. A. Ismach, C. Druzgalski, S. Penwell, A. Schwartzberg, M. Zheng, A. Javey, J. Bokor, and Y. G. Zhang, "Direct Chemical Vapor Deposition of Graphene on Dielectric Surfaces," Nano Letters **10**, 1542-1548 (2010).

61. M. S. Dresselhaus, A. Jorio, M. Hofmann, G. Dresselhaus, and R. Saito, "Perspectives on Carbon Nanotubes and Graphene Raman Spectroscopy," Nano Letters **10**, 751-758 (2010).

62. L. M. Malard, M. A. Pimenta, G. Dresselhaus, and M. S. Dresselhaus, "Raman spectroscopy in graphene," Physics Reports-Review Section of Physics Letters **473**, 51-87 (2009).

63. A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, "Raman spectrum of graphene and graphene layers," Physical Review Letters **97**, 4 (2006).

64. J. A. Rogers, "Electronic materials - Making graphene for macroelectronics," Nature Nanotechnology **3**, 254-255 (2008).

65. F. N. Xia, T. Mueller, Y. M. Lin, A. Valdes-Garcia, and P. Avouris, "Ultrafast graphene photodetector," Nature Nanotechnology **4**, 839-843 (2009).

66. F. Chen, J. L. Xia, and N. J. Tao, "Ionic Screening of Charged-Impurity Scattering in Graphene," Nano Letters **9**, 1621-1625 (2009).

67. F. Chen, J. L. Xia, D. K. Ferry, and N. J. Tao, "Dielectric Screening Enhanced Performance in Graphene FET," Nano Letters **9**, 2571-2574 (2009).
68. J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, "Charged-impurity scattering in graphene," Nature Physics **4**, 377-381 (2008).
69. S. Adam, and S. Das Sarma, "Transport in suspended graphene," Solid State Communications **146**, 356-360 (2008).
70. I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, topgated graphene field-effect transistors," Nature Nanotechnology **3**, 654-659 (2008).