Multi-Input Multi-Output Deletion Channel

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Abstract—We describe a new channel model suitable in certain applications, namely the multi-input multi-output (MIMO) deletion channel. This channel models the scenarios where multiple transmitters and receivers suffering from synchronization errors are employed. We then consider a coding scheme over such channels based on a serial concatenation of a low-density parity check (LDPC) code, a marker code and a layered space-time code. We design two detectors operating at the bit level which jointly achieve synchronization for the deletion channel (with the help of the marker code) and detection for the MIMO channel. Utilizing the proposed detector together with an LDPC code with powerful error-correction capabilities, we demonstrate that reliable transmission over a MIMO deletion channel is feasible.

Index Terms—MIMO, deletion channel, marker codes, LDPC codes.

I. INTRODUCTION

CHANNELS with synchronization errors due to the mismatches between the transmitter and receiver clocks can be modeled using bit drop-outs (deletions) and insertions [1]. There has been significant work to understand such channels for over fifty years including capacity upper and lower bound computations [2]–[4], and practical channel coding schemes [5], [6]. The previous works in the literature focus exclusively on the case where there is a single transmitter and a single receiver. On the other hand there are many applications in which multiple-transmit and multiple-receive elements are employed [7]. The main objective of this letter is to bring about a new channel modeling synchronization errors by also considering possible mismatches between different transmit and receive element pairs, and to consider a practical channel coding solution that can be employed for reliable communication. Specific focus is on the case of deletion type synchronization errors (i.e., the MIMO deletion channel) with the understanding that incorporation of insertion type errors is also possible in a similar manner.

The MIMO deletion channel model we advocate is motivated by some practical digital communications applications, e.g., multitrack bit-patterned media recoding (BPMR) systems [8], [9]. In this recording technology, the medium is prepatterned with magnetically stable (small) islands which suffer from imperfect synchronization. Furthermore, synchronization of the islands in the parallel tracks are not guaranteed. During the writing process, the signals are recorded

in multiple tracks and synchronization errors occur due to possible imperfect alignment between the write head and the magnetic islands [10]. Assume that there are M heads reading N tracks simultaneously, yielding an $N \times M$ MIMO channel. Combining the errors occurring in the write and read processes, a multitrack BPMR system can be viewed as the cascade of a deletion channel and an $N \times M$ MIMO channel. A different example of the MIMO deletion channel can be given in the context of wireless sensor networks. In a wireless sensor network, due to the power consumption constraints and other hardware limitations [11], perfect synchronization may not be feasible among different sensor nodes. When multiple sensors communicate simultaneously (over a multiple access channel) with one or more receivers, each transmitted sequence may experience deletion events independently from the other transmissions, and the corresponding channel model becomes a MIMO channel with deletion errors. More precisely, the resulting channel would be an asynchronous multiple access channel; however, to avoid complications related to the multi-user communications setting, we focus only on the centralized scenario with mismatched transmitters and receivers.

We consider an $N \times M$ MIMO channel with independent and identically distributed (i.i.d.) deletion errors. Specifically, during transmission, symbols may be deleted independently of each other (both spatially and temporally). This model is an extension of the i.i.d. deletion channel model for the single-input single-output communications scenario considered in various papers in the literature (see [2]). We further consider modulated symbols (using binary phase shift keying (BPSK)) and the effects of the electronic noise at the receiver(s). To communicate reliably over the MIMO deletion channel, we adopt a coding scheme, which is a serial concatenation of an LDPC code, a marker code [6] and a layered space-time code, and design two channel detectors. At the receiver, a bit-level maximum-a-posteriori (MAP) detector is deployed which jointly achieves synchronization for the deletion channel and detection for the MIMO channel. The resulting soft information is then fed to the message passing decoder (for the LDPC code). We also propose an alternative detector exploring the idea of interference cancellation (IC) which enables a layer-by-layer detection, and therefore, existing synchronization algorithms (such as the one in [6]) can be directly utilized.

The letter is organized as follows. The system model including the specific channel model and the coding scheme is described in Section II. In Section III, two different channel detectors are proposed. Simulation results are provided in Section IV, and concluding remarks are given in Section V.

II. SYSTEM MODEL

In this section, we describe the details of the MIMO deletion channel, focusing, particularly, on the case of $N = 2$ and

Fig. 1.   Channel model.

Fig. 2.   Example of state transitions on the trellis diagram.
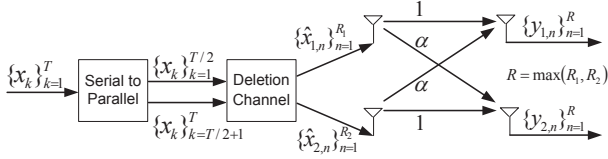
$M = 2$ with the stipulation that extensions to arbitrary N, M are straightforward. The channel model, shown in Fig. 1, is the concatenation of a deletion channel with a 2×2 MIMO channel. The deletion channel is a standard i.i.d. deletion channel with symbol deletion probability P_d. For the MIMO channel, if the transmitted sequence is $\mathbf{x}$, the received signal is given by $\mathbf{y} = \mathbf{A} \cdot \mathbf{x}$, where

$$\mathbf{A} = \begin{bmatrix} 1 & \alpha \\ \alpha & 1 \end{bmatrix} \qquad (1)$$

whose ij-th entry is the channel gain from the j-th transmitter to the i-th receiver. The matrix $\mathbf{A}$ is assumed to be deterministic and symmetric for simplicity. For instance, the coefficient α could represent the amount of intertrack interference (ITI) in a magnetic recording channel.

As for the proposed channel coding solution, we adopt a concatenated coding scheme similar to the one in [6], which consists of the interleaved serial concatenation of an outer LDPC code with an inner marker code and a layered space-time code. Specifically, the information bits are first encoded by an LDPC code, then marker bits are periodically inserted, e.g., by inserting a two-bit marker "01" after every 10 LDPC-coded bits. Assume that the resulting bit sequence is of length T. This sequence is first modulated using BPSK, i.e., $\mathbf{x}_1^T = \{x_k\}_{k=1}^T$, and then converted into two parallel subsequences, each with length $T/2$. Due to the i.i.d. deletions, random symbols get deleted resulting in a total number of R_1 symbols in the first subsequence $\hat{\mathbf{x}}_1$ and R_2 symbols in the second subsequence $\hat{\mathbf{x}}_2$, where R_1 and R_2 are random variables (both binomial with parameters $T/2$ and P_d). The received signals at the two receive elements are

$$\mathbf{y}_1 = \hat{\mathbf{x}}_1 + \alpha \hat{\mathbf{x}}_2 + \mathbf{z}_1, \quad \mathbf{y}_2 = \alpha \hat{\mathbf{x}}_1 + \hat{\mathbf{x}}_2 + \mathbf{z}_2, \qquad (2)$$

where $\mathbf{z}_1, \mathbf{z}_2$ are independent white Gaussian noise sequences with zero mean and variance σ^2. Note that $\hat{\mathbf{x}}_1$ and $\hat{\mathbf{x}}_2$ may be of different lengths, i.e., $R_1 \neq R_2$, therefore, we define their vector sum as

$$\text{if } \mathbf{a} + \mathbf{b} = \mathbf{c}, \quad \text{then } c_k = \begin{cases} a_k + b_k & \text{if } k \leq \min(|\mathbf{a}|, |\mathbf{b}|) \\ a_k & \text{if } |\mathbf{b}| < k \leq |\mathbf{a}| \\ b_k & \text{if } |\mathbf{a}| < k \leq |\mathbf{b}| \end{cases},$$

where k and $|\cdot|$ represent the element index and the length of the vector, respectively.

III. DETECTION ALGORITHMS FOR MIMO CHANNELS WITH DELETIONS

At the receiver side, a soft-output channel detection algorithm is first executed to re-gain synchronization in the received sequence and after being deinterleaved, the soft information is fed to the outer decoder, which generates estimates
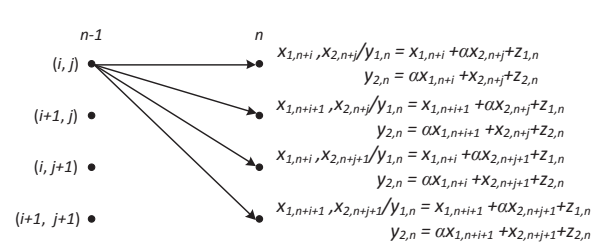
of the information bits via a message passing algorithm. In this section, we propose two solutions for the channel detection algorithm at the bit level, which generates soft information on the transmitted bits, i.e., the log-likelihood ratio (LLR) $\log\left\{\frac{P(x_k=1|\mathbf{y}_1,\mathbf{y}_2)}{P(x_k=-1|\mathbf{y}_1,\mathbf{y}_2)}\right\}$ for $k \in \{1, \ldots, T\}$. The first one is the MAP detector, which jointly achieves synchronization and channel detection. The second one provides a low-complexity alternative, which utilizes the idea of interference cancellation.

A. Joint MAP Detection Algorithm

The joint MAP detector generates soft information for all the LPDC-coded bits based on the received signals $\mathbf{y}_1 = [y_{1,1}, y_{1,2}, \ldots, y_{1,R}]$ and $\mathbf{y}_2 = [y_{2,1}, y_{2,2}, \ldots, y_{2,R}]$, where $R = \max(R_1, R_2)$. Similar to the general forward backward algorithm (FBA) [12], we define the state of the trellis to be $s_n = (d_{1,n}, d_{2,n})$, where $d_{i,n}$ denotes the total number of deletions for the i-th stream of bits at time n (i.e., by the time the n-th symbol in $\mathbf{y}_i$ is received), $i = 1, 2$. An example of state transitions is shown in Fig. 2.

Defining $\mathbf{Y}_1^R = \begin{bmatrix} \mathbf{y}_1 \\ \mathbf{y}_2 \end{bmatrix}$, we first express the forward and backward quantities as

$$\alpha_n(s_n) = P\big(s_n = (d_{1,n}, d_{2,n}), \mathbf{Y}_1^n\big), \qquad (3)$$

$$\beta_n(s_n) = P\big(\mathbf{Y}_{n+1}^R | s_n = (d_{1,n}, d_{2,n})\big), \qquad (4)$$

which can be calculated by means of the following recursion:

$$\alpha_n(s_n) = \sum_{s_{n-1}} P\big(s_{n-1} = (d_{1,n-1}, d_{2,n-1}), s_n, \mathbf{Y}_1^{n-1}, \mathbf{Y}_n\big)$$
$$= \sum_{s_{n-1}} P\big(s_n, \mathbf{Y}_n | s_{n-1} = (d_{1,n-1}, d_{2,n-1})\big) \alpha_{n-1}(s_{n-1}),$$
$$(5)$$

$$\beta_n(s_n) = \sum_{s_{n+1}} P\big(\mathbf{Y}_{n+1}, \mathbf{Y}_{n+2}^R, s_{n+1} = (d_{1,n+1}, d_{2,n+1}) | s_n\big)$$
$$= \sum_{s_{n+1}} P\big(s_{n+1} = (d_{1,n+1}, d_{2,n+1}), \mathbf{Y}_{n+1} | s_n\big) \beta_{n+1}(s_{n+1}),$$
$$(6)$$

where $\mathbf{Y}_n = [y_{1,n}, y_{2,n}]^T$ is the n-th column in $\mathbf{Y}$. By exploiting the "frame synchronization" assumption [6], the forward recursion can be initialized by setting

$$\alpha_0(s_0) = \begin{cases} 1, & \text{if } s_0 = (0,0), \\ 0, & \text{else.} \end{cases} \qquad (7)$$

Similarly for the backward recursion, we have

$$\beta_R(s_R) = \begin{cases} 1, & \text{if } s_R = (T/2 - R_1, T/2 - R_2), \\ 0, & \text{else.} \end{cases} \quad (8)$$

Define $\gamma_n(s_{n-1}, s_n) = P(s_n, \mathbf{Y}_n | s_{n-1})$, where $s_n = (d_{1,n}, d_{2,n})$ and $s_{n-1} = (d_{1,n-1}, d_{2,n-1})$. It is straightforward to show that

$$\gamma_n(s_{n-1}, s_n) = P(\mathbf{Y}_n | s_{n-1}, s_n) P(s_n | s_{n-1}), \quad (9)$$

where

$$P(s_n | s_{n-1}) = P_d^{d_{1,n} + d_{2,n} - d_{1,n-1} - d_{2,n-1}} (1 - P_d)^2, \quad (10)$$

if $d_{1,n} \geq d_{1,n-1}$, $d_{2,n} \geq d_{2,n-1}$, and 0 otherwise. Also

$$
\begin{aligned}
& P(\mathbf{Y}_n | s_{n-1}, s_n) \\
&= \sum_{i,j=\pm 1} P(\mathbf{Y}_n | x_{1,n+d_{1,n}} = i, x_{2,n+d_{2,n}} = j) \\
& \qquad \cdot P(x_{1,n+d_{1,n}} = i) P(x_{2,n+d_{2,n}} = j) \\
&= \frac{1}{2\pi\sigma^2} \sum_{i,j=\pm 1} \exp\left\{ -\frac{(y_{1,n} - (i + \alpha j))^2}{2\sigma^2} \right\} P_1(i) \\
& \qquad \cdot \exp\left\{ -\frac{(y_{2,n} - (\alpha i + j))^2}{2\sigma^2} \right\} P_2(j). \quad (11)
\end{aligned}
$$

where $P_1(i) = P(x_{1,n+d_{1,n}} = i)$ and $P_2(j) = P(x_{2,n+d_{2,n}} = j)$. They are equal to 0 or 1 for the marker bits and 0.5 for the LDPC-coded bits.

Having the forward and backward quantities, it is easy to show the following equations:

$$
\begin{aligned}
P(\mathbf{Y}_1^R | x_k) = \sum_{s_n} \sum_{s_{n-1}} \alpha_{n-1}(s_{n-1}) P(s_n | s_{n-1}) \\
\cdot P(\mathbf{Y}_n | s_{n-1}, s_n, x_k) \beta_n(s_n), \quad (12)
\end{aligned}
$$

where $n = k - d$, $d = d_{n,2}$ if $k > \frac{T}{2}$ and $d = d_{n,1}$ otherwise. Also, we have

$$
P(\mathbf{Y}_n | s_{n-1}, s_n, x_k)
$$

$$
= \begin{cases}
\frac{1}{2\pi\sigma^2} \sum_{i=\pm 1} \exp\left\{ -\frac{(y_{1,n} - (i + \alpha x_k))^2}{2\sigma^2} \right\} \\
\quad \cdot \exp\left\{ -\frac{(y_{2,n} - (\alpha i + x_k))^2}{2\sigma^2} \right\} P_1(i) \\
\qquad\qquad\qquad\qquad\qquad , \quad \text{if } k > \frac{T}{2}, \\
\frac{1}{2\pi\sigma^2} \sum_{i=\pm 1} \exp\left\{ -\frac{(y_{1,n} - (x_k + \alpha i))^2}{2\sigma^2} \right\} \\
\quad \cdot \exp\left\{ -\frac{(y_{2,n} - (\alpha x_k + i))^2}{2\sigma^2} \right\} P_2(i) \\
\qquad\qquad\qquad\qquad\qquad , \quad \text{else.}
\end{cases}
$$

After obtaining $P(\mathbf{Y}_1^R | x_k)$, we can compute the LLR $\log\left\{ \frac{P(x_k=1 | \mathbf{Y}_1^R)}{P(x_k=-1 | \mathbf{Y}_1^R)} \right\}$ (assuming equally likely LDPC-coded bits).

B. Separate Detection with Interference Cancellation

In order to apply IC with iterative decoding, the system model is slightly different from the previous case. Instead of choosing one LDPC code and a serial-to-parallel converter, we select two LDPC codes with the same length to be transmitted as the two parallel bit streams. Two IC schemes are considered, as described in detail below.

1) IC with non-decoded bits: Using the QR decomposition [7], we can write the received sequences as

$$\mathbf{Y}_1^R = \begin{bmatrix} 1 & \alpha \\ \alpha & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{\mathbf{x}}_1 \\ \hat{\mathbf{x}}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{z}_1 \\ \mathbf{z}_2 \end{bmatrix} = \mathbf{QR} \begin{bmatrix} \hat{\mathbf{x}}_1 \\ \hat{\mathbf{x}}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{z}_1 \\ \mathbf{z}_2 \end{bmatrix}, \quad (13)$$

where $\mathbf{R}$ is a 2×2 upper triangular matrix and $\mathbf{Q}$ is a 2×2 unitary matrix with $\mathbf{Q}^H \mathbf{Q} = \mathbf{I}_2$.

Let us left-multiply $\mathbf{Y}_1^R$ with $\mathbf{Q}^H$, which gives

$$\hat{\mathbf{Y}} = \mathbf{Q}^H \mathbf{Y}_1^R = \mathbf{R} \cdot \begin{bmatrix} \hat{\mathbf{x}}_1 \\ \hat{\mathbf{x}}_2 \end{bmatrix} + \hat{\mathbf{Z}}, \quad (14)$$

where $\hat{\mathbf{Z}} = \mathbf{Q}^H \begin{bmatrix} \mathbf{z}_1 \\ \mathbf{z}_2 \end{bmatrix}$. Since $\mathbf{R}$ is an upper triangular matrix, the second row in $\hat{\mathbf{Y}}$, $\hat{\mathbf{y}}_2$, solely consists of the transmitted sequence from the second layer. Therefore, the MAP detection algorithm in [6] can be directly applied to generate the soft information for the outer LDPC decoder[1].

For the first bit stream, an estimate of $\hat{\mathbf{x}}_2$ (as a hard decision) is first made based on $\hat{\mathbf{y}}_2$. Then, it is multiplied by the off-diagonal coefficient α and subtracted from $\mathbf{y}_1$. If all the decisions on $\hat{\mathbf{x}}_2$ are correctly made, the interference from the second stream is cancelled out and the same decoding procedure as in [6] can be performed.

2) IC with decoded bits: The interference cancellation scheme in the previous subsection does not utilize the error-correction capability offered by the outer LDPC decoder. In the following, we consider an IC scheme where the LDPC decoder is integrated into the process.

Let $\tilde{\mathbf{x}}_2$ be the final LDPC decoding output of the coded bits transmitted as the second stream, and $LLR(\mathbf{x}_2)$ be the vector of the corresponding log-likelihood ratios generated by the MAP detector. We group $\tilde{\mathbf{x}}_2$ into consecutive blocks, each consisting of all the LDPC-coded bits between two adjacent markers. The blocks of bits with successful transmissions, i.e., when no deletions occur, are marked "good", while the remaining blocks of bits are determined to be "contaminated" by deletions and are not used in the IC process. The positions of deletion errors can be found by identifying when the LLR values are close to zero, e.g., by obtaining the average of absolute values of the LLRs for each block and making a decision on the presence of deletion errors by comparing this value to a pre-determined threshold. Recall that without deletion errors, the mean of the absolute LLR value is $2/\sigma^2$, and therefore, we set the threshold to be $\eta \cdot 2/\sigma^2$, where $0 < \eta < 1$. The positions of these blocks in the received sequence are then estimated as [5]

$$\hat{k} = \arg\max_k \alpha_n(k) \beta_n(k), \quad (15)$$

where $\alpha_n(k)$ and $\beta_n(k)$ are the forward/backward quantities defined in the FBA in [6][2], n is the index of the last bit of the previous block in the transmitted sequence and k is the index of the corresponding received bit. Finally, the sequence to be subtracted from $\mathbf{y}_1$ is generated by substituting the bits in the hard decision of $\hat{\mathbf{x}}_2$ with the "good" bits from $\tilde{\mathbf{x}}_2$ (the starting positions are estimated using (15)).

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[1]A slight change in the algorithm is needed, since [6] only considers substitution-type errors instead of additive white Gaussian noise.

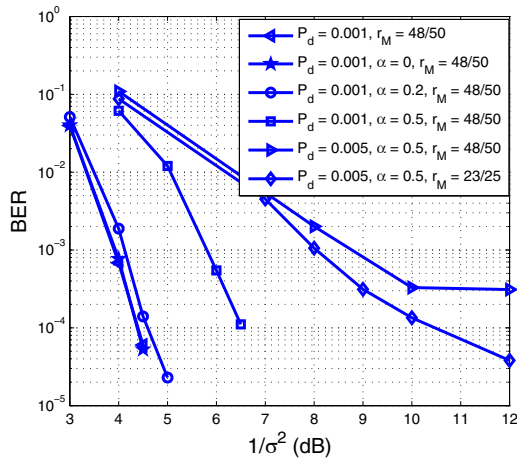[2]The definitions are different from the ones in Section III-A.

Fig. 3.   Error rate performance with various P_d, α and marker code rate.

Fig. 4.   Error rate performance for different IC schemes.

When $\tilde{\mathbf{x}}_1$ is obtained, this information can also be utilized to cancel the interference for the second bit stream. The same procedure follows and iterative decoding between the first and the second data streams can be performed.

IV. SIMULATION RESULTS

In this section, we consider an example of the proposed coding scheme with the aim of demonstrating reliable communication through the MIMO deletion channel. In particular, we utilize a $(3001, 2000)$ LDPC code and two marker codes with rates $r_M = 23/25$ and $48/50$, obtained by inserting a two-bit marker "01" every 23 or 48 LDPC-coded bits. Utilizing the joint detection algorithm, in Fig. 3, we plot the error-rate performance for different P_d and α values, where the signal-to-noise ratio (SNR) is set to be $1/\sigma^2$. It is clear that when the deletion rate is high and the marker code rate is not sufficiently low, there exists an error floor, which indicates that deletion errors are not fully-corrected. When the α value is decreased, e.g., the ITI from the adjacent track is less severe, the performance improves dramatically. The last comment is that when $\alpha = 0$, the MIMO channel degrades to a conventional additive white Gaussian noise (AWGN) channel (as can be inferred from (2)), and the scheme offers the same result as for the case of the cascade of an i.i.d. deletion channel and an AWGN channel.

Fig. 4 compares the BER performance for different interference cancellation schemes. We focus on the case of $P_d = 0.001$ and $r_M = 48/50$, and we set $\eta = 0.6$. There is a noticeable gap between the joint detection algorithm in Section III-A and the IC scheme in Section III-B1 (about 1dB gap for the first layer and 1.5dB gap for the second layer). We can narrow this gap by applying the scheme introduced in Section III-B2. It is shown in the figure that, for this example, the performance improves with further iterations and the bit error rate finally converges to the result of using the joint detection algorithm. However, we also observe an error floor, which indicates existence of persistent errors when determining the locations of deletions. This problem may be alleviated by using a lower rate marker code at the expense of a larger overhead.
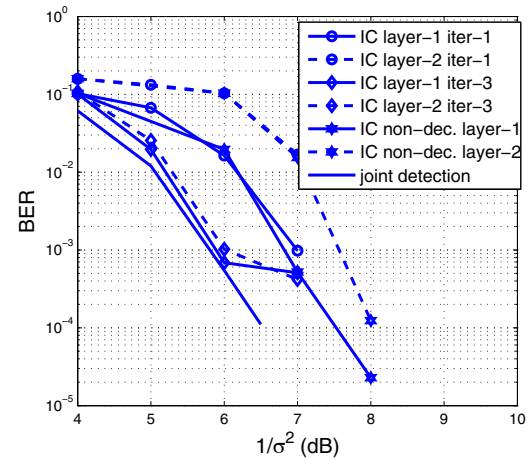
V. CONCLUSIONS

We have described a channel model suitable for applications employing multiple transmit/receive elements with imperfect synchronization, and considered channel coding (concatenation of an LDPC code, a marker code and a layered space-time code) and detection/decoding algorithms for this model. We have developed two detection algorithms operating at the bit level and studied their performance by several simulations.

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