Thin-Film ZnO Charge-Trapping Memory Cell Grown in a Single ALD Step

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***Abstract*—A thin-film ZnO-based single-transistor memory cell with a gate stack deposited in a single atomic layer deposition step is demonstrated. Thin-film ZnO is used as channel material and charge-trapping layer for the first time. The extracted mobility and subthreshold slope of the thin-film device are 23 $\mathrm{cm^2/V \cdot s}$ and 720 mV/dec, respectively. The memory effect is verified by a 2.35-V hysteresis in the I_{drain}–V_{gate} curve. Physics-based TCAD simulations show very good agreement with the experimental results providing insight to the charge-trapping physics.**

***Index Terms*—Atomic layer deposition (ALD), Flash memory, thin-film transistor (TFT), ZnO.**

I. Introduction

METAL-oxide semiconductors (ZnO and IGZO) have been extensively investigated recently as channel materials for thin-film transistors (TFTs). For low-cost flexible electronics, low-temperature techniques are of critical importance. TFTs were demonstrated using ZnO channels deposited by sputtering [1]–[5], atomic layer deposition (ALD) [6]–[9], and pulsed laser deposition [10], [11]. For functional electronics, integrated sensors and data storage devices are also required on such a cost-effective platform. Flash memory devices with low-cost ZnO channel materials are demonstrated [12]–[15]. The ALD technique is promising due to low-temperature growth, large-area uniformity, precise thickness control, highly conformal deposition, and scalability to roll-to-roll processes. Memory devices using the ALD ZnO channel are recently demonstrated [15]; however, the gate stack and the trapping layer are grown by the plasma-enhanced CVD technique. In addition, there are earlier reports on the use of wide band-gap amorphous semiconductors [13] and semiconductor nanoparticle [16] layers as both channel and trap layers in memory devices. However, in these reports, amorphous GaInZnO layers are deposited by RF magnetron sputtering [13], and ZnO nanoparticles are coated by solution processing [16]; whereas other techniques are used to deposit dielectric layers. An ALD approach offers a simplified high-throughput single-step approach to obtain very high-quality complete gate stacks. Such an approach avoids risk of contamination or incorporation of impurities in the gate stack, increase the throughput significantly by eliminating multiple equipment utilization for the gate stack, and therefore offer a novel path for ultralow-cost integrated devices.

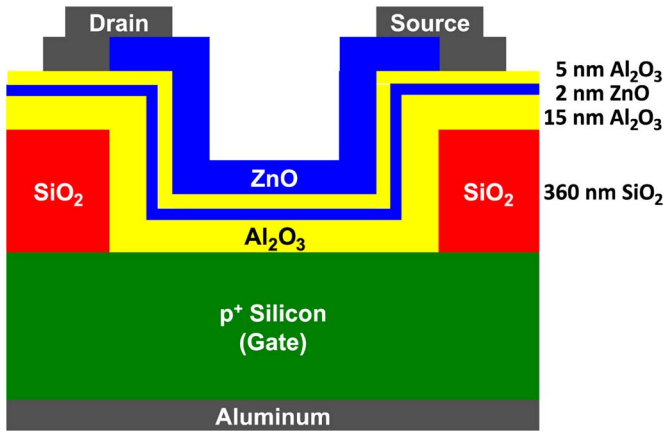

Fig. 1. Schematic of the thin-film all-ALD memory cell.

In this letter, we demonstrate a memory device with a gate stack fabricated in a single ALD step. Wide band-gap ZnO is used as the charge trapping and channel layer for concept demonstration. Fig. 1 depicts the structure of an all-ALD memory cell illustrating the ALD-deposited gate stack, including the transistor channel (ZnO), tunnel oxide (Al_2O_3), charge-trapping layer (ZnO), and charge blocking layer (Al_2O_3). In addition, physics-based TCAD simulations are compared with experimental results providing further insight into the charge-trapping mechanism.

II. Device Fabrication and Characterization

A. Fabrication

Channel-last all-ALD memory devices are fabricated on a highly doped (10–18 $\mathrm{m\Omega \cdot cm}$) p-type (111) Si wafer. The active region of the device is grown in a single continuous ALD step at 250 °C. A 15-nm-thick Al_2O_3 blocking layer is first deposited followed by a 2-nm-thick ZnO charge-trapping layer, a 5-nm-thick Al_2O_3 tunneling oxide, and, finally, an 11-nm-thick ZnO channel. The top ZnO layer (channel) is patterned

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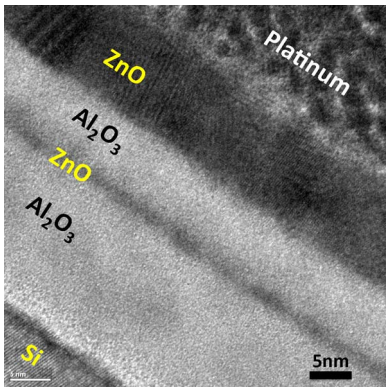

Fig. 2. Cross-sectional TEM image of the active area of the thin-film all-ALD memory cell.

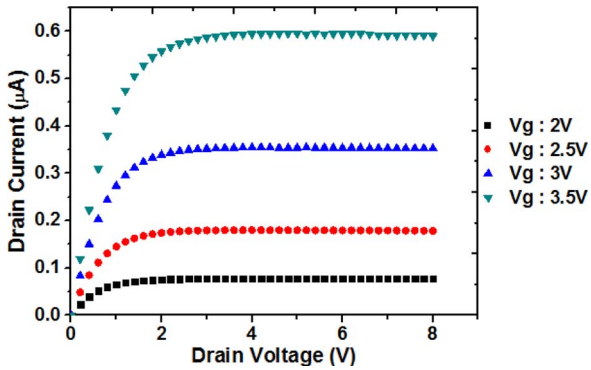

Fig. 3. Measured I_{drain}–V_{drain} of the thin-film all-ALD memory cell.

and etched for 2 s using a 5 : 95 $H_2SO_4 : H_2O$ solution. A 100-nm-thick Al layer is thermally evaporated and patterned by a liftoff technique to form source and drain contacts. A 360-nm-thick electron-beam evaporated SiO_2 layer is used for device isolation. A highly doped silicon substrate is used as a back-gate electrode. Finally, the samples are annealed in forming gas ($H_2 : N_2$ 5 : 95) for 10 min at 400 °C. Different size channel length L (2–150 μm) and width W (10–100 μm) devices are fabricated. Cross-sectional transmission electron microscope (TEM) image of a completed thin-film ZnO memory cell is shown in Fig. 2.

B. Experimental Characterization

The current–voltage (I–V) characteristics of devices are measured using a Keithley 4200 semiconductor characterization system at room temperature. Fig. 3 plots the transfer characteristics (I_{drain}–V_{drain}) of fabricated devices for different gate biases.

The device behaves as n-channel MOSFETs because the ALD-deposited ZnO is n-type due to native crystallographic defects such as interstitial zinc and oxygen vacancy that behave as electron donors [17], [18]. The maximum on-to-off ratio of 10^2 (limited by high effective doping concentration of the ZnO channel due to 250 °C deposition) is obtained for a device with a gate length and a width of 50 μm, with a subthreshold slope

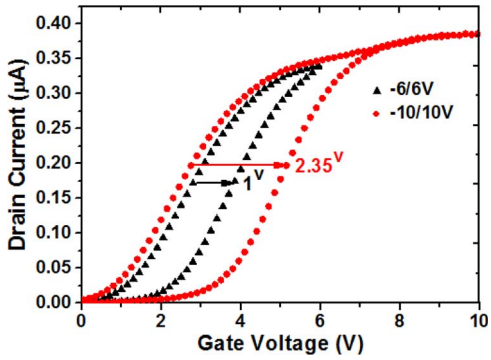

Fig. 4. Measured hysteresis behavior of the I_{drain}–V_{gate} characteristics with the gate voltage sweep.

TABLE I
MATERIAL PROPERTIES FOR ZnO AND DIELECTRIC LAYERS

	Al_2O_3	SiO_2	ZnO
Relative permittivity	*9.5 (6 to 9)*	*3.9*	*8.75*
Energy bandgap	6.65 eV	9 eV	3.37 eV
Electron affinity	2.58 eV	0.9 eV	4.5 eV
Electron tunnel mass	$0.43m_0$	$0.44m_0$	$0.24m_0$
Hole tunnel mass	$0.5m_0$	$1m_0$	$0.59m_0$

of 720 mV/dec. The electron mobility μ_e in the ZnO channel is found to be 23 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ using

$$I_{\mathrm{drain}} = \left(\frac{\mu_e \varepsilon_o \varepsilon_r W}{2t_{\mathrm{ox}} L}\right)(V_{\mathrm{gate}} - V_t)^2$$

in the saturation region ($V_{\mathrm{drain}} > V_{\mathrm{gate}} - V_t$), where ε_o and ε_r are the dielectric constants of the vacuum and the Al_2O_3 ($\varepsilon_r = 9.5$) layer, respectively. V_t is the threshold voltage, and t_{ox} is the thickness of the gate insulator.

In order to experimentally verify the device behaving as a memory, an I_{drain}–V_{gate} hysteresis is measured. Fig. 4 shows a typical hysteresis behavior for ±6- and ±10-V gate voltage sweeps verifying the memory effect. From the figure, there is a 2.35-V hysteresis in the ±10-V gate voltage sweep. Control samples, with no ZnO trapping layer, show a $<$ 0.6-V hysteresis, which is attributed to unintentional charge trapping in the gate oxide and the oxide–channel interface [19]. The devices exhibit poor retention characteristics potentially due to a continuous ZnO trapping layer. It should be noted the retention was not optimized in this seminal demonstration.

C. TCAD Simulations

In addition to the experiential results, physics-based TCAD simulations using Synopsys TCAD tools is carried out. Material property data used for ZnO [20] and Al_2O_3 [21] are listed in Table I.

The calculated energy band diagram of the structure at zero applied voltage is shown in Fig. 5(a). Both Fowler–Nordheim and direct tunneling models were used throughout the *program* and *erase* cycles, allowing electrons to tunnel from the ZnO channel layer to the trapping layer, and vice versa. The simulation model also includes energy states in the ZnO layer

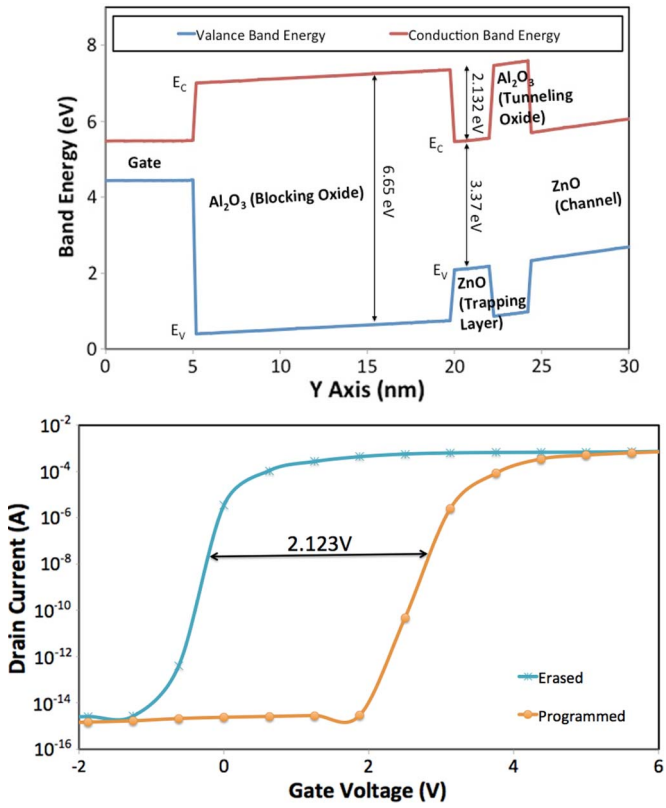

Fig. 5. (a) Calculated energy band diagram of the memory cell. (b) Computed $I_{\rm drain}$–$V_{\rm gate}$ for both program and erase states.

due to crystallographic defects such as interstitial zinc and oxygen vacancy. The $I_{\rm drain}$–$V_{\rm gate}$ characteristics for *program* and *erase* states are shown in Fig. 5(b) showing a 2.12-V hysteresis. The V_t shift obtained with TCAD agrees well with the V_t shift experimentally. This confirms that the electrons that tunnel across the Al_2O_3 tunnel oxide are either trapped due to confinement in a quantum well of 2 eV formed by the conduction band offsets between ZnO and Al_2O_3 or in the available energy states within the ZnO trapping layer.

III. Conclusion

In summary, a thin-film charge-trapping ZnO memory cell using a single ALD step has been fabricated for the first time. A hysteresis memory operation is demonstrated with a 2.35-V V_t shift measured. TCAD simulations combined with the experimental results provide insight into the charge-trapping mechanisms. In addition, the ZnO transistor characteristics obtained a rank among the best reported in literature. These results are promising for future low-cost, flexible, and transparent electronic applications.

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