Zinc-oxide charge trapping memory cell with ultra-thin chromium-oxide trapping layer

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Citation: AIP Advances **3**, 112116 (2013); doi: 10.1063/1.4832237

View online: http://dx.doi.org/10.1063/1.4832237

View Table of Contents: http://scitation.aip.org/content/aip/journal/adva/3/11?ver=pdfcov

Published by the AIP Publishing

Zinc-oxide charge trapping memory cell with ultra-thin chromium-oxide trapping layer

Nazek El-Atab,[1] Ayman Rizk,[1] Ali K. Okyay,[2,3] and Ammar Nayfeh[1]
[1]*Institute Center for Microsystems – iMicro, Department of Electrical Engineering and Computer Science (EECS), Masdar Institute of Science and Technology Abu Dhabi, United Arab Emirates*
[2]*Department of Electrical and Electronics Engineering, Bilkent University, 06800 Ankara, Turkey*
[3]*UNAM-National Nanotechnology Research Center and Institute of Materials Science and Nanotechnology, Bilkent University, 06800 Ankara, Turkey*

(Received 11 October 2013; accepted 6 November 2013; published online 13 November 2013)

A functional zinc-oxide based SONOS memory cell with ultra-thin chromium oxide trapping layer was fabricated. A 5 nm CrO_2 layer is deposited between Atomic Layer Deposition (ALD) steps. A threshold voltage (V_t) shift of 2.6V was achieved with a 10V programming voltage. Also for a 2V V_t shift, the memory with CrO_2 layer has a low programming voltage of 7.2V. Moreover, the deep trapping levels in CrO_2 layer allows for additional scaling of the tunnel oxide due to an increase in the retention time. In addition, the structure was simulated using Physics Based TCAD. The results of the simulation fit very well with the experimental results providing an understanding of the charge trapping and tunneling physics. [http://dx.doi.org/10.1063/1.4832237]

Nanotechnology has emerged as a vital enabler to allow memory devices to support future super hand-held computing devices.[1–4] In recent years, ZnO has been considered as a promising candidate to be used in flexible and/or transparent nano-devices due to its wide bandgap, good transparency, and low light sensitivity.[4–7] Earlier we validated a functional ZnO charge trapping memory grown by single step atomic layer deposition.[4] In this work, a ZnO based charge trapping memory cell is fabricated with a CrO_2 nanolayer sandwiched between the ALD deposited Al_2O_3 tunnel and blocking oxides. In addition, the structure is simulated using TCAD which allowed the exploration of the CrO_2 charge trapping and tunneling models.

The bottom-gate memory devices are fabricated as follows: first a 15-nm-thick Al_2O_3 blocking oxide layer is first ALD deposited followed by a sputtering of a 5-nm-thick CrO_2 as the charge trapping layer, then a 4-nm-thick ALD deposited Al_2O_3 tunneling oxide and finally an 11-nm-thick ALD deposited ZnO channel. A solution of 2:98 H_2SO_4:H_2O is used for 2 sec to etch the channel. A highly doped (10-18 milliohm-cm) p-type (111) silicon substrate is used as a back-gate electrode. The source and drain contacts were created by depositing 100 nm Al by thermal evaporation followed by lift off. Using Plasma Enhanced Chemical Vapor Deposition (PECVD), a 360-nm-thick SiO_2 layer is deposited for device isolation. Finally, Rapid Thermal Annealing (RTA) in forming gas (H_2:N_2 5:95) for 10 min at 400 °C was performed on the samples. Fig. 1 shows a cross section of the final device structure with the CrO_2 nanolayer. Fig. 2 shows the atomic force microcopy (AFM) image of the CrO_2 layer grown on top of the Al_2O_3 layer. The RMS is 1-nm which highlights the continuity of the nanolayer.

In order to study the effect of the CrO_2 nanolayer, the threshold voltage is quantified before and after programing. The memory cell is programmed (writing a '1') by applying a constant voltage (+8V) for 15 sec on the gate while grounding the drain and source. In order to erase the memory cell by removing the charge trapped in the CrO_2 layer, (writing a '0'), −8V is applied for 15 sec.

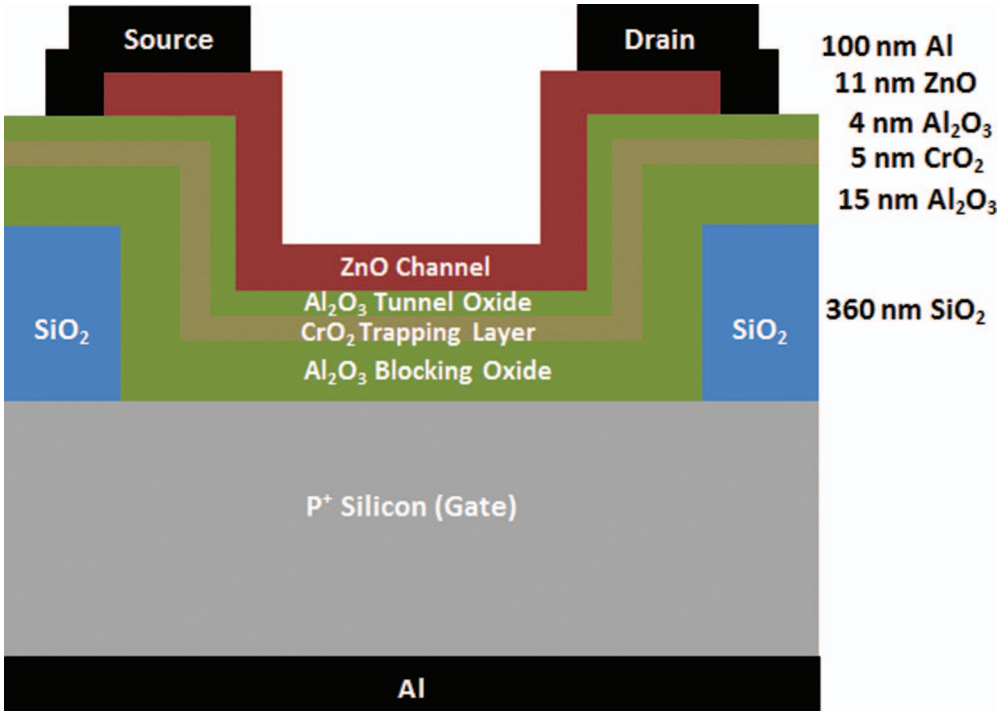

FIG. 1. Schematic cross-section of the fabricated memory cell with embedded CrO_2 nanolayer.

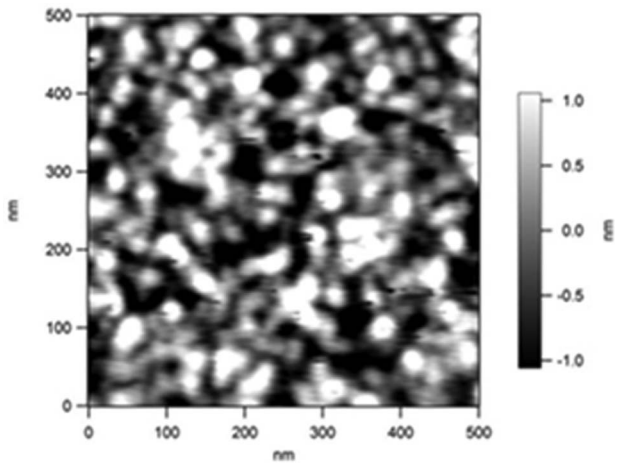

FIG. 2. AFM scan of the CrO_2 deposited on the Al_2O_3; RMS = ~1nm.

Fig. 3 shows the I_d-V_g curve for both programming and erase states, and the structure with the CrO_2 layer shows a V_t shift of 2.143V. Fig. 4 plots the threshold voltage shift vs. programming voltage. Compared to the ZnO charge trapping memory,[4] where we used a ZnO charge trapping layer; for a 2V V_t shift the CrO_2 nanolayer layer provides a ~2.5V reduction in programming voltage. Fig. 5 plots V_t shift as a function of time. The figure shows a long retention time with the addition of the CrO_2 layer. This is due to the extra states available and the larger barrier achieved between the charge trapping layer and the tunneling oxide. As a result, the tunnel oxide thickness can be scaled without sacrificing on retention.

Physics Based TCAD simulations using Synopsys™ TCAD tools are also studied. Because the experimental results showed a good charge trapping effect of the CrO_2 ultrathin layer with long retention time, and because there is no quantum well created by the CrO_2 layer due to its lower

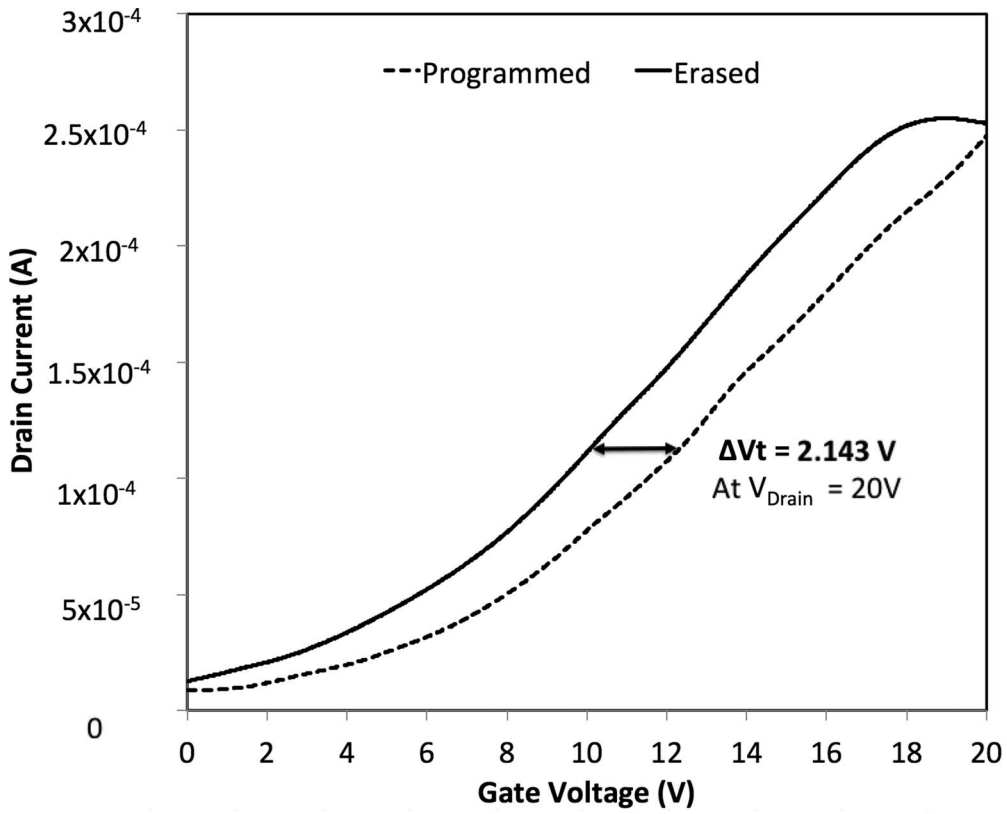

FIG. 3. I_d–V_g showing the V_t shift obtained with the memory cell with CrO_2 nanolayer using a drain voltage $V_d = 20V$.

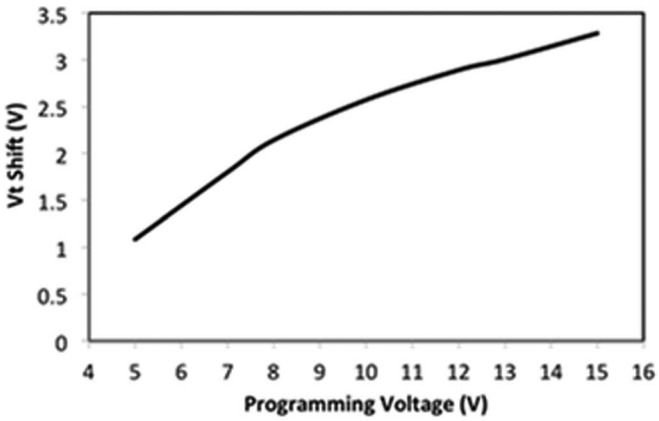

FIG. 4. Measured V_t shift vs. programming voltage.

electron affinity than the adjacent oxides electron affinities, which means that the electrons must be trapped within the trapping states available in ZnO only; thus we modeled the CrO_2 nanolayer such that the charge trapping levels are deep with high densities. To the best of our knowledge, there are still no published studies on the CrO_2 charge trapping and tunneling properties, but using TCAD simulations we were able to get an approximate model of the CrO_2 trapping and tunneling characteristics such as trapping levels, trapping densities, and electron and hole effective masses. In fact, a wide combination of different trapping levels with different trapping densities, and electron and hole CrO_2 effective tunnel masses were tested using TCAD simulations. The final structure that gave similar results to the experimental ones has the following parameters: a donor level in CrO_2 at

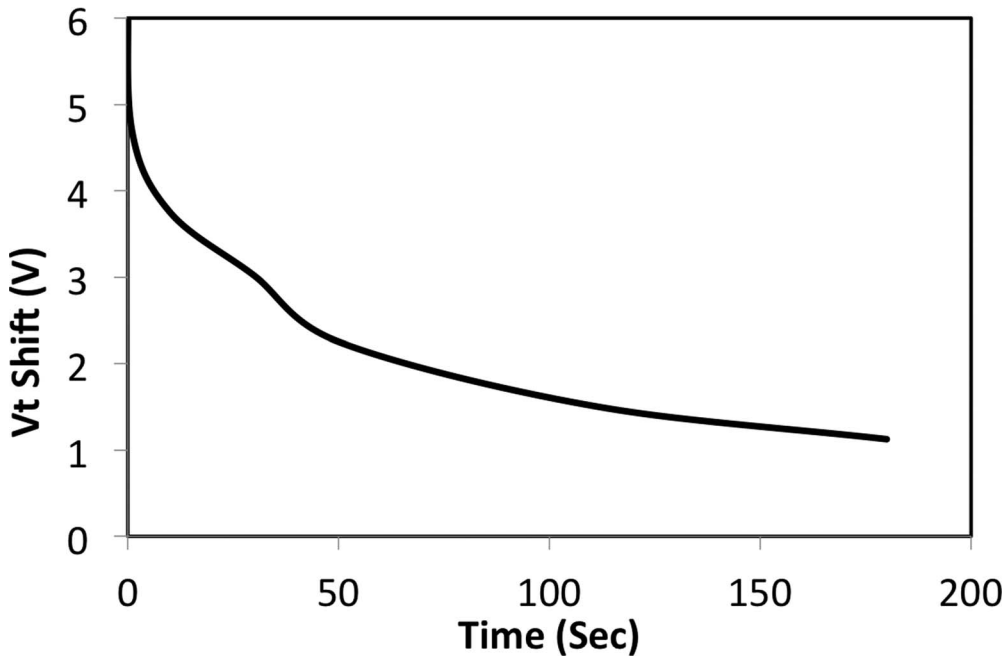

FIG. 5. Measured V_t shift vs time for the memory device with CrO_2 nanolayer.

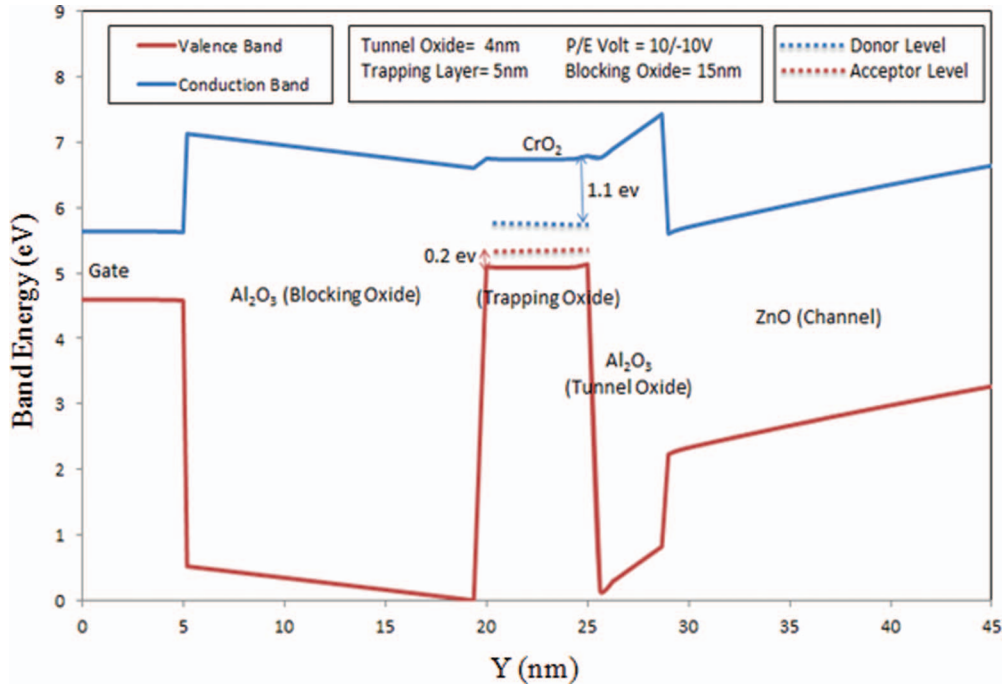

FIG. 6. Energy band diagram of the memory cell with CrO_2 nanolayer.

1.1 eV from the conduction band with a density of 10^{21} cm^{-3}, an acceptor level in CrO_2 at 0.2 eV from the valence band with a density of 10^{21} cm^{-3}, and electron and hole effective masses of 0.29m0. The energy band diagram of the simulated structure at zero applied voltage is depicted in Fig. 6. The tunneling models that were used in TCAD are: Fowler-Nordheim, trap assisted tunneling (TAT), and direct tunneling. These models are included to allow charges to tunnel across the tunnel oxide and charge or discharge the charge trapping ZnO layer when programming or erasing the memory cell.

TABLE I. Material properties for ZnO, Al_2O_3, and CrO_2.

	Al_2O_3	ZnO	CrO_2
Energy bandgap	6.65 eV	3.37 eV	1.7 eV
Relative permittivity	9.5	8.75	5
Electron affinity	2.58 eV	4.5 eV	2.41 eV
Electron tunnel mass	$0.43m_0$	$0.24m_0$	$0.29m_0$
Hole tunnel mass	$0.5m_0$	$0.59m_0$	$0.29m_0$

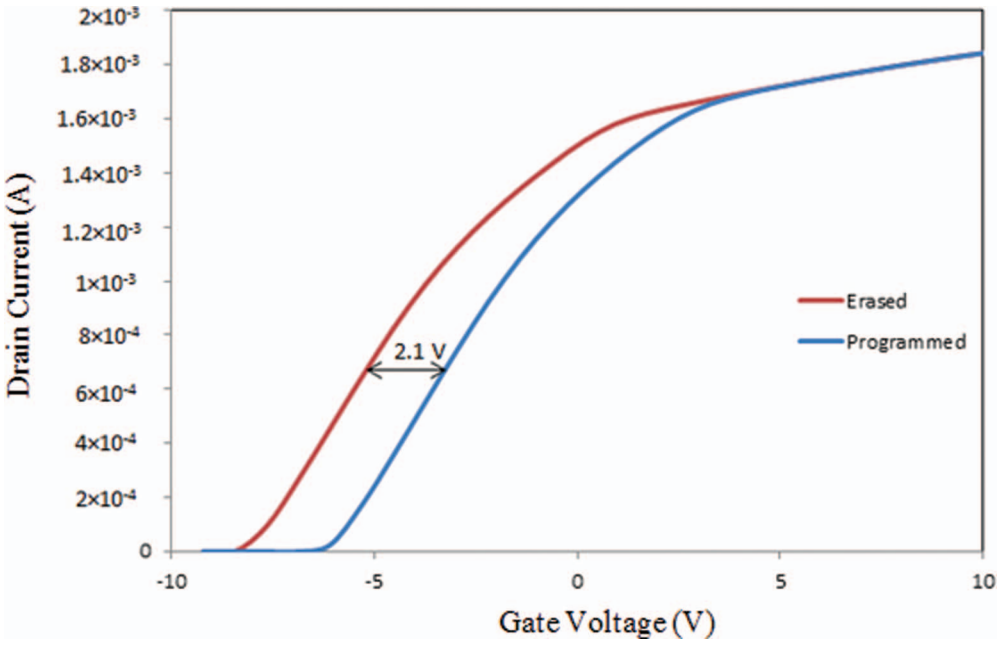

FIG. 7. Computed I_{drain}–V_{gate} for both program and erase states with P/E voltage of 8V/-8V.

Also, to ensure that the ZnO substrate is n-type due to crystallographic defects such as interstitial zinc and oxygen vacancies;[7] energy states were included in the ZnO layer of the TCAD simulated model. The material properties of ZnO,[8] Al_2O_3,[9] and CrO2[10–12] that were included in the simulations are listed in Table I. The I_{drain} - V_{gate} curves of the memory cell with an applied program/erase (P/E) voltage of 8V/−8V are shown in Fig. 7. The obtained V_t shift of 2.1V is consistent with the V_t shift obtained experimentally proving the accuracy of the proposed CrO_2 trapping and tunneling properties: electron and hole effective masses, charge trapping levels and their densities.

In summary, a ZnO charge trapping memory cell is fabricated with a CrO_2 charge trapping layer. Experimental results combined with TCAD simulations provide an understanding of the charge trapping mechanisms. The memory achieved a 2.6V V_t shift, a reduced programming voltage, and a long retention time. The results show that use of ultra-thin nanolayers can reduce the required programming voltage for future nanomemory devices which is promising for future low cost electronic devices.

ACKNOWLEDGMENTS

We gratefully acknowledge financial support for this work provided by the Masdar Institute of Science and Technology and the Advanced Technology Investment Company (ATIC).

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