Selective-Area High-Quality Germanium Growth for Monolithic Integrated Optoelectronics

Hyun-Yong Yu, Jin-Hong Park, Ali K. Okyay, and Krishna C. Saraswat

***Abstract*—Selective-area germanium (Ge) layer on silicon (Si) is desired to realize the advanced Ge devices integrated with Si very-large-scale-integration (VLSI) components. We demonstrate the area-dependent high-quality Ge growth on Si substrate through SiO_2 windows. The combination of area-dependent growth and multistep deposition/hydrogen annealing cycles has effectively reduced the surface roughness and the threading dislocation density. Low root-mean-square surface roughness of 0.6 nm is confirmed by atomic-force-microscope analysis. Low defect density in the area-dependent grown Ge layer is measured to be as low as 1×10^7 cm^{-2} by plan-view transmission-electron-miscroscope analysis. In addition, the excellent metal–semiconductor–metal photodiode characteristics are shown on the grown Ge layer to open up a possibility to merge Ge optoelectronics with Si VLSI.**

***Index Terms*—Area dependent, germanium, monolithic, optoelectronics.**

I. Introduction

AFTER the development of low-loss and low-dispersion silica fibers, III–V compound lasers, and Ge photodetectors, photonics research has focused on the demonstration of individual devices for wideband and multifunctional optical signal processing [1]. Because the growing photonics market requires more functionality and lower cost, photonic circuitry is desired to be monolithically integrated and to utilize the CMOS processing and low-cost substrates. Germanium and Si CMOS-compatible materials have thus been a natural choice for lower cost platforms [1], [2] and process integration with III–V optoelectronics. Ge emerges as a multifunctional material for the electronic–photonic integration on Si platform, due to its III–V and CMOS compatibility, and direct band-gap energy in the telecommunication wavelengths. The integration of III–V and Ge photonic components onto Si CMOS chips is the shortest route for meeting market expectations.

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The direct growth of Ge on Si is hampered by 4.2% lattice mismatch resulting in high density of dislocations and surface roughness. Graded SiGe and superlattice buffer layers are shown to reduce the dislocation density [3]–[9]. Very high temperature molecular beam epitaxy growth is known to confine threading dislocation near the Ge/Si interface [10]. In addition, full-wafer Ge growth on Si without annealing is also suggested to implement high-quality Ge growth [11], [12]. Moreover, necking method is shown to reduce defects where Ge is grown in SiO_2 trenches on Si, and the defects are arrested by the sidewalls of SiO_2 [13]. However, some of them require very thick buffer layer and complex process, and others have difficulty in obtaining single-crystal Ge layers with smooth surface.

In this letter, we report area-dependent multistep deposition/hydrogen annealing technique for Ge layers on Si. Transmission electron miscroscope (TEM) analysis and atomic-force-microscope surface morphology studies indicate that this technique yields Ge layers with very low dislocation density and surface roughness. In addition, the excellent metal–semiconductor–metal (MSM) photodiode characteristics are shown on the grown Ge layer to confirm the electronic–photonic integration on Si platform.

II. Experiment

A 300-nm-thick thermally grown SiO_2 film was patterned by dry etch followed by wet etch to define desired locations for Ge growth. Samples were dipped in 50 : 1 H_2O:HF for 30 s and immediately loaded into a cold-wall Applied Materials Centura epitaxial reactor. A hydrogen bake at 900 °C was carried out to remove any native oxide on Si surface. A very thin Si epilayer was first grown using dichlorosilane (DCS) at 700 °C to improve the final film quality. DCS provides good selectivity to SiO_2, allowing the thin Si layer to be selectively grown only on Si surface. Using SiO_2 as a masking pattern, Ge films were epitaxially grown using GeH_4 and H_2 as carrier gas. A 400-nm-thich Ge film was initially grown at 400 °C and 8 Pa. The initial Ge film is annealed in H_2 ambient for 30 min at 825 °C, which is known to reduce surface roughness and defects of the epigrown layer [14]. The growth temperature was increased to 600 °C for the following Ge layer followed by a 15-min H_2 bake at 800 °C. This grow–anneal cycle is repeated until the desired epilayer thickness is reached.

III. Results and Discussion

The growth rate varies along different crystal directions. This was verified by cross-sectional SEM images in Fig. 1(a) and

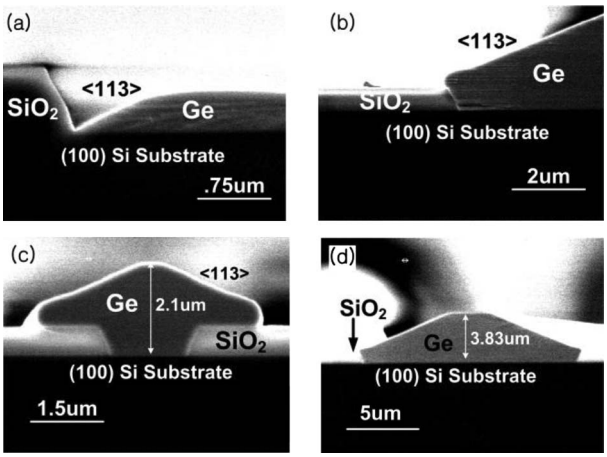

Fig. 1. Cross-sectional SEM images for growth temperatures of (a) 400 °C and (b) 600 °C with SiO_2 windows of 15 μm. SEM images of selectively grown Ge layers in (c) 2- and (d) 15-μm SiO_2 window sizes showing 2.1- and 3.83-μm thicknesses of the grown films.

(b) for films grown at 400 °C and 600 °C, respectively. At 400 °C, the growth rates along ⟨100⟩ and ⟨113⟩ directions are 30 and 3 nm/min, respectively, determined by SEM film thickness measurements for different growth times. Therefore, ⟨100⟩ growth dominates at 400 °C, resulting films exhibiting facets with {113} surfaces. When the growth temperature was raised to 600 °C, however, significant deposition on {113} facets, along with ⟨100⟩ direction, was observed. The measured growth rates at 600 °C, are 60 and 12 nm/min along ⟨100⟩ and ⟨113⟩, respectively. SEM images in Fig. 1(c) and (d) show that the film thickness at the center of the growth opening is dependent on the size of the opening in the SiO_2 masking layer, keeping other conditions unchanged. Fig. 1(c), having a 2-μm window size resulted in a thinner layer showing pyramid shape, as compared with Fig. 1(d), which has a window size of 15 μm with a truncated-pyramid shape. SEM images in Fig. 1(c) and (d) exemplify that the film thickness and shape depend on the size of the opening in the SiO_2 masking layer, other conditions remaining unchanged. Fig. 1(c), having a 2-μm window size, shows a pyramid-shaped layer with a thickness of 2.1 μm, as compared with Fig. 1(d), which has a window size of 15 μm and exhibits a 3.83-μm-thick truncated-pyramid shape. A complete growth rate polar diagram could not be determined due to limited starting surface orientations. However, our estimations employing Wulff construction and the growth rates determined for 400 °C and 600 °C are in good agreement with experimental results [15].

The rough surface of as-deposited Ge film on Si was considerably smoothed after high temperature hydrogen annealing at 825 °C. Measured surface root-mean-square (RMS) roughness significantly dropped from 9.5 to 3.9 nm. These results are in good agreement with the suggested surface roughness reduction model explained in [12]. Resulting RMS surface roughness values after each deposition/hydrogen-annealing cycle are plotted in Fig. 2. After each deposition and annealing, the surface becomes smoother. After the fourth cycle, surface roughness reaches 0.61 nm, which is one of the lowest values without chemical mechanical planarization process for selective heteroepitaxial growth of Ge on Si [16], [17].

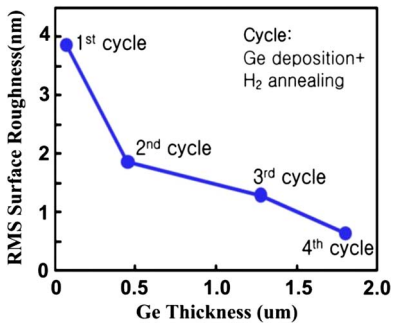

Fig. 2. RMS surface roughness as a function of Ge growth thickness after each Ge deposition and annealing cycle.

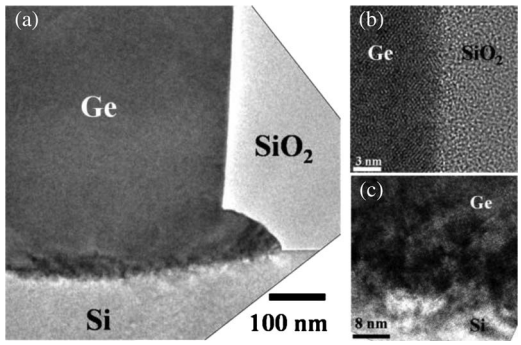

Fig. 3. (a) Cross-sectional TEM image of epi-Ge layer by using selective Multiple Hydrogen Annealing for Heteroepitaxy technique. (b) High-resolution image at the interface between Ge layer and SiO_2 sidewall. (c) High-resolution image at the interface between the Ge layer and the Si substrate.

Cross-sectional TEM images were obtained to better understand Ge crystal defects originating from 4.2% lattice mismatch. High-resolution TEM images in Fig. 3 show high-quality Ge films grown selectively in patterned SiO_2 windows. Defects can be found only in the first 60-nm-thick region from the Ge and Si interface. Since most defects are confined within the first 60 nm, growing a high-quality epi-Ge layer with much smaller overall thickness was possible [13], [18]. The SiO_2 sidewalls provide termination for dislocations. The rearrangement of Ge atoms will facilitate dislocations to glide to the Ge and SiO_2 interface and to be annihilated. Multistep Ge deposition/hydrogen-annealing cycles result in very low defect density films. Plan-view TEM analysis yields threading dislocation density counts as low as 1×10^7 cm^{-2}.

In order to confirm the electronic–photonic integration on a Si platform, interdigitated MSM photodetectors were fabricated on the area-controlled grown Ge layers. A low temperature chemical-vapor-deposited oxide layer was used as surface passivation. However, this oxide thickness is not optimized for the antireflection coating. Fifteen-nanometer Ti and 35-nm Au electrodes were sequentially deposited by electron-beam evaporation and patterned by liftoff technique to form Schottky contacts [23]. Fig. 4(a) shows the measured current–voltage (I–V) characteristic under the dark, showing decent Schottky behavior. The measured dark current density is 32 mA/cm^2 at 1 V. Although doped junctions are shown to exhibit low dark current values [19], [20], this is one of lowest reported dark current density values among the Ge MSM photodiodes [21], [22]. Such low dark current density figures also verify very

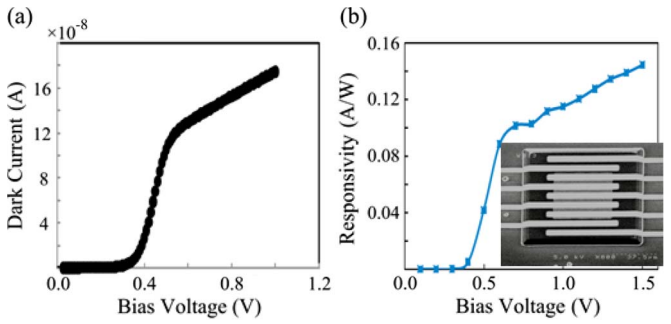

Fig. 4. (a) Dark current versus reverse bias curves of MSM photodetectors. (b) Photodetector responsivity at $\lambda = 1.55$ μm versus reverse bias for the MSM Ge photodetectors.

low defect density Ge films. Detector responsivity values were measured at a 1550-nm wavelength, as plotted in Fig. 4(b). We calculated the absorption coefficient (1000 cm^{-1}) at 1550 nm from the measured photocurrent, assuming 90% internal quantum efficiency and correcting for the reflection from the surface. Photocurrent rapidly increases until around 0.6-V bias when the surface of the semiconductor is completely depleted. Photocurrent continues to rise with applied bias owing to depletion region extending deeper and allowing the collection of more photogenerated carriers.

IV. Conclusion

In conclusion, we have demonstrated very high quality Ge growth technique on Si. The combination of area-controlled growth through SiO_2 window and multistep deposition/hydrogen-annealing cycle technique can be used to reduce the dislocation density and the surface roughness. Ge MSM photodiode characteristics fabricated on grown Ge layer promises the electronic–photonic integration on a Si very-large-scale-integration platform.

References

[1] C. D. A. B. Miller, "Physical reasons for optical interconnection," *Int. J. Optoelectron.*, vol. 11, no. 3, pp. 155–168, 1997.

[2] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, no. 6, pp. 728–749, Jun. 2000.

[3] H. Chen, L. W. Guo, Q. Cui, Q. Huang, and J. M. Zhoi, "Low-temperature buffer layer for the growth of a low-dislocation-density SiGe layer on Si by molecular-beam-epitaxy," *J. Appl. Phys.*, vol. 79, no. 2, pp. 1167–1169, Jan. 1996.

[4] K. K. Linder, F. C. Zhang, J. S. Rieh, and P. Bhattacharya, "Characterization of mismatched SiGe grown on low temperature Si buffer layers by molecular beam epitaxy," *J. Cryst. Growth*, vol. 175/176, no. 1, pp. 499–503, 1997.

[5] J. H. Li, C. S. Peng, Y. Wu, D. Y. Dai, J. M. Zhou, and Z. H. Mai, "Relaxed Si0.7Ge0.3 layers grown on low-temperature Si buffers with low threading dislocation density," *Appl. Phys. Lett.*, vol. 71, no. 21, pp. 3132–3134, Nov. 1997.

[6] C. S. Peng, Z. Y. Zhao, H. Chen, J. H. Li, Y. K. Li, L. W. Guo, D. Y. Dai, Q. Huang, J. M. Zhou, T. T. Sheng, and C. H. Tung, "Relaxed Ge0.9Si0.1 alloy layers with low threading dislocation densities grown on low-temperature Si buffers," *Appl. Phys. Lett.*, vol. 72, no. 24, pp. 3160–3162, Jun. 1998.

[7] T. Ueno, T. Irisawa, Y. Shiraki, A. Uedono, and S. Tanigawa, "Low temperature buffer grown for modulation doped SiGe/Ge/SiGe heterostructures with high hole mobility," *Thin Solid Films*, vol. 369, no. 1/2, pp. 320–323, Jul. 2000.

[8] S. Luryi, A. Kastalsky, and J. C. Bean, "New infrared detector on a silicon chip," *IEEE Trans. Electron Devices*, vol. ED-31, no. 9, pp. 1135–1139, Sep. 1984.

[9] R. Beanland, D. J. Dunstan, and P. J. Goodhew, "Plastic relaxation and relaxed buffer layers for semiconductor epitaxy," *Adv. Phys.*, vol. 45, no. 2, pp. 87–146, Mar. 1996.

[10] D. P. Malta, J. B. Posthill, R. J. Markunas, and T. P. Humphreys, "Low-defect-density germanium on silicon obtained by novel growth phenomenon," *Appl. Phys. Lett.*, vol. 60, no. 7, pp. 844–846, Feb. 1992.

[11] Y. Kang, H. Liu, M. Morse, M. J. Paniccia, M. Zadka, S. Litski, G. Sarid, A. Pauchard, Y. Kuo, H. Chen, W. S. Zaoui, J. E. Bowers, A. Beling, D. C. McIntosh, X. Zheng, and J. C. Campbell, "Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain–bandwidth product," *Nat. Photon.*, vol. 3, no. 1, pp. 59–63, 2009.

[12] A. Ramaswamy, N. Nunoya, L. A. Johansson, J. E. Bowers, M. N. Sysak, and T. Yin, "A high power Ge n-i-p waveguide photodetector on silicon-on-insulator substrate," in *Proc. 6th IEEE Int. Conf. Group IV Photon.*, 2009, pp. 19–21.

[13] J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, "Defect reduction of selective Ge epitaxy in trenches on Si(001) substrates using aspect ratio trapping," *Appl. Phys. Lett.*, vol. 90, no. 5, p. 52 113, Jan. 2007.

[14] A. Nayfeh, C. O. Chui, and K. C. Saraswat, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality," *Appl. Phys. Lett.*, vol. 85, no. 14, pp. 2815–2817, Oct. 2004.

[15] S. H. Jones, L. K. Seidel, K. M. Lau, and M. Harold, "Patterned substrate epitaxy surface shapes," *J. Cryst. Growth*, vol. 108, no. 1/2, pp. 73–88, Jan. 1991.

[16] J. Nakatsuru, H. Date, S. Mashiro, and M. Ikemoto, "Growth of high quality Ge epitaxial layer on Si (100) substrate using ultra thin SiGe buffer," in *Proc. Mater. Res. Soc.*, 2006, pp. 315–320.

[17] J. Wang and S. Lee, "Ge-photodetectors for Si-based optoelectronic integration," *Sensors*, vol. 11, no. 1, pp. 696–718, 2011.

[18] H. Luan, D. Lim, K. Lee, K. Chen, J. Sandland, K. Wada, and L. Kimerling, "High-quality Ge epilayers on Si with low threading dislocation densities," *Appl. Phys. Lett.*, vol. 75, no. 19, pp. 2909–2911, Nov. 1999.

[19] H. Zang, S. J. Lee, W. Y. Loh, J. Wang, K. T. Chua, M. B. Yu, B. J. Cho, G. Q. Lo, and D.-L. Kwong, "Dark-current suppression in metal–germanium–metal photodetectors through dopant-segregation in NiGe—Schottky barrier," *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 161–164, Feb. 2008.

[20] H. Y. Yu, S. L. Chen, P. B. Griffin, Y. Nishi, and K. C. Saraswat, "Germanium *in situ* doped epitaxial growth on Si for high-performance n+/p-junction diode," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 1002–1004, Sep. 2009.

[21] L. Vivien, M. Rouvière, J. Fédéli, D. Marris-Morini, J. Damlencourt, J. Mangeney, P. Crozat, L. Melhaoui, E. Cassan, X. Roux, D. Pascal, and S. Laval, "High speed and high responsivity germanium photodetector integrated in a silicon-on-insulator microwaveguide," *Opt. Exp.*, vol. 15, no. 15, pp. 9843–9848, Jul. 2007.

[22] L. Chen, P. Dong, and M. Lipson, "High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding," *Opt. Express*, vol. 16, no. 15, pp. 11513–11518, Jul. 2008.

[23] A. Okyay, A. Nayfeh, K. Saraswat, T. Yonehara, and A. Marshall, "High-efficiency metal-semiconductor-metal photodetectors on heteroepitaxially grown Ge on Si," *Opt. Lett.*, vol. 31, no. 17, pp. 2565–2567, Sep. 2006.