Design and Realization of a Fully On-Chip High-Q Resonator at 15 GHz on Silicon

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***Abstract*—We develop and demonstrate an on-chip resonator working at 15 GHz with a high quality factor (Q-factor) of 93.81 while only requiring a small chip size of 195 μm $\times$ 195 μm on Si by using our new design methodology. In our design, unlike previous approaches, we avoid the need for any external capacitance for tuning; instead, we utilize the film capacitance as the capacitor of the LC tank circuit and realize a fully on-chip resonator that shows a strong transmission dip of $>$ 30 dB on resonance as required for telemetric-sensing applications. We present the design, theory, methodology, microfabrication, experimental characterization, and theoretical analysis of these resonators. We also demonstrate that the experimental results are in excellent agreement with the theoretical (both analytical and numerical) results. Based on our proof-of-concept demonstration, such high-Q on-chip resonators hold great promise for use in transmissive telemetric sensors.**

***Index Terms*—Fabrication, quality factor (Q-factor), resonators, RFIC, silicon, spiral inductors.**

I. Introduction

IMPROVING the quality of the resonators is a major concern for satellite communications in the superhigh-frequency (SHF) band. High-performance resonators operating in this frequency range are also required for other wireless applications such as mobile phones. Additionally, such resonators find applications in sensing. However, it is not a simple task to increase the quality factor (Q-factor) while satisfying the other specifications including small size and low cost. In general, to fulfill these requirements, micromachined cavity resonators are used [1], [2]. Although these cavity architectures exhibit sufficiently high Q-factors, their sizes are quite large (on the order of 10 mm on one side with a minimum volume of 24.5 mm^3) [1]. Thus, as an alternative, structures based on spiral-coil inductors are investigated to satisfy the minimal area requirement while increasing the Q-factor [3]–[8]. However, these previous studies reported Q-factors only up to $\sim$50. In this paper, we develop and demonstrate an on-chip resonator on silicon, working in the K_u-band (at 15 GHz) with a very high Q-factor (93.81) while only requiring a small chip size (195 μm $\times$ 195 μm) by using our new design methodology. In our design, unlike previous approaches, we do not treat the spiral coil as only an inductor and do not use an external capacitor for tuning. Instead, we make use of the intrinsic capacitances and LC tank behavior of the structure to set the resonance.

Avoiding the need for an external capacitor to develop such an on-chip resonator was first reported in our previous work [9]. However, this previous work led to only a Q-factor of 47 at 7 GHz. In this paper, we implement a self-tuning spiral-coil-based architecture without a cavity on the chip using improved design parameters at a higher operating frequency. Thus, we achieved significantly small-size and high-Q resonators in comparison with those of previous reports of our group and others [6], [9]–[11]. Typically, the resonator Q-factor decreases as the frequency increases. By our novel design, we realize the highest Q-factor with the smallest lateral area of 3.8×10^{-2} mm^2 (and with the smallest volume of 1.9×10^{-2} mm^3) at 15 GHz reported to date.

Furthermore, considering the high demand for good-quality resonators in medical applications and BioMEMS sensors, we design our on-chip resonators with biocompatible materials (Si as the substrate, Au as the metal layers, and Si_3N_4 as the thin dielectric film). In addition, we restrict our device designs to thin-enough metal layers to avoid the need for using specially thick high metal layers, sometimes called "RF layers," which further reduces fabrication cost, if implemented in CMOS technology. These designs can also use the standard CMOS metal-layer thicknesses, if desired. This is particularly important if such resonators are to be manufactured in high volumes as a part of sensors.

Given these restrictions, we start our resonator design by theoretical computations and numerical simulations for verification (using the CoventorWare RF Package). We further study the design S parameters (using Microwave Studio). Fabricating the designs and characterizing the resulting devices, we observe an excellent agreement between the experimental and the numerical results, with a good conformity between theoretical and experimental resonance frequency and Q-factor.

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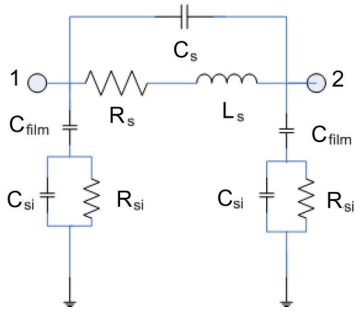

Fig. 1. Conventional lumped-element circuit model.

The rest of this paper is organized as follows. We first describe the physical and mathematical background in Section II. We then explain our new design methodology, including numerical RF simulations, in Section III. We describe the fabrication and experimental characterization in Section IV and, finally, conclude in Section V.

II. Theory

Spiral-coil structures are used as on-chip inductors. Owing to the parasitic capacitances of the coil metal with the substrate and the air bridge, such structures display a built-in resonance behavior. This resonance is normally considered to be past the structure's useful range of operation as an inductor. To utilize this structure as a resonator, in this paper, we model its behavior around this natural resonance point.

To form a circuit model, we analyze a rectangular spiral coil as consisting of segments. We conceive each segment of the coil as a transmission line and proceed according to established transmission-line theory [12], [13]. To model the device, we consider the following design parameters: L_c and W_c as the outer lengths of the coil, l as the total coil length, w as the linewidth, s as the line spacing, N as the number of turns, t as the coil thickness, and $t_{\rm film}$ as the thickness of the dielectric thin film between the substrate and the Au metal layer. The geometrical design parameters L_c, W_c, N, w, and s set the coil inner diameter. These device parameters are used to calculate the parameters for the conventional lumped-element model shown in Fig. 1 [9].

In the figure, L_s and R_s correspond to the coil inductance and resistance, respectively. $C_{\rm film}$ represents the capacitance between the substrate and the coil. $C_{\rm si}$ and $R_{\rm si}$ are the substrate capacitance and resistance, respectively. C_s denotes the capacitance between coil segments.

L_s is calculated by taking into account the self-inductance $L_{\rm Self}$, the positive mutual inductance M^+, and the negative mutual inductance M^- as given in the following [14]:

$$L_s = |L_{\rm Self}| + |M^+| - |M^-|. \tag{1}$$

The coil resistance (R_s) is a function of the skin-depth δ, where R_s and δ are given in the following:

$$R_s = \frac{\rho \ell}{w\delta \times \left(1 - e^{-\frac{t}{\delta}}\right)} \tag{2}$$

where

$$\delta = \sqrt{\frac{2\rho}{\omega\mu_0}} \quad \omega = 2\pi f. \tag{3}$$

$C_{\rm film}$ and C_s are calculated using the parallel-plate-capacitor formula [15]

$$C_{\rm film} = \frac{\varepsilon_0 \varepsilon_r \ell w}{t_{\rm film}} \tag{4}$$

$$C_s = \frac{\varepsilon_0 \ell t}{S}. \tag{5}$$

The elements $C_{\rm si}$ and $R_{\rm si}$, which represent substrate effects, are calculated by (6) and (7), respectively (our special design approach for $R_{\rm si}$ will be explained in detail in Section III).

$$C_{\rm si} = 0.5 \ell w C_{\rm Sub} \quad C_{\rm Sub} = 1.6 \times 10^{-10} \frac{F}{\rm cm^2} \tag{6}$$

$$R_{\rm si} = \frac{2}{\ell w G_{\rm Sub}} \quad G_{\rm Sub} = 0.4 \frac{1}{\Omega {\rm cm}^2}. \tag{7}$$

Here, $C_{\rm Sub}$ and $G_{\rm Sub}$ are fitting parameters as defined in [15] and obtained from measurements.

The Q-factor can be defined in two different ways. The first is the basic Q-factor definition for a resonator [10]

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}}. \tag{8}$$

The earlier equation gives the total resonator Q-factor. Another form for this equation is given as follows [16]:

$$Q = \frac{f_0}{\Delta f}. \tag{9}$$

Δf is the full width at 3 dB above the minimum S_{21}, which is at f_0, the resonance frequency. Using S_{21} measurements taken with microwave probes, we can calculate the loaded Q-factor.

Although (9) is useful to extract the resonator Q-factor from experimental characterization (e.g., from the experimental data of S_{21} as in Section IV), it does not give us information about which elements store or dissipate energy. To design a high-quality on-chip resonator, we need a better grasp of the system. Therefore, we exploit the definition of the Q-factor for the inductor instead of the entire LC tank circuit. For the inductor, only the energy stored in the magnetic fields is of interest. Therefore, when the difference between the peak magnetic field and the peak electric field is at the maximum value, we get the maximum $Q_{\rm max}$ of the inductor Q-factor $Q_{\rm ind}$ [10]

$$Q_{\rm ind} = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}}. \tag{10}$$

By this definition, we can ascertain which elements store and dissipate the energy and how we can improve the design.

An alternate form for $Q_{\rm ind}$ is [10]

$$Q_{\rm ind} = \frac{R}{\omega L}\left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]. \tag{11}$$

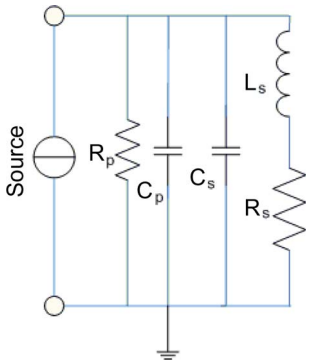

Fig. 2. Conventional simplified one-port parallel RLC circuit.

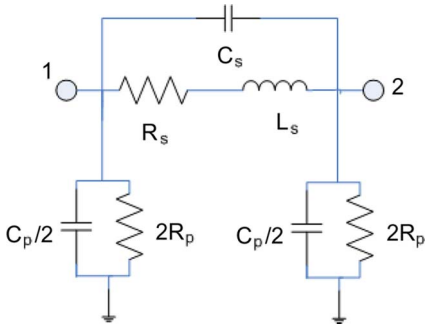

Fig. 3. Our two-port circuit model to calculate the Q-factor.

The earlier equation reveals that $Q_{\rm ind}$ is zero at the structure's self-resonance frequency. This frequency in a classical LC circuit is given by as follows [10]:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{12}$$

The resonator Q-factor can be obtained by combining the inductor and capacitor Q-factors [16]: $(1/Q_{\rm res}) = (1/Q_{\rm ind}) + (1/Q_c)$. Q_c is not affected extensively by structural design once a material system has been selected. $Q_{\rm ind}$, on the other hand, depends on geometrical design as well as the materials. Thus, by using the classical resonance definition and the design techniques for better $Q_{\rm ind}$, we can maximize the resonator Q-factor for our small on-chip resonator.

For optimizing $Q_{\rm ind}$, we start by simplifying the equivalent lumped-circuit model whose parameters we use to calculate $Q_{\rm ind}$. In the literature, one of the ports of the two-port model in Fig. 1 is shorted to obtain a one-port circuit [15], [17]. By simplifying this circuit to a parallel RLC circuit, we get the circuit shown in Fig. 2. Here, R_p and C_p represent the combination of $C_{\rm film}$, $C_{\rm si}$, and $R_{\rm si}$ as shown in (13) and (14), respectively

$$R_p = \frac{1}{\omega^2 C_{\rm film}^2 R_{\rm si}} + \frac{R_{\rm si}(C_{\rm film}+C_{\rm si})^2}{C_{\rm film}^2} \tag{13}$$

$$C_p = C_{\rm film}\frac{1+\omega^2(C_{\rm film}+C_{\rm si})C_{\rm si}R_{\rm si}^2}{1+\omega^2(C_{\rm film}+C_{\rm si})^2R_{\rm si}^2}. \tag{14}$$

At this point, we change the model shown in Fig. 2 into a two-port model as shown in Fig. 3 and proceed with the calculations. Combining all the concepts explained so far, $Q_{\rm ind}$ becomes

$$Q_{\rm ind} = \frac{\omega L_s}{R_s} \times \frac{2R_p}{2R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right]R_s} \times \left[1 - \frac{R_s^2\left(\frac{C_p}{2}+C_s\right)}{L_s} - \omega^2 L_s\left(\frac{C_p}{2}+C_s\right)\right]. \tag{15}$$

From (15), we identify the two factors which affect $Q_{\rm ind}$ and $Q_{\rm max}$: the substrate-loss factor and the self-resonance factor, both given as follows. Here, we note that the substrate-loss factor mainly affects $Q_{\rm max}$, and the self-resonance mainly affects the resonance frequency

Substrate-Loss Factor

$$= \frac{2R_p}{2R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right]R_s} \tag{16}$$

Self-Resonance Factor

$$= \left[1 - \frac{R_s^2\left(\frac{C_p}{2}+C_s\right)}{L_s} - \omega^2 L_s\left(\frac{C_p}{2}+C_s\right)\right]. \tag{17}$$

III. Design

Our main objective is to design the smallest resonator working at 15 GHz with the highest possible Q-factor. To this end, understanding each of the device parameters correctly allows us to accomplish a superior design. In the literature, ways to increase $Q_{\rm max}$ are sought as in [6] and [11], with $Q_{\rm ind}$ as the target Q-factor to be maximized (the difference between Q and $Q_{\rm ind}$ was given in Section II).

In the literature, the film capacitance is considered as a parasitic capacitance [10]. However, our approach is to use this built-in capacitance as the capacitor of LC tank so that there is no need to tune the circuit with an external capacitor; thus, we can obtain a small fully on-chip resonator that can be used, e.g., for transmissive telemetric sensing. We presented the physical design factors in Section II. Here, we examine the effects of these parameters.

A. Effect of the Substrate

Minimizing substrate losses is important to achieve a considerable increase in $Q_{\rm ind}$ and $Q_{\rm max}$, as the substrate is the main lossy component in the system. In general, to prevent substrate loss in resonators, researchers prefer to use GaAs, which is harmful to the human body and would render the BioMEMS sensor nonbiocompatible. Here, we chose Si as the substrate for a biocompatible device.

For low loss, a high $R_{\rm si}$ (and, thus, a highly resistive substrate) is required. However, a completely nonconductive substrate would hinder the formation of a parallel-plate capacitor between the metal layer and substrate, contradicting the on-chip resonator concept. Thus, we select a substrate at 5–10 $\Omega \cdot$ cm,

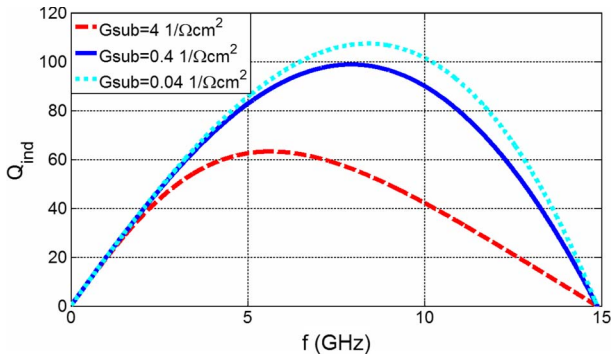

Fig. 4. Relationship between $Q_{\rm ind}$ and substrate resistivity.

which is resistive enough to prevent excessive loss but still conductive enough to serve as the second plate of a parallel-plate capacitor. Fig. 4 shows the relationship between $Q_{\rm ind}$ and the substrate resistivity as obtained by our simulations.

B. Effect of the Dielectric Thin Film

The dielectric layer is also an important factor for a high-Q-factor design. To optimize the capacitor between the metal and the substrate, which serves as the C of the LC circuit, we need a dielectric layer with a high dielectric constant. On the other hand, to minimize the loss, a low-loss dielectric is required. Therefore, Si_3N_4, with a dielectric constant of eight and a loss tangent of 5×10^{-4}, is chosen as the dielectric film to satisfy these conditions.

C. Effect of the Film Thickness

The thickness of the dielectric layer $(t_{\rm film})$ is another effective parameter to design a high-Q-factor resonator. For our target resonance frequency of 15 GHz, we set the dielectric-layer thickness to 0.1 μm.

D. Effect of the Metal-Layer Parameters

The metal type used in the design is critical, particularly for the BioMEMS sensor applications where biocompatibility is crucial. There are several metals (e.g., Al and Cu) being used in the generic CMOS or MEMS processes. However, since these restrict biocompatibility, instead, Au, which is biocompatible, is chosen as the metal layer.

The thickness of the metal layer is also significant to determine $Q_{\rm ind}$. The thicker the metal is, the higher $Q_{\rm ind}$ and $Q_{\rm max}$ are. However, as we aim for an RFIC resonator achievable without the need for special fabrication steps in a CMOS process, we set the metal thickness to 0.1 μm. In spite of the thin layer, we can achieve a high $Q_{\rm ind}$ by decreasing the substrate loss sufficiently. In that case, increasing the metal thickness would still affect the Q-factor but not as significantly as it would in a structure with a too low substrate resistance.

E. Effect of the Linewidth and the Spacing

Optimizing the linewidth (w) and spacing (s) is critical for our design. Although increasing the width improves $Q_{\rm ind}$, it also results in a larger area. In addition, an excess increase in the width with respect to the spacing s further increases the parasitic capacitance and diminishes $Q_{\rm ind}$. On the other hand, by decreasing the spacing, both the resonance frequency and $Q_{\rm ind}$ can be increased. However, continuing to decrease the spacing with respect to the linewidth causes an increase in the parasitic capacitance and a decrease in the Q-factor. Considering these constraints, we chose the width and the spacing as thick as 35 and 5 μm, respectively.

F. Effect of the Number of Turns

To increase $Q_{\rm ind}$ while keeping the size small, we decrease the number of turns (N). This decreases the net inductance, pushing the self-resonance frequency higher. Thus, we restrict the number of turns to two.

G. Effect of the Area

The chip size is influential to adjust the resonance frequency and $Q_{\rm ind}$. As we intend to have resonance at 15 GHz, which is in the SHF range, we need to decrease the area as much as possible. This is also consistent with our aim of a compact resonator. A smaller area also increases $Q_{\rm ind}$. As in (15), $Q_{\rm ind}$ is related to the ratio of $\omega L_s/R_s$ and the substrate-loss factor (the self-resonance factor mainly affects the resonance frequency). In our design methodology, the substrate-loss factor is almost one, and generally, the ratio of L_s/R_s is almost the same; so, a higher ω increases $Q_{\rm ind}$. If we have a smaller area, we have higher resonance frequency, and as a result, we can see the $Q_{\rm ind}$ at higher frequencies (we can observe $Q_{\rm ind}$ up to the self-resonance frequency). Therefore, we have higher ω and thus higher $Q_{\rm ind}$. As a result, we set the area $(L_c \times W_c)$ to the minimum value possible with the limiting factors such as N, w, and s.

H. Effect of the Inner Diameter

If all the other design parameters are fixed, the increase in inner diameter increases the area. This decreases the resonance frequency and, hence, $Q_{\rm ind}$. Therefore, a smaller inner diameter enhances $Q_{\rm ind}$ and the resonance frequency. However, we can only decrease the inner diameter down to the thickness of the spacing s, since decreasing below this value causes the parasitic capacitance to dominate and degrade $Q_{\rm ind}$. Therefore, our inner diameter is set equal to s.

I. Effect of R_p

R_p, representing the combined impedances of $C_{\rm film}$, $C_{\rm si}$, and $R_{\rm si}$, as in (13), is one of the most important factors in determining the substrate loss. If R_p is high, the substrate-loss factor becomes almost one, as indicated by (16). On the other hand, since energy loss is more apparent at higher frequencies, we need to optimize R_p to minimize these losses.

Targeting 15-GHz operation, we already need to fix w and l at low values. In addition, we adjust the other parameters to minimize the coil size. Therefore, the total l also decreases,

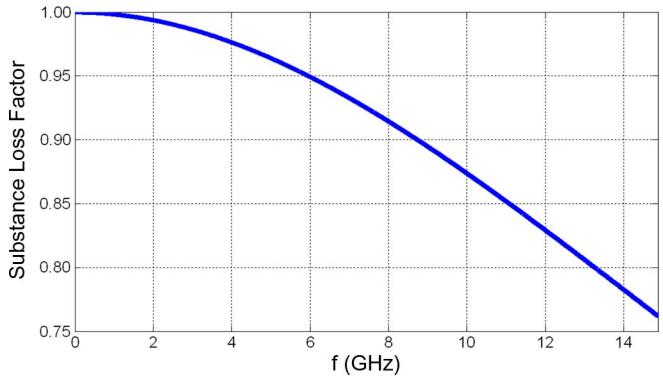

Fig. 5. Substrate-loss factor as a function of the operating frequency.

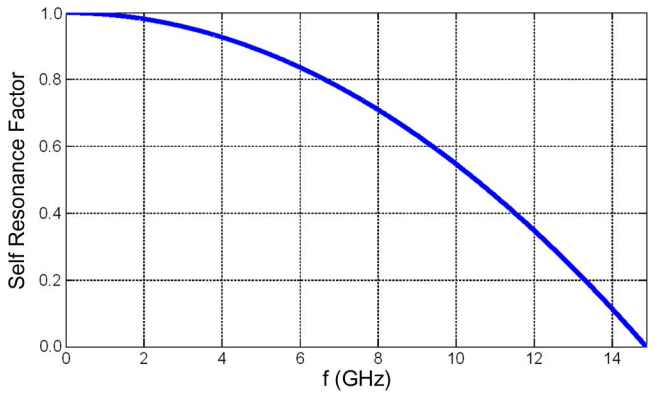

Fig. 6. Self-resonance frequency factor as a function of the operating frequency.

which enhances $R_{\rm si}$. As a result, we obtain a high $R_{\rm si}$, giving rise to a high R_p almost independent of the frequency. Because of the increased frequency and smaller dimensions, we obtain a higher R_p and observe a smaller change in R_p as a function of the frequency compared to R_p in our previous design [9].

We notice that R_p is rather high with a slight decrease at higher frequencies. Hence, the substrate-loss factor is also high, and it decreases from 1 to nearly 0.75 with the increase in the frequency from 1 to 15 GHz, as shown in Fig. 5. With our design parameters, we obtain high $Q_{\rm ind}$ and high $Q_{\rm max}$. Because of the high substrate loss, $Q_{\rm max}$ is observed at higher frequencies. If the substrate-loss factor decreases, $Q_{\rm max}$ shifts to lower frequencies. The substrate-loss factor does not have a significant effect on the resonance frequency, whereas it mainly affects $Q_{\rm ind}$, $Q_{\rm max}$, and the frequency at which $Q_{\rm max}$ is detected. If we had an R_p of infinity, the substrate-loss factor would become one, and we would observe a minimal increase in $Q_{\rm max}$.

J. Effects of C_p

C_p is a compound of $C_{\rm film}$, $C_{\rm si}$, and $R_{\rm si}$, as presented in (14). It mainly depends on $C_{\rm si}$ and $C_{\rm film}$. It is essentially a function of w and l. C_p determines the resonance frequency. For a higher resonance frequency, a low C_p is required. Therefore, l is decreased to attain a low C_p and a high resonance frequency with a small device volume. Thus, by reducing the size, we decrease C_p and increase the resonance frequency. As in (14), $R_{\rm si}$ should be high for C_p to be independent of the frequency. How to obtain a high $R_{\rm si}$ is explained earlier. In comparison with the C_p in [9], we realize a lower C_p and observe a slight decrease in C_p with the increasing frequency and smaller dimensions. As a result, the substrate-loss factor decreases to zero at 14.88 GHz. With a low C_p, the self-resonance frequency factor slowly decreases to zero at 15 GHz, and we obtain a high-frequency resonator. Fig. 6 shows the self-resonance frequency factor with respect to the frequency.

By combining all these effects, we obtain the design parameters as shown in Table I.

To design our device, we compute the inductance L_s by simulating in the RF simulation tool of CoventorWare and compare these values with our theoretical calculations. The calculated and simulated L_s values are almost identical as shown in Table II. Our theoretical calculation for L_s is done as in (1), where $L_{\rm Self}$, M^+, and M^- are calculated as in [14].

TABLE I
PARAMETERS OF OUR DEVICE

L_c (μm)	W_c (μm)	N	w (μm)	s (μm)	t_{ox} (μm)	t (μm)
195	195	2	35	5	0.1	0.1

TABLE II
THEORETICAL AND NUMERICAL L_S VALUES FOR OUR DEVICE

	Theoretical	Numerical
L_s (nH)	2.54	2.56

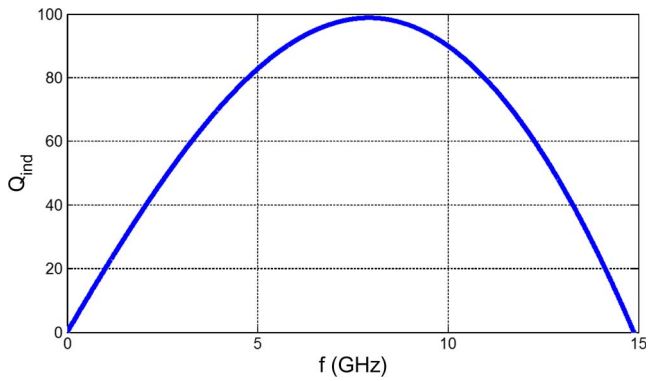

Fig. 7. $Q_{\rm ind}$ versus the operating frequency.

In Fig. 7, we present the theoretical $Q_{\rm ind}$ as a function of the operating frequency. At the resonance frequency (15 GHz), the inductor Q-factor crosses the zero line.

IV. EXPERIMENTAL REALIZATION, CHARACTERIZATION, AND ANALYSIS

Our fabrication process follows standard photolithography, metallization, wet etching, and plasma-enhanced chemical-vapor-deposition (PECVD) steps [9]. We use lithography to pattern the first metal layer (0.1-μm-thick Au) on the Si substrate with lift off following the metallization by evaporator. We deposit the 0.1-μm-thick dielectric Si_3N_4 film with PECVD. Then, we perform again lithography to open the holes in Si_3N_4 film using wet etching in HF. After this process, we carry out vertical interconnect metallization by evaporating a 0.1-μm-thick Au film. Finally, we lay down the spiral coil using

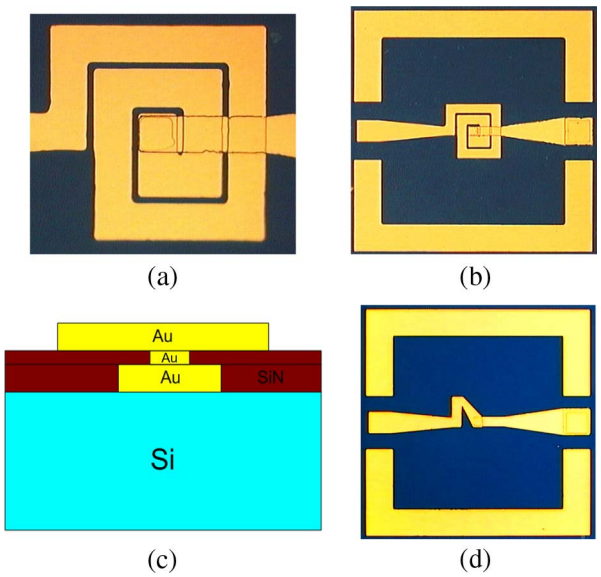

Fig. 8. Micrographs of one of our fabricated devices showing (a) spiral coil zoomed at the center and (b) in its entirety, along with (c) its cross-sectional layer diagram and (d) that of the "thru" structure used for calibration purposes.

lithography, metallization, and lift off of a top 0.1-μm-thick Au layer. Fig. 8(a)–(c) shows the resulting fabricated device and its cross-sectional layer diagram to show these different layers of the device from the side.

The network analyzer is used to obtain the spectral transmission response of the fabricated devices. We use GSG microwave probes for S-parameter measurements after performing an impedance-standard-substrate calibration. In a further calibration process before measuring the S_{21} parameters, we first measure the response of the through ("thru") calibration structure given in Fig. 8(d), which consists of just the GSG probe pads and interconnects, to exclude the effect of parasitic capacitance when later measuring the values of the device under test. The measurements were taken using the maximum number of points (801 point), with an averaging factor of 128.

Fig. 9 shows the experimentally measured S_{21} parameter (in decibels) along with the numerically simulated one up to a maximum operating frequency of 18 GHz (which is the upper limit of the measurement range in our setup). We observe an excellent agreement between the experimental and theoretical results. In particular, we observe very good matches between the experimental and theoretical f_0 (the resonance frequency) and the resonator Q-factor.

Here, the resonator Q-factor is calculated from the experimental results by examining the dip in the transmitted power. The minimum point of S_{21} is shown in Fig. 9. This corresponds to f_0 (at $\sim$15 GHz). Here, we observe a very strong dip of $>$ 30 dB in transmission. To calculate the resonator Q-factor from the experimental data as defined in (9), we use those frequencies with S_{21} parameters 3 dB above the resonance frequency. Here, we find Δf to be 160 MHz, yielding a Q-factor of 93.81. This is the Q-factor of the entire resonator for the case when the chip is loaded with microwave probes.

In summary, Table III lists the resonance frequencies and the resonator Q-factors obtained both experimentally and theoretically. The theoretically calculated resonance frequency is 14.88 GHz, whereas the experimental resonance frequency is 15.01 GHz. The theoretical Q-factor is 98.77, while the experimental Q-factor is 93.81. This experimental demonstration shows that such a fully on-chip resonator leads to a very high Q-factor and a very strong dip in transmission, making it possible to use for telemetric-sensing applications.

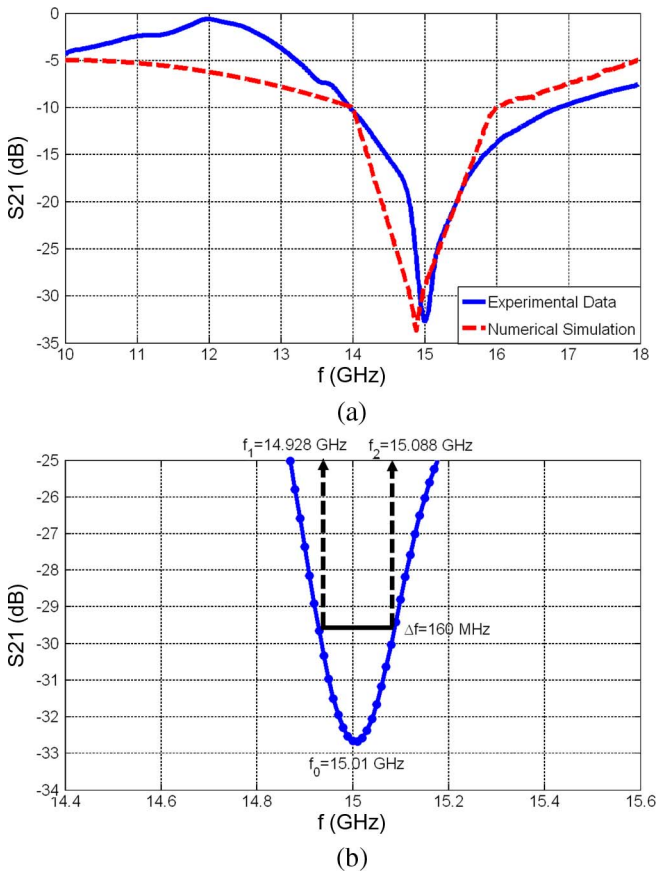

Fig. 9. (a) Experimental data and numerical simulation results for parameters, and (b) zoom-in experimental S_{21} data to illustrate the Q-factor extraction from the experimental data.

TABLE III
THEORETICAL AND EXPERIMENTAL RESONANCE FREQUENCY AND Q-FACTOR

f_0 (GHz)		Q-Factor	
Theoretical	Experimental	Theoretical	Experimental
14.88	15.01	98.77	93.81

We also consider other design parameter sets given in Table IV. In this table, Device-1 and Device-2 are the devices that have lower resonance frequencies than our device, which are optimally designed for their operating resonance frequencies with our design methodology. In addition, we used and inspected Device-1 in [9]. Device-3, Device-4, and Device-5 are the devices that have same resonance frequency as our device in this paper. In Fig. 10(a), we show the Q_{ind} factors of Device-1 and Device-2. In Fig. 10(b), we show the experimental S_{21} parameters of Device-1 as a function of operating frequency, and in Fig. 10(c), we show the experimental S_{21} parameters of Device-2 with respect to frequency. From Fig. 10(b) and (c), we

TABLE IV
DESIGN PARAMETERS OF SOME EXEMPLARY DEVICES WITH $N = 2$, $t_{ox} = 0.1$ μm, AND $t = 0.1$ μm. DEVICE-1 AND DEVICE-2 ARE OPTIMALLY DESIGNED FOR THEIR RESONANCE FREQUENCIES WITH OUR DESIGN METHODOLOGY. THE f_0 OF DEVICE-1 AND DEVICE-2 ARE EXPERIMENTAL VALUES WHILE THOSE OF DEVICE-3, DEVICE-4, AND DEVICE-5 ARE THEORETICAL VALUES. THE Q VALUES ARE EXPERIMENTAL AND Q_{max} VALUES ARE THEORETICAL

	L_c (μm)	W_c (μm)	w (μm)	s (μm)	f_0 (GHz)	Q	Q_{max}
Device-1	540	540	100	10	6.97	47.1	55.0
Device-2	1080	1080	200	20	3.58	28.1	33.3
Device-3	212	212	10	10	14.95		41.9
Device-4	270	270	5	20	15.05		23.7
Device-5	332	332	3	30	14.96		14.9

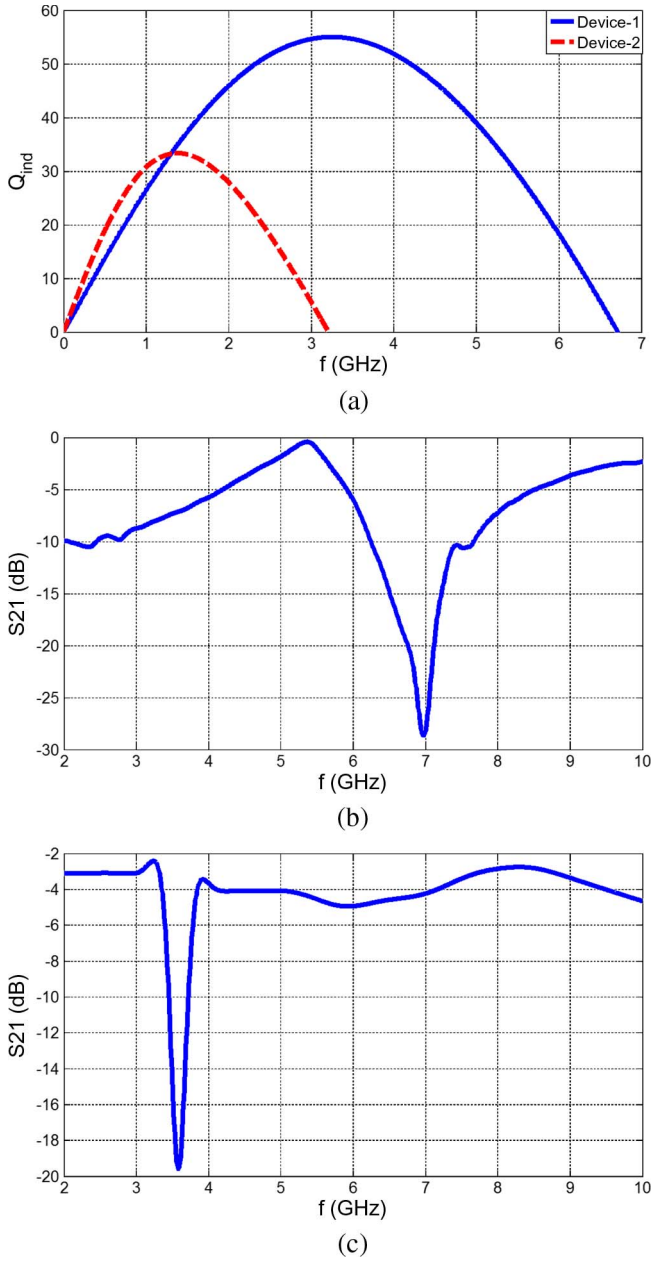

Fig. 10. (a) $Q_{\rm ind}$ of Device-1 and Device-2. (b) Experimental S_{21} parameter of Device-1 with respect to frequency. (c) Experimental S_{21} parameter of Device-2 with respect to frequency.

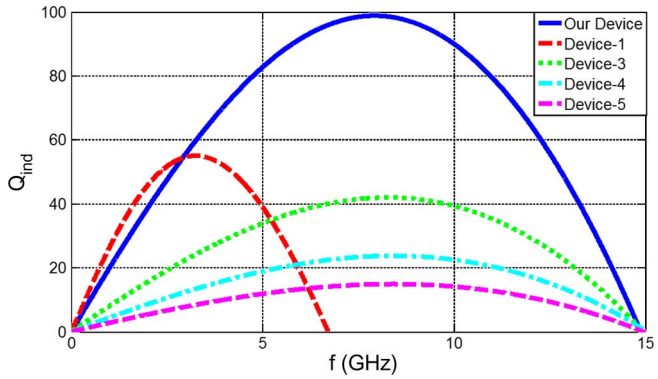

Fig. 11. $Q_{\rm ind}$ values of Our Device, Device-1 (where Our Device and Device-1 are optimally designed with our design methodology for their resonance frequencies), Device-3, Device-4, and Device-5.

find out that Device-1 has a resonance frequency of 6.97 GHz with a Q-factor of 47.1 while Device-2 has 3.58-GHz resonance frequency and 28.1 Q-factor. By comparing these results with our device results, we observe that, when the resonance frequency increases, the Q-factor increases. In Fig. 11, we show the $Q_{\rm ind}$ factors of our device, Device-1, Device-3, Device-4, and Device-5. We see that Device-3, Device-4, and Device-5 have almost the same resonance frequency as our device, but their $Q_{\rm max}$ is smaller than even Device-1, which has lower resonance frequency. From these results, we observe that Device-3, Device-4, and Device-5 will have lower Q-factors than our device in this paper. These results show that designs that are made using our design methodology yield higher Q-factors with higher $Q_{\rm max}$ levels for the same resonance frequency.

V. CONCLUSION

We have designed, fabricated, and demonstrated the operation of a 195 μm $\times$ 195 μm on-chip resonator on Si, working at 15 GHz with a Q-factor of 93.81, which is much larger than the Q-factors of the current state-of-the-art on-chip resonators that have been realized without cavity geometries. In addition, in the experimental transmission characterization, we observed a very strong dip of > 30 dB, which renders our design particularly useful for sensing applications. By using the two-port circuit model, we precisely set and controlled the device resonance frequency and Q-factor with the device parameters at the design stage. We observed an excellent agreement between our experimental measurement results and theoretical simulation results. Our approach is unique in its Q-factor optimized even for very high frequencies while avoiding the need for the use of an external capacitor. Thus, we have realized a fully on-chip resonator. In a typical design of such a device, increasing frequency decreases the Q-factor. However, using our new design technique, we achieved higher Q-factors at increasing frequencies even with smaller chip sizes. Such a high-Q on-chip resonator has a high potential for use in different high-frequency applications, particularly for telemetric-sensing applications where the changes in the transmission and resonance frequency are monitored.

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