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# Application of asymptotic waveform evaluation for time-domain analysis of nonlinear circuits

SATILMIŞ TOPÇU†, ABDULLAH ATALAR‡ and MEHMET A. TAN‡

A method is described to exploit asymptotic waveform evaluation (AWE) in the time-domain analysis of nonlinear circuits by using SPICE models for nonlinear devices such as diodes, transistors, etc. Although AWE has been used for linearized circuits only, the aim is to enhance the accuracy of the simulation while preserving the computational efficiency obtained with AWE and to eliminate the piecewise-linear modelling problem. Practical examples are given to illustrate significant improvements in accuracy. For circuits containing weakly nonlinear devices, it is demonstrated that this method is typically at least one order of magnitude faster than SPICE.



## 1. Introduction

Asymptotic waveform evaluation (AWE) (Pillage 1990) is a recent technique which is effective in the time-domain analysis of linear(ized) circuits (Huang 1990). It accurately produces a reduced-order model of the time-domain response of a linear circuit in terms of few dominant complex poles and residues. After it being developed by Pillage (1990), AWE has been applied to many CAD problems. A survey of all these studies and the evolution of AWE is presented by Raghavan (1993).

AWE is typically two or three orders of magnitude faster than traditional simulators in analysing large circuits. However, it can handle only linear(ized) circuits, whereas the time domain analysis problem is generally nonlinear due to the presence of nonlinear devices such as diodes and transistors in VLSI circuits. Previous attempts to apply AWE to the transient analysis of nonlinear circuits (Dikmen 1991, Kao 1992) solved this problem by using piecewise-linear (PWL) models for nonlinear elements. Although there exist programs that provide PWL models for given analytical expressions, it is difficult to find a good PWL model that fits well to the actual $i$–$v$ characteristics of a nonlinear device. The problem is that if the PWL model consists of a few segments, this reduces the accuracy level of the simulation results; but if the PWL model is formed with too many segments, this time the user suffers from very long simulation times. The method presented in this paper uses SPICE models for nonlinear elements in the circuit. Hence, there is no modelling problem and we can obtain very accurate results which can be useful, for instance, in evaluating the critical path in a given circuit. In addition to this, we can adjust the

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† Department of Electrical and Electronic Engineering, Eastern Mediterranean University, Gazimağusa, via Mersin 10, Turkey. Fax: +90 392 3669240; e-mail: topcu@eenet.ee.emu.edu.tr.

‡ Electrical and Electronics Engineering Department, Bilkent University, 06533 Bilkent, Ankara, Turkey.

accuracy level by varying some parameters. If the required level of accuracy is increased, more simulation time is needed, as expected.

We describe the method and explain the extraction of linear equivalents of nonlinear elements using SPICE models in § 2. In § 3 some examples are provided to illustrate the efficiency and accuracy of our method compared with the SPICE performance. Finally, our concluding remarks are given in § 4.

## 2. The method

Our method is a new approach using the AWE technique to find the time-domain response of nonlinear circuits containing diodes, transistors, etc. With the given SPICE models, our method can extract a linear equivalent for each nonlinear element about its bias point. For each nonlinear element, it can also calculate the error caused by the linear equivalent while the operating point moves to any arbitrary direction. We have an easily calculated error criterion used for this purpose. When the error of any nonlinear device exceeds a user-specified threshold at any time, the new linear equivalents are produced for all nonlinear elements about their present operating points. The steps of our method, for which a flowchart is given in Fig. 1, can be outlined as follows.

(*a*) Find the DC operating point of the circuit by using the Newton–Raphson iteration (Vlach 1983). This step is the first nonlinear DC analysis which gives the initial conditions.

(*b*) Obtain linearized equivalents for all nonlinear elements in the circuit. For a diode, this step is simply replacing the diode by a Norton equivalent which represents the tangent approximation to its *i*–*v* curve about the presumed operating point.

(*c*) Perform an AWE to find the time-domain behaviour of energy storage elements in the circuit.

(*d*) Increment the time by the internal time step: $t_{k+1} = t_k + \Delta t_k$. If the end time of the simulation is reached, then stop. Otherwise, continue with the next step.

(*e*) Solve the linear circuit equations to find the branch currents and branch voltages of nonlinear elements. Compute the error due to linear equivalents of individual nonlinear elements. If at least one of them has an error greater than a user-specified threshold value, then go to the step (*b*). Otherwise, go to step (*d*).

### 2.1. *Linearization of an MOS transistor*

In general, a nonlinear circuit may contain various types of transistors. Without loss of generality, we can concentrate on the MOS transistors. For simplicity, we have used the Level 1 MOSFET model of the SPICE (HSPICE 1992) which represents the basic device characteristics, including the body effect and the channel length modulation (Divekar 1988). The DC drain-to-source current $i_{ds}$ in the Level 1 MOS model is determined as follows.

Cutoff region: $v_{gs} \leq v_t$

$$i_{ds} = 0 \tag{1}$$

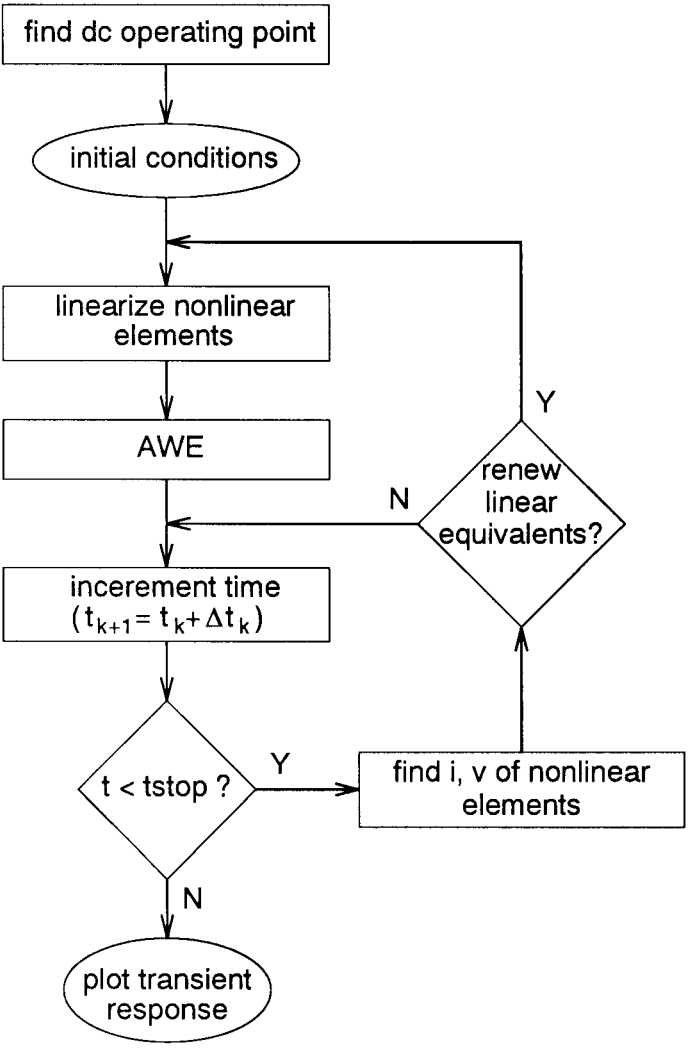


Figure 1. Flowchart for the nonlinear transient analysis.

Linear region: $0 < v_{ds} < v_{gs} - v_t$

$$i_{ds} = \beta(1 + LAMBDA \times v_{ds})\left(v_{gs} - v_t - \frac{v_{ds}}{2}\right) v_{ds} \tag{2}$$

Saturation region: $0 < v_{gs} - v_t \leq v_{ds}$

$$i_{ds} = \frac{\beta}{2}(1 + LAMBDA \times v_{ds})(v_{gs} - v_t)^2 \tag{3}$$

where

$$\beta = KP\left(\frac{W}{L}\right) \tag{4}$$

The threshold voltage is calculated as follows:

$$v_t = \begin{cases} VTO + GAMMA(\sqrt{PHI + v_{sb}} - \sqrt{PHI}), & \text{if } v_{sb} \geq 0 \\ VTO + GAMMA\left(0{\cdot}5\dfrac{v_{sb}}{\sqrt{PHI}}\right), & \text{if } v_{sb} < 0 \end{cases} \quad (5)$$

where *LAMBDA*, *KP*, *VTO*, *GAMMA* and *PHI* are the SPICE MOS model parameters (HSPICE 1992). The parameters $W$ and $L$ represent the width and length of an MOS transistor, respectively.

The linear DC equivalent circuit of an n-type MOSFET is given in Fig. 2. As may be seen, the transistor is modelled by a voltage controlled current source shunted by a conductance and a constant current source. In this linearized model, the drain-to-source current is calculated as follows:

$$I_{ds} = g_m v_{gs} + g_d v_{ds} + I_0 \quad (6)$$

where

$$g_m = \frac{\partial(i_{ds})}{\partial(v_{gs})} \quad (7)$$

$$g_d = \frac{\partial(i_{ds})}{\partial(v_{ds})} \quad (8)$$

$$I_0 = i_{ds} - g_m v_{gs} - g_d v_{ds} \quad (9)$$

The partial derivatives $g_m$ and $g_d$ are called the transconductance and conductance, respectively, and they are calculated in each operating region of the transistor as follows.

Cutoff region:

$$g_m = g_d = 0 \quad (10)$$

Linear region:

$$g_m = \beta(1 + LAMBDA \times v_{ds})v_{ds} \quad (11)$$

$$g_d = \beta(v_{gs} - v_t - v_{ds} + 2 \times LAMBDA \times v_{ds}(v_{gs} - v_t - 0{\cdot}75v_{ds})) \quad (12)$$



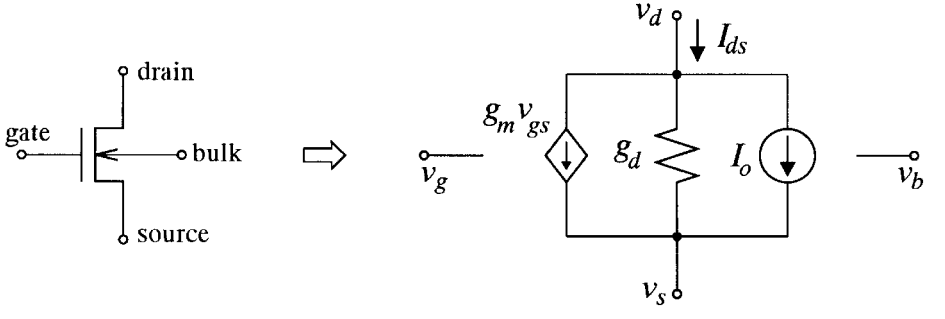


Figure 2. The linear DC equivalent circuit of an n-type MOSFET used in transient analysis.

Saturation region:

$$g_m = \beta(1 + LAMBDA \times v_{ds})(v_{gs} - v_t) \tag{13}$$

$$g_d = \frac{\beta}{2} LAMBDA(v_{gs} - v_t)^2 \tag{14}$$

2.2. *Deciding to renew the linear equivalents of nonlinear elements*

As seen in Fig. 1, after incrementing the time we must decide about whether the linear equivalents of nonlinear elements will be renewed or not. This decision is made by finding the difference between the actual $i$–$v$ characteristics of the device and the operating point calculated by using the linear equivalent. If this difference is greater than a user-defined threshold value, than the new linear equivalents are created for all nonlinear elements. For an MOS transistor, the difference mentioned above is equal to

$$\delta i = |i_{ds} - I_{ds}| \tag{15}$$

where $i_{ds}$ and $I_{ds}$ are the drain-to-source current values calculated from the SPICE Level 1 MOS model and the linear equivalent, respectively, using the branch voltages $v_{gs}$ and $v_{ds}$. Calculation of the difference in the case of a diode is shown in Fig. 3. As seen in Fig. 3, the diode has been linearized about $v_d = v_0$ and it is replaced by the Norton equivalent which consists of a current source of value $I_0$ shunted by a conductance $G_0$. In this case, when the diode branch voltage $v_d$ becomes equal to $v_1$, the difference between the linear segment and the nonlinear $i$–$v$ characteristics is $\delta i = i_d - I_d$. If the value of $\delta i$ is greater than a user-specified error tolerance limit, than a new linearization must be made for the diode at $v_d = v_1$. Note that, to find the error caused by the linear equivalents, we use the difference between current values

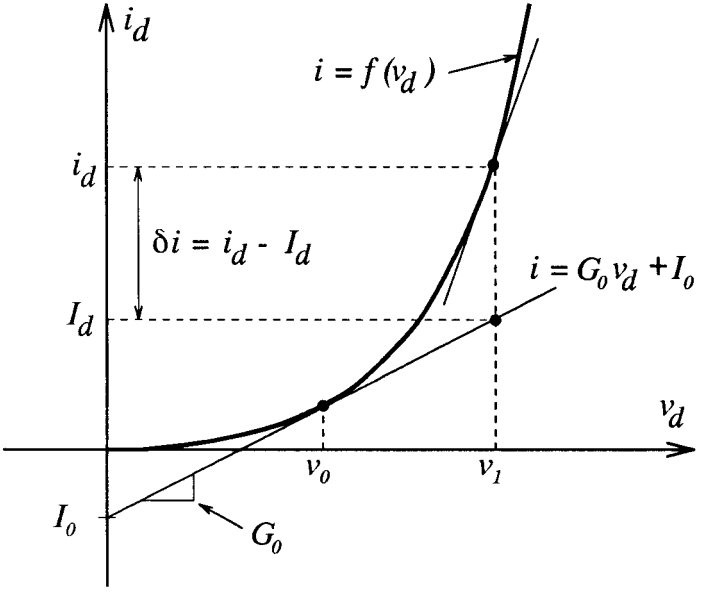


Figure 3. Calculation of the error resulting from a diode equivalent circuit.

instead of voltage values. Calculation of the difference in current values requires less computation than the calculation of the difference in voltage values, especially for three-terminal elements such as MOS transistors, because we concentrate on the voltage-controlled devices without loss of generality.

## 3. Results

To illustrate the accuracy performance of our method, we have chosen some example circuits. The first example is an opamp circuit with unity gain feedback, shown in Fig. 4. The schematic of the opamp (Gray 1983) is given in Fig. 5. The capacitors from each node to ground are not shown in Fig. 5, for clarity. We have used a pulse of small amplitude for the input voltage.

We have simulated this example circuit by using our method, HSPICE (HSPICE 1992) and SPICE3 (Quarles 1989) with different error thresholds. First of all, a reference result that is assumed to be very accurate is obtained by means of HSPICE using very tight error tolerance parameters and a very small internal time step. Then we have assumed this result to be the exact response of the circuit and all other simulation outputs are compared with this result to estimate their accuracy. The error in a simulation output is calculated by finding the average of absolute differences with respect to the exact response at every timepoints where the output waveforms are printed. That is

$$\text{average absolute difference} = \frac{1}{N}\sum_{k=1}^{N}\left|v_{\text{exact}}(t_k) - v_c(t_k)\right| \tag{16}$$

where $v_{\text{exact}}(t)$ and $v_c(t)$ are the exact and calculated responses of the circuit, respectively. For all simulations, $N$ is chosen as 1000. The accuracy versus number of timepoints for our method, HSPICE and SPICE3 is plotted in Fig. 6 for the opamp circuit. Here, the horizontal axis denotes the number of timepoints that a simulator needs to take to preserve the corresponding accuracy. At each timepoint HSPICE or SPICE3 performs a Newton–Raphson iteration whereas our method performs, in addition to Newton–Raphson, an AWE which costs one LU-decomposition and a few forward-backward substitutions (FBSs). This means that, for a single timepoint, our method spends approximately twice as many CPU seconds than HSPICE or SPICE3. It is assumed that one FBS takes negligible CPU time compared to the time taken by one LU-decomposition for large circuits.



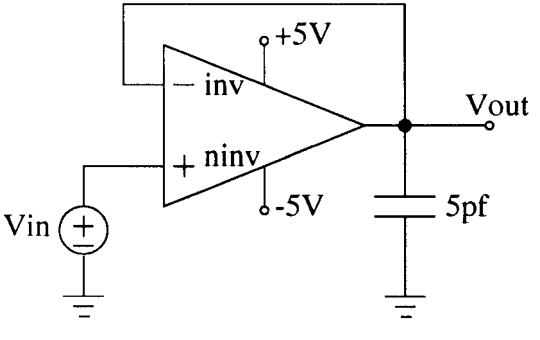


Figure 4. Opamp circuit with unity gain feedback.

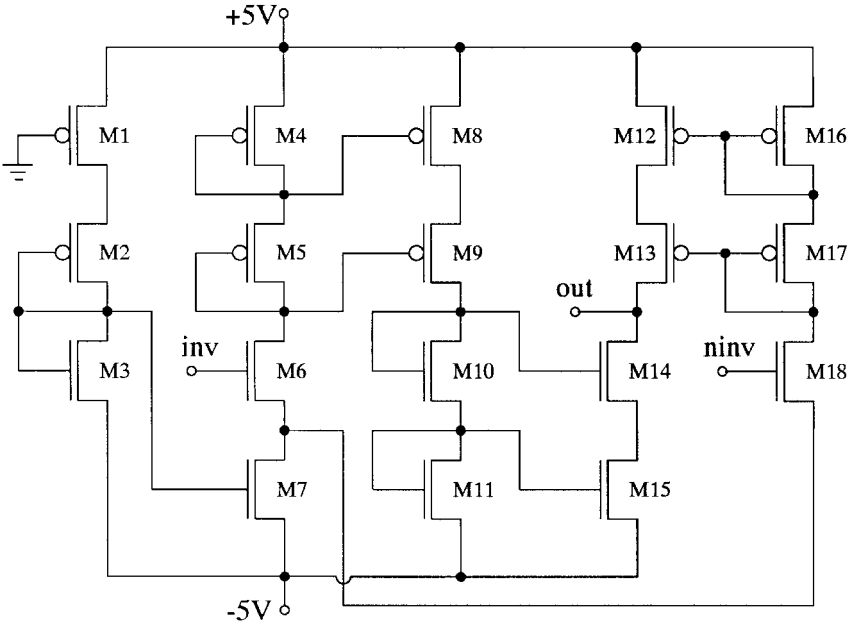


Figure 5. Schematic of the operational amplifier at transistor level.

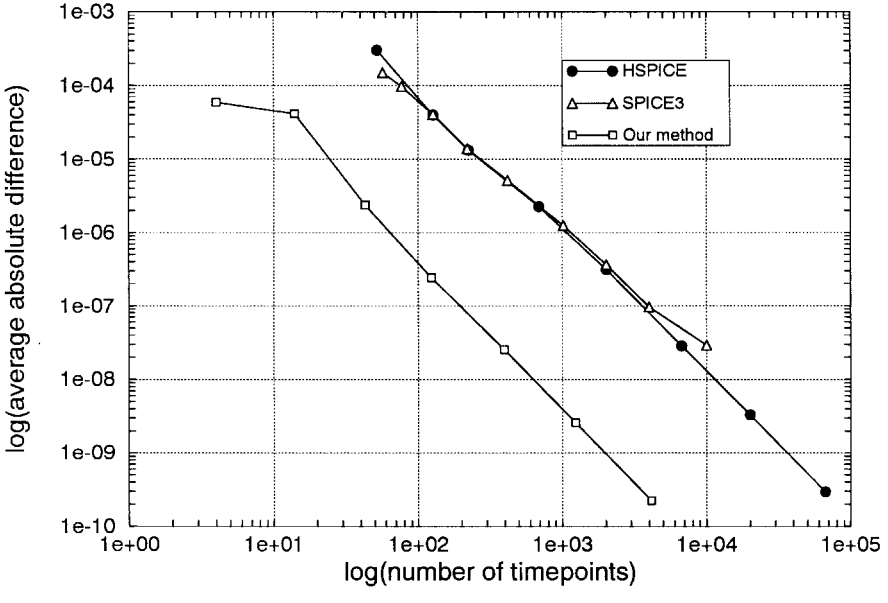


Figure 6. Accuracy comparison between our method and SPICE for the opamp circuit.

It is observed from Fig. 6 that HSPICE and SPICE3 have the same accuracy versus speed graphs because both of them are using a trapezoidal integration algorithm in the transient analysis. It is seen that our method can produce transient responses which are accurate up to nine significant digits and it requires approximately $\frac{1}{20}$ of the number of timepoints needed by HSPICE to provide the same

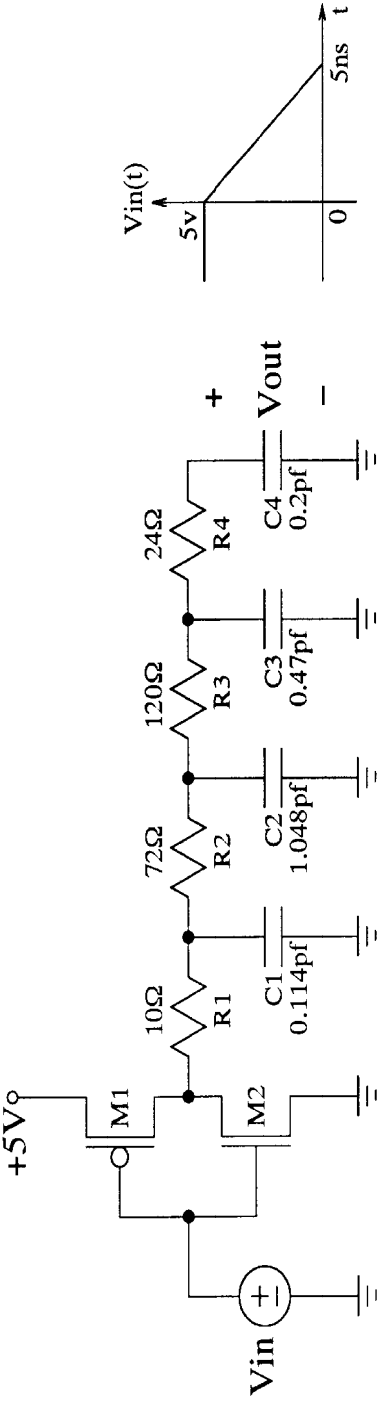


Figure 7. RC tree driven by a CMOS inverter and the input voltage function.

accuracy. If the user agrees to obtain less accurate results, such as having an error about $10^{-4}$, this ratio becomes $\frac{1}{30}$. Then our method becomes approximately 15 times faster than HSPICE or SPICE3.

Our second example, given in Fig. 7, is a small RC tree driven by a CMOS inverter. This circuit is chosen as an example to explore the effect of inserting nonlinear elements into a linear circuit for which AWE provides very accurate results efficiently. Again, by using HSPICE we have obtained a reference result which is assumed to be extremely close to the exact result. Then we have simulated the example circuit using our method and HSPICE by changing the error tolerance parameters. These simulation results are compared with the reference result to estimate their accuracy levels. We have plotted the graph in Fig. 8 which shows the accuracy versus number of timepoints required by each simulator. It is observed from Fig. 8 that if the desired accuracy is low, our method is several times faster than HSPICE. However, when the accuracy is increased, both simulators need approximately the same number of timepoints.

In the third example, shown in Fig. 9, we have inserted additional MOS transistors into the second example to increase the number of nonlinear elements in the circuit. In a similar way to the previous example, we have obtained the graph of accuracy versus number of timepoints required by our simulator and HSPICE. The resultant graph is shown in Fig. 10. It can be observed from Fig. 8 and Fig. 10 that increasing the number of nonlinear elements inserted into a linear circuit causes a degradation in the speed performance of our method. Because the overall nonlinearity of the circuit is increased by additional MOS transistors, we need to renew the linear equivalents for the nonlinear elements more frequently as time goes on.



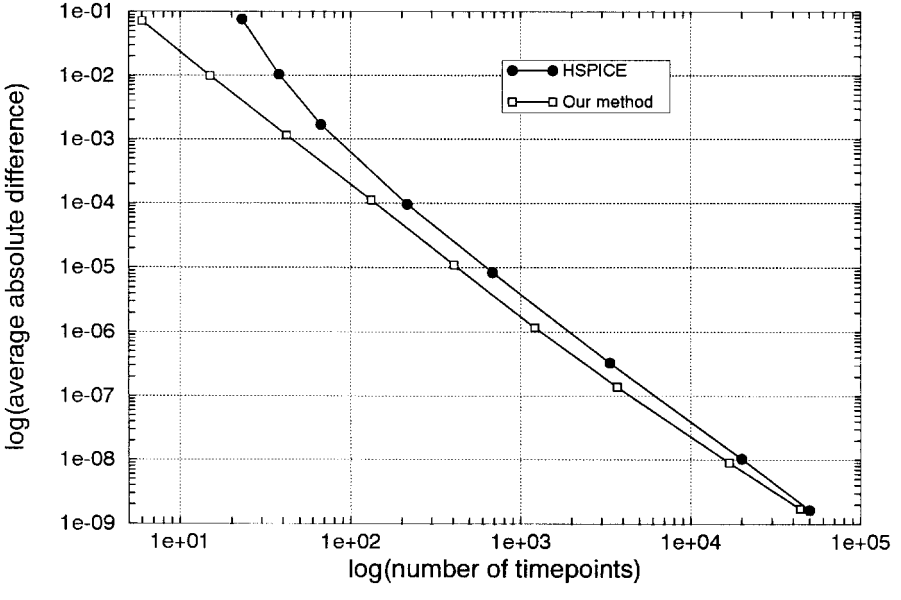


Figure 8. Accuracy versus speed graphs for our simulator and HSPICE in the second example.

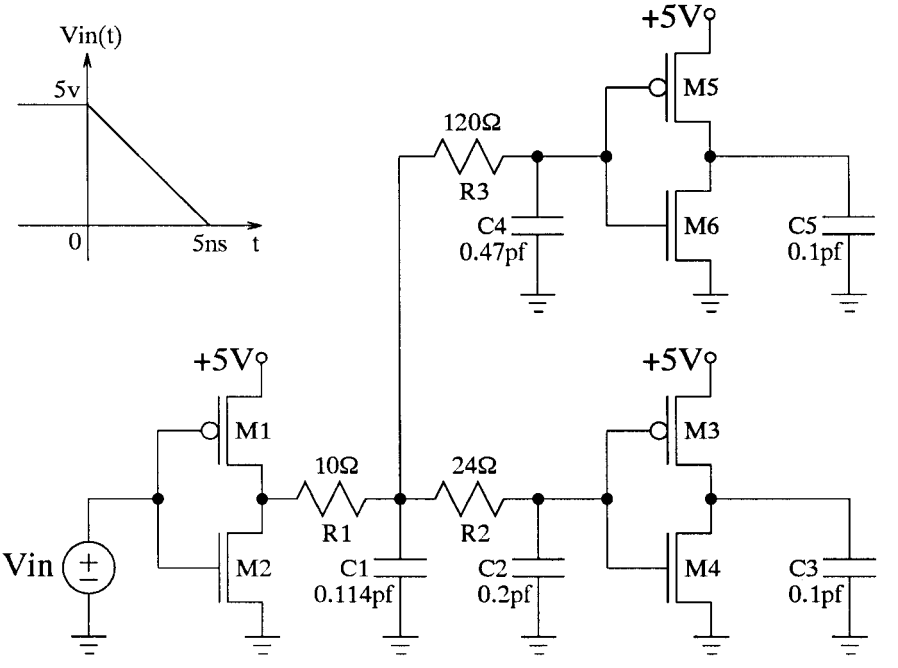


Figure 9. Two CMOS inverters driven by the same inverter.



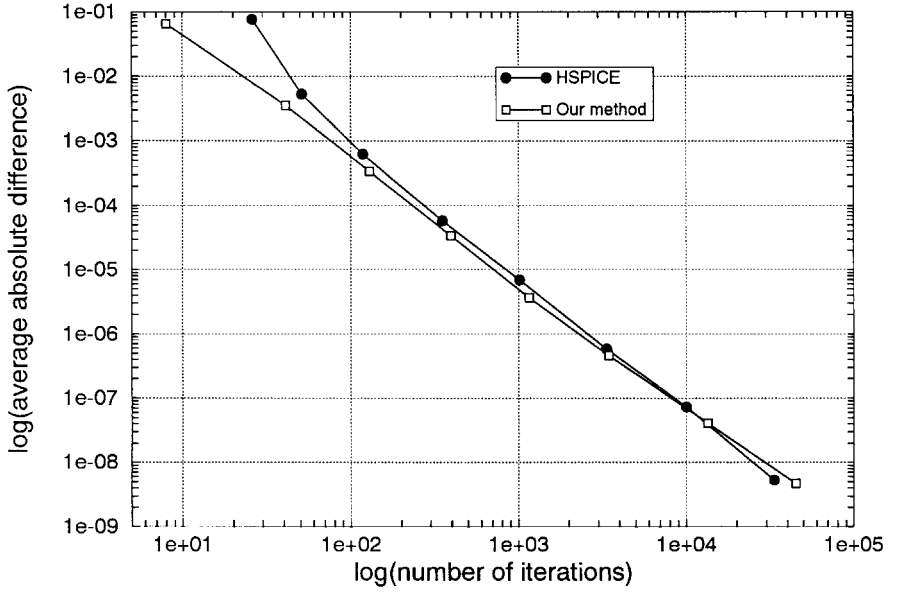


Figure 10. Accuracy versus speed graphs for our simulator and HSPICE in the third example.

## 4. Conclusions

A new method is proposed to apply the AWE technique to the time-domain analysis of nonlinear circuits. The existing approaches which addressed this problem have utilized the PWL modelling for nonlinear elements. However, those methods have two major drawbacks: Finding good PWL models for nonlinear elements is a difficult problem; and PWL approximation results in low accuracy in time-domain responses. Our method overcomes these disadvantages by using the SPICE models for nonlinear elements. In our method, by means of error tolerance parameters the accuracy level of the simulation can be adjusted by the user. The software implementation of the method is very easy. We have presented some examples to show the efficiency and the accuracy performance of the method and to compare them with those of SPICE. The method is capable of providing an accuracy of $10^{-9}$ which cannot be obtained by the PWL modelling approach.

It is observed from the examples that our method is of advantage in situations when weak nonlinear circuits are studied. However, just for those cases, PWL AWE is also possible but our method is considerably superior to PWL AWE in terms of accuracy. As the nonlinearity of a circuit is increased by inserting additional nonlinear elements, the efficiency of the method begins to decrease. That is, it will work for mild nonlinearities where the accuracy of SPICE is dictated by local truncation error of trapezoidal integration algorithm. Unfortunately, we can say that for large circuits with many nonlinear elements it may take more CPU time than taken by HSPICE to preserve the same accuracy level.



### Acknowledgment

HSPICE is a trademark of Meta-Software Inc.

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