Development of a miniaturized spectrum-type plasma wave receiver comprising an application-specific integrated circuit analog front end and a field-programmable gate array

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Title: Development of a miniaturized spectrum-type plasma wave receiver comprising an ASIC analogue front end and an FPGA

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Abstract
Plasma waves are an important target for satellite-based in-situ observation to understand electromagnetic phenomena in space. Recent scientific satellites have carried fast Fourier transform (FFT)-based spectrum receivers; however, such receivers have a disadvantage because they use wideband analogue part. The new receiver overcomes the disadvantage by adding bandlimiting in the first stage of the analogue part, and it covers the entire observation frequency range of each band by switching its cutoff frequency. In order to miniaturize circuit size, the new receiver comprises an application-specific integrated circuits (ASICs) and a field-programmable gate array (FPGA). The ASIC chip includes the analogue part of the receiver and the analogue-to-digital converter, and the FPGA includes an FFT module and the controller of the receiver. The proposed spectrum receiver was successfully implemented with a size of 55 mm × 80 mm × 35 mm and a total power consumption of 948.3 mW. The time resolution of the receiver was 112 ms, and the frequency resolutions for frequency bands from 10 Hz to 1 kHz, from 1 kHz to 10 kHz, and from 10 kHz to 100 kHz were 13 Hz, 130 Hz, and 1.3 kHz, respectively. Overall, the developed receiver showed sufficient performance for plasma wave observation.

1. Introduction

Space is filled with diluted plasmas, and they change their kinetic energy through interactions with plasma waves. Thus, the observation of plasma waves is important in understanding plasma phenomena; in particular, in-situ observations of plasma waves via satellites are essential for the investigation of local physical processes [1]. Consequently, plasma wave observations by plasma wave instrument on board scientific satellites have been carried out [2-5].

Plasma wave receivers that observe plasma waves combining with sensors are categorized into two types, waveform receivers and spectrum receivers [6]. Spectrum

receivers have an advantage of the continuous observation of plasma waves because of smaller data generation rate than that of the waveform receivers [7]. Most of recent scientific satellites have carried spectrum receivers based on onboard fast Fourier transform (FFT) calculations. For instance, the Arase satellite which is launched to explore in the Earth's radiation belt, carries the plasma wave instrument named Plasma Wave Experiment (PWE), and the onboard frequency analyzer (OFA), which is one of the receivers installed in the PWE, is an FFT-based spectrum receiver [5]. The FFT-based receiver is composed of a wideband receiver and a digital signal processor. The wideband receiver measures waveform, and the digital signal processor execute FFT calculation. These FFT-based spectrum receivers have the advantage of providing flexibility in the balance between frequency and time resolution; however, they also have a disadvantage which stems from its widebandness. In wideband receivers, the gain of the receiver must be set for the most intense waves in the observation frequency range. This causes the sensitivity to weaker waves to become worse when multiple waves with different intensities are received. To resolve this disadvantage, the spectrum receiver must contain individual narrowband analogue circuits; however, this leads to the increased size and weight of the receiver.

The authors have previously proposed a new spectrum receiver to overcome the above disadvantage and developed the analogue part of the receiver, which is the core component of the new receiver [8]. The proposed spectrum receiver applies narrowband amplification and measures a wide frequency range by switching the observation band. It gets the frequency spectrum by applying the FFT to the waveform in each observation band. This new spectrum receiver cannot be realized without using the application-specific integrated circuits (ASICs), because the size of the receiver should be large in the development using commercial discrete electronic parts. The ASIC allows us to implement necessary circuits on a chip by designing it by ourselves. Zushi et al. (2017) introduced the successful development of the chip for the new spectrum receiver and verified its functions and performance [8]. Zushi et al. (2017) focused on the design of the analogue circuits on the chip and substituted the necessary digital parts such as FFT calculations including an analogue-to-digital converter (ADC) with the PC.

In this study, the proposed spectrum receiver was implemented and assessed using an ASIC and a field-programmable gate array (FPGA). The ASIC chip containing all components for analog front end of the receiver: the improved analogue part developed in Zushi et al. (2017) and an ADC. Because the receiver requires a digital processor to calculate the frequency spectrum and control each component of the receiver, a digital

part was designed and implemented using a FPGA. Finally, the proposed receiver was realized using the ASIC analogue front end and the FPGA.

The present paper describes in detailed design and performance of the new receiver. A design summary of the receiver is given in Section 2. In Section 3, each component of the developed receiver is described, and the overall performance of the receiver is shown in Section 3.3.

2. Receiver overall design

This section introduces the design summary of the new spectrum receiver. As mentioned in the Introduction, the gain of wideband receivers must be set for the most intense waves in the observation frequency range, and it leads to decreasing the sensitivity. To avoid this disadvantage, the new spectrum receiver was proposed [8]. The new receiver has a filter for bandlimiting in the first stage, and it covers the entire observation frequency range of each band by switching its cutoff frequency. Figure 1 shows a simplified block diagram of the new receiver. The components of the receiver consist of three parts: the analogue part, the ADC, and the digital part. The analogue part is composed of a bandlimiting filter, a main amplifier, and an anti-aliasing filter. The main role of the analogue part is to bandlimit and amplify the signals of plasma waves picked up by sensors. The signal through the analogue circuits is digitalized at the ADC. The digital part includes an FFT module and a controller of the receiver function. The digitalized signal is transferred to the FFT module, and the calculated frequency spectrum is output as a final result.

The frequency coverage of the new receiver is 10 Hz to 100 kHz, and it measures the entire frequency range by dividing it into following three observation bands: 10 Hz to 1 kHz (Band 1), 1 to 10 kHz (Band 2), and 10 to 100 kHz (Band 3). The receiver changes its observation frequency band by changing the following three properties: the gain frequency response of the analogue part, the sampling frequency of the ADC, and the signal input rate of the FFT module. The controller controls these properties by outputting digital signals for each component. The configuration of filters implemented inside the analogue chip is changeable by the external digital signal to enable the change of cutoff frequencies. The controller maintains the state of the receiver and changes the state in accordance with a predetermined sequence.

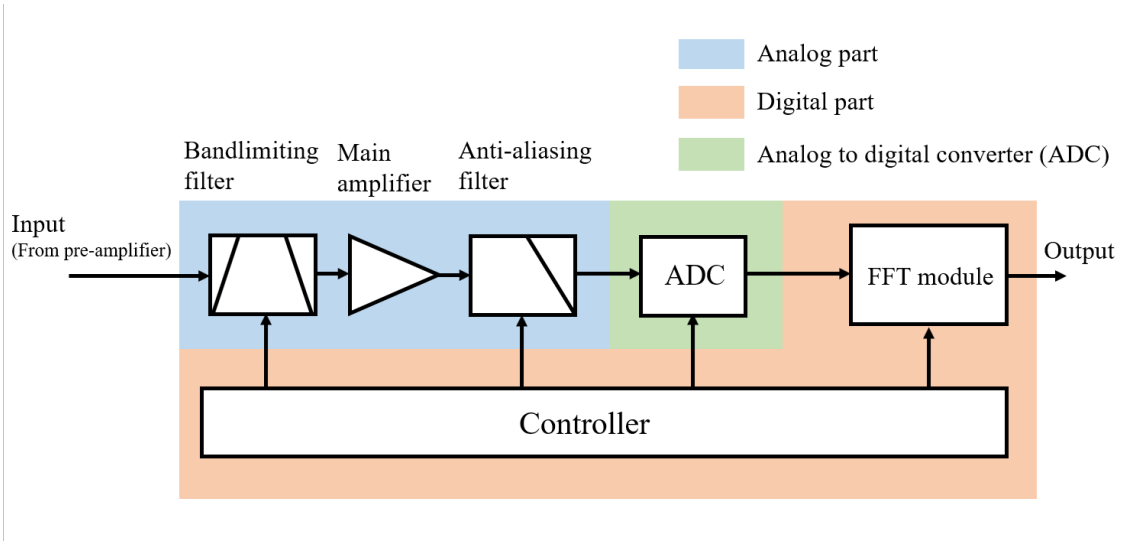


Figure 1. Block diagram of the proposed spectrum plasma wave receiver.

3. Description and characteristics of the developed receiver components

To confirm the performance of the new receiver, a prototype of the new receiver was constructed. In this receiver, the analogue front end was implemented as an ASIC chip. The ASIC chip includes the bandlimiting filters, main amplifier, anti-aliasing filter, and ADC shown in Figure 1. The detailed design of the ASIC analogue front end is described in Section 3.1. The hardware-based architecture was selected in the digital part considering processing speed and power consumption. In the developed receiver, the digital part was designed using Verilog HDL and implemented using an FPGA. The detailed design of the digital part is presented in Section 3.2.

3.1 ASIC analogue front end

The analogue front end of the receiver was implemented as an ASIC chip. It includes all analogue circuits for the receiver and an ADC. The chip was developed using a complementary metal–oxide–semiconductor (CMOS) 0.25-μm mixed-signal process provided by Taiwan Semiconductor Manufacturing Co., Ltd. The power supply voltages of the circuit are 3.3 V for the analogue components and the analogue part of the ADC and 2.5 V for the digital part of the ADC.

The design of the analogue part is based on the previously developed analogue ASIC chip, and the detailed circuit design is given in Zushi et al. (2017). From the previous design, the design of the anti-aliasing filter is modified to improve the flatness of the gain frequency response within the passband. The analogue circuits include three components: a bandlimiting filter, a main amplifier, and an anti-aliasing filter. The

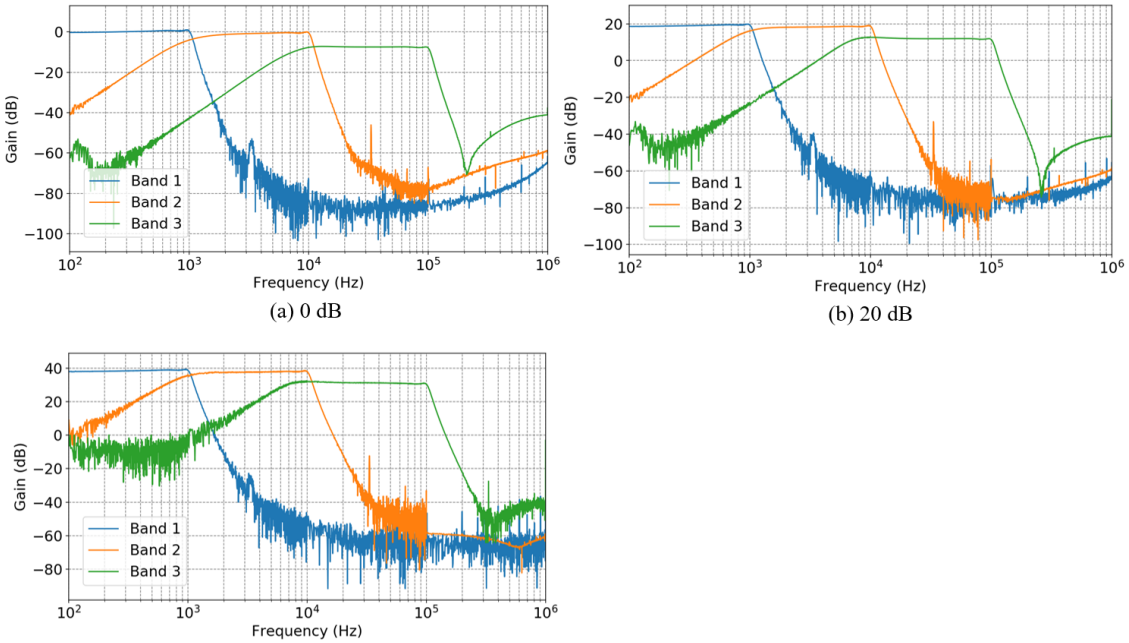
characteristics of the analogue components can be changed depending on the external signal, and the receiver has three measurement frequency bands. To change the observation band, the filters are able to switch their cutoff frequency depending on the external control signal. The control signal for the analogue circuits is a 2-bit digital signal, and internal logic gates decode the control signal and send an appropriate signal to each component. The gain of the main amplifier can also change by the external signal to one of three modes: 0, 20, and 40 dB. The gain frequency response of the analogue components is shown in Figure 2, and the equivalent input noise level is shown in Figure 3. The frequency responses of the analogue part are significantly improved in the passband in each mode comparing with that in the previous design of Zushi et al. (2017) [8]. In each plot in Figure 3, the noise level within the observation band is represented by a vivid color. Table 1 gives the gain in the passband for each observation frequency band. The circuits have a flat response within the passband and steep damping characteristics at the upper cutoff frequency because of the anti-aliasing filter. Because the demand for the damping characteristics of the bandlimiting at lower frequencies is not so strict, the circuit has more gentle damping characteristics at the lower cutoff frequency than at the upper cutoff frequency. The passband gain in Band 3 is lower than those in Bands 1 and 2 because of attenuation in the bandlimiting filter.

We adopt a design of the commercial device as the ADC which is developed by ASO Inc. and SiliConsortium Ltd. The ADC has a pipeline-type architecture, 14-bit resolution, and a maximum sampling frequency of 33 MHz. Its output latency is 13 clocks. The sampling data are output in a parallel line directly connected to the FPGA in the receiver.

Figure 4 shows the circuit layout of the ASIC. The analogue components and ADC occupy areas of 4.5 mm × 1.2 mm and 3.2 mm × 0.8 mm, respectively. The final packaged chip used in the developed receiver has dimensions of 1.5 cm × 1.5 cm.

Table 1. Passband gain of the analogue part for each gain and frequency band.

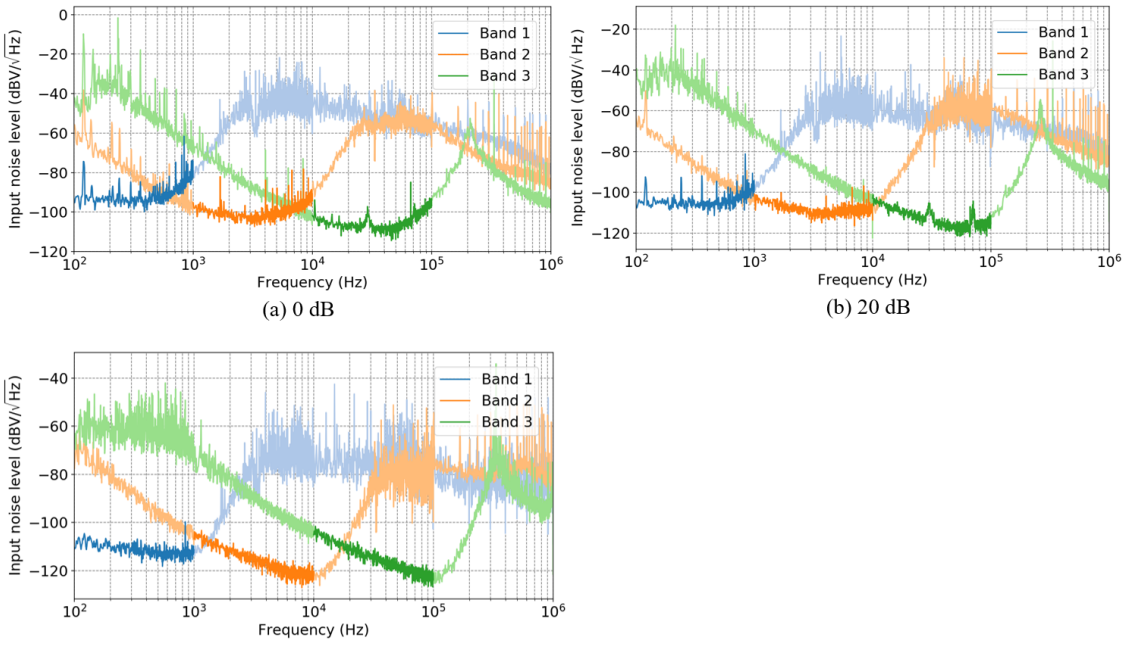
	Band 1 (at 500 Hz)	Band 2 (at 5 kHz)	Band 3 (at 50 kHz)
0 dB	0.42	0.6	-7.45
20 dB	19.27	18.47	11.96
40 dB	38.76	37.86	31.13



(a) 0 dB (b) 20 dB

(c) 40 dB

Figure 2. Typical gain frequency response of the analogue part.



(a) 0 dB (b) 20 dB

(c) 40 dB

Figure 3. Input equivalent noise density of the analogue part.

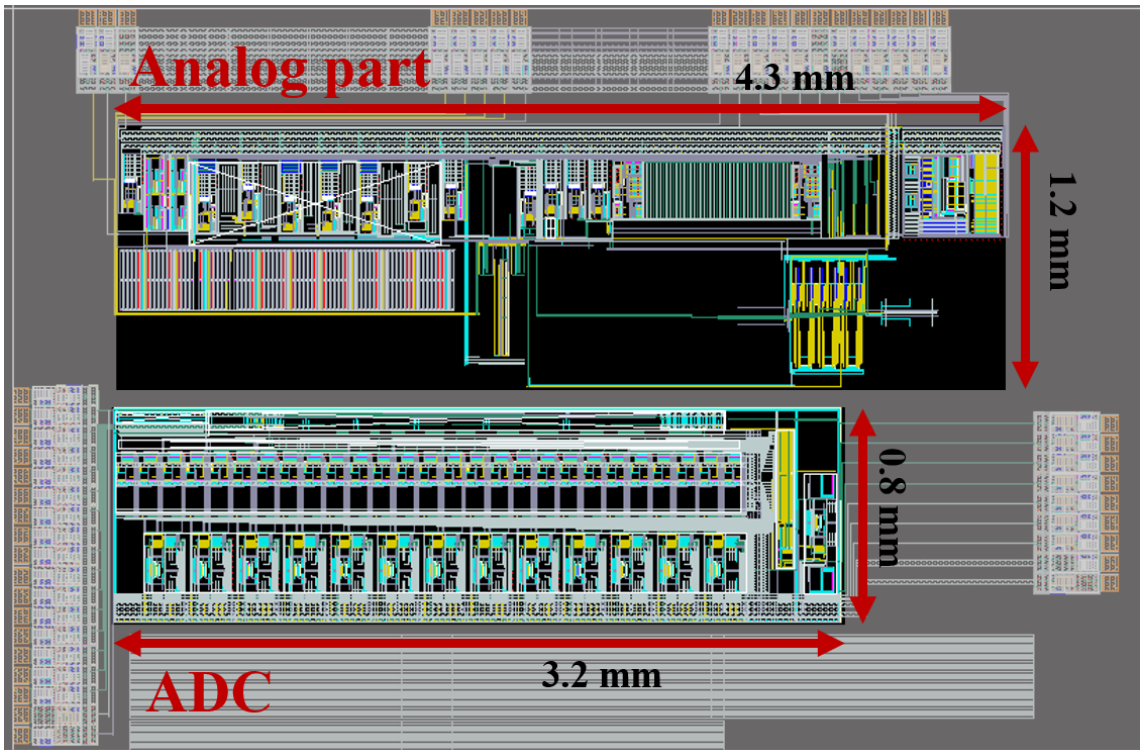


Figure 4. Circuit layout of the ASIC.

3.2 Digital part

All components of the digital part are implemented in the FPGA. The receiver uses the DE0-Nano development board (Telasic), which includes the Cyclone IV EP4CE22F17C6N FPGA (Intel) and peripheral circuits. Figure 5 shows a block diagram of the digital part, which comprises the FFT module, the controller, and the output buffer. The FFT module executes a 256-point FFT calculation, and the controller controls all the components, including the digital part.

The FFT module calculates the complex frequency spectrum from the 256 sampled data points. The operating frequency of the module is 10 MHz, and the calculation time is 839 clocks. The numbers of bits for input and output are 14 and 37 bits, respectively. The output data are composed of the real and imaginary parts of the spectrum, each of which has 18 bits. In addition, the FFT module outputs an “FFT finish” signal to indicate the end of the calculation. These 37 bits are output from the FFT module, and all signals are output in parallel and synchronously with the master clock. To reduce the number of output pins, the FFT results are output through the buffer. In addition to the output from the FFT module, a 2-bit receiver state signal is output from the controller. The signal indicates the current receiver state to determine the frequency band of the output data.

The controller outputs control signals for the analogue part, ADC, FFT module, and output buffer. For the analogue part, the controller outputs signals to determine the observation band of the analogue part. The controller controls the sampling frequency of the ADC by an output sampling clock. For the FFT module, the controller outputs signals to set the input rate and calculation start time. The controller changes from one state to the next based on the time.

Figure 6 shows the time sequence of the receiver. The receiver has six states: 1A, 1B, 2A, 2B, 3A, and 3B. The receiver performs an observation when the state is 1B, 2B, or 3B. The difference between these three states is the observation band of the receiver. States 1B, 2B, and 3B correspond to the observation of Bands 1 (10 Hz to 1 kHz), 2 (1 to 10 kHz), and 3 (10 to 100 kHz), respectively. When the state is 1A, 2A, or 3A, the receiver stops observation to avoid measuring the transient response accompanying a change in the observation band. Using this waiting time, the FFT module calculates and transfers the frequency spectrum from the sampling data received in the immediately preceding state. The bottom of Figure 6 shows the detailed sequence of the calculation and data transfer times.

The waiting times for 1A, 2A, and 3A are 20, 2.0, and 0.2 ms, respectively. These times are determined from the measurement results of the settling time. Because the total time for the FFT calculation and result output is 0.14 ms, the FFT module can finish preparing for the next observation band within the waiting time. The waiting times for 1B, 2B, and 3B are determined from the time to measure 256 points with the sampling frequency of the corresponding band including the ADC latency of 13 clocks, and the observation times in 1B, 2B, and 3B are 81, 8.1, and 0.81 ms, respectively. The time resolution of the receiver is 112 ms, which is the total time required to measure the three observation bands. The frequency resolutions for Bands 1, 2, and 3 are 13 Hz, 130 Hz, and 1.3 kHz, respectively.

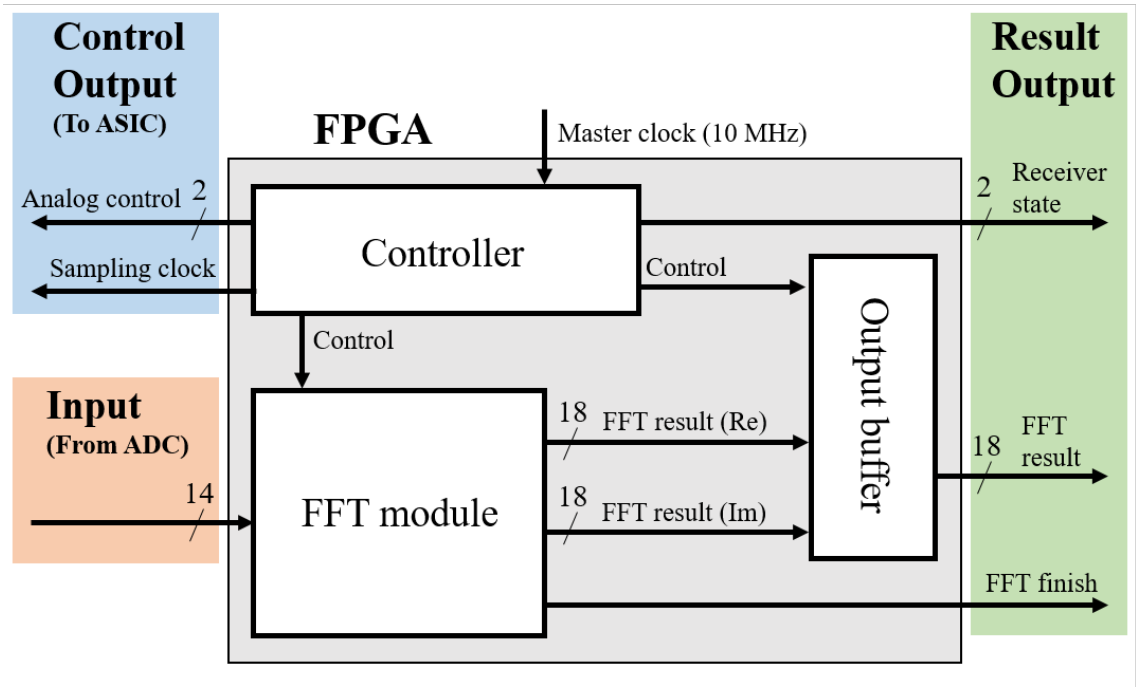


Figure 5. Block diagram of the digital part.

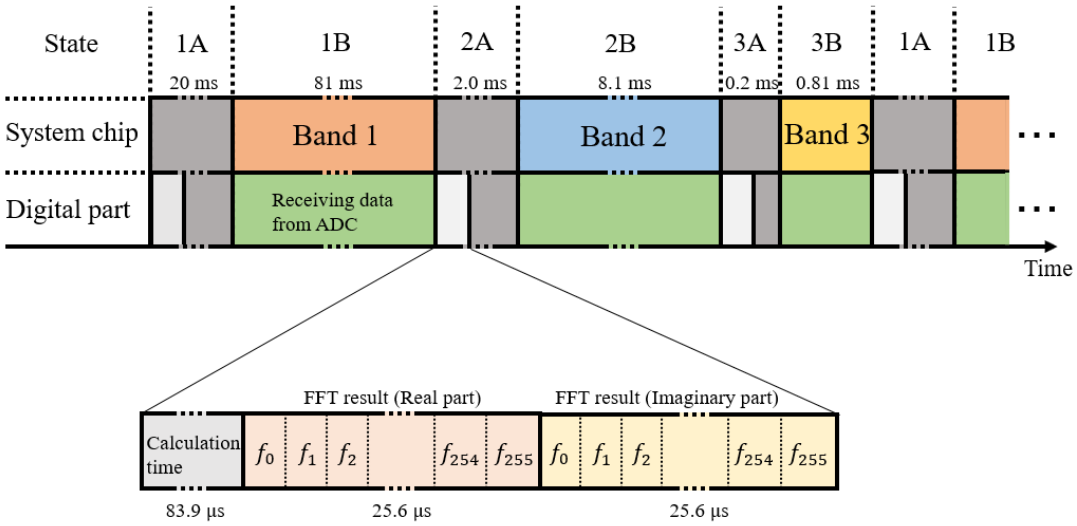


Figure 6. Time sequence of the receiver.

3.3 Overall performance

Figure 7 shows a photograph of the developed receiver. The ASIC analogue front end was implemented on a prototyping board designed as a daughter board for the FPGA board. The size of the receiver is 55 mm × 80 mm × 35 mm. The power consumption of

each component is given in Table 2. Because the power consumption depends on the state of the receiver, Table 2 gives the consumption averaged over the whole observation cycle.

The sample output of the receiver is shown in Figure 8. In the sample output, the input signal is a sinusoidal wave with a frequency of 20 kHz and amplitude of 100 mV, and the gain of the receiver is 0-dB mode. Figure 9 shows the equivalent input noise level of the proposed receiver. The blue line shows the noise level of the analogue part, and it is the same as the noise level within the observation band of each band mode shown in Figure 3. The noise levels of the receiver are almost the same with that of the analogue circuit in the 20- and 40-dB modes; however, at 0-dB mode, the noise level of the receiver is always higher than that of analogue circuit. The cause of increasing noise level is noise from ADC. Because the output noise level in the 0-dB mode is the lowest among all gain modes, the effect from ADC is appear only in the 0-dB mode.

Component	Analogue part	ADC	FPGA	Total
Power	42.9 mW	455.4 mW	450.0 mW	948.3 mW

Table 2. Power consumption of the developed receiver.

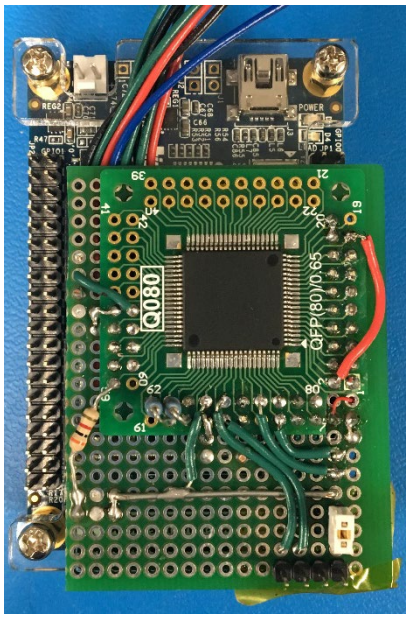


Figure 7. Photograph of the developed receiver.

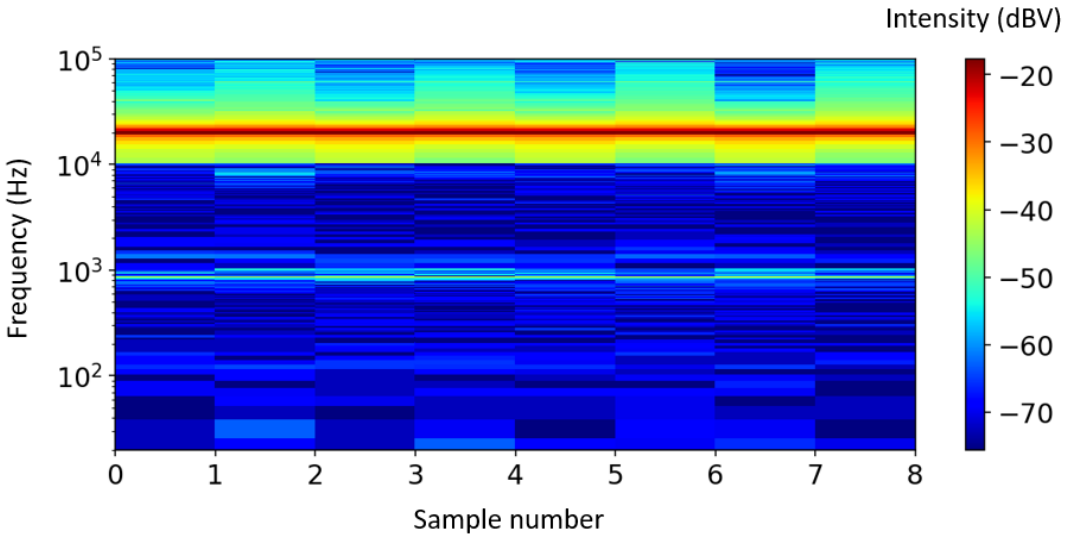


Figure 8. Sample output of the new receiver.

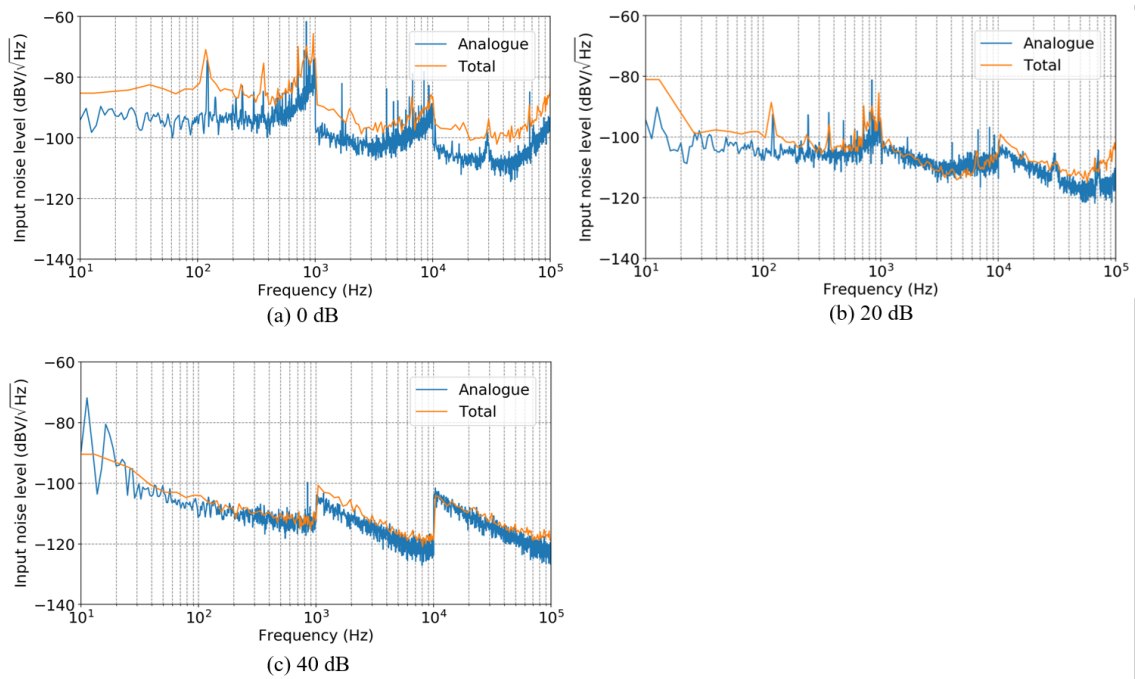


Figure 9. Input equivalent noise level of the new receiver.

4. Conclusion

The observation of plasma waves is essential for understanding the electromagnetic environment in space. In recent missions, the FFT-based spectrum receiver is generally

used because it has advantages in saving instruments size and flexibility in the balance between frequency and time resolution. However, the conventional FFT-based receiver has a disadvantage caused by its widebandness. We proposed the new spectrum receiver which overcomes the disadvantage, and we developed the ASIC analogue circuit for the new receiver in order to miniaturizing the receiver (Zushi et al. 2017). In this study, the entire new spectrum receiver was implemented using an ASIC analogue front end and an FPGA digital part. The ASIC analogue front end includes an analogue part for the receiver and an ADC in a 1.5 cm × 1.5 cm chip. The FPGA digital part includes an FFT module, a data buffer, and a controller for the receiver. The new receiver was successfully implemented, and it was then verified that the developed receiver is suitable for plasma wave observation.

In this study, the new receiver was developed using an FPGA board and a prototyping board without considering the environmental conditions for practical use in space. Consequently, when used in a space mission, the ASIC, FPGA, and peripheral circuits should be installed on a printed circuit board. In addition, selection of another FPGA is necessary for missions which require radiation resistant because the Cyclone IV EP4CE22F17C6N is non space-grade.

The implemented receiver verified the previously developed design of the proposed spectrum receiver, especially its digital part using an FPGA. Because the digital part was designed using Verilog HDL, a digital part with the same function as an ASIC can be implemented, and future work will involve the development of a mixed-signal ASIC that includes all of the components of the proposed receiver. This "one-chip receiver" would have the advantage of being easily mass produced in addition to reduced size and power consumption. Because of these features, the new receiver is well-suited for multiple-point observations using microsatellites. The proposed receiver is expected to make a big contribution to realizing the multiple-point observation of plasma waves.

Acknowledgments

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