Design and Implementation of Simplified Sliding-Mode Control of PWM DC-DC Converters for CCM

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By

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Humam A. Al-Baidhani ENTITLED Design and Implementation of Simplified Sliding-Mode Control of PWM DC-DC Power Converters for CCM BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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Abstract

Al-Baidhani, Humam A. Ph.D., Department of Electrical Engineering, Wright State University, 2020. *Design and Implementation of Simplified Sliding-Mode Control of PWM DC-DC Converters for CCM.*

The pulse-width modulated (PWM) dc-dc converters play a vital role in several industrial applications that include motor drives, electric vehicles, dc distribution systems, and consumer electronics. The switched-mode power converters step the input voltage up or down based on their typology and provide a regulated output voltage. The stability and regulation performance of a power converter can tremendously be improved via a suitable control design. However, due to the nonlinearity of the power converters and the presence of the line and load disturbances, the design of a robust and low-cost control circuit becomes a challenging task. The sliding-mode control of the dc-dc converters has been studied for decades because of its robustness, design simplicity, and suitability for variable structure systems. Despite the merits of the sliding-mode control method, the linear controllers are still dominant and attractive to the commercial applications since they require less design efforts and can be implemented using simple analogue circuits.

This research aims to develop simplified sliding-mode control circuits for the classical PWM dc-dc converters in continuous-conduction mode (CCM). The control objectives are to maintain a constant switching frequency, enhance the transient response, provide wide operating range, and track the desired reference voltage under large disturbances. In order to design and test the control circuit, an accurate power converter model should be derived. Hence, large-signal non-ideal averaged models of dc-dc buck and boost converters in CCM are developed. The models are simulated in MATLAB/SIMULINK and compared with the corresponding circuits in SaberRD simulator for validation purpose. Next, PWM-based simplified sliding-mode voltage

and current control schemes are designed for the dc-dc buck and boost converters in CCM, respectively. The design procedure and the analogue realization of the control equations are presented, where the control circuits are constructed with minimal added components. The derivation of the existence and stability conditions is also provided to select the controller gains accordingly. The closed-loop control systems are simulated in MATLAB/SIMULINK and SaberRD under various operating conditions to validate the design approach. The tracking, disturbance rejection, and regulation performance have been investigated. Finally, a PCB prototype of a simplified sliding-mode voltage controlled PWM dc-dc buck converter is designed and tested under large disturbances condition, where the experimental results have showed a good agreement with the simulated results.

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1 Introduction

The PWM dc-dc converters are utilized in various industrial applications such as dc motor drives, electric vehicles, dc distribution systems, and communication equipment [1]. The power converters are nonlinear time-varying systems that step the dc input voltage up or down based on their topology [2]. Since the characteristics of the power sources and electrical loads become more complex and unpredictable, the control of dc-dc power supplies is crucial in optimizing the power conversion process and providing constant output voltage under line and load disturbances. The linear control techniques such as the voltage-mode and current-mode control of dc-dc converter are widely applied in industrial applications because they have simple and affordable design. It is known that the linear controllers are designed based on the small-signal model, so they tend to be effective methods over small variations around a local operating point and incapable of handling large-signal disturbances. Therefore, much research effort has been dedicated to apply the modern control theory to the power converters in order to maintain large-signal stability and improve their dynamics and regulation performance. For instance, the design of adaptive, fuzzy logic, back-stepping, and sliding-mode control have been proposed and their feasibility has been discussed. Among the robust control techniques, the sliding-mode control (SMC) has been investigated for decades as a promising candidate for such dynamical systems due to the design simplicity, flexibility of choosing control parameters, and suitability for variable structure systems (VSS) [3].

The concept of SMC is first introduced and applied by Russian engineers in 1930s for ship-course and dc generators control [4]. Later on 1977s, the work was spread outside Russia in English language by Utkin via written manuscripts, which captured the interest of many researchers and control engineers. The first application of SMC to the dc-dc buck converter was reported in 1983 by Bilalovic et al. [5]. Since

then, this control method has been extended to cover all other types of dc-dc power converters. Although the SM controller is robust against large disturbances and system parameters variations, the linear controller is still dominant in industrial applications. This is because the classical control schemes require less design efforts and can be implemented in simple analogue form. Additionally, there are some practical design issues accompanied with the implementation of SM controller in dc-dc converters such as the chattering phenomenon, variable switching frequency, and steady-state error [6]. In 2005, Tan et al. have introduced encouraging results for designing and implementing analogue SMC schemes of dc-dc buck converter [7]. Furthermore, the authors have addressed most of the practical limitations of SMC in their design approach and come up with systematic design procedures for the basic power converter typologies.

Following the trend of the aforementioned research efforts, it is timely to design the SMC of dc-dc converters from circuit prospective using the simplest possible structure. In this dissertation, a simplified SM controller of PWM dc-dc converters in continuous conduction mode (CCM) is designed in detail. The proposed nonlinear controller is realized in simple analogue form and validated via MATLAB/SIMULINK and SaberRD simulations. Finally, a prototype of simplified SM voltage control of PWM dc-dc buck converter is developed and tested under various operating conditions to verify the design methodology.

1.1 Background

The ideal SMC law, which is mainly developed for VSS, is a time-varying state feedback control law. It is a discontinuous function that switches between the system structures at an infinite frequency depending on the state variable location in the state-space [3]. The control objective is to force the state variables being controlled to follow a reference path called a sliding manifold and eventually settle upon a desired equilibrium point. Two phases are involved in the sliding-mode operation. In the first

phase, which is called the reaching phase, the trajectory is forced by the SMC law toward the sliding manifold. This phase is achieved through the compliance of the hitting condition, which guarantees that the system trajectory is directed from its arbitrary location toward the sliding surface [8]. Next, the system enters the sliding phase, in which the system is subjected to infinite switching actions so as to maintain the controlled trajectory on the sliding surface and force it toward the origin. This is possible if the existence and stability conditions are satisfied. The existence condition ensures that the trajectory stays within the neighborhood of the sliding surface. The stability condition, on the other hand, guarantees that the state variable of the system being controlled reaches the desired steady-state in finite time [8].

It has been assumed that the ideal SMC operates at infinite switching frequency such that the controlled trajectory is forced to follow the desired path, so the controlled system is robust against parameters variations and large disturbances. Moreover, the system under ideal SM operation enjoys fast dynamics and tracks the desired trajectory with zero steady-state error. However, such controller is not feasible due to the non-ideality of the switching devices, which must operate in finite switching frequency. Thus, the controlled trajectory under non-ideal SMC oscillates at high switching frequency during the sliding phase, creating what is so-called the chattering phenomenon [9]. Fig. 1.1 shows the controlled trajectory during ideal and non-ideal SMC.

1.2 Current State-of-the-Art Sliding-Mode Control of Power Converters

As mentioned earlier, the application of ideal SMC is not possible in actual dc-dc converters, so practical design considerations should be taken into account. For example, the implementation of SM controller with high switching frequency in dc-dc converters increases the switching losses and electromagnetic interference (EMI) [10].

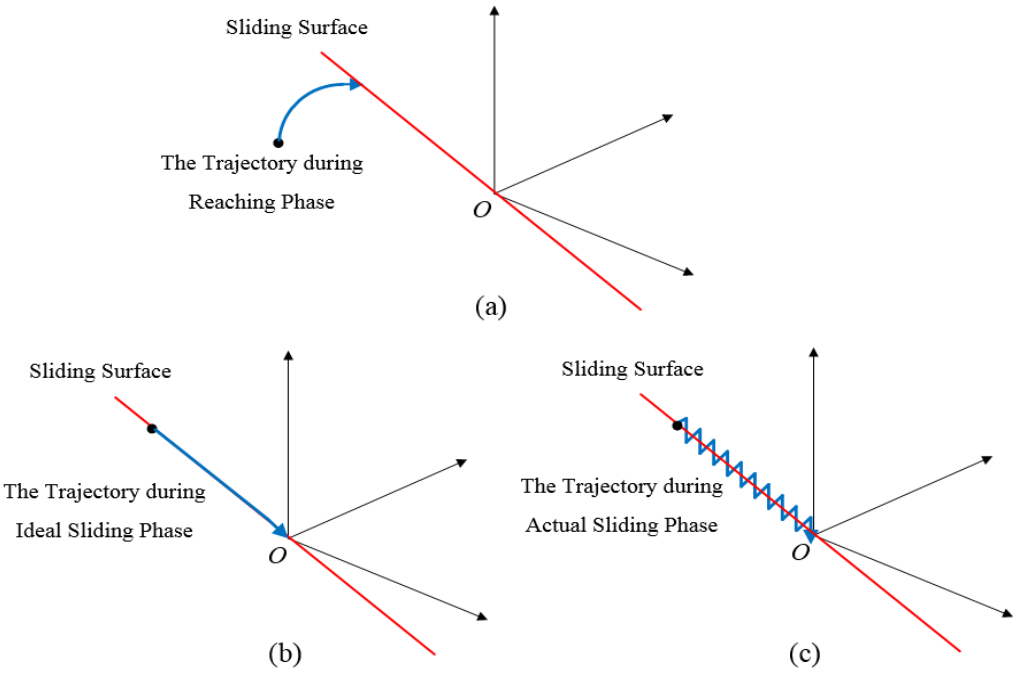


Figure 1.1: The controlled trajectory during ideal and non-ideal SMC. a) Reaching phase. b) Ideal sliding phase. c) Non-ideal sliding phase.

Thus, the hysteresis modulation (HM) has been implemented in the SMC of dc-dc converter to limit the switching frequency and eliminate the chattering phenomenon [11], [12]. Various SMC implementation techniques have been proposed using embedded systems [13]-[48]. Some approaches have utilized digital signal controller such as dsPICF3010 and STM32F407VG [13], [14], DSP [15]-[21], ATMEGA16 microprocessor [22], [23], and FPGA [24]-[26]. Other techniques have included computerized platforms [27]-[29], real-time MATLAB environment using DAQ-Advantech [30]-[32], dSPACE system [33]-[38], Arcon RISC Machine (ARM)-based micro-controller [39], [40], OPAL-RT real-time digital simulator [41]-[44], and CMOS chip [45]-[48]. The aforementioned techniques are characterized by the programmability, flexibility, and fast signal processing capability, but they are more expensive than linear control methods that utilize single op-amp with few capacitors and resistors. Therefore, the

embedded systems-based implementation is not suitable for low-cost commercial and industrial applications.

Alternatively, the analogue circuits have been introduced in [49]-[56] using conventional HM-based SMC, which are more affordable as compared to embedded systems-based methods. Unfortunately, the HM-based SMC method produces variable switching frequency, which is not a desirable feature because the design of input and output filters of dc-dc converters becomes more complicated [4]. The adaptive hysteresis modulation [55],[56], and hysteresis modulation with a synchronization to external trigger [57] have also been proposed to maintain constant switching frequency using analogue control circuit. However, such method is more complicated than conventional HM-based SMC and thus unattractive for commercial applications. On the other hand, the PWM-based SMC using analogue control schemes built with op-amps have been reported in [6], [7], [58]-[66] as alternatives for the sophisticated implementation techniques. Table I summarizes the main SMC implementation techniques of dc-dc converters.

The idea of designing a SMC for PWM dc-dc converters using the equivalent control method can be traced back to [11], where it was proposed that the control signal obtained from the equivalent control method in SMC and the duty cycle obtained from a PWM-based controller are equivalent. Later, a geometric framework that maps the PWM control onto SMC has been provided by [67], [68], in which it has been shown that the averaged dynamics of the SM controlled system and PWM controlled system are equivalent as the switching frequency tends to infinity. In [69], the first application of equivalent control method to the SMC of PWM dc-dc buck converter has been reported. Next, Mahdavi et al. have incorporated the state-space averaging technique into the modeling of SMC of dc-dc converters [70], [71]. Thus, the relation between the equivalent control law and duty cycle has been established, and the implementation

of PWM with SM controller has become possible.

1.3 Motivation

The technical aspects of the design and implementation of PWM-based SM controller for basic dc-dc converters using analogue integrated circuits (ICs) have already been introduced in [6], [7], [61]-[66]. The authors have proposed a systematic procedure to design and realize a fixed switching frequency PWM-based SMC schemes that have simpler structure and lower implementation cost than adaptive HM-based SM controllers and embedded systems-based SMC methods. The design of SM controller of power converters in a form that it is close to the classical linear controller is preferable in industrial applications, where the low cost, robust tracking, and good regulation performance are required. However, the application of such SM controllers is still limited in industrial and commercial applications compared to the linear controllers. This is attributed to the fact that the majority of previous research work in SMC have mainly been discussed from control prospective rather than circuit perspective [6].

The SMC of power converters is still uncommon among the power electronics specialists who prefer using linear control theory to design and implement PID, type II, and type III controllers, thus avoiding the cumbersome mathematics in modern control techniques. On the other hand, the control engineers tend to introduce various SM controllers in detailed mathematical form rather than offering simple implementation techniques for such control systems. However, if the gap between the two communities is bridged, then the design and implementation of robust control systems based on simple electronic components can be achieved. Hence, based on the research endeavors proposed in [6], [7], [62], and [63], it is highly motivating:

1. To simplify the design of SMC systems of basic PWM dc-dc converters so as to encourage the utilization of such robust controllers.

2. To provide detailed design methodology for such controllers and facilitate the choice of proper control system parameters.

3. To convert the proposed control law into the simplest analogue form and simulate the nonlinear controller using accurate power converter models and reliable software.

4. To develop an analogue prototype for the simplified nonlinear controller that fits the low-cost industrial applications and validate the practical design via experimental results.

1.4 Objectives

The main objectives of this dissertation that is related to the design of simplified SMC of PWM dc-dc power converters are:

1) To develop nonlinear models of PWM dc-dc buck and boost converters for CCM based on the averaging techniques, which are necessary to

   - present accurate dynamics of the system being controlled instead of using linearized models and transfer functions.
   - create convenient mathematical forms for the dc-dc converters so as to test the SMC system performance in MATLAB/SIMULINK environment.

2) To design simplified PWM-based SM controllers of dc-dc buck and boost converters for CCM, in which the derivation of equivalent control law, existence, and stability conditions are introduced in detail.

3) To convert the proposed control law into a simple analogue circuit presented by few resistors and operational amplifiers, and simulate the closed-loop control system in MATLAB/SIMULINK and SaberRD.

4) To investigate the tracking and regulation performance of the analogue closed-loop control systems during large line and load disturbances.

5) To develop a PCB prototype for Simplified SM voltage control of PWM dc-dc buck converter for CCM, and perform experimental tests to study the tracking and regulation performance of the nonlinear controller during large disturbances.

6) To validate the theoretical control design approach using simulation and experimental results.

1.5 Structure and Contents

The organization of the dissertation is summarized as follows:

Chapter 1: Introduction to the SMC theory, current state-of-the-art SMC of power converters, the need for simplifying the design of SM controller, and dissertation outcomes are introduced.

Chapter 2: Open-loop large-signal averaged models of PWM dc-dc buck and boost converters for CCM are developed. Additionally, the nonlinear models of power stages are simulated in MATLAB/SIMULINK and compared with SaberRD for validation purpose.

Chapter 3: Design of closed-loop simplified SM voltage controlled PWM dc-dc buck converter for CCM is introduced. The analogue realization of the nonlinear controller is presented. The steady-state response, disturbance rejection, and regulation performance are investigated based on MATLAB/SIMULINK and SaberRD simulations.

Chapter 4: Design and analogue representation of closed-loop double-integral (proportional-integral) simplified SM voltage controlled PWM dc-dc buck converter for CCM are presented. MATLAB/SIMULINK and SaberRD simulations are utilized to validate the control design approach.

Chapter 5: Design of closed-loop double-integral simplified SM current controlled PWM dc-dc boost converter for CCM is introduced. The analogue representation and design procedure are given. The simulation results using MATLAB/SIMULINK and SaberRD are also presented.

Chapter 6: The PCB prototyping and analogue implementation of closed-loop simplified SM voltage controlled PWM dc-dc buck converter for CCM are discussed. The experimental results of the nonlinear control system are compared with the simulation results during steady-state and large disturbance conditions to verify the design methodology.

Chapter 7: dissertation summary, conclusions, key contributions, and future work are summarized.

Table I: Summary of SMC Implementation of DC-DC Converters

Implementation Method	**Merits**	**Drawbacks**	**References**
Embedded systems that include Micro-controllers, dSPACE, DSP, and FPGA.	Programability, flexibility, robustness, and fast signal processing capability.	High cost and complexity. Not suitable for low-cost commercial applications.	[13]-[48]
Analogue circuit via hysteresis modulation.	Simple control circuit and direct implementation. Reduced components count as compared to the other methods. Robust tracking.	High and variable switching frequency. Complicates filters design. Increases switching losses. Worsens EMI issues.	[49]-[54]
Analogue circuit via adaptive hysteresis modulation.	Constant switching frequency. Simpler structure as compared to embedded systems. Reduces switching losses. Robust tracking.	Additional circuitry and cost are required to maintain a constant switching frequency. Requires capacitor and load current sensors.	[55],[56]
Analogue circuit via hysteresis modulation with synchronization to external trigger.	Constant switching frequency. Simpler structure as compared to embedded systems. Reduces switching losses. Robust tracking.	Additional circuitry and cost are required to maintain a constant switching frequency.	[57]
Analogue circuit via pulse-width modulation and equivalent control method.	Constant switching frequency. Simpler than adaptive hysteresis modulation. Reduces switching losses. Robust tracking.	Utilizes adaptive ramp voltage. Additional circuitry and cost are required to sense the capacitor current. Efficiency and output voltage ripple are affected.	[6], [7], [61]-[66]

2 Nonlinear Modeling of Open-Loop DC-DC Converters for CCM

2.1 Introduction

The large-signal averaged models of PWM dc-dc buck and boost converters are developed using state-space averaging techniques. Furthermore, MATLAB/SIMULINK model with s-function is utilized to simulate the dc-dc converters dynamics for CCM. The steady-state open-loop time response obtained from MATLAB and SaberRD are compared to verify the nonlinear models of the power stages.

2.2 State-Space Averaging Method of DC-DC Converters

The PWM power converters are highly nonlinear systems due to the presence of power MOSFET and diode, which construct the switching network. In order to design a SM controller that maintains a constant output voltage during large disturbances, the knowledge of the converter model is required. Since the dc-dc converters are variable structure systems, the state-space averaging technique can be used to obtain their nonlinear models.

The state-space averaged model is derived via averaging the differential equations obtained from the equivalent circuit that is associated with a certain switching status. The differential equations, which are derived using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL), are weighed by the corresponding time interval at which the circuit operates at certain switching status [72]. Thus, the weighed dynamics during an entire switching cycle represent the large-signal model of the dc-dc converter. The state-space averaging technique results in a model that is suited for MATLAB simulations. In this research, s-function is implemented to simulate the dynamics of dc-dc buck and boost converters in MATLAB/SIMULINK [74], [75].

The dc-dc converters models are derived in this chapter considering the following

assumptions:

1. The capacitance of the switching elements is neglected.

2. The MOSFET on-resistance is linear, whereas the MOSFET off-resistance is infinite.

3. The diode is modeled as a linear forward resistance and a battery when it is ON, and as an infinite resistance when it is OFF.

4. The inductor and capacitor are linear, time invariant, and frequency independent.

2.2.1 Large-Signal Model for CCM

The nonlinear state-space switched model of the power converter can be written as

$$\dot{x}(t) = A(u_s(t))x(t) + B(u_s(t))u(t), \tag{2.1}$$

where $A(u_s(t))$ and $B(u_s(t))$ are given by

$$\begin{cases} A(u_s(t)) = A_1 u_s(t) + A_2(1 - u_s(t)) \\ \\ B(u_s(t)) = B_1 u_s(t) + B_2(1 - u_s(t)). \end{cases} \tag{2.2}$$

The state and input matrices are $A \in \mathcal{R}^{n\times n}$ and $B \in \mathcal{R}^{n\times m}$, respectively. The state and input vectors are denoted as $x \in \mathcal{R}^n$ and $u \in \mathcal{R}^m$, respectively. The state and input matrices during the time interval $t \in [0, d_T T]$ are given as A_1 and B_1, whereas state and input matrices during the time interval $t \in [d_T T, T]$ are A_2 and B_2, respectively. The switching control input u_s is defined as follows

$$u_s = \begin{cases} 1 & \text{for } \ t \in [0, d_T T] \\ \\ 0 & \text{for } \ t \in [d_T T, T]. \end{cases} \tag{2.3}$$

Using the averaging method, the nonlinear switched model can be averaged during

the time interval $[0, T]$, yielding the nonlinear large-signal averaged model

$$\dot{\bar{x}}(t) = \Big[A_1 d_T(t) + A_2 \bar{d_T}(t)\Big]\bar{x}(t) + \Big[B_1 d_T(t) + B_2 \bar{d_T}(t)\Big]u(t), \tag{2.4}$$

where the large-signal quantity of duty cycle $d_T \in [0, 1]$ and $\bar{d_T}$ is $1 - d_T$.

2.2.2 Ideal Large-Signal Averaged Model of Buck Converter

The buck converter circuit is depicted in Fig. 2.1. The circuit is made up of a power MOSFET S, a diode D_1, inductor L, and a capapcitor C. In CCM, the equivalent circuits of the power converter during the ON-OFF state of the switching elements are shown in Fig. 2.1(b) and (c), respectively. The dynamics of the buck converter when S is ON and D_1 is OFF are obtained via applying KVL and KCL to Fig. 2.1(b), yielding

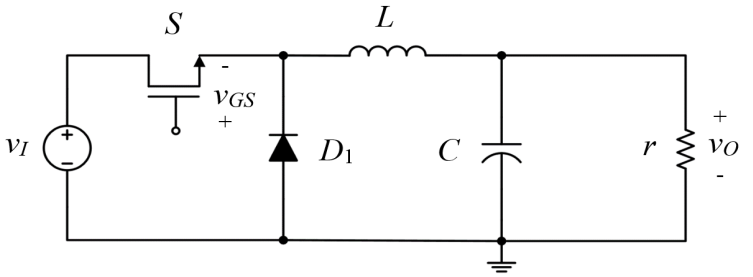
$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_C + \frac{1}{L} v_I \\ \frac{1}{C} i_L - \frac{1}{C} i_O \end{bmatrix}. \tag{2.5}$$

Similarly, applying KVL and KCL to Fig. 2.1(c) yields the buck converter dynamics when S is OFF and D_1 is ON

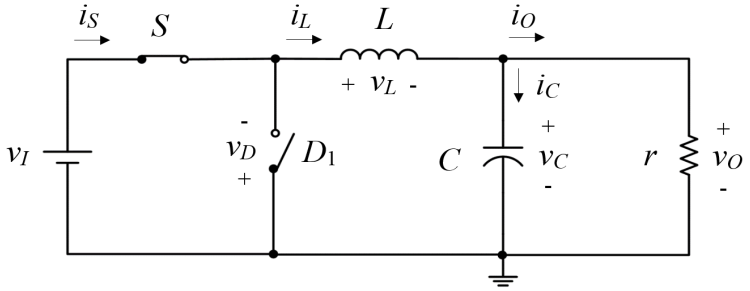
$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_C \\ \frac{1}{C} i_L - \frac{1}{C} i_O \end{bmatrix}. \tag{2.6}$$

The variables that represent large-signal quantities of the capacitor voltage, inductor current, input voltage, output current, output voltage, and load resistance are defined as v_C, i_L, v_I, i_O, v_O, and r respectively. According to the averaging technique, (2.5) and (2.6) can be averaged during the time interval $[0, T]$, yielding the ideal large-signal averaged model of the dc-dc buck converter

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \bar{v}_C + \frac{1}{L} \bar{v}_I d_T \\ \frac{1}{C} \bar{i}_L - \frac{1}{C} \bar{i}_O \end{bmatrix}, \tag{2.7}$$



(a)



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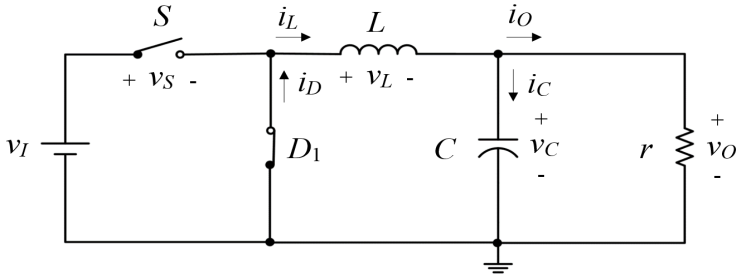


(c)

Figure 2.1: DC-DC buck converter. a) The circuit. b) Ideal equivalent circuit during the time interval $0 < t \leq d_T T$. c) Ideal equivalent circuit during the time interval $d_T T < t \leq T$.

and the output voltage is

$$\bar{v}_O = \bar{v}_C. \tag{2.8}$$

On the other hand, the ideal switched buck converter model yields

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_C + \frac{1}{L} v_I u_s \\ \frac{1}{C} i_L - \frac{1}{C} i_O \end{bmatrix}. \tag{2.9}$$

In state-space form, (2.9) can be written as

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{rC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{u_s}{L} \\ 0 \end{bmatrix} v_I, \tag{2.10}$$

and the output equation is

$$\begin{bmatrix} v_O \end{bmatrix} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{2.11}$$

At steady-state, one can solve for the equilibrium point, yielding the steady-state values of inductor current I_L and capacitor voltage V_C

$$\begin{cases} I_L = \frac{V_C}{R} \\ V_C = DV_I, \end{cases} \tag{2.12}$$

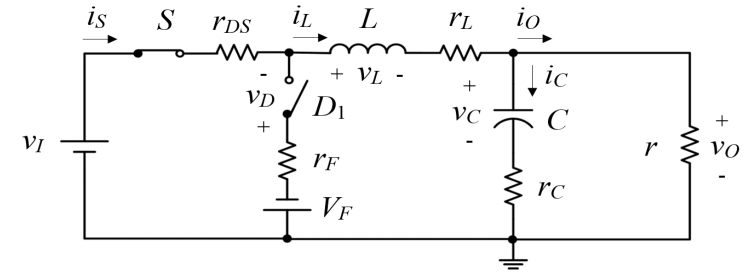
where D, R, and V_I are the steady-state values of the duty cycle, load resistance, and input voltage, respectively.

2.2.3 Non-Ideal Large-Signal Averaged Model of Buck Converter

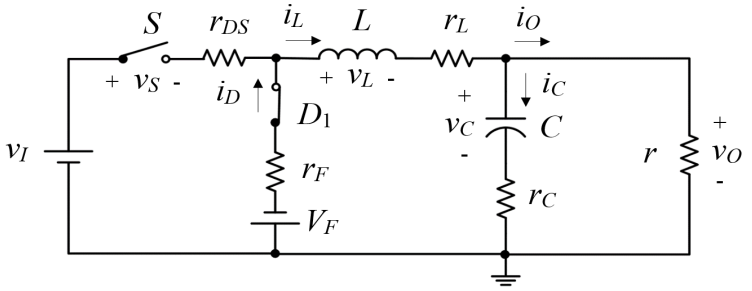
The non-ideal large-signal averaged model is obtained when the parasitic components of the power converter circuit are included. Such model emulates the non-ideal power converter dynamics, which can be utilized to test the control system performance using MATLAB/SIMULINK. The equivalent circuits of the non-ideal buck converter during the ON-OFF state of the power MOSFET are shown in Fig. 2.2. The equivalent series resistances (ESRs) of the capacitor and inductor are defined as r_C and r_L, respectively. The parasitic components of the switching network are represented by the MOSFET on-resistance r_{DS}, diode forward resistance, r_F, and diode threshold voltage V_F.

The dynamics of the buck converter when S is ON and D_1 is OFF are obtained via applying KVL and KCL to Fig. 2.2(a), yielding

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_{DS} + r_L)i_L - \frac{1}{L}v_O + \frac{1}{L}v_I \\ \frac{1}{C}i_L - \frac{1}{C}i_O \end{bmatrix}. \tag{2.13}$$



(a)



(b)

Figure 2.2: a) Non-ideal equivalent circuit during the time interval $0 < t \leq d_T T$. b) Non-ideal equivalent circuit during the time interval $d_T T < t \leq T$.

Similarly, applying KVL and KCL to Fig. 2.2(b) yields the buck converter dynamics when S is OFF and D_1 is ON

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_F + r_L)i_L - \frac{1}{L}v_O + \frac{1}{L}V_F \\ \frac{1}{C}i_L - \frac{1}{C}i_O \end{bmatrix}. \tag{2.14}$$

Thus, based on the averaging technique, (2.13) and (2.14) are combined together, yielding the non-ideal large-signal averaged buck converter model for CCM

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\Big[r_{DS}d_T + r_F(1-d_T) + r_L\Big]\bar{i}_L - \frac{1}{L}\bar{v}_O + \frac{1}{L}\Big[\bar{v}_I d_T + V_F(1-d_T)\Big] \\ \frac{1}{C}\bar{i}_L - \frac{1}{C}\bar{i}_O \end{bmatrix}. \tag{2.15}$$

and the output voltage is

$$\bar{v}_O = r_C\bar{i}_L + \bar{v}_C - r_C\bar{i}_O. \tag{2.16}$$

Alternatively, the non-ideal switched buck converter model is

$$\begin{bmatrix}\dot{i}_L\\ \dot{v}_C\end{bmatrix} = \begin{bmatrix}-\frac{1}{L}(r_{DS}u_s + r_F\bar{u}_s + r_L)i_L - \frac{1}{L}v_O + \frac{1}{L}(v_I u_s + V_F\bar{u}_s)\\ \frac{1}{C}i_L - \frac{1}{C}i_O\end{bmatrix}, \tag{2.17}$$

which can be written as a state-space model

$$\begin{bmatrix}\dot{i}_L\\ \dot{v}_C\end{bmatrix} = \begin{bmatrix}-\frac{1}{L}(r_L + \frac{r_C r}{r_C+r} + r_{DS}u_s + r_F\bar{u}_s) & -\frac{1}{L}(\frac{r}{r_C+r})\\ \frac{1}{C}(\frac{r}{r_C+r}) & -\frac{1}{C}(\frac{1}{r_C+r})\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix} + \begin{bmatrix}\frac{u_s}{L} & \frac{\bar{u}_s}{L}\\ 0 & 0\end{bmatrix}\begin{bmatrix}v_I\\ V_F\end{bmatrix} \tag{2.18}$$

with an output equation

$$\begin{bmatrix}v_O\end{bmatrix} = \begin{bmatrix}\frac{r_C r}{r_C+r} & \frac{r}{r_C+r}\end{bmatrix}\begin{bmatrix}i_L\\ v_C\end{bmatrix}. \tag{2.19}$$

Note that the inverse logic of the switching control input is defined as $\bar{u}_s$, which is equal to $1 - u_s$.

2.2.4 Ideal Large-Signal Averaged Model of Boost Converter

The boost converter can be modeled based on the same approach. The boost converter circuit is given in Fig. 2.3(a), whereas Figs. 2.3 (b) and (c) show the equivalent circuits when the power MOSFET is ON and OFF, respectively. If S is ON and D_1 is OFF, the converter dynamics are obtained from Fig. 2.3(b) based on KVL and KCL, hence

$$\begin{bmatrix}\dot{i}_L\\ \dot{v}_C\end{bmatrix} = \begin{bmatrix}\frac{1}{L}v_I\\ -\frac{1}{C}i_O\end{bmatrix}, \tag{2.20}$$

and the boost converter dynamics during the interval at which S is OFF and D_1 is

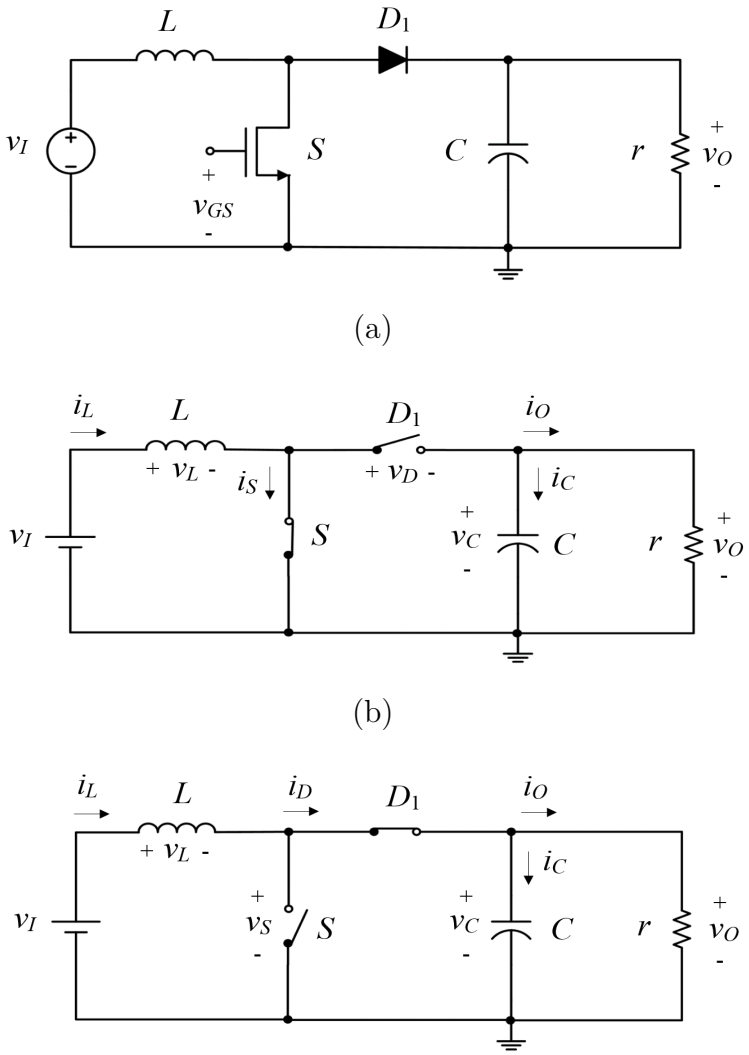


Figure 2.3: DC-DC boost converter. a) The circuit. b) Ideal equivalent circuit during the time interval $0 < t \leq d_T T$. c) Ideal equivalent circuit during the time interval $d_T T < t \leq T$.

ON are obtained from Fig. 2.3(c) as

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_C + \frac{1}{L} v_I \\ \frac{1}{C} i_L - \frac{1}{C} i_O \end{bmatrix}. \tag{2.21}$$

Thus, (2.20) and (2.21) can be combined according to the averaging method, which results in ideal large-signal averaged model of dc-dc boost converter for CCM

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\bar{v}_C(1-d_T) + \frac{1}{L}\bar{v}_I \\ \frac{1}{C}\bar{i}_L(1-d_T) - \frac{1}{C}\bar{i}_O \end{bmatrix}, \tag{2.22}$$

and the output equation is

$$\bar{v}_O = \bar{v}_C. \tag{2.23}$$

The ideal switched model, on the other hand, is given by

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}v_C\bar{u_s} + \frac{1}{L}v_I \\ \frac{1}{C}i_L\bar{u_s} - \frac{1}{C}i_O \end{bmatrix}, \tag{2.24}$$

while the state-space representation of the ideal switched model is

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L}\bar{u_s} \\ \frac{1}{C}\bar{u_s} & -\frac{1}{rC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_I, \tag{2.25}$$

and the output equation is

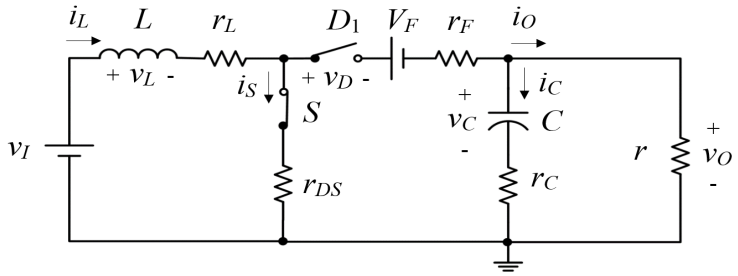
$$\begin{bmatrix} v_O \end{bmatrix} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}. \tag{2.26}$$

The steady-state values of inductor current I_L and capacitor voltage V_C of the ideal boost converter are

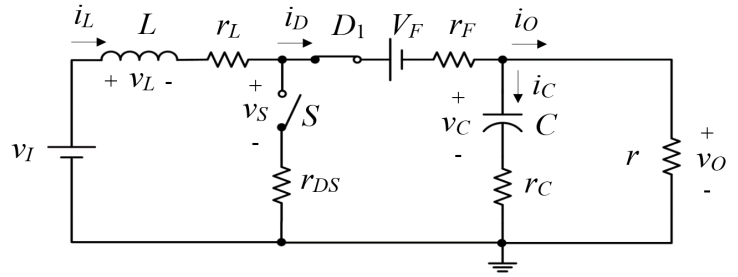
$$\begin{cases} I_L = \frac{{V_C}^2}{V_I R} \\ V_C = \frac{V_I}{1-D}. \end{cases} \tag{2.27}$$

2.2.5 Non-Ideal Large-Signal Averaged Model of Boost Converter

The equivalent circuits of the non-ideal converter during the ON-OFF state of the power MOSFET are shown in Fig. 2.4. The dynamics of the boost converter when S



(a)



(b)

Figure 2.4: a) Non-ideal equivalent circuit during the time interval $0 < t \leq d_T T$. b) Non-ideal equivalent circuit during the time interval $d_T T < t \leq T$.

is ON and D_1 is OFF are obtained via applying KVL and KCL to Fig. 2.4(a), yielding

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_{DS} + r_L)i_L + \frac{1}{L}v_I \\ -\frac{1}{C}i_O \end{bmatrix}. \tag{2.28}$$

Similarly, applying KVL and KCL to Fig. 2.4(b) yields the boost converter dynamics when S is OFF and D_1 is ON

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_F + r_L)i_L - \frac{1}{L}v_O + \frac{1}{L}v_I - \frac{1}{L}V_F \\ \frac{1}{C}i_L - \frac{1}{C}i_O \end{bmatrix}. \tag{2.29}$$

According to the averaging technique, (2.28) and (2.29) are combined together, yielding the non-ideal large-signal averaged model of dc-dc boost converter for CCM

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\Big[r_{DS}d_T + r_F(1-d_T) + r_L\Big]\bar{i}_L - \frac{1}{L}\bar{v}_O(1-d_T) + \frac{1}{L}\bar{v}_I - \frac{1}{L}V_F(1-d_T)) \\ \frac{1}{C}\bar{i}_L(1-d_T) - \frac{1}{C}\bar{i}_O \end{bmatrix}. \tag{2.30}$$

and the output voltage is

$$\bar{v}_O = r_C\bar{i}_L(1-d_T) + v_C - r_C\bar{i}_O. \tag{2.31}$$

Alternatively, the non-ideal switched model yields

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_{DS}u_s + r_F\bar{u_s} + r_L)i_L - \frac{1}{L}v_O\bar{u_s} + \frac{1}{L}v_I - \frac{1}{L}V_F\bar{u_s} \\ \frac{1}{C}i_L\bar{u_s} - \frac{1}{C}i_O \end{bmatrix}, \tag{2.32}$$

which gives the non-ideal state-space model

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}(r_L + r_{DS}u_s + r_F\bar{u_s} + \frac{r_Cr}{r_C+r}\bar{u_s}) & -\frac{1}{L}(\frac{r}{r_C+r})\bar{u_s} \\ \frac{1}{C}(\frac{r}{r_C+r})\bar{u_s} & -\frac{1}{C}(\frac{1}{r_C+r}) \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & -\frac{\bar{u_s}}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_I \\ V_F \end{bmatrix} \tag{2.33}$$

with the following output equation

$$\Big[v_O\Big] = \Big[\frac{r_Cr}{r_C+r}\bar{u_s} \quad \frac{r}{r_C+r}\Big] \begin{bmatrix} i_L \\ v_C \end{bmatrix}. \tag{2.34}$$

2.3 Analytical Periodic Solution of Ideal DC-DC Converters

2.3.1 General Periodic Solution

The analytical solution of the power converter dynamics during the time interval at which S is ON and D_1 is OFF gives

$$x(t) = e^{A_1t}x(0) + \int_0^t e^{A_1(t-\tau)}B_1u(\tau)d\tau, \tag{2.35}$$

where

$$e^{A_1t} = \mathcal{L}^{-1}\Big[(sI - A_1)^{-1}\Big]. \tag{2.36}$$

During this time interval, (2.35) can be written as

$$x(d_T T) = e^{A_1 d_T T} x(0) + \int_0^{d_T T} e^{A_1 (d_T T - \tau)} B_1 u(\tau) d\tau. \tag{2.37}$$

On the other hand, the solution of the power converter dynamics during the time interval at which S is OFF and D_1 is ON yields

$$x(t) = e^{A_2 (t - d_T T)} x(d_T T) + \int_{d_T T}^{t} e^{A_2 (t-\tau)} B_2 u(\tau) d\tau, \tag{2.38}$$

where

$$e^{A_2 t} = \mathcal{L}^{-1}\Big[(sI - A_2)^{-1}\Big]. \tag{2.39}$$

Thus, the solution at the switching period T becomes

$$x(T) = e^{A_2 (1-d_T) T}\Big[e^{A_1 d_T T} x(0) + \int_0^{d_T T} e^{A_1 (d_T T - \tau)} B_1 u(\tau) d\tau\Big] + \int_{d_T T}^{T} e^{A_2 (T-\tau)} B_2 u(\tau) d\tau. \tag{2.40}$$

Now, if the periodicity condition is applied such that $x(0) = x(T)$ [76], then the initial condition $x(0)$ is determined as follows

$$\begin{aligned} x(0) = &\Big[I - e^{A_2 (1-d_T) T} e^{A_1 d_T T}\Big]^{-1}\Big[e^{A_2 (1-d_T) T} \int_0^{d_T T} e^{A_1 (d_T T - \tau)} B_1 u(\tau) d\tau \\ &+ \int_{d_T T}^{T} e^{A_2 (T-\tau)} B_2 u(\tau) d\tau\Big], \end{aligned} \tag{2.41}$$

and the analytical periodic solution is

$$\hat{x}(t) = \begin{cases} e^{A_1 t} x(0) + \int_0^t e^{A_1 (t-\tau)} B_1 u(\tau) d\tau, & \text{for } \; t \in [0, d_T T] \\ e^{A_2 (t - d_T T)}\Big[e^{A_1 d_T T} x(0) + \int_0^{d_T T} e^{A_1 (d_T T - \tau)} B_1 u(\tau) d\tau\Big] & \\ + \int_{d_T T}^{T} e^{A_2 (t-\tau)} B_2 u(\tau) d\tau, & \text{for } \; t \in [d_T T, T] \end{cases} \tag{2.42}$$

2.3.2 Analytical Periodic Solution of Ideal Buck Converter

The ideal switched model of the dc-dc buck converter is defined as

$$\begin{bmatrix} \dot{i}_L \\ \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \\ \frac{1}{C} & -\frac{1}{rC} \end{bmatrix} \begin{bmatrix} i_L \\ \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{u_s}{L} \\ \\ 0 \end{bmatrix} v_I. \tag{2.43}$$

Druing the time interval $[0, d_T T]$ with initial conditions $i_L(0)$ and $v_C(0)$, the analytical solution of the buck converter dynamics is given by

$$\begin{aligned} i_L(t) = \frac{v_I}{r} + e^{-\frac{t}{2rC}} \Bigg\{ \Big(i_L(0) - \frac{v_I}{r}\Big) \cos \omega t + \frac{1}{\omega} \Big[\frac{1}{2rC} \Big(i_L(0) - \frac{v_I}{r}\Big) - \frac{1}{L} \Big(v_C(0) - v_I\Big) \Big] \\ \times \sin \omega t \Bigg\} \end{aligned} \tag{2.44}$$

$$\begin{aligned} v_C(t) = v_I + e^{-\frac{t}{2rC}} \Bigg\{ \Big(v_C(0) - v_I\Big) \cos \omega t + \frac{1}{\omega} \Big[\frac{1}{C} \Big(i_L(0) - \frac{v_I}{r}\Big) - \frac{1}{2rC} \Big(v_C(0) - v_I\Big) \Big] \\ \times \sin \omega t \Bigg\}, \end{aligned} \tag{2.45}$$

where

$$\omega = \sqrt{\frac{1}{4r^2C^2} - \frac{1}{LC}}. \tag{2.46}$$

On the other hand, druing the time interval $[d_T T, T]$ with initial conditions $i_L(d_T T)$ and $v_C(d_T T)$, the analytical solution yields

$$\begin{aligned} i_L(t) = e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ i_L(d_T T) \cos \omega (t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{2rC} i_L(d_T T) - \frac{1}{L} v_C(d_T T) \Big] \\ \times \sin \omega (t - d_T T) \Bigg\} \end{aligned} \tag{2.47}$$

$$\begin{aligned} v_C(t) = e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ v_C(d_T T) \cos \omega (t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{C} i_L(d_T T) - \frac{1}{2rC} v_C(d_T T) \Big] \\ \times \sin \omega (t - d_T T) \Bigg\}, \end{aligned} \tag{2.48}$$

where the terms $i_L(d_T T)$ and $v_C(d_T T)$ are defined as

$$i_L(d_TT) = \frac{v_I}{r} + e^{-\frac{d_TT}{2rC}}\Bigg\{\Big(i_L(0) - \frac{v_I}{r}\Big)\cos\omega d_TT + \frac{1}{\omega}\Big[\frac{1}{2rC}\Big(i_L(0) - \frac{v_I}{r}\Big) - \frac{1}{L}\Big(v_C(0) - v_I\Big)\Big]\sin\omega d_TT\Bigg\} \tag{2.49}$$

$$v_C(d_TT) = v_I + e^{-\frac{d_TT}{2rC}}\Bigg\{\Big(v_C(0) - v_I\Big)\cos\omega d_TT + \frac{1}{\omega}\Big[\frac{1}{C}\Big(i_L(0) - \frac{v_I}{r}\Big) - \frac{1}{2rC}\Big(v_C(0) - v_I\Big)\Big]\sin\omega d_TT\Bigg\}. \tag{2.50}$$

Hence, the analytical periodic solution of the ideal dc-dc buck converter dynamics in CCM becomes

$$\hat{i}_L(t) = \begin{cases} \frac{v_I}{r} + e^{-\frac{t}{2rC}}\Bigg\{\Big(i_L(0) - \frac{v_I}{r}\Big)\cos\omega t + \frac{1}{\omega}\Big[\frac{1}{2rC}\Big(i_L(0) - \frac{v_I}{r}\Big) \\ -\frac{1}{L}\Big(v_C(0) - v_I\Big)\Big]\sin\omega t\Bigg\}, \quad \text{for} \;\; t \in [0, d_TT] \\ \frac{v_I}{r} + e^{-\frac{(d_TT)}{2rC}}\Bigg\{\frac{1}{\omega}\Big[\frac{v_I}{L} - \frac{v_I}{2r^2C}\Big]\sin\omega(d_TT) - \frac{v_I}{r}\cos\omega(d_TT)\Bigg\} \\ +e^{-\frac{t}{2rC}}\Bigg\{i_L(0)\cos\omega t + \frac{1}{\omega}\Big[\frac{1}{2rC}i_L(0) - \frac{1}{L}v_C(0)\Big]\sin\omega t\Bigg\}, \quad \text{for} \;\; t \in [d_TT, T] \end{cases} \tag{2.51}$$

$$\hat{v}_C(t) = \begin{cases} v_I + e^{-\frac{t}{2rC}}\Bigg\{\Big(v_C(0) - v_I\Big)\cos\omega t + \frac{1}{\omega}\Big[\frac{1}{C}\Big(i_L(0) - \frac{v_I}{r}\Big) \\ -\frac{1}{2rC}\Big(v_C(0) - v_I\Big)\Big]\sin\omega t\Bigg\}, \quad \text{for} \;\; t \in [0, d_TT] \\ v_I - e^{-\frac{(d_TT)}{2rC}}\Bigg\{v_I\cos\omega(d_TT) + \frac{1}{2\omega rC}\sin\omega(d_TT)\Bigg\} + e^{-\frac{t}{2rC}}\Bigg\{v_C(0)\cos\omega t \\ +\frac{1}{\omega}\Big[\frac{1}{C}i_L(0) - \frac{1}{2rC}v_C(0)\Big]\sin\omega t\Bigg\}, \quad \text{for} \;\; t \in [d_TT, T]. \end{cases} \tag{2.52}$$

Note that $i_L(0)$ and $v_C(0)$ are determined according to (2.41) and substituted in (2.51) and (2.52) to solve for $\hat{i}_L(t)$ and $\hat{v}_C(t)$, respectively.

2.3.3 Analytical Periodic Solution of Ideal Boost Converter

The switched model of the ideal dc-dc boost converter is

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{\bar{u_s}}{L} \\ \frac{\bar{u_s}}{C} & -\frac{1}{rC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_I. \tag{2.53}$$

The analytical solution of the boost converter dynamics druing the time interval $[0, d_T T]$ with initial conditions $i_L(0)$ and $v_C(0)$ is

$$i_L(t) = i_L(0) + \frac{v_I}{L} t \tag{2.54}$$

$$v_C(t) = v_C(0) e^{-\frac{t}{rC}}. \tag{2.55}$$

Alternatively, the analytical solution druing the time interval $[d_T T, T]$ with initial conditions $i_L(d_T T)$ and $v_C(d_T T)$ gives

$$\begin{aligned} i_L(t) = \frac{v_I}{r} + e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ \Big(i_L(d_T T) - \frac{v_I}{r} \Big) \cos \omega (t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{2rC} \Big(i_L(d_T T) - \frac{V_I}{r} \Big) \\ - \frac{1}{L} \Big(v_C(d_T T) - v_I \Big) \Big] \sin \omega (t - d_T T) \Bigg\} \end{aligned} \tag{2.56}$$

$$\begin{aligned} v_C(t) = v_I + e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ \Big(v_C(d_T T) - v_I \Big) \cos \omega (t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{C} \Big(i_L(d_T T) - \frac{v_I}{r} \Big) \\ - \frac{1}{2rC} \Big(v_C(d_T T) - v_I \Big) \Big] \sin \omega (t - d_T T) \Bigg\}, \end{aligned} \tag{2.57}$$

where the terms $i_L(d_T T)$ and $v_C(d_T T)$ are

$$i_L(t) = i_L(0) + \frac{v_I}{L} d_T T \tag{2.58}$$

$$v_C(t) = v_C(0) e^{-\frac{d_T T}{rC}}. \tag{2.59}$$

Thus, the analytical periodic solution of the ideal dc-dc boost converter dynamics in CCM results in

$$\hat{i}_L(t) = \begin{cases} i_L(0) + \frac{v_I}{L}t, \quad \text{for} \;\; t \in [0, d_T T] \\ \frac{v_I}{r} + e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ \Big(i_L(0) + \frac{v_I}{L} d_T T - \frac{v_I}{r} \Big) \cos\omega(t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{2rC} \Big(i_L(0) \\ + \frac{v_I}{L} d_T T - \frac{v_I}{r} \Big) - \frac{1}{L} \Big(v_C(0) e^{-\frac{d_T T}{rC}} - v_I \Big) \Big] \sin\omega(t - d_T T) \Bigg\}, \quad \text{for} \;\; t \in [d_T T, T] \end{cases} \tag{2.60}$$

$$\hat{v}_C(t) = \begin{cases} v_C(0) e^{-\frac{t}{rC}}, \quad \text{for} \;\; t \in [0, d_T T] \\ v_I + e^{-\frac{(t-d_T T)}{2rC}} \Bigg\{ \Big(v_C(0) e^{-\frac{d_T T}{rC}} - v_I \Big) \cos\omega(t - d_T T) + \frac{1}{\omega} \Big[\frac{1}{C} \Big(i_L(0) + \frac{v_I}{L} d_T T \\ - \frac{v_I}{r} \Big) - \frac{1}{2rC} \Big(v_C(0) e^{-\frac{d_T T}{rC}} - v_I \Big) \Big] \sin\omega(t - d_T T) \Bigg\}, \quad \text{for} \;\; t \in [d_T T, T]. \end{cases} \tag{2.61}$$

As mentioned previously, $i_L(0)$ and $v_C(0)$ can be determined according to (2.41) and then substituted in (2.60) and (2.61) to solve for $\hat{i}_L(t)$ and $\hat{v}_C(t)$, respectively.

2.4 Validation of Large-Signal Averaged Models

2.4.1 Pulse-Width Modulator

The pulse-width modulator of the dc-dc converter is an inverting comparator, in which the control voltage u_e is applied to the non-inverting input, whereas the ramp voltage V_t is applied to the inverting input. As u_e increases, the duty cycle d_T also increases, resulting in an increase in v_O. Fig. 2.5 shows the circuit and waveforms in a typical pulse-width modulator. The slope M of the ramp voltage V_t can be written as [72]

$$M = tan(\phi) = \frac{u_e}{d_T T} = \frac{V_T}{T}, \tag{2.62}$$

where V_T is the peak ramp voltage, and the transfer function of the pulse-width modulator is

$$T_m = \frac{1}{V_T} = \frac{1}{MT}. \tag{2.63}$$

According to [72], the relationship among the large-signal duty cycle d_T, peak ramp voltage V_T, and the control signal u_e is

$$d_T = \frac{u_e}{V_T}. \tag{2.64}$$

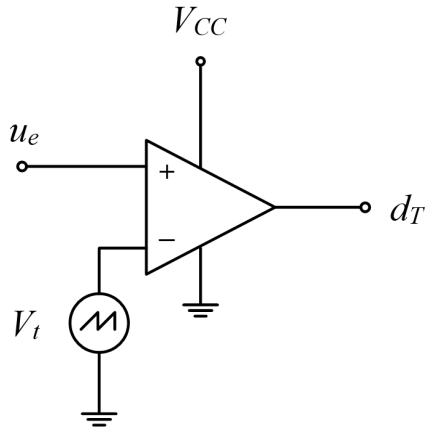
The behavioral model of the pulse-width modulator can be created in MATLAB/SIMULINK via emulating the function of the inverting comparator to generate the required duty cycle d_T. The control signal u_e is a time-varying large-signal quantity that adjusts d_T such that the output voltage v_O is maintained constant during large disturbances.

Table II: PWM DC-DC Converter Parameters

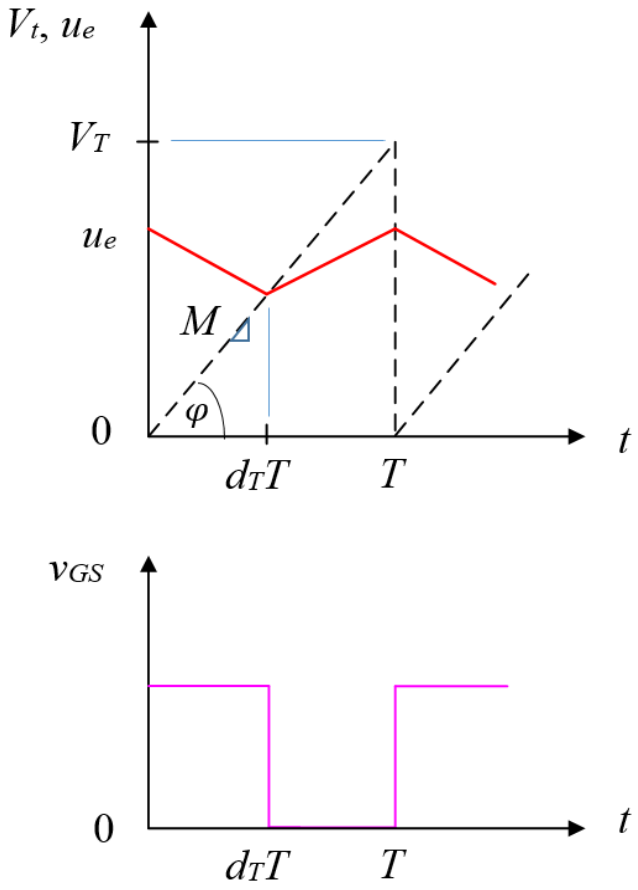
Description	**Parameter**	**Buck Converter**	**Boost Converter**
Inductor	L	301 µH	156 µH
Capacitor	C	51.2 µF	68 µF
Load Resistor	r	$(20 - 100)\ \Omega$	$(40 - 200)\ \Omega$
Inductor ESR	r_L	0.050 Ω	0.190 Ω
Capacitor ESR	r_C	0.200 Ω	0.111 Ω
MOSFET On-Resistance	r_{DS}	0.180 Ω	0.180 Ω
Diode Forward Resistance	r_F	0.022 Ω	0.072 Ω
Diode Threshold Voltage	V_F	0.700 V	0.700 V
Input Voltage	v_I	28 ± 4 V	12 ± 3 V
Output Voltage	V_O	14 V	20 V
Switching Frequency	f_s	100 kHz	100 kHz
Ramp Voltage Amplitude	V_T	10 V	5 V

2.4.2 Steady-State Open-Loop Response of Nonlinear Models

The nonlinear models of the power converters are simulated in MATLAB/SIMULINK. The design specifications and parameters of buck and boost converters are given in Table II [72]. The large-signal non-ideal dynamics of the dc-dc converters are



(a)



(b)

Figure 2.5: (a) The circuit and (b) the waveforms of the pulse-width modulator.

simulated using s-function with zero initial conditions. The behavioral model of PWM is constructed to generate a square waveform with a duty cycle of 0.5 for buck converter and 0.44 for boost converter. An automatic ode solver with 1 µs step size are selected for the time-domain simulation. The MATLAB/SIMULINK model of dc-dc converters is shown in Fig. 2.6.

In order to validate the power converters nonlinear models, the open-loop response obtained from MATLAB and SaberRD has been compared. The operating conditions of the buck and boost converters are (V_I = 28 V, R = 40 Ω) and (V_I = 12 V, R = 60 Ω), respectively, while their steady-state waveforms are shown in Figs. 2.7 and 2.8, respectively. The steady-state values of the open-loop responses are summarized in Table III. It can be noticed that the results are in good agreement, which validate the nonlinear models of dc-dc converters for CCM. The slight difference between the results of the two simulation platforms is due to the non-ideality of switching network and circuit components in SaberRD compared to the mathematical models in MATLAB.

Table III: Stead-State Values of PWM DC-DC Converters

Parameter	**Buck Converter**		**Boost Converter**	
	SaberRD	*MATLAB*	*SaberRD*	*MATLAB*
D	0.5142	0.5000	0.4387	0.4400
V_O (V)	13.930	13.980	19.599	19.660
I_L (A)	0.3505	0.3580	0.5910	0.5700
I_C (A)	0.0023	0.0018	0.0016	0.0020

2.4.3 Transient Open-Loop Response of Nonlinear Models

The output voltage response of the dc-dc buck converter in CCM to a large step change in input voltage, load current, and duty cycle are shown in Figs. 2.9, 2.10, and 2.11, respectively. On the other hand, the output voltage response of the dc-dc boost

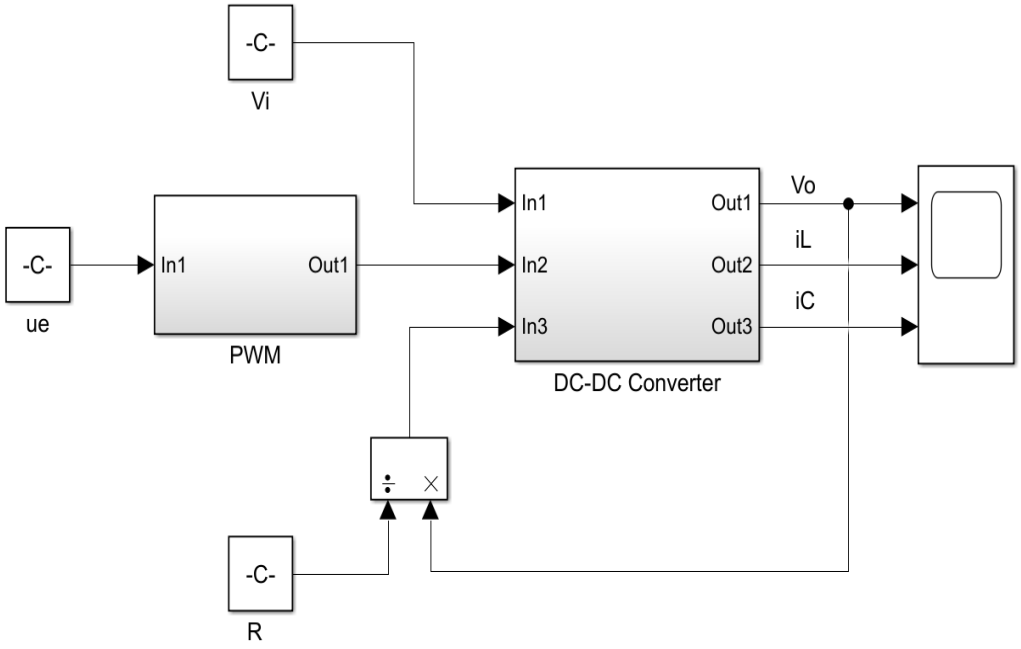


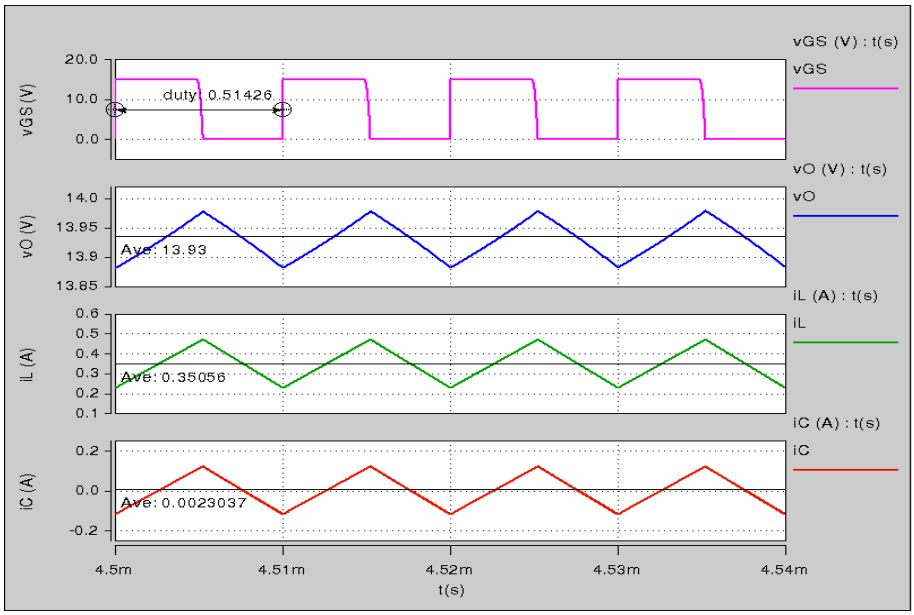
Figure 2.6: MATLAB/SIMULINK model of PWM dc-dc converters.

converter in CCM to a large step change in input voltage, load current, and duty cycle are shown in Figs. 2.12, 2.13, and 2.14, respectively. The inductor current waveforms show that the abrupt decrease in input voltage, load current, and duty cycle moves the power converters operation from CCM towards DCM. Hence, the designer should identify the large disturbance limits, so as to maintain the power supply operation in CCM. Otherwise, the dc-dc converter enters the DCM operation, thus the model and the corresponding control design become invalid.

Table IV: Open-Loop Buck Converter Response Parameters During Large Disturbance

Disturbance	PO/PU **(%)**	t_s **(ms)**	V_O **(V)**	I_L**(A)**
$\Delta V_I = 28 \rightarrow 42$ (V)	21.6	4.5	20.8	0.35
$\Delta V_I = 28 \rightarrow 20$ (V)	25.0	4.5	10.0	0.16
$\Delta R = 60 \rightarrow 15$ (Ω)	9.0	3.5	13.9	0.93
$\Delta R = 15 \rightarrow 200$ (Ω)	12.5	5.5	14.0	0.07

The parameters of the open-loop response of the buck and boost converters under



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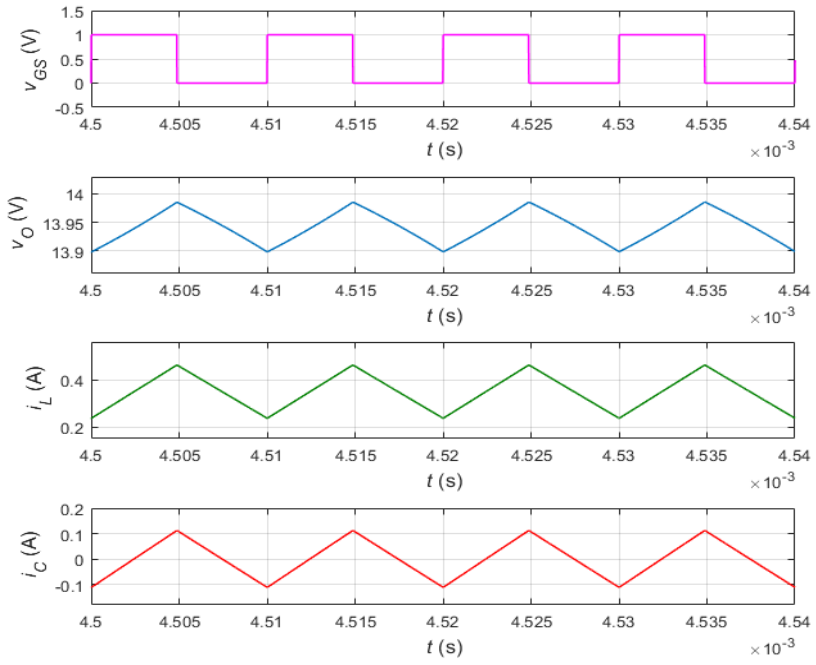
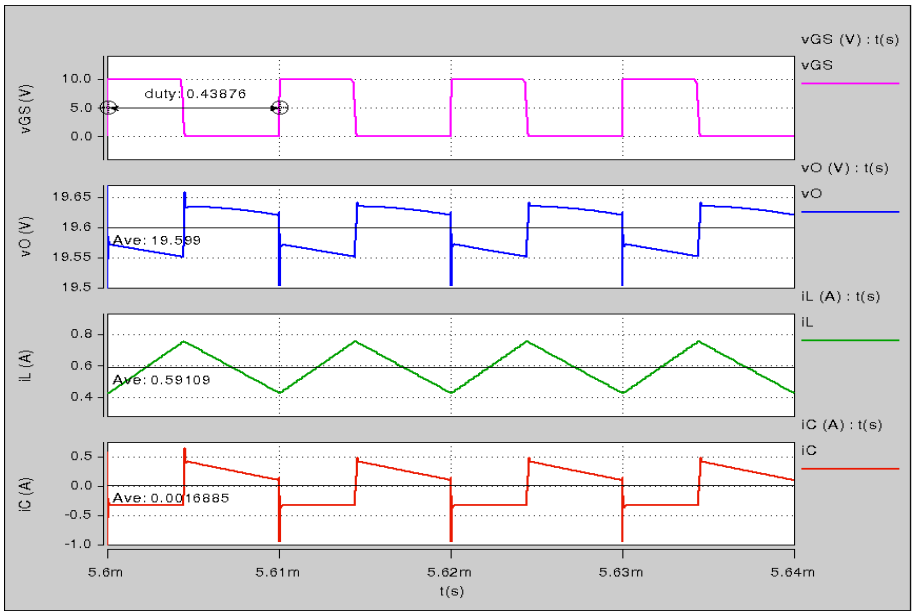


(b)

Figure 2.7: Buck converter steady-state waveforms. a) SaberRD results. b) MATLAB results.



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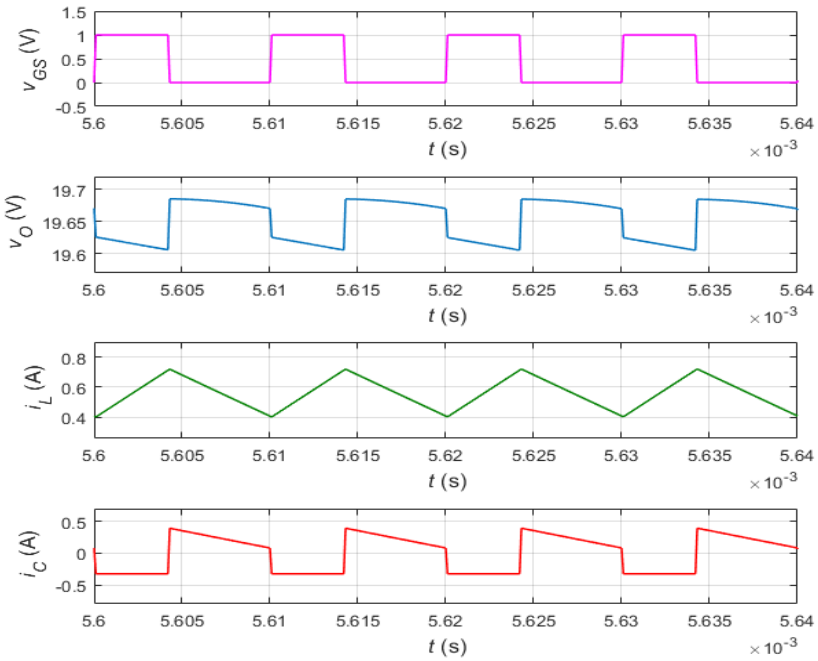


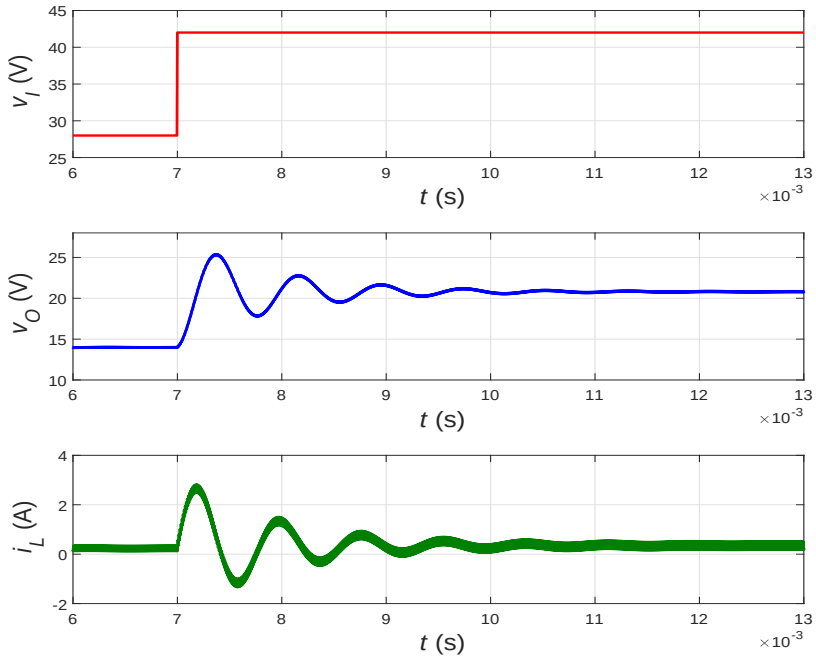
(b)

Figure 2.8: Boost converter steady-state waveforms. a) SaberRD results. b) MATLAB results.

large disturbances are summarized in Tables IV and V, respectively. The tabulated results show that the line disturbance deviates the output voltage from the desired value significantly, whereas the steady-state output voltage is closer to the desired value during the load disturbance. In addition, it can be noticed that the percentage overshoot/undershoot and settling time of the output voltage response are significantly large and undesirable. Thus, the open-loop power stages must be controlled via robust control circuits to achieve the desired transient response characteristics and improve the regulation performance.

Table V: Open-Loop Boost Converter Response Parameters During Large Disturbance

Disturbance	PO/PU **(%)**	t_s **(ms)**	V_O **(V)**	I_L**(A)**
$\Delta V_I = 12 \rightarrow 18$ (V)	16.0	5.0	30.35	0.89
$\Delta V_I = 12 \rightarrow 7$ (V)	35.5	3.5	11.4	0.33
$\Delta R = 60 \rightarrow 20$ (Ω)	5.4	3.0	19.35	1.70
$\Delta R = 20 \rightarrow 200$ (Ω)	7.6	3.5	21	0.20



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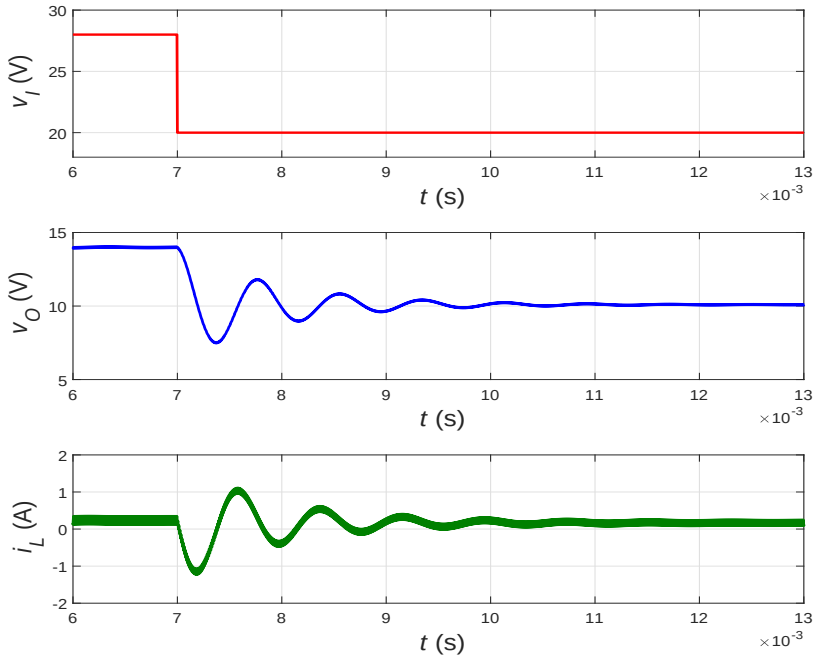
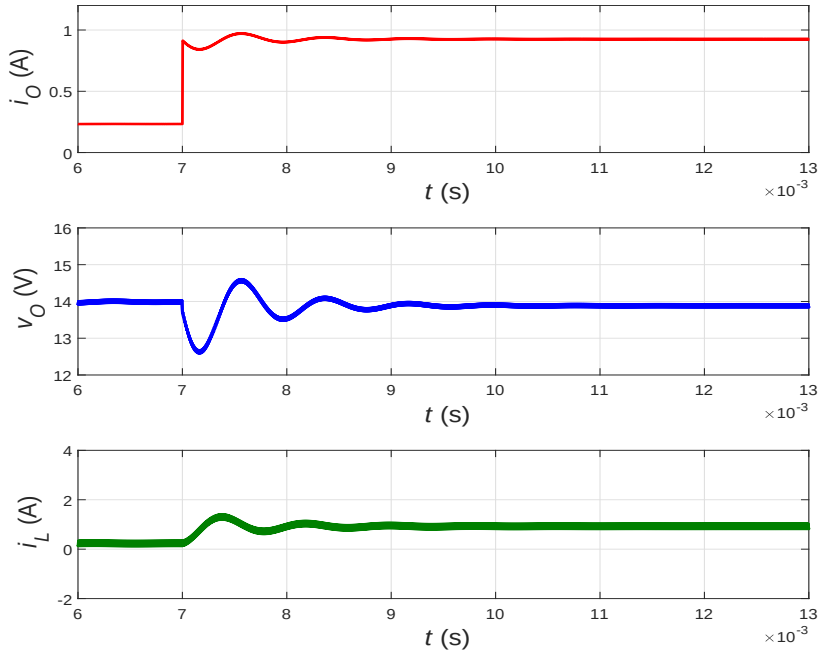


(b)

Figure 2.9: The open-loop response of the buck converter during a large step change in input voltage v_I. a) Step change in v_I from 28 V to 42 V. b) Step change in v_I from 28 V to 20 V.



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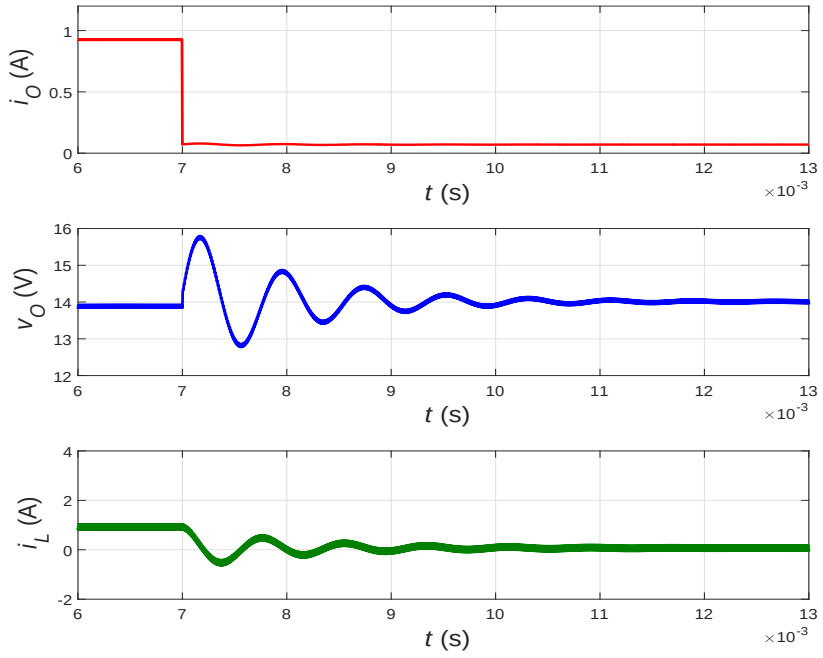
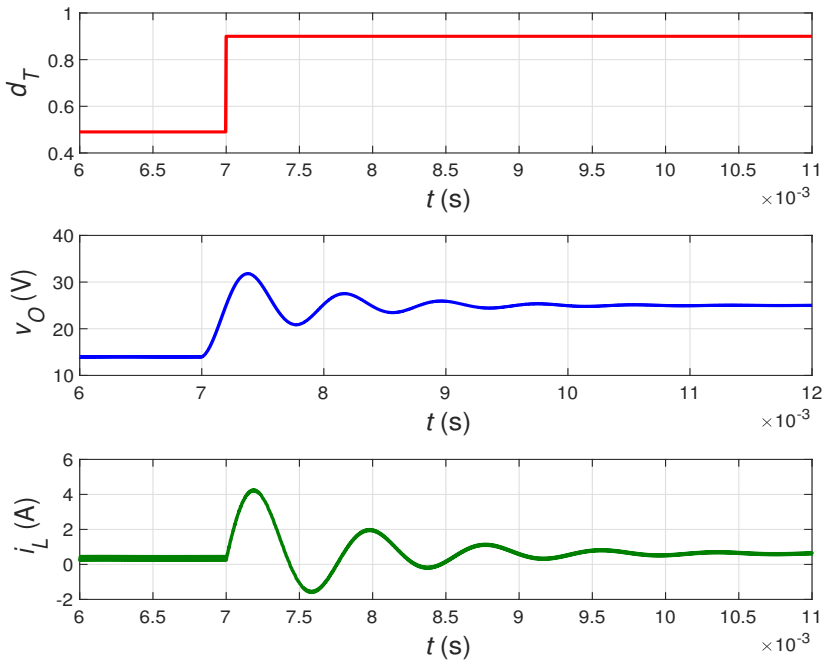


(b)

Figure 2.10: The open-loop response of the buck converter during a large step change in load resistor r. a) Step change in r from 60 Ω to 15 Ω. b) Step change in r from 15 Ω to 200 Ω.



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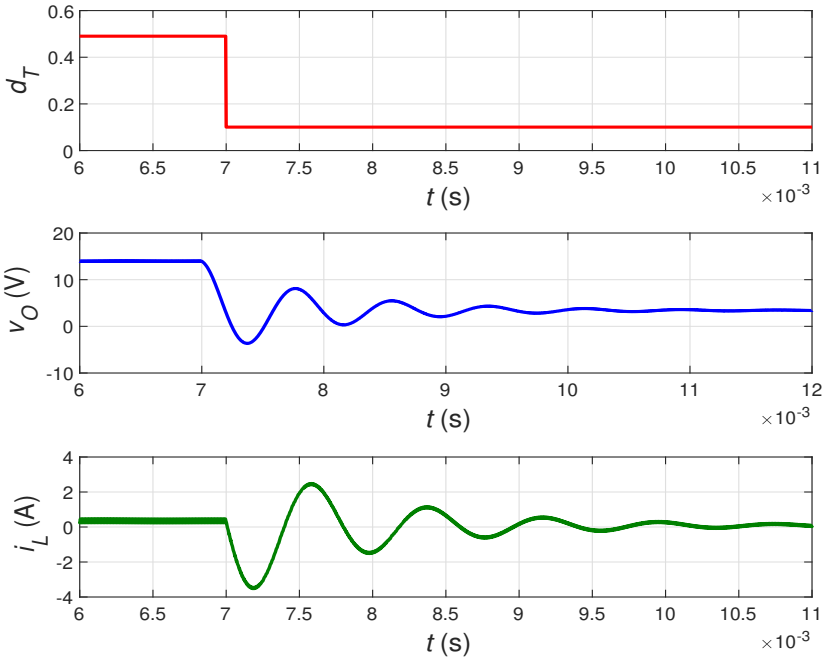
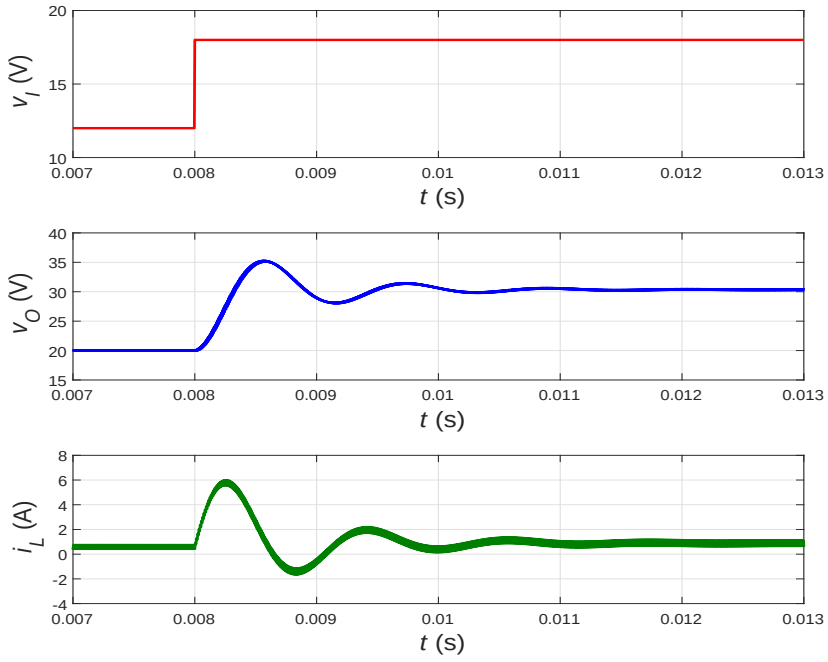
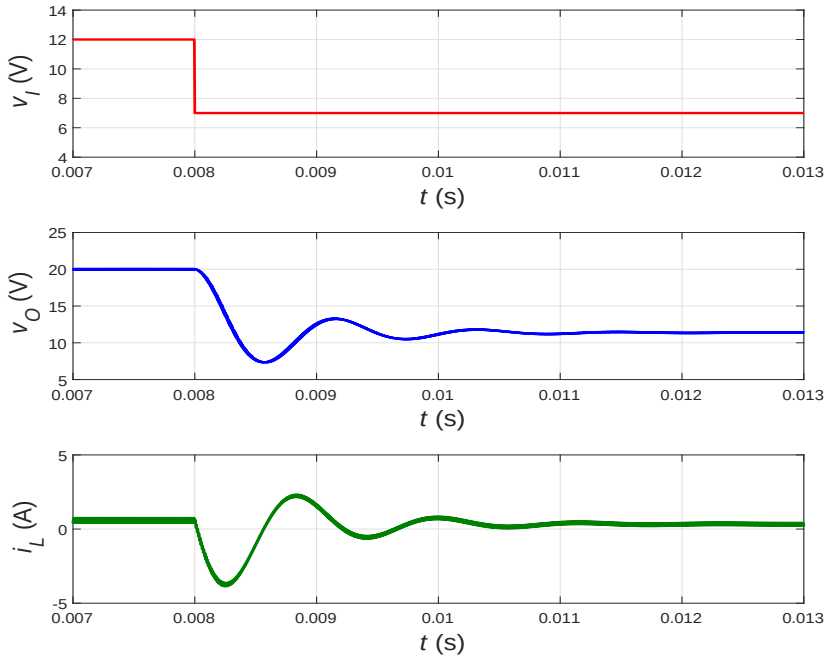


(b)

Figure 2.11: The open-loop response of the buck converter during a large step change in duty cycle d_T. a) Step change in d_T from 0.5 to 0.9. b) Step change in d_T from 0.5 to 0.1.

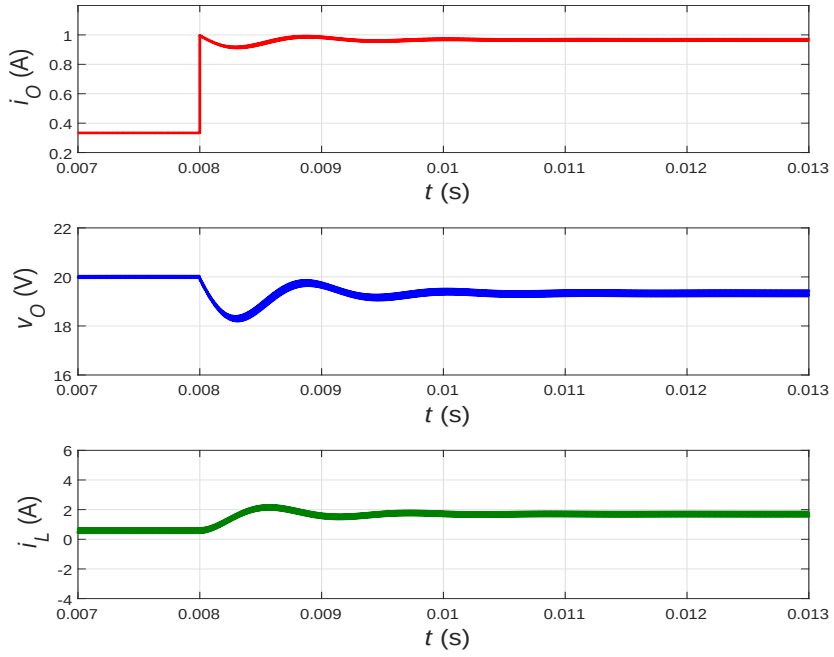


(a)



(b)

Figure 2.12: The open-loop response of the boost converter during a large step change in input voltage v_I. a) Step change in v_I from 12 V to 18 V. b) Step change in v_I from 12 V to 7 V.



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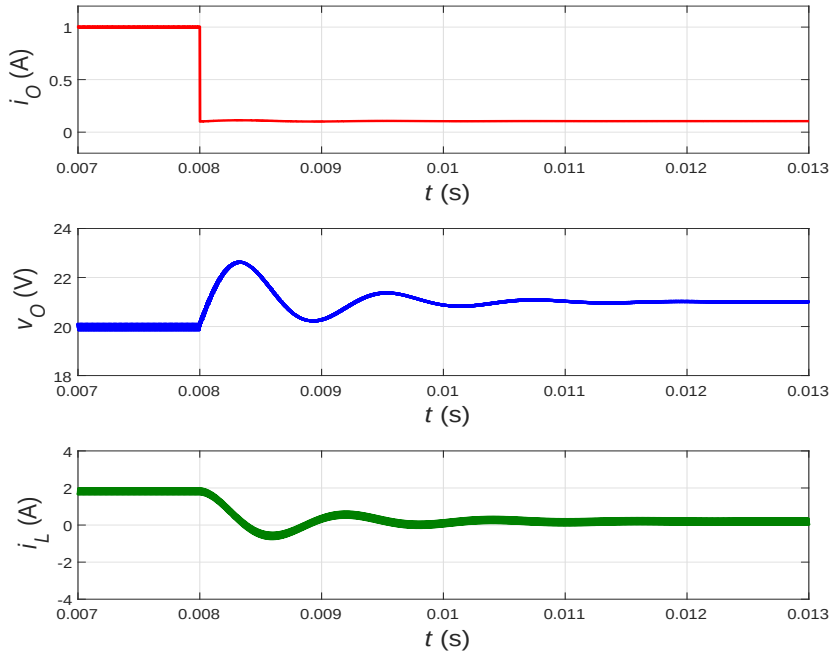
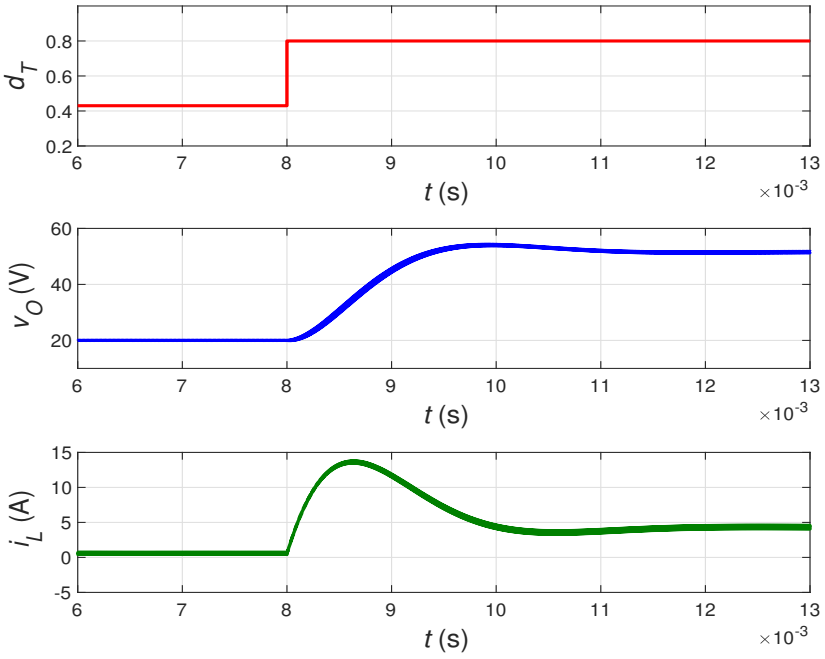


(b)

Figure 2.13: The open-loop response of the boost converter during a large step change in load current r. a) Step change in r from 60 Ω to 20 Ω. b) Step change in r from 20 Ω to 200 Ω.



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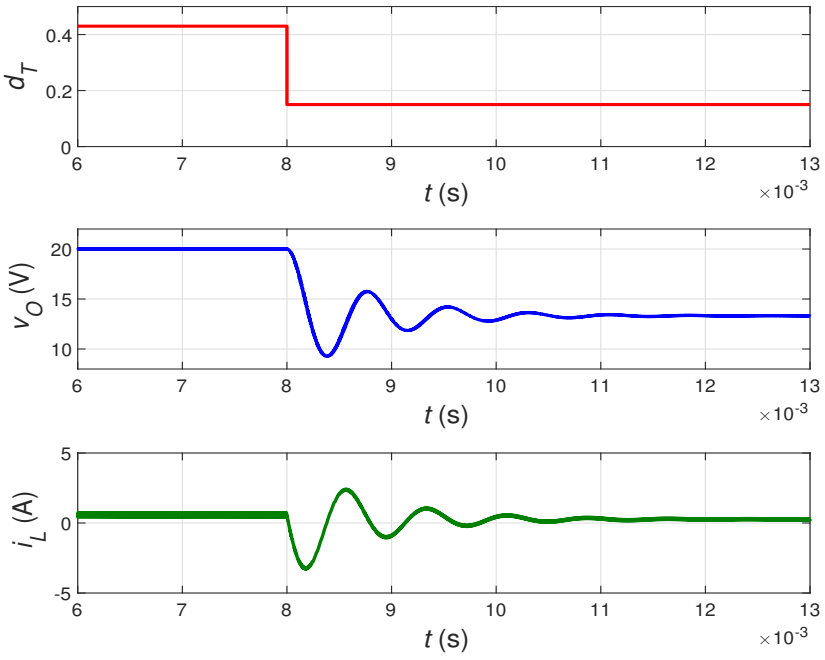


(b)

Figure 2.14: The open-loop response of the boost converter during a large step change in duty cycle d_T. a) Step change in d_T from 0.44 to 0.8. b) Step change in d_T from 0.44 to 0.15.

3 Closed-Loop SSMVC of PWM DC-DC Buck Converter

3.1 Introduction

In this chapter, a SSMVC of PWM dc-dc buck converter for CCM is introduced. Based on the behavioral model of the buck converter, the averaged control-oriented model is developed, and the equivalent control law is derived based on the invariance conditions. The existence and stability conditions are derived to determine the choice of the controller gains. The control equation is realized using a simple analogue circuit. The design procedure of the control circuit is given in detail. Simulation results based on MATLAB/SIMULINK and SaberRD are also presented. The regulation and tracking performance are investigated. Finally, the tracking performance and disturbance rejection capability of the proposed voltage-mode control system are compared with the other PWM-based control schemes.

3.2 Background

It is known that the pulse-width modulator compares the ramp voltage with the control signal to generate a square wave, which goes as an input to the gate driver of the power converter. Therefore, the fixed switching frequency of the ramp voltage is inherited to the v_{GS} that turns the switch ON and OFF. Such feature also exists in the design of linear voltage- and current-mode control of PWM dc-dc converter. However, this research focuses on deriving the SMC law based on the equivalent control method and mapping it onto a duty cycle for pulse-width modulator implementation.

As explained in Chapter 1, the idea of moving from the hysteresis modulation to the pulse-width modulation in SMC design of dc-dc converters was not straightforward. Considerable research efforts have been conducted to establish this theory and implement the PWM-based SM controller. The motivation of designing and implementing

PWM-based SMC using analogue components has been initiated by [7] and other related articles. The aforementioned endeavors are the base of designing a simplified version of SMC schemes of power converters that provides robust tracking and wide operating range. The key of designing the proposed nonlinear controllers relies on considering the averaged power converter dynamics under SM operation in the control design process, which is explained in the following sections.

3.3 Simplified Sliding-Mode Voltage Control

The control design procedure is introduced in the following subsections, and it is summarized as follows. First, a suitable switching function is defined to meet the hitting condition, which guarantees that all the trajectories reach the sliding surface regardless of their initial conditions. Next, the equivalent control law is derived and mapped onto a duty cycle to suit the pule-width-modulator implementation. Finally, the existence and stability conditions are derived to determine the criteria of choosing proper sliding coefficients. The existence condition ensures that all the trajectories remain in the neighborhood of the sliding manifold during the sliding phase, while the stability condition forces the trajectories toward the desired equilibrium point.

3.3.1 Control-Oriented Model of DC-DC Buck Converter

In order to design the SMC system, the dynamics of the dc-dc converter in terms of control state variables are required. In this chapter, the SM voltage control of PWM dc-dc buck converter for CCM is discussed. The control state variables can be chosen as

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} V_r - \beta v_O \\ \dot{x}_1 \\ \int x_1 dt \end{bmatrix}, \tag{3.1}$$

where V_r and β are the reference voltage and feedback network gain, respectively. The choice of states variables is decided based on the error output voltage, its time

derivative, and its integral terms. Hence, deriving the error output voltage signals to zero ensures that the control objective is achieved via tracking the desired trajectory. It is worth mentioning that the choice of state variables is similar to the one being made in HM-based PID SMVC [7]. However, in this design approach, the HM is replaced by a PWM with an equivalent control law to prevent the variation in switching frequency.

If the ideal nonlinear model of PWM dc-dc buck converter for CCM is reflected into (3.1), the control state variables yield

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} V_r - \beta v_O \\ -\frac{\beta}{C} i_C \\ \int (V_r - \beta v_O) dt \end{bmatrix}, \tag{3.2}$$

Thus, deriving (3.2) with respect to time results in the dynamics of the buck converter required for the design of SM controller [7]

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} -\frac{\beta}{C} i_C \\ \frac{\beta}{rC^2} i_C + \frac{\beta}{LC} v_O - \frac{\beta}{LC} v_I u \\ V_r - \beta v_O \end{bmatrix}. \tag{3.3}$$

In (3.3), u is the switching control law that takes the value 0 or 1. The dynamics given in (3.3) can also be described by control state variables as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} x_2 \\ -\frac{1}{LC} x_1 - \frac{1}{rC} x_2 + \frac{V_r}{LC} - \frac{\beta}{LC} v_I u \\ x_1 \end{bmatrix}. \tag{3.4}$$

According to [73], if the averaging theory is applied to a system defined by the dynamics $\dot{x} = f(x, t, \epsilon)$ with a small positive parameter ϵ, where $\dot{x}$ is T-periodic in t, then the averaged system dynamics are

$$\dot{\overline{x}} = \frac{1}{T} \int_0^T f(\overline{x}, \tau, \epsilon) d\tau. \tag{3.5}$$

Suppose that the Jacobian of (3.5) is Hurwitz. Then, the T-periodic solution of the average system $\dot{\overline{x}}$ is an $O(\epsilon)$ approximation for the exact solution of the system $\dot{x}$.

Hence, applying the averaging theory to (3.4) results in the averaged control-oriented model of dc-dc buck converter for CCM

$$\begin{bmatrix} \dot{\overline{x}}_1 \\ \dot{\overline{x}}_2 \\ \dot{\overline{x}}_3 \end{bmatrix} = \begin{bmatrix} \overline{x}_2 \\ -\frac{1}{LC}\overline{x}_1 - \frac{1}{\overline{r}C}\overline{x}_2 + \frac{V_r}{LC} - \frac{\beta}{LC}\overline{v}_I u_e \\ \overline{x}_1 \end{bmatrix}, \tag{3.6}$$

which can be expressed in terms of voltage and current as

$$\begin{bmatrix} \dot{\overline{x}}_1 \\ \dot{\overline{x}}_2 \\ \dot{\overline{x}}_3 \end{bmatrix} = \begin{bmatrix} -\frac{\beta}{C}\overline{i}_C \\ \frac{\beta}{\overline{r}C^2}\overline{i}_C + \frac{\beta}{LC}\overline{v}_O - \frac{\beta}{LC}\overline{v}_I u_e \\ V_r - \beta\overline{v}_O \end{bmatrix}, \tag{3.7}$$

where u_e is the averaged quantity of the switching control law u. The average capacitor current $\overline{i}_C$ is the difference between the averaged quantities of inductor and load currents

$$\overline{i}_C = \overline{i}_L - \overline{i}_O = 0. \tag{3.8}$$

In fact, the averaged capacitor current is zero at steady-state due to the charge/discharge process of the output filter capacitor at every switching period. In the following sections, it can be shown that the averaged control-oriented model is important in simplifying the equivalent control law and shaping the control system structure.

3.3.2 Equivalent Control Method

As shown in Fig. 3.1, the instantaneous trajectory during the sliding phase can be identified by high- and low-frequency components [6]. Obviously, the high-frequency component fluctuates up and down the sliding surface. On the other hand, the low-frequency component slides toward the origin. It is known that the instantaneous trajectory moves due to the action of the switching control law u. Therefore, the low-frequency component of the trajectory can be associated with a continuous switching function u_L such that $U^- < u_L < U^+$. Furthermore, the high-frequency component of

the trajectory is related to a discontinuous switching function u_H that is given by

$$u_H = \begin{cases} U^+ - u_L & \text{for } \psi > 0 \\ U^- - u_L & \text{for } \psi < 0 \end{cases}, \tag{3.9}$$

where ψ is the sliding surface or the instantaneous trajectory, which can be defined as a linear combination of the control state variables. Thus, the switching function is the sum of u_L and u_H. The component u_H is considered as unwanted high-frequency ripple, which can be removed from the switching control law u by the output filter of the converter. Hence, the movement of the instantaneous trajectory ψ can be decided by the component u_L only. Consequently, it is possible to assume that the component u_L is equivalent to the ideal switching function u that drives the instantaneous trajectory along the sliding manifold. This assumption results in the equivalent control law u_e, which has been summarized in [6] as follows.

For a dynamical system $\dot{x} = f(x, u, t)$ with an ideal SMC law, the instantaneous trajectory ψ moves on the sliding manifold toward the equilibrium point, yielding $\psi = 0$. If the high-frequency component of the instantaneous trajectory is ignored, then the dynamics of this trajectory $\dot{\psi}$ is also zero. Now, assuming that there is a control law u_e similar to the ideal control law u, which controls the trajectory under the sliding-mode operation. Hence, substituting the system $\dot{x}$ into the sliding surface dynamics $\dot{\psi}$ yields

$$\dot{\psi} = \frac{\partial \psi}{\partial x} f(x, u, t) = 0, \tag{3.10}$$

which may also be expressed as

$$\dot{\psi} = \frac{\partial \psi}{\partial x} f(x, u_e, t) = 0. \tag{3.11}$$

If (3.11) is solved for u_e, an equivalent control law is obtained. Additionally, substituting u_e into the system dynamics $\dot{x}$ yields

$$\dot{x} = f(x, u_e, t) = 0, \tag{3.12}$$

where the latter is called the system dynamics under SM operation.

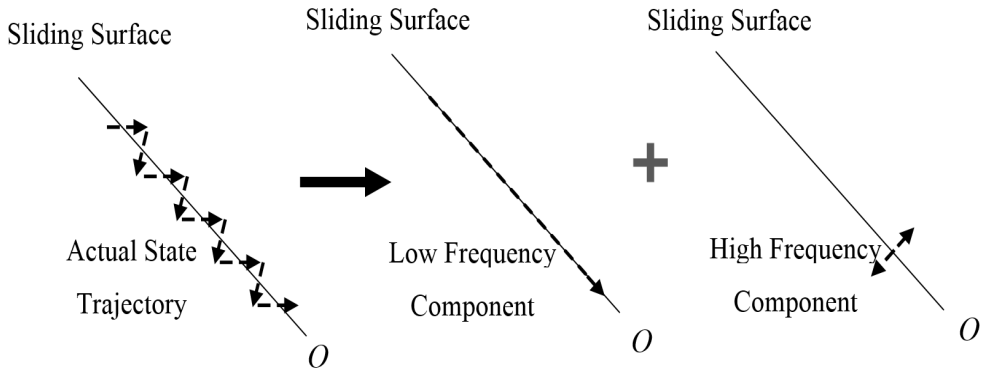


Figure 3.1: The state trajectory with low and high frequency components during sliding phase.

3.3.3 Derivation of Equivalent Control Law

The derivation process is summarized as follows [7]. First, the equivalent control law u_e is derived from the sliding surface dynamics by solving $\dot{\psi} = 0$. Next, u_e is mapped onto a duty cycle d_T to implement the pulse-width modulator. The general sliding-mode control law that meets the hitting condition is defined as a switching function

$$u = \begin{cases} 1 & \text{for } \psi > 0 \\ \\ 0 & \text{for } \psi < 0 \end{cases}, \tag{3.13}$$

whereas the sliding surface ψ is chosen as

$$\psi = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3. \tag{3.14}$$

The parameters α_1, α_2, and α_3 are positive constants that represent the sliding coefficients.

The implementation of the SM controller via a pulse-width modulator is not straightforward. The equivalent control law should be derived and translated to a duty cycle, so that it becomes applicable to PWM dc-dc converters [7], [62]. Moreover, the pulse-width modulator is needed to maintain a constant switching frequency during the SM operation, thus the complications associated with the design of required filters and EMI issues are reduced [6]. The equivalent control law can be derived based on

the invariance conditions [7], in which the sliding surface dynamics $\dot{\psi}$ yield

$$\dot{\psi} = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 = 0. \tag{3.15}$$

Next, substituting the averaged control-oriented model into (3.15) results in

$$\alpha_1 \Big(- \frac{\beta \bar{i}_C}{C} \Big) + \alpha_2 \Big[\frac{\beta \bar{i}_C}{\overline{r} C^2} + \frac{\beta}{LC} (\overline{v}_O - \overline{v}_I u_e) \Big] + \alpha_3 \Big(V_r - \beta \overline{v}_O \Big) = 0. \tag{3.16}$$

It is known that the averaged capacitor current $\bar{i}_C$ is zero at steady-state. Hence, if $\bar{i}_C$ terms are neglected, then $\dot{\psi}$ becomes

$$\alpha_2 \Big[\frac{\beta}{LC} (\overline{v}_O - \overline{v}_I u_e) \Big] + \alpha_3 \Big(V_r - \beta \overline{v}_O \Big) = 0. \tag{3.17}$$

Thus, solving for the equivalent control law yields

$$u_e = LC \frac{\alpha_3}{\alpha_2} \frac{V_r - \beta \overline{v}_O}{\beta \overline{v}_I} + \frac{\overline{v}_O}{\overline{v}_I}. \tag{3.18}$$

The equivalent control law u_e is a continuous function, where $0 < u_e < 1$. Now, if (3.18) is substituted into the inequality, and the latter is multiplied by $\beta \overline{v}_I$, one obtains the following

$$0 < \hat{u}_e = LC \frac{\alpha_3}{\alpha_2} \Big(V_r - \beta \overline{v}_O \Big) + \beta \overline{v}_O < \beta \overline{v}_I. \tag{3.19}$$

According to [7], the relationship among the duty cycle d_T, control signal $\hat{u}_e$, and peak ramp voltage V_T can be written as

$$0 < d_T = \frac{\hat{u}_e}{V_T} < 1. \tag{3.20}$$

Thus, the comparison between the equivalent control equation and the duty cycle yields

$$\hat{u}_e = K(V_r - \beta \overline{v}_O) + \beta \overline{v}_O \tag{3.21}$$

and

$$V_T = \beta \overline{v}_{I(nom)}, \tag{3.22}$$

where $\overline{v}_{I(nom)}$ is the nominal input voltage and K is the sliding-mode controller gain that is defined by

$$K = LC\frac{\alpha_3}{\alpha_2}. \tag{3.23}$$

The block diagram of the SSMVC of PWM dc-dc buck converter is shown in Fig. 3.2. Unlike [7], [62], the capacitor current is not required in the control equation, which results in a control scheme with reduced complexity and components count. Additionally, the peak ramp voltage V_T in (3.22) is defined by the nominal input voltage $\overline{v}_{I(nom)}$. Thus, the feedback signal is constructed by the sum of the sensed output voltage and the output voltage error scaled by the controller gain K. As reported in [62], the control equation can be scaled down by a constant γ, where $0 < \gamma < 1$. Such modification keeps the SM controller parameters within practical range for the analogue implementation. Hence, (3.21) and (3.22) can be rewritten as

$$\hat{u}_e = \gamma K(V_r - \beta \overline{v}_O) + \gamma \beta \overline{v}_O \tag{3.24}$$

and

$$V_T = \gamma \beta \overline{v}_{I(nom)}. \tag{3.25}$$

3.3.4 Remarks

1) It can be noticed that the control equation $\hat{u}_e$ contains the averaged value of the output voltage, but the instantaneous output voltage is utilized in the control scheme. This is because the averaged output voltage is the main component that contributes in the control action, whereas the effect of the output voltage ripple is negligible.

2) The implementation of the pulse-width modulator reduces the robustness of the sliding-mode controller, but it maintains a constant and finite switching frequency.

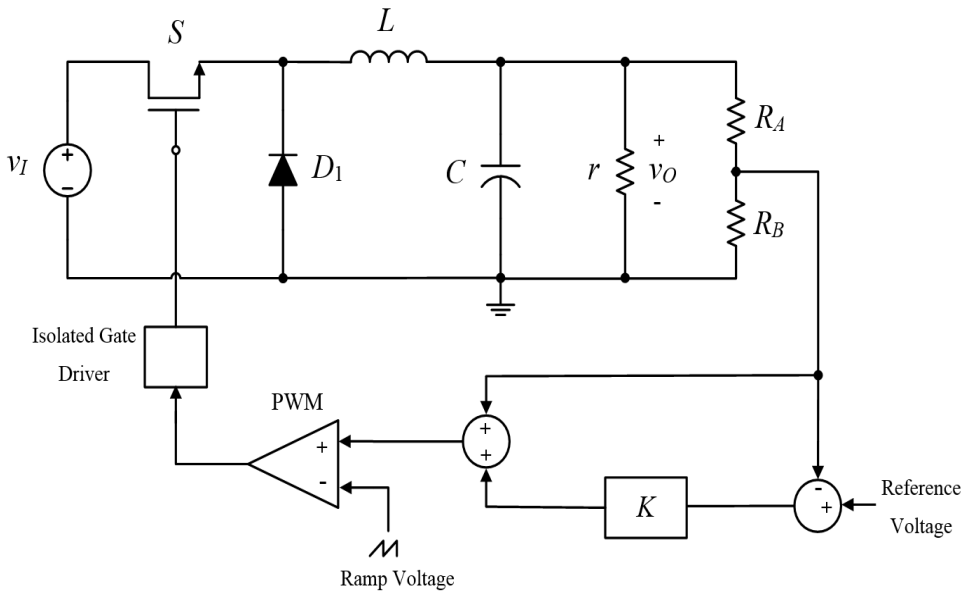


Figure 3.2: The block diagram of the PWM-based SM voltage control of dc-dc buck converter for CCM.

Thus, the problems associated with the high and variable switching frequency can be avoided.

3.3.5 Existence and Stability Conditions

The existence and stability conditions must be considered to achieve a proper choice for the sliding coefficients. According to [7], the existence condition is obtained via inspecting the local reachability condition $\psi\dot{\psi} < 0$, which is the time derivative of the Lyapunov function $V(\psi) = \frac{1}{2}\psi^2$, such that the inequality

$$\lim_{\psi \to 0} \psi\dot{\psi} < 0 \tag{3.26}$$

is satisfied. The condition (3.26) can be also be expressed in two cases:

$$\begin{cases} \psi \to 0^+ & \text{, where } \dot{\psi} < 0 \text{ and } u = 1 \\ \psi \to 0^- & \text{, where } \dot{\psi} > 0 \text{ and } u = 0 \end{cases}. \tag{3.27}$$

The first case yields

$$\alpha_2 \frac{\beta}{LC}(v_O - v_I) + \alpha_3(V_r - \beta v_O) < 0, \tag{3.28}$$

whereas the second case gives

$$\alpha_2 \frac{\beta}{LC} v_O + \alpha_3 (V_r - \beta v_O) > 0. \tag{3.29}$$

Combining the two cases, one obtains the local existence condition

$$0 < \beta V_O + K(V_r - \beta V_O) < \beta V_I. \tag{3.30}$$

On the other hand, the local stability condition is derived as follows. First, the ideal sliding dynamics of buck converter in CCM is obtained, and the switching function is replaced by the equivalent control law. Next, the stability of the equilibrium point is analyzed via checking the Eigenvalues of the linearized sliding dynamics of the buck converter. If the Jacobian matrix is Hurwitz, then it can be concluded that the instantaneous trajectory converges to the desired equilibrium point on the sliding surface.

The ideal nonlinear buck converter model is given by

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_O + \frac{1}{L} v_I u \\ \frac{1}{C} i_L - \frac{1}{rC} v_O \end{bmatrix}, \tag{3.31}$$

where $v_O = v_C$. If the switching control law u is replaced by the equivalent control law u_e, one obtains the ideal sliding dynamics

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} v_O + \frac{1}{L} v_I u_e \\ \frac{1}{C} i_L - \frac{1}{rC} v_O \end{bmatrix}. \tag{3.32}$$

Assuming that the system dynamics have a stable equilibrium point at the origin, if $\dot{i}_L$ and $\dot{v}_O$ are set to zero, the equilibrium point $I_L = V_O/R$ is obtained. Hence, the ideal sliding dynamics can be linearized around the equilibrium point, yielding

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & \frac{\beta(1-K)-1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \end{bmatrix} = \begin{bmatrix} j_{11} & j_{12} \\ j_{21} & j_{22} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \end{bmatrix}, \tag{3.33}$$

where j_{11}, j_{12}, j_{21}, and j_{22} are the Jacobian matrix elements. Note that $\tilde{i}_L$ and $\tilde{v}_O$ represent the perturbed quantities of i_L and v_O around the equilibrium point. The linearization process has been performed assuming that $v_I = V_I$, $r = R$, and $V_r = \beta V_O$. It has also been assumed that $I_L \gg \tilde{i}_L$ and $V_O \gg \tilde{v}_O$. The characteristic equation of the linearized system is

$$\lambda^2 - (j_{11} + j_{22})\lambda + (j_{11}j_{22} - j_{12}j_{21}) = 0. \tag{3.34}$$

If the system given in (3.33) is stable, then (3.34) must satisfy the following

$$\begin{cases} j_{11} + j_{22} < 0 \\ j_{11}j_{22} - j_{12}j_{21} > 0 \end{cases}, \tag{3.35}$$

from which the local stability conditions yield

$$\begin{cases} \frac{1}{RC} > 0 \\ K > \frac{\beta - 1}{\beta} \end{cases}. \tag{3.36}$$

Hence, based on the existence and stability conditions given in (3.30) and (3.36), the SM voltage controller gain K can be selected.

3.4 Analogue Implementation of SSMVC Scheme

In this section, the MATLAB/SIMULINK model of the SSMV controlled PWM dc-dc buck converter for CCM is introduced. In addition, The analogue realization and the design procedure of the control circuit elements are presented.

3.4.1 Control Equation Parameters

The PWM dc-dc buck converter parameters have been given in Table II. The feedback network gain β is defined as $\beta = V_r/V_O$. If V_r and V_O are 5 V and 14 V, respectively, then β is 0.3571. The SM controller gain K can be set to 250, which satisfies the existence and stability conditions. Since the nominal input voltage is 28 V, the peak

ramp voltage V_T is set to 5 V according to (3.25). Furthermore, a suitable scaling factor γ of 0.5 is selected to scale down V_T and K within the practical range of the analogue components. Hence, the SSMVC equation becomes

$$\hat{u}_e = 0.5\Big[250(V_r - \beta\overline{v}_O) + \beta\overline{v}_O\Big]. \tag{3.37}$$

The MATLAB/SIMULINK model of the SSMVC system is depicted in Fig. 3.3. The s-function template is coded inside the *Buck Converter* subsystem, which contains the nonlinear dynamics of the dc-dc buck converter for CCM. The pulse-width modulator and the equivalent control equation are coded inside the *PWM* and *SMC* subsystems, respectively.

3.4.2 Control Circuit Structure

The mathematical expression of the SSMVC law of PWM dc-dc converter should be converted into a simple analogue circuit. The circuit should also be simulated and compared with the corresponding design in MATLAB before moving to the experimental and prototype phases. Clearly, the control equation in (3.37) requires differential, summing, and inverting operational amplifiers. The output voltage can be sensed via a voltage divider. The analogue realization of SSMV controlled PWM dc-dc buck converter is shown in Fig. 3.4, which can be simulated and tested using SaberRD software.

3.4.3 Design Procedure

The design procedure of the control circuit parameters is partially adopted from [7], which can be summarized as follows:

1. Output voltage sensor: Assuming that V_r is 5 V, the feedback network gain $\beta = V_r/V_O = R_B/(R_A + R_B) = 0.3571$. If R_A is assumed to be 9.1 kΩ/1 %/0.25 W, then R_B is 5.1 kΩ/1 %/0.25 W.

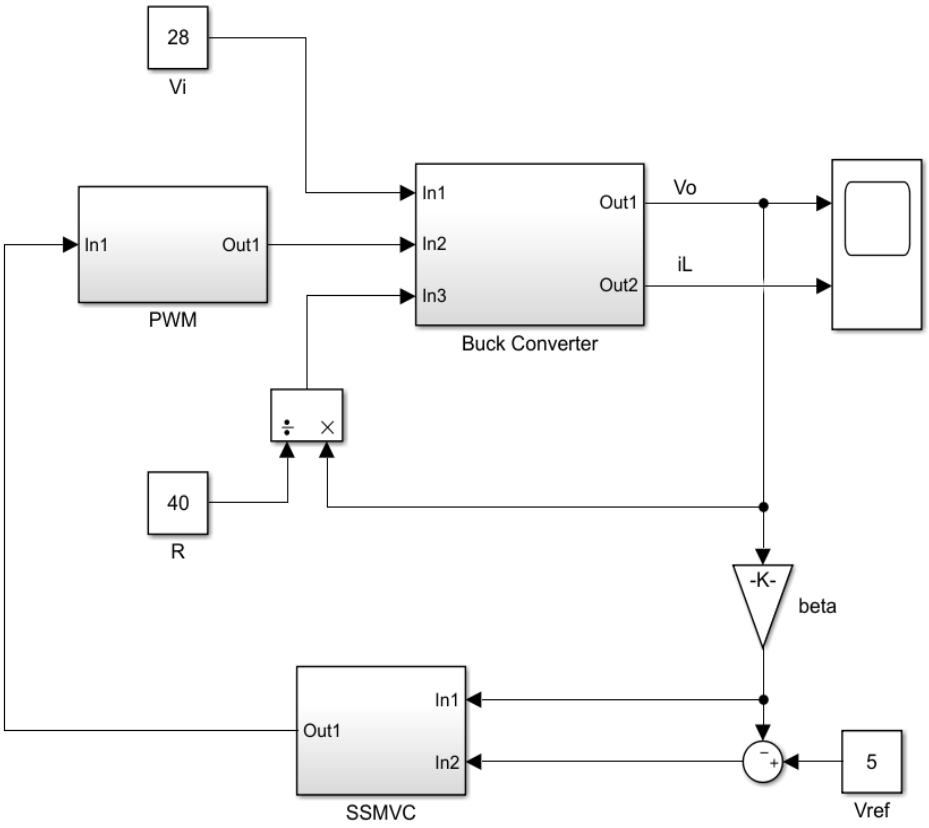


Figure 3.3: MATLAB/SIMULINK model of the SSMV controlled PWM dc-dc buck converter.

2. Differential amplifier: The controller gain K is selected as 250. Assuming that $R_F = R_D$ and $R_1 = R_2$ for the differential op-amp, K can be realized by the ratio R_F/R_{V1}. If R_1 and R_2 are chosen as 1 kΩ/5 %/0.25 W, then R_F and R_D are 250 kΩ/5 %/0.25 W.

3. Summing and inverting amplifiers: The resistors R_{S1}, R_{S2}, and R_{S3} for the summing op-amp and R_{I1} and R_{I2} for the inverting op-amp can be set to 5.1 kΩ/5 %/0.25 W.

4. PWM generator: Since the nominal input voltage is 28 V, the ramp voltage $V_T = \beta V_I = 10$ V, and a switching frequency of 100 kHz is selected.

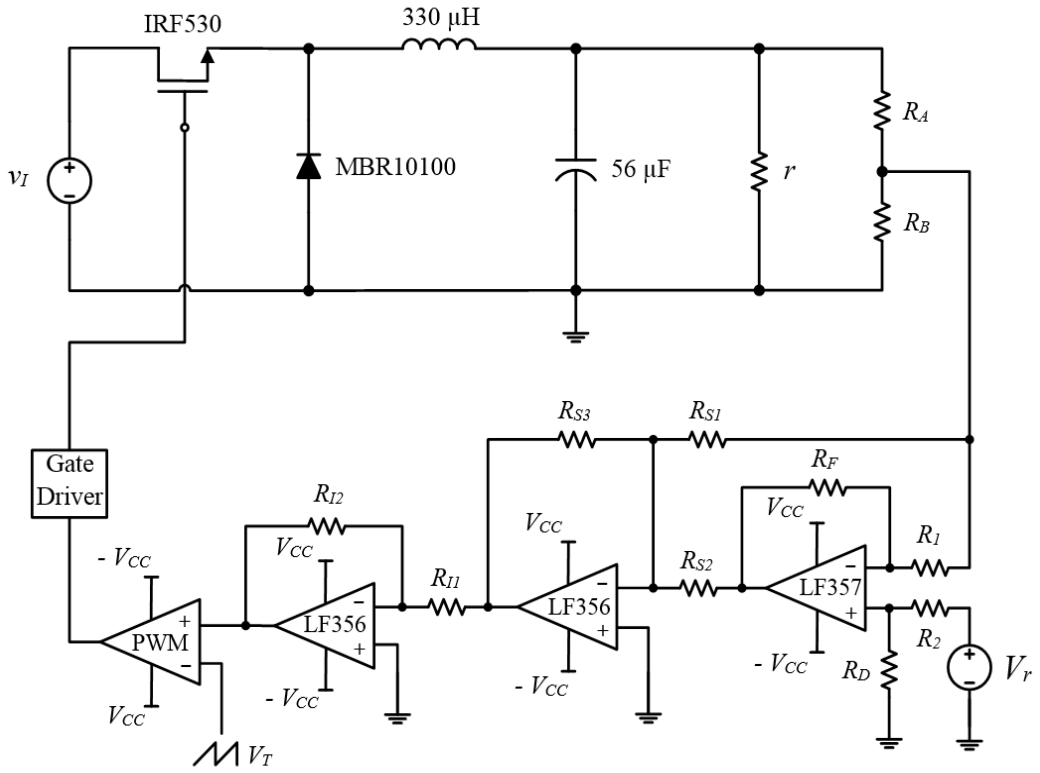


Figure 3.4: Analog realization of SSMV controlled PWM dc-dc buck converter for CCM.

5. Scaling factor: If a scaling factor γ is required to scale down V_T to 5 V, then R_{I1} and R_{I2} can be set to 2.5 kΩ/5 %/0.25 W and 5.1 kΩ/5 %/0.25 W, respectively.

It is worth mentioning that the choice of the SM controller gain K is not unique. The designer can choose any value within the practical range, but the gain must meet both the existence and stability conditions for a valid SMC design. In addition, the corresponding differential op-amp resistors R_F and R_D can be tuned to achieve an accurate tracking and a consistent transient response. It should also be noticed that the feedback resistors values should be selected such that $R_A + R_B >> R_{(max)}$ in order to minimize the loading effect of the control circuit.

3.5 Simulation Results and Discussions

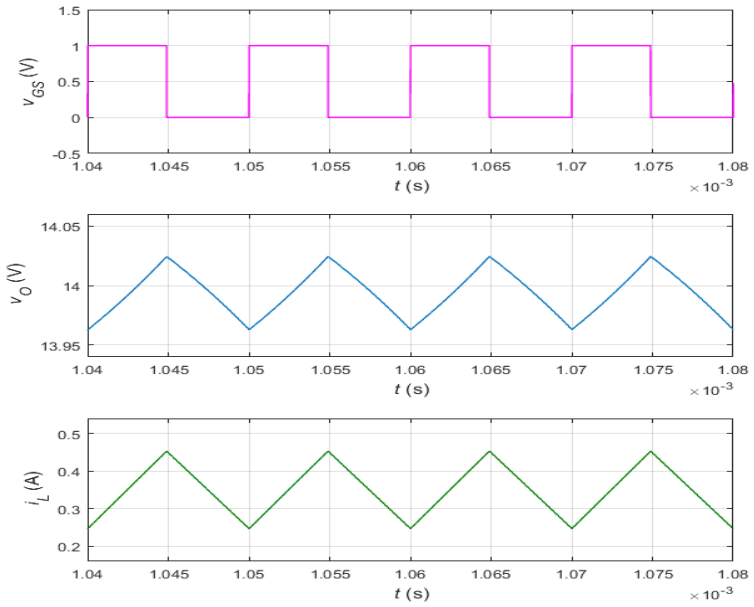
3.5.1 Steady-State Performance

The SSMV controlled PWM dc-dc buck converter has been simulated in SaberRD and compared with the corresponding MATLAB/SIMULINK model. The steady-state waveforms of the control system are depicted in Fig. 3.5. It can be noticed that the steady-state values of d_T, v_O, and i_L in MATLAB results are 0.51, 14.00 V, and 0.352 A, respectively. As for SaberRD results, the corresponding steady-state values are 0.5126, 13.997 V, and 0.35074 A, respectively. It can be seen that the simulated results of SaberRD and MATLAB are in good agreement, which validate the theoretical design approach. Notably, the tracking performance is excellent during steady-state, and the switching frequency is maintained constant, which is the main advantage of implementing the PWM-based voltage-mode control system.

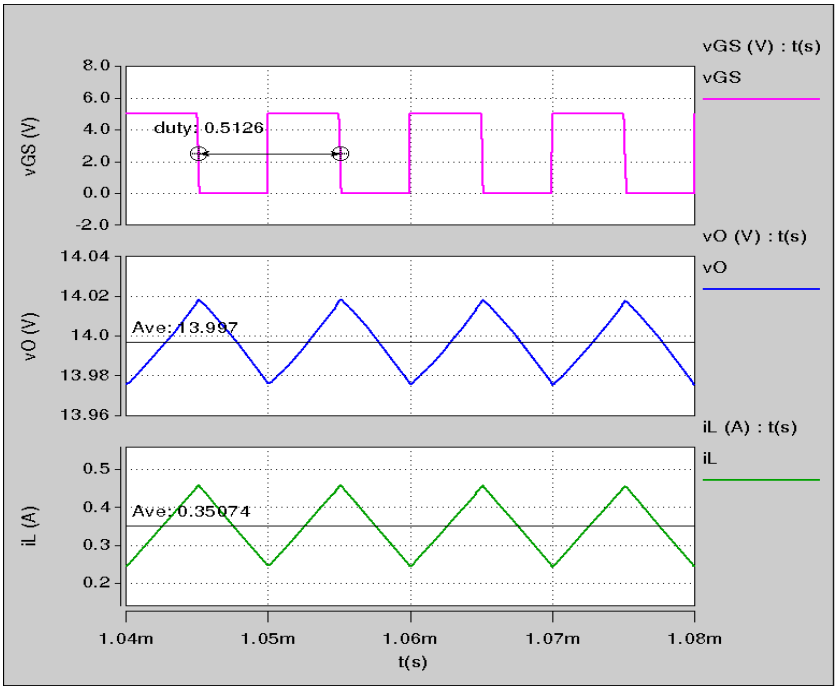
3.5.2 Tracking Performance under Large Disturbances

The response of the SSMVC of PWM dc-dc buck converter during abrupt and large line and load disturbances are shown in Figs. 3.6, 3.7, 3.8, and 3.9. The simulation is conducted using MATLAB/SIMULINK and SaberRD. The comparison between the two simulation platforms shows that the transient response in SaberRD is slightly different from the transient response obtained using MATLAB. This is due to the non-ideality of the switching elements and analogue components in SaberRD, which are not included in MATLAB/SIMULINK model. However, MATLAB results provide a good prediction for the analogue control circuit behavior in SaberRD and the practical implementation.

The load current i_O and output voltage v_O waveforms during abrupt increase and decrease in load current are depicted in Figs. 3.6 and 3.7, respectively. Based on the simulation results, it can be noticed that when i_O changes from 0.35 A to 0.7 A, the output voltage has an undershoot around 0.7 % and recovers the steady-state value



(a)



(b)

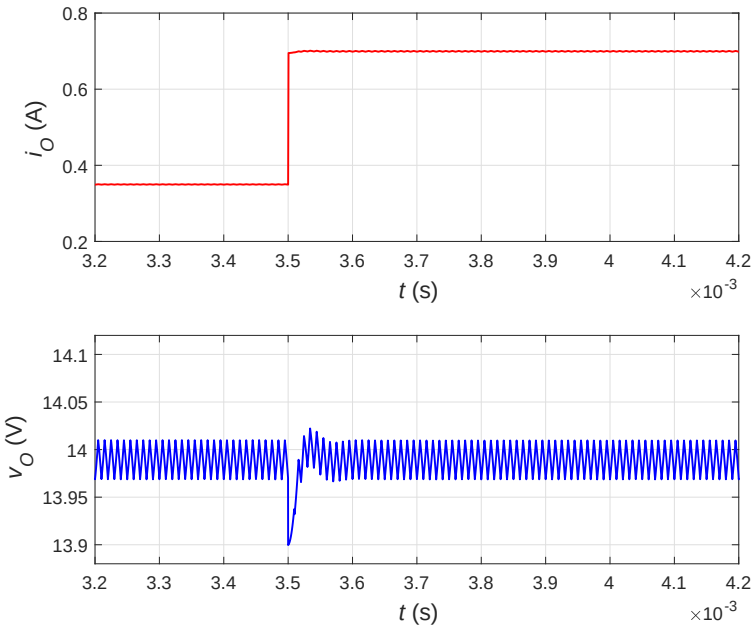
Figure 3.5: Steady-state waveforms of SSMV controlled PWM dc-dc buck converter for CCM. a) MATLAB results b) SaberRD results.

after 50 µs. On the other hand, when i_O deceases from 0.35 A to 0.08 A, v_O exhibits an overshoot of 0.5 %. After 50 µs, the output voltage settles at the steady-state value.

The input voltage v_I and output voltage v_O waveforms during abrupt increase and decrease in input voltage are shown in Figs. 3.8, and 3.9. It can be seen that the major effect of the line disturbance has been rejected, but there is a small deviation at the steady-state value of v_O, which is about ±30 mV. Hence, the output voltage tracks the desired value with a 3 % steady-state error. The tracking error has occured due to the implementation of the equivalent control equation via a pulse-width modulator. That is, the integral term does not appear in the SMC scheme, which is derived based on the equivalent control method. In order to improve the tracking performance of the proposed controller, a different control state variables should be chosen. One possible approach to eliminate the steady-state error is the design of the double-integral SSMVC, which has been introduced in Chapter 4.

3.5.3 Line and Load Regulation Performance

The regulation performance of the nonlinear controller of PWM dc-dc buck converter for CCM is investigated. The dc output voltage V_O versus dc load resistance R at different dc input voltage levels is plotted in Fig. 3.10. The range of dc quantities of load resistance and input voltage considered in this study is within 20 Ω to 190 Ω and 20 V to 42 V, respectively. It can be noticed that the output voltage remains close to the desired value 14 V within the entire range of load. Additionally, it can be noticed that as the input voltage level reduces, so does the dc output voltage. Obviously, the line regulation performance is degraded at $R = 20$ Ω and $V_I = 20$ V compared to all other operating conditions. The output voltage V_O is 13.96 V under maximum loading resistance and minimum input voltage, so V_O deviates 40 mV from the desired value. Hence, even at the worst operating condition, the output voltage is still within



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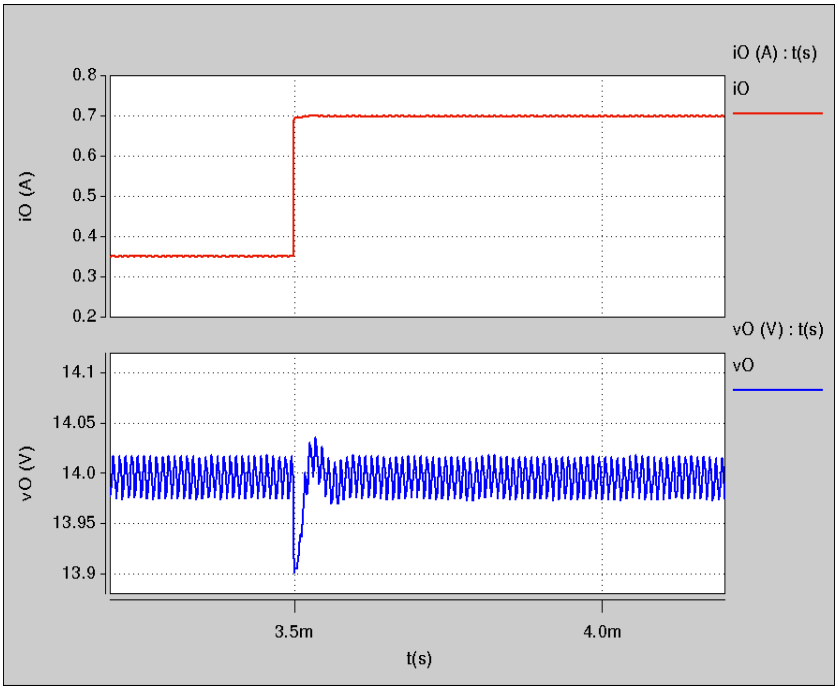
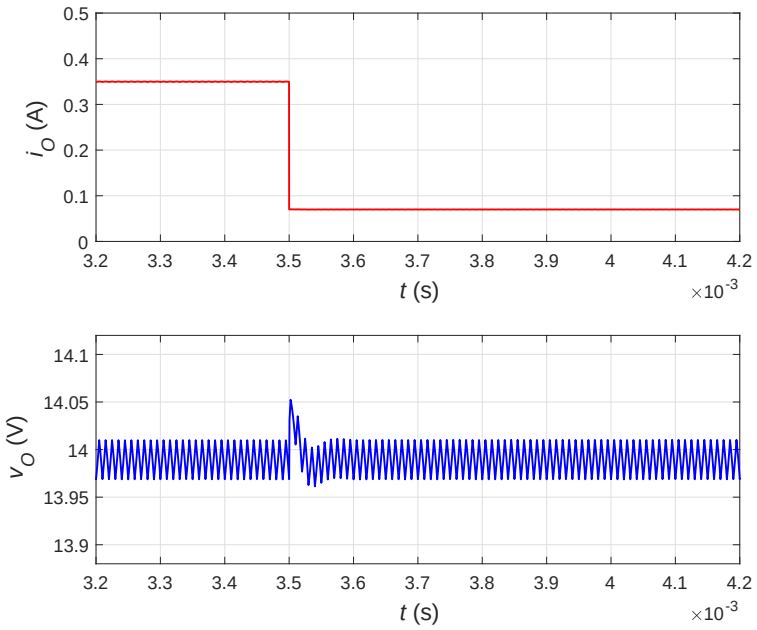


(b)

Figure 3.6: The SSMVC system response during abrupt increase in load current. a) MATLAB results b) SaberRD results.



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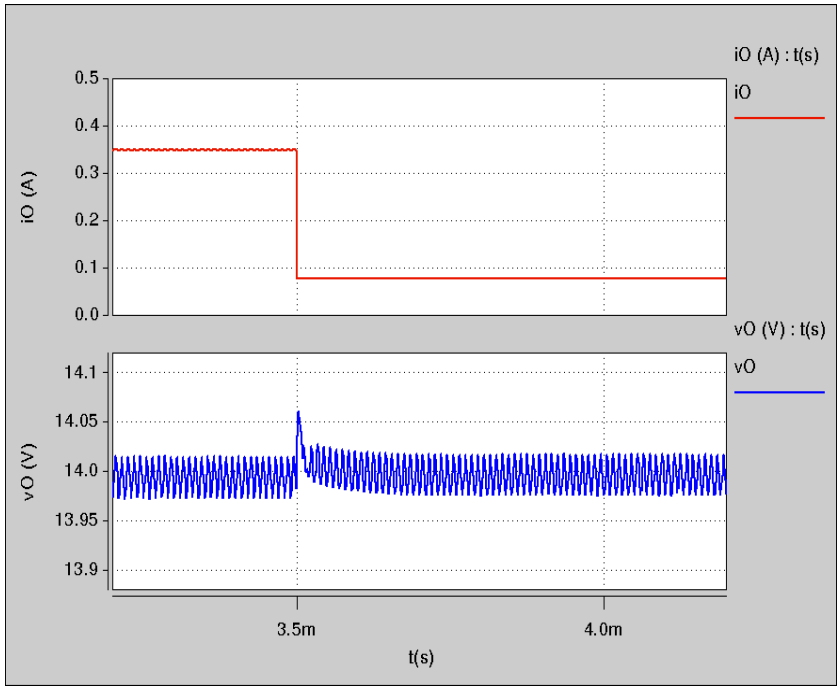
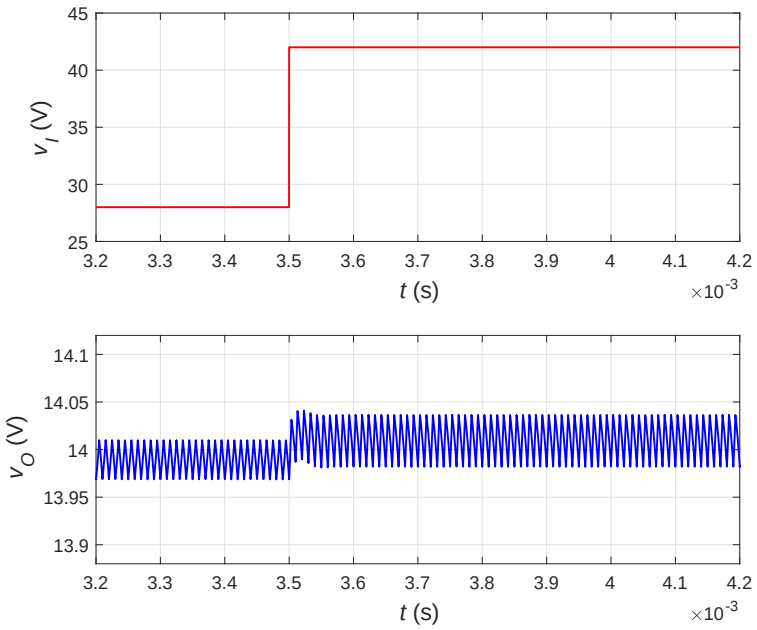


(b)

Figure 3.7: The SSMVC system response during abrupt decrease in load current. a) MATLAB results b) SaberRD results.



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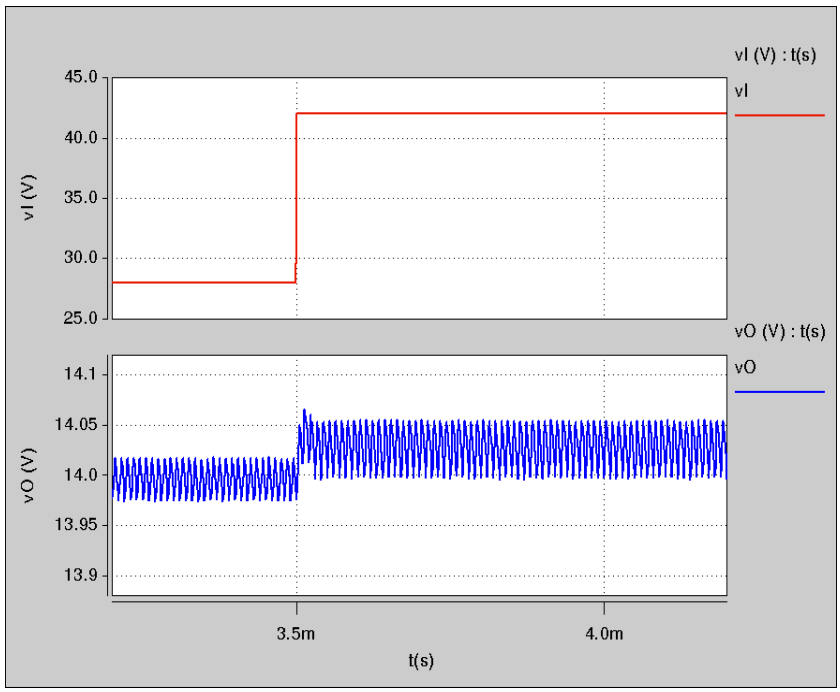

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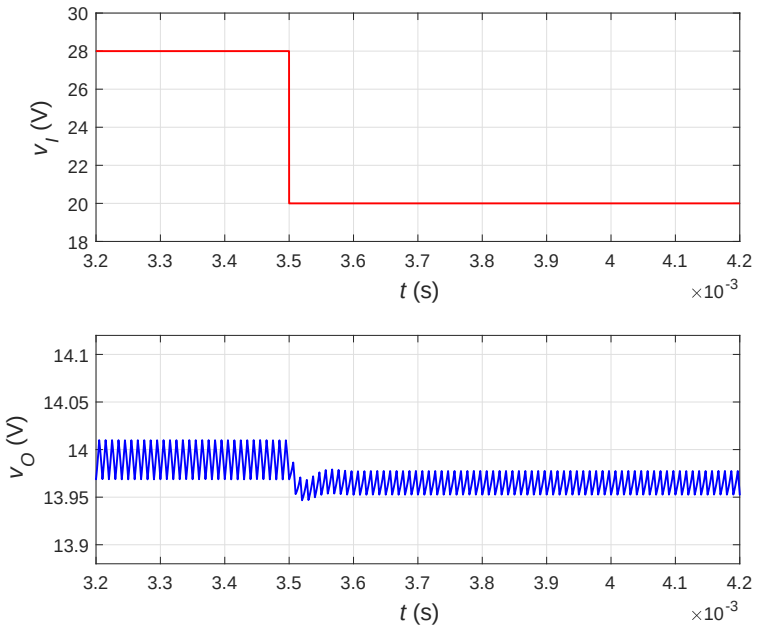
Figure 3.8: The SSMVC system response during abrupt increase in input voltage. a) MATLAB results b) SaberRD results.



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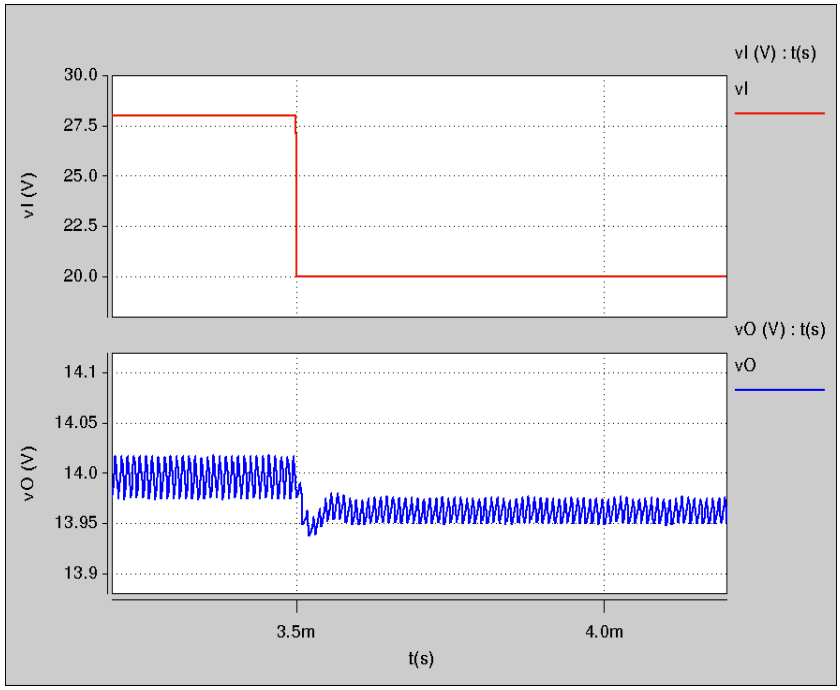


(b)

Figure 3.9: The SSMVC system response during abrupt decease in input voltage. a) MATLAB results b) SaberRD results.

an acceptable level.

According to [72], the line and load regulation performance of power converters can be analyzed using the percentage line and load regulation measures. The percentage line regulation $PLNR$ can be computed by

$$PLNR = \frac{\Delta V_O / V_{O(nom)} \times 100\%}{\Delta V_I}. \tag{3.38}$$

On the other hand, the percentage load regulation $PLOR$ is

$$PLOR = \frac{V_{O_{R_{(max)}}} - V_{O_{R_{(min)}}}}{V_{O_{R_{(min)}}}} \times 100\%, \tag{3.39}$$

Hence, based on (3.38) and (3.39), the $PLNR$ and $PLOR$ of the PWM-based SSMVC of dc-dc buck converter are calculated for several cases as shown in Tables VI and VII, respectively.

Table VI: Percentage Load Regulation of SSMVC System

$\boldsymbol{V_I}$ (V)	$\boldsymbol{\Delta V_O = V_{O_{R_{(max)}}} - V_{O_{R_{(min)}}}}$ (V)	$\boldsymbol{PLOR}$ (%)
20	0.005	0.0358
28	0.010	0.0715
35	0.019	0.1356
42	0.022	0.1568

Table VII: Percentage Line Regulation of SSMVC System

$\boldsymbol{R}$ (Ω)	$\boldsymbol{PLNR}$ (%/V)		
	$\boldsymbol{\Delta V_I = 28 \rightarrow 20}$ (V)	$\boldsymbol{\Delta V_I = 28 \rightarrow 35}$ (V)	$\boldsymbol{\Delta V_I = 28 \rightarrow 42}$ (V)
20	0.0313	0.0184	0.0168
50	0.0321	0.0194	0.0179
90	0.0321	0.0204	0.0179
130	0.0330	0.0204	0.0189
190	0.0357	0.0276	0.0230

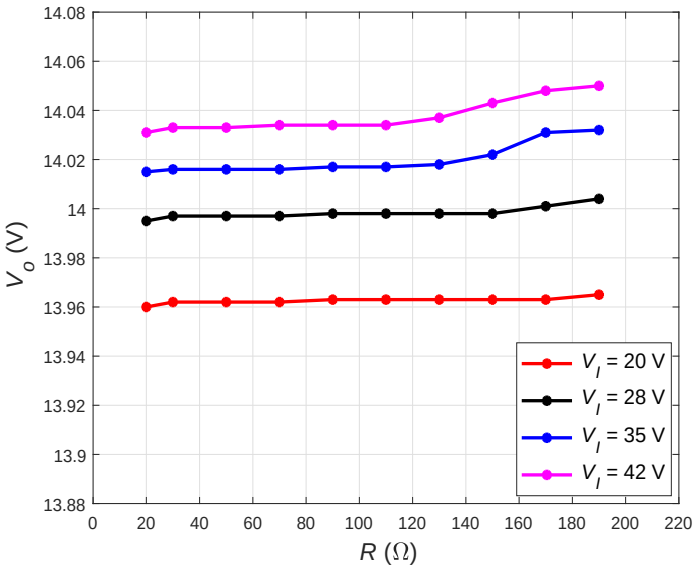


Figure 3.10: The output voltage V_O versus load resistance R at different input voltages V_I.

It can be noticed the control system provides good line and load regulation. As shown in Table VI, the maximum $PLOR$ is 0.1568 %, which occurs at the input voltage $V_I = 42$ V. At this operating condition, when the load resistance changes from minimum 20 Ω to maximum 190 Ω, the deviation in output voltage is only 22 mV. On the other hand, the maximum $PLNR$ is 0.0357 %/V, which occurs when the input voltage changes from the nominal value 28 V to 20 V at 190 Ω load resistance. Thus, the tabulated results show that the proposed control system maintains the output voltage of the buck converter close to the desired value under various operating condition.

3.5.4 Comparison with Other PWM-Based Controllers

The tracking performance of the proposed control system is compared with two PWM-based linear voltage-mode controllers, which are a PI controller and a Type II controller. The proportional and integral gains of the PI controller are set to 3.6 and 1650, respectively. Type II controller, on the other hand, is designed based on [72] to

achieve a phase margin of 42°, from which the transfer function of the controller is

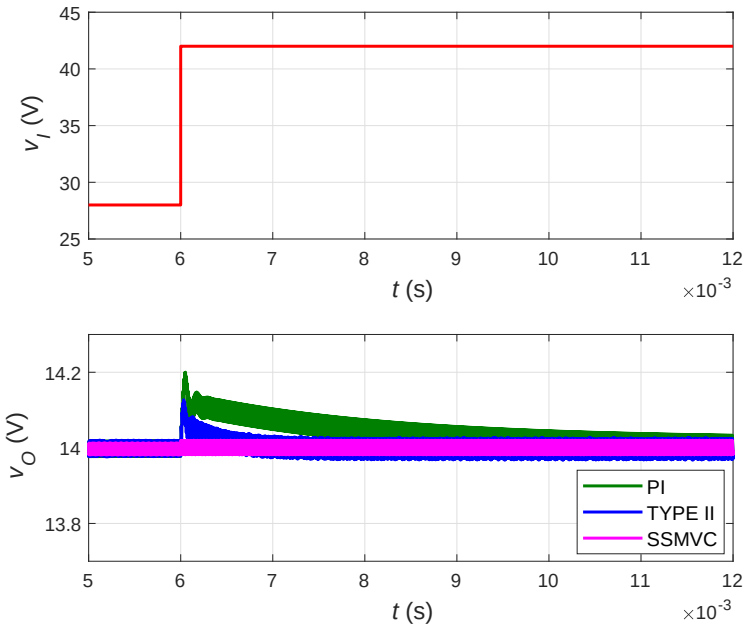
$$T_c(s) = \frac{v_o(s)}{d(s)} = 4.4 \times 10^7 \frac{s + 2691}{s(s + 1.467 \times 10^6)}. \tag{3.40}$$

The output voltage response of the proposed, PI, and Type II controllers during large line and load disturbances are shown in Figs. 3.11 and 3.12, respectively. It can be noticed that the PWM-based SSMVC system exhibits a lower percentage overshoot and a shorter settling time as compared to the other control systems. This is due to the fact that the linear controllers are designed based on the linearized buck converter model, thus they are only effective for a small deviation around the operating point. On the other hand, it can be seen that the response of the proposed controller shows a steady-state error, especially during the line disturbance. This is attributed to the implementation of the equivalent control method, which yields a degraded SMC performance. Table VIII summarizes the transient response characteristics of the PWM-based controllers during large disturbances.

Table VIII: Transient Response Characteristics of SSMVC, PI, and Type II Controllers during Large Disturbance

$\boldsymbol{\Delta V_I / \Delta R}$	**SSMVC**			**TYPE II**			**PI**		
	PO/PU (%)	t_s (ms)	V_O (V)	PO/PU (%)	t_s (ms)	V_O (V)	PO/PU (%)	t_s (ms)	V_O (V)
$\Delta V_I =$ $28 \rightarrow 42$ (V)	0.13	0.05	14.03	0.7	0.50	14	1.3	5.0	14
$\Delta V_I =$ $28 \rightarrow 20$ (V)	0.14	0.05	13.97	0.9	1.50	14	1.6	6.0	14
$\Delta R =$ $60 \rightarrow 15$ (Ω)	1.3	0.03	13.99	1.4	0.2	14	1.6	0.2	14
$\Delta R =$ $15 \rightarrow 200$ (Ω)	1.3	0.03	13.99	1.6	0.15	14	2.0	0.2	14

Additionally, the proposed controller is compared with the conventional PWM-



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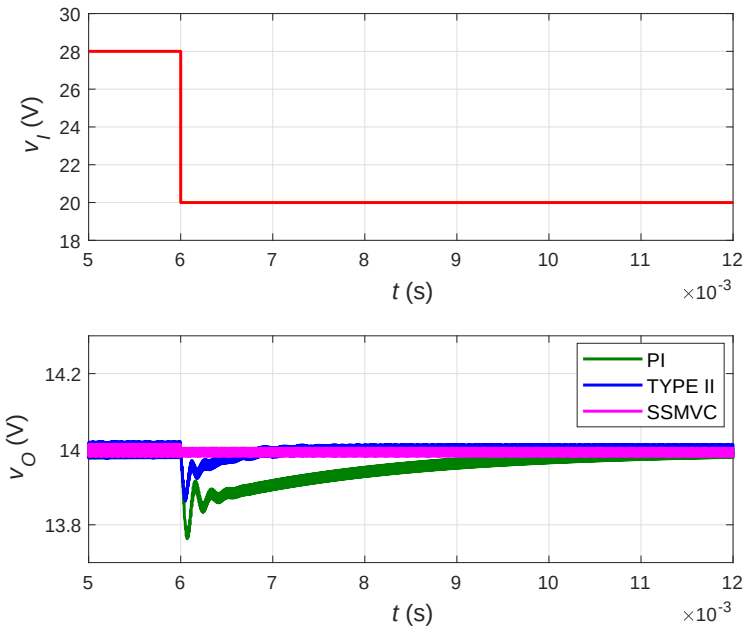
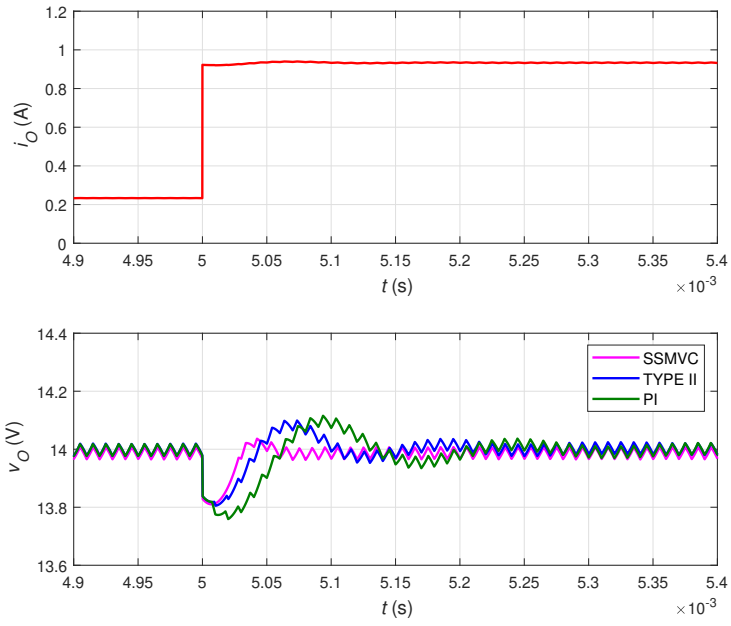
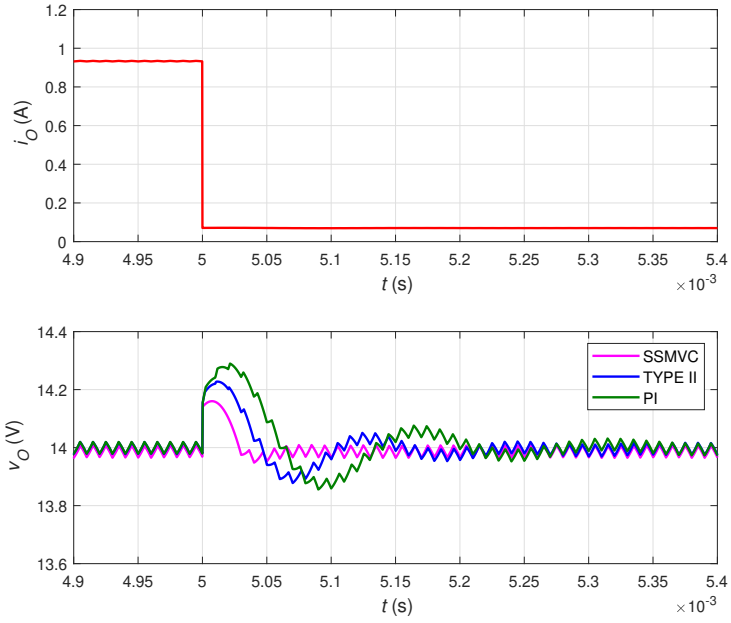


(b)

Figure 3.11: The output voltage response v_O of the proposed, PI, and Type II control systems under large (a) increase and (b) decrease in input voltage v_I.



(a)



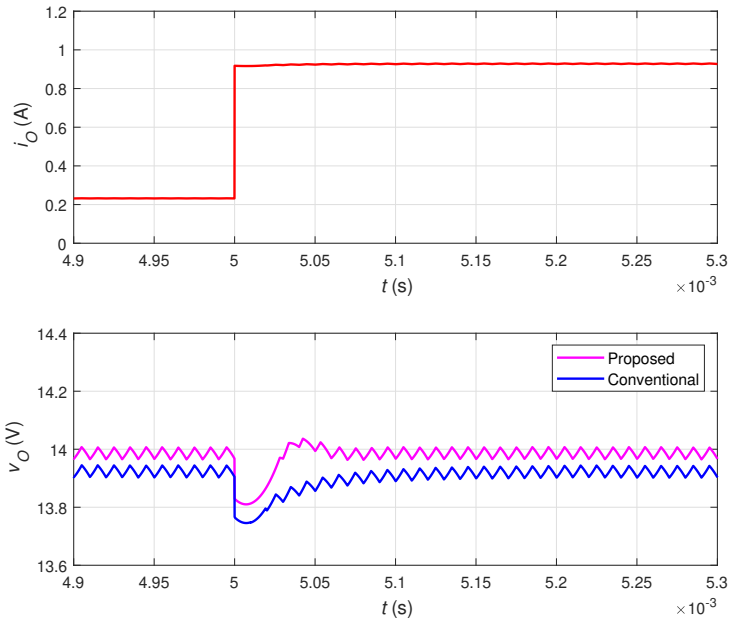
(b)

Figure 3.12: The output voltage response v_O of the proposed, PI, and Type II control systems under large (a) increase and (b) decrease in load current i_O.

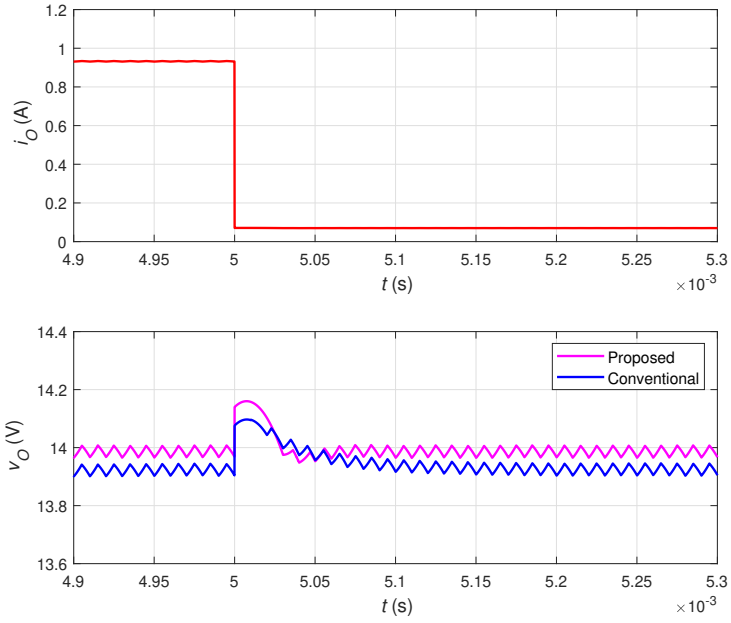
based SMVC system given in [7], [62], where the latter is designed to achieve a system bandwidth of 10 kHz and defined by

$$\begin{cases} u_e^* = -13.3 i_C + 60.8(V_r - \beta v_O) + \beta v_O \\ V_T = 10\text{V} \end{cases} . \tag{3.41}$$

The output voltage response of the two control systems during large load disturbance is depicted in Fig. 3.13. It can be noticed that proposed controller is featured with a simpler control law and produces a smaller steady-state error as compared to the controller given in [7], [62]. It can also be noticed that the effect of the capacitor current is not significant in the control action. In contrast, the sensed output voltage βv_O and the output voltage error $V_r - \beta v_O$ play a vital role in the tracking, regulation, and disturbance rejection.



(a)



(b)

Figure 3.13: The output voltage response v_O of the proposed and conventional SMVC systems under large (a) increase and (b) decrease in load current i_O.

4 Closed-Loop PI-SSMVC of PWM DC-DC Buck Converter

4.1 Introduction

A PI-SSMVC of PWM dc-dc buck converter for CCM is designed. The averaged control-oriented model is obtained based on the behavioral buck converter model, and a proper sliding surface is selected. The equivalent control law along with the existence and stability conditions are derived. The design procedure and analogue realization of the control circuit are explained. The control design is also validated using MATLAB/SIMULINK and SaberRD simulations. The regulation performance is analyzed, and the tracking performance is compared with the other PWM-based sliding-mode voltage control circuits.

4.2 PI-Simplified Sliding-Mode Voltage Control

The PWM-based SSMVC of dc-dc buck converter has been discussed in Chapter 3. It has been noticed that the choice of the control state variables and averaging the control-oriented model can shape the SM control circuit. In addition, both of the traditional PWM-based SMVC and the simplified control schemes exhibit the disturbance rejection property, but they introduce a steady-state error at the output voltage response. This is attributed to the implementation of the equivalent control law via a pulse-width modulator. Although an integral term is included in the control state variables, the application of the equivalent control method does not benefit from the entire combination of the control state variables. According to [61], one possible approach to eliminate the steady-state error can be achieved using a double-integral sliding term in the control state variables to increase the system type. Such design approach results in a PWM-based SSMVC scheme cascaded with a proportional-integral (PI) controller, which is called PWM-based PI-SSMVC system.

The control state variables x_1, x_2, x_3, and x_4 can be chosen as an output voltage error, a time derivative of output voltage error, an integral of output voltage error, and a double integral of output voltage error, respectively

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} V_r - \beta v_O \\ \dot{x}_1 \\ \int x_1 dt \\ \iint x_1 dt \end{bmatrix}. \tag{4.1}$$

The fourth state in (4.1) contains a double integral term, which is added to ensure a precise tracking performance during the large disturbance condition.

4.2.1 Control-Oriented Model of DC-DC Buck Converter

If the buck converter model in CCM is reflected by the control state variables given by (4.1), one obtains

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} V_r - \beta v_O \\ -\frac{\beta}{C} i_C \\ \int (V_r - \beta v_O) dt \\ \iint (V_r - \beta v_O) dt \end{bmatrix}. \tag{4.2}$$

The control state variables can be derived with respect to time, which give

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} x_2 \\ \frac{\beta}{rC^2} i_C - \frac{\beta v_I}{LC} u + \frac{\beta v_O}{LC} \\ x_1 \\ x_3 \end{bmatrix}. \tag{4.3}$$

Thus, the averaged control-oriented model is obtained via averaging (4.3), yileding

$$\begin{bmatrix} \dot{\overline{x}}_1 \\ \dot{\overline{x}}_2 \\ \dot{\overline{x}}_3 \\ \dot{\overline{x}}_4 \end{bmatrix} = \begin{bmatrix} \overline{x}_2 \\ \frac{\beta}{rC^2} \overline{i}_C - \frac{\beta \overline{v}_I}{LC} u_e + \frac{\beta \overline{v}_O}{LC} \\ \overline{x}_1 \\ \overline{x}_3 \end{bmatrix}. \tag{4.4}$$

The expression in (4.4) can also be written as

$$\begin{bmatrix} \dot{\overline{x}}_1 \\ \dot{\overline{x}}_2 \\ \dot{\overline{x}}_3 \\ \dot{\overline{x}}_4 \end{bmatrix} = \begin{bmatrix} -\frac{\beta}{C}\overline{i}_C \\ \frac{\beta}{rC^2}\overline{i}_C - \frac{\beta\overline{v}_I}{LC}u_e + \frac{\beta\overline{v}_O}{LC} \\ V_r - \beta\overline{v}_O \\ \int(V_r - \beta\overline{v}_O)dt \end{bmatrix}. \tag{4.5}$$

4.2.2 Equivalent Control Law

A switching control law can be defined as

$$u = \begin{cases} 1 & \text{for } \psi > 0 \\ \\ 0 & \text{for } \psi < 0 \end{cases} \tag{4.6}$$

to satisfy the hitting condition, where the sliding surface ψ is given by

$$\psi = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4. \tag{4.7}$$

If (4.7) is derived with respect to time, one obtains the following

$$\dot{\psi} = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 + \alpha_4 \dot{x}_4 = 0, \tag{4.8}$$

which is equated to zero based on the invariance conditions. The averaged control-oriented model in (4.5) can be substituted into (4.8), yielding

$$\alpha_1\Big(-\frac{\beta}{C}\overline{i}_C\Big) + \alpha_2\Big(\frac{\beta}{rC^2}\overline{i}_C - \frac{\beta\overline{v}_I}{LC}u_e + \frac{\beta\overline{v}_O}{LC}\Big) + \alpha_3\Big(V_r - \beta\overline{v}_O\Big) + \alpha_4\Big[\int(V_r - \beta\overline{v}_O)dt\Big] = 0. \tag{4.9}$$

If the terms $\overline{i}_C$ are neglected, then (4.9) becomes

$$\alpha_2\Big(-\frac{\beta\overline{v}_I}{LC}u_e + \frac{\beta\overline{v}_O}{LC}\Big) + \alpha_3\Big(V_r - \beta\overline{v}_O\Big) + \alpha_4\Big[\int(V_r - \beta\overline{v}_O)dt\Big] = 0. \tag{4.10}$$

Thus, rearranging (4.10) yields the equivalent control equation

$$u_e = LC\frac{\alpha_3}{\alpha_2}\Big(\frac{V_r - \beta\overline{v}_O}{\beta\overline{v}_I}\Big) + LC\frac{\alpha_4}{\alpha_2}\Big[\frac{\int(V_r - \beta\overline{v}_O)dt}{\beta\overline{v}_I}\Big] + \frac{\overline{v}_O}{\overline{v}_I}, \tag{4.11}$$

which can also be expressed as

$$u_e = K_p\Big(\frac{V_r - \beta\overline{v}_O}{\beta\overline{v}_I}\Big) + K_i\Big[\frac{\int(V_r - \beta\overline{v}_O)dt}{\beta\overline{v}_I}\Big] + \frac{\overline{v}_O}{\overline{v}_I}. \tag{4.12}$$

The controller gains K_p and K_i are given by

$$\begin{cases} K_p = LC\frac{\alpha_3}{\alpha_2} \\ K_i = LC\frac{\alpha_4}{\alpha_2}. \end{cases} \tag{4.13}$$

The next step is to map the equivalent control equation onto a duty cycle, yielding

$$\hat{u}_e = K_p\Big(V_r - \beta\overline{v}_O\Big) + K_i\Big[\int(V_r - \beta\overline{v}_O)dt\Big] + \beta\overline{v}_O \tag{4.14}$$

and

$$V_T = \beta\overline{v}_{I(nom)}. \tag{4.15}$$

It should be emphasized that (4.14) and (4.15) can be scaled down by a constant γ between 0 and 1 to accommodate the practical limitation of the analogue components. The block diagram of the PI-SSMVC of PWM dc-dc buck converter is shown in Fig. 4.1.

4.2.3 Existence and Stability Conditions

The existence condition for steady-state operation is derived according to the local reachability condition [4], which gives

$$\begin{cases} K_p x_{1(max)} + K_i x_{3(max)} < \beta(V_{I(min)} - V_O) \\ -K_p x_{1(min)} - K_i x_{3(min)} < \beta V_O. \end{cases} \tag{4.16}$$

The minimum and maximum quantities are included to take the full-load operating conditions into account. This condition ensures that all the state trajectories remain within the vicinity of the sliding surface ψ.

In order to analyze the stability of the closed-loop dynamics of the buck converter around the desired equilibrium point, the linearized closed-loop model is required.

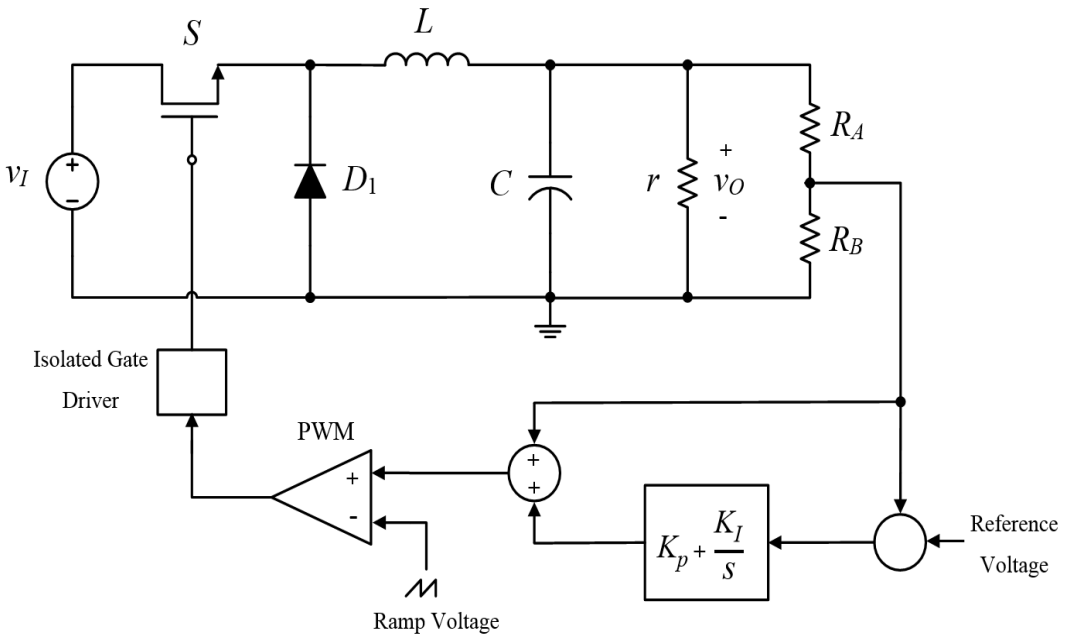


Figure 4.1: The block diagram of the SSMVC of PWM dc-dc buck converter.

The closed-loop nonlinear dynamics are given by

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}v_O + \frac{1}{L}v_I u_e \\ \frac{1}{C}i_L \overline{u}_e - \frac{1}{rC}v_O \end{bmatrix}, \tag{4.17}$$

where u_e is the equivalent control law given in (4.12). The linearized model is obtained by perturbing (4.17) around the equilibrium point $I_L = V_O/R$, which results in

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_O}{dt} \\ \frac{d[\int \tilde{v}_O dt]}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{K_p}{L} & -\frac{K_i}{L} \\ \frac{1}{C} & -\frac{1}{CR} & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix}, \tag{4.18}$$

where (4.18) can also be expressed as

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_O}{dt} \\ \frac{d[\int \tilde{v}_O dt]}{dt} \end{bmatrix} = \begin{bmatrix} 0 & j_{12} & j_{13} \\ j_{21} & j_{22} & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix}. \tag{4.19}$$

The linearized model has been obtained assuming that $v_I = V_I$, $r = R$, and $V_r - \beta V_O = 0$. It has also been assumed that $I_L \gg \tilde{i}_L$ and $V_O \gg \tilde{v}_O$.

The characteristic equation of the linearized model is

$$\begin{vmatrix} \lambda & -j_{12} & -j_{13} \\ -j_{21} & \lambda - j_{22} & 0 \\ 0 & -1 & \lambda \end{vmatrix} = \lambda^3 + P_1\lambda^2 + P_2\lambda + P_3 = 0, \tag{4.20}$$

where

$$\begin{cases} P_1 = -j_{22} \\ P_2 = -j_{12}j_{21} \\ P_3 = -j_{13}j_{21}. \end{cases} \tag{4.21}$$

Hence, using Routh-Hurwitz stability criterion, one obtains the stability conditions

$$\begin{cases} P_1 > 0 \\ P_3 > 0 \\ P_2 > \frac{P_3}{P_1}. \end{cases} \tag{4.22}$$

The gains K_p and K_i should be selected according to (4.16) and (4.22) to ensure a proper sliding-mode control operation.

4.3 Analogue Implementation of PI-SSMVC Scheme

In this section, the MATLAB/SIMULINK model of the PI-SSMVC of PWM dc-dc buck converter is presented in this section. The analogue realization and the design procedure of the control circuit are also introduced in detail.

4.3.1 Control Equation Parameters

The PWM dc-dc buck converter parameters have been given in Table I. The feedback network gain β is computed as $\beta = V_r/V_O$, whereas V_r and V_O are 5 V and 14 V, respectively. The controller gains K_p and K_i are set to 910 and $4{\times}10^6$, respectively. Furthermore, a scaling factor γ of 0.4 is selected, yielding the PI-SSMVC equations

$$\begin{cases} \hat{u}_e = 0.4\Big\{910(V_r - \beta\overline{v}_O) + 4 \times 10^6\Big[\int(V_r - \beta\overline{v}_O)dt\Big] + \beta\overline{v}_O\Big\} \\ V_T = 4\text{V}. \end{cases} \tag{4.23}$$

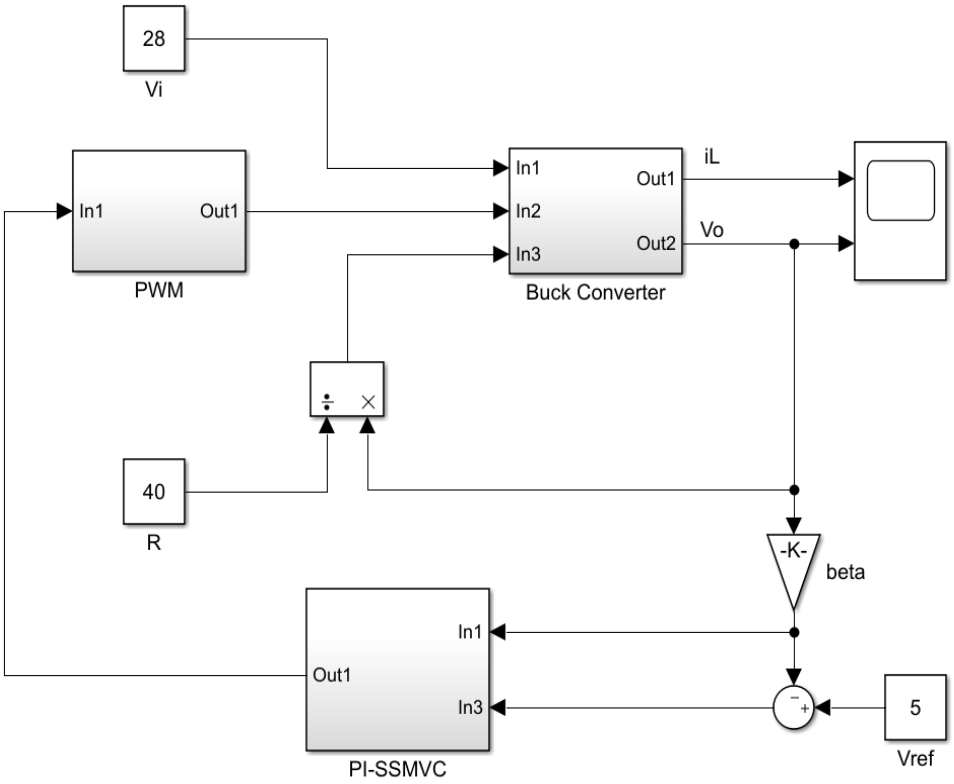


Figure 4.2: MATLAB/SIMULINK model of the PI-SSMVC controlled PWM dc-dc buck converter.

The MATLAB/SIMULINK model of the control system is depicted in Fig. 4.2. The power stage model is coded inside *Buck Converter* subsystem, whereas the pulse-width modulator and the equivalent control equation are coded inside the *PWM* and *PI-SSMVC* subsystems, respectively.

4.3.2 Control Circuit Structure

The analogue realization of the PI-SSMVC system is shown in Fig. 4.3. The control equation requires differential, summing, and inverting operational amplifiers. An op-amp is also required to build the PI controller. The output voltage, on the other hand, can be sensed via a voltage divider.

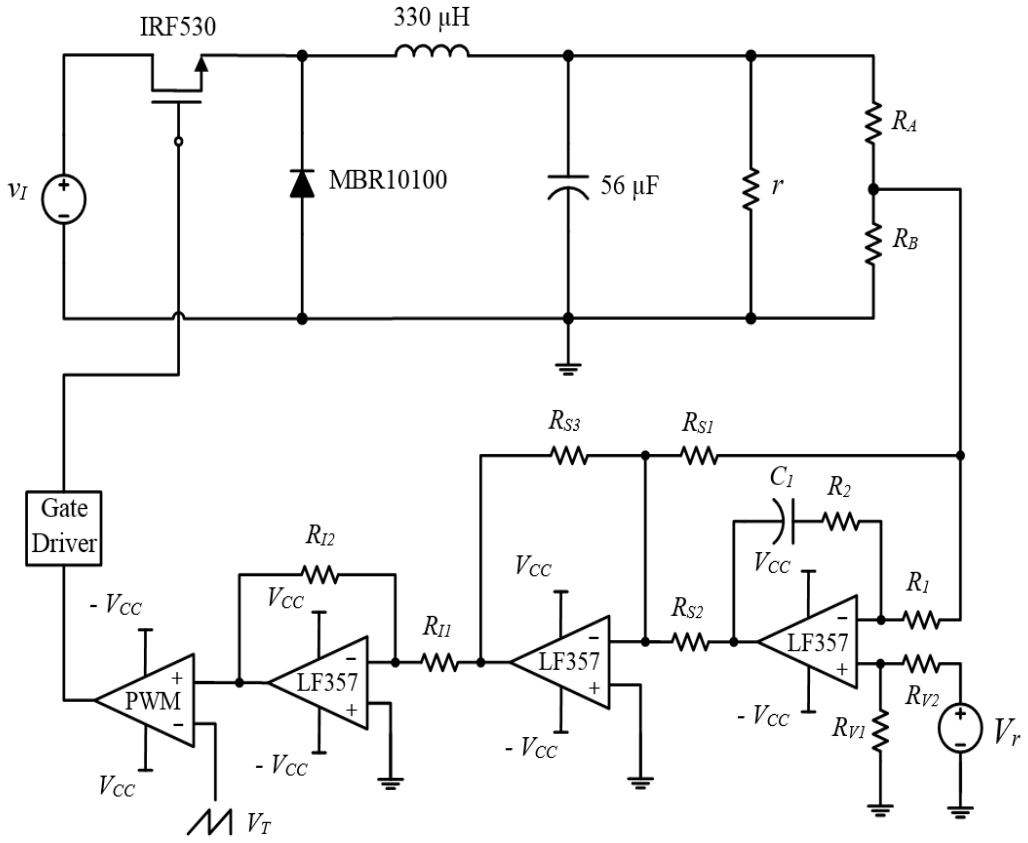


Figure 4.3: Analog realization of PI-SSMVC controlled PWM dc-dc buck converter for CCM.

4.3.3 Design Procedure

The design procedure of the control circuit parameters is summarized as follows:

1. Output voltage sensor: The voltage sensor gain β is set to 0.3571, where $\beta = V_r/V_O = R_B/(R_A + R_B)$. If R_A is assumed to be 9.1 kΩ/1 %/0.25 W, then R_B is 5.1 kΩ/1 %/0.25 W.

2. Summing and inverting amplifiers: The resistors R_{S1}, R_{S2}, and R_{S3} for the summing op-amp and R_{I1} and R_{I2} for the inverting op-amp can be set to 5.1 kΩ/5 %/0.25 W.

3. PWM generator: Since the nominal input voltage is 28 V, the peak ramp voltage

$V_T = \beta V_I = 10$ V, and a switching frequency of 100 kHz is selected.

4. Scaling factor: If a scaling factor γ is required to scale down V_T to 4 V, then R_{I1} and R_{I2} can be set to 2 kΩ/5 %/0.25 W and 5.1 kΩ/5 %/0.25 W, respectively.

5. Proportional gain K_p: According to [72], the proportional gain of the PI controller is defined as $K_p = R_2/R_1$. Thus, if K_p is 910 and R_1 is selected as 1 kΩ/5 %/0.25 W, then R_2 becomes 910 kΩ/5 %/0.25 W.

6. Integral gain K_i: In [72], the integral gain of the PI controller is defined as $K_i = 1/(R_1C_1)$. If the value of K_i is set to 4 $\times 10^6$, then C_1 can be selected as 220 pF/12 V .

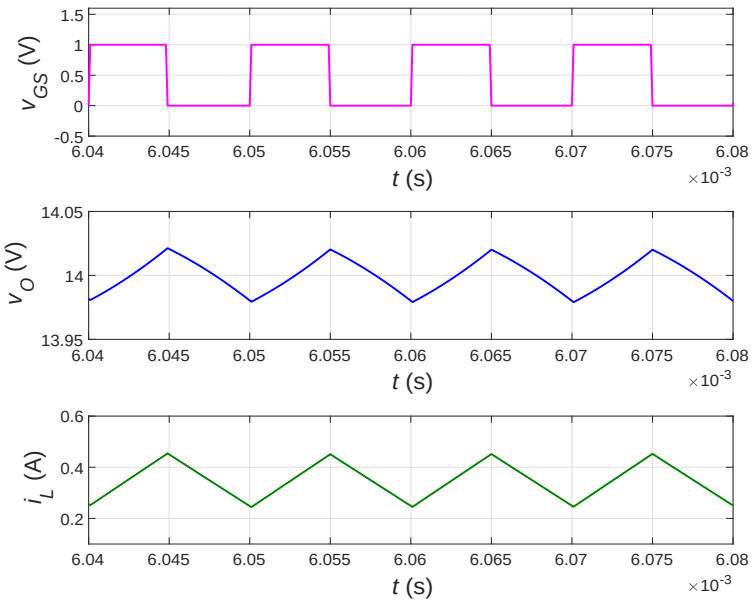
4.4 Simulation Results and Discussions

4.4.1 Steady-State Performance

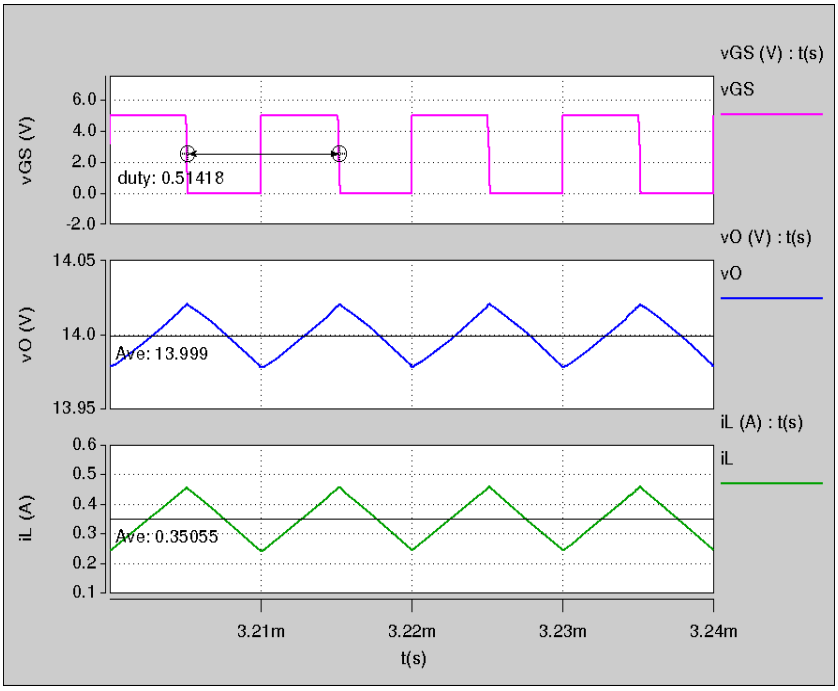
The PI-SSMV controlled PWM dc-dc buck converter has been simulated in SaberRD and compared with the corresponding MATLAB/SIMULINK model. The steady-state waveforms of the control system are depicted in Fig. 4.4. It can be noticed that the steady-state values of d_T, v_O, and i_L in MATLAB results are 0.51, 14.00 V, and 0.352 A, respectively. As for SaberRD results, the corresponding steady-state values are 0.51418, 13.999 V, and 0.35055 A, respectively. It can be seen that the simulated results of SaberRD and MATLAB are in good agreement, which validate the theoretical design approach.

4.4.2 Tracking Performance under Large Disturbances

The response of the PI-SSMVC of PWM dc-dc buck converter during abrupt and large line and load disturbances are shown in Figs. 4.5, 4.6, 4.7, and 4.8. The simulation is conducted using MATLAB/SIMULINK and SaberRD. The comparison between the two simulation platforms shows that the transient response in SaberRD is slightly



(a)



(b)

Figure 4.4: Steady-state waveforms of PI-SSMV controlled PWM dc-dc buck converter for CCM. a) MATLAB results b) SaberRD results.

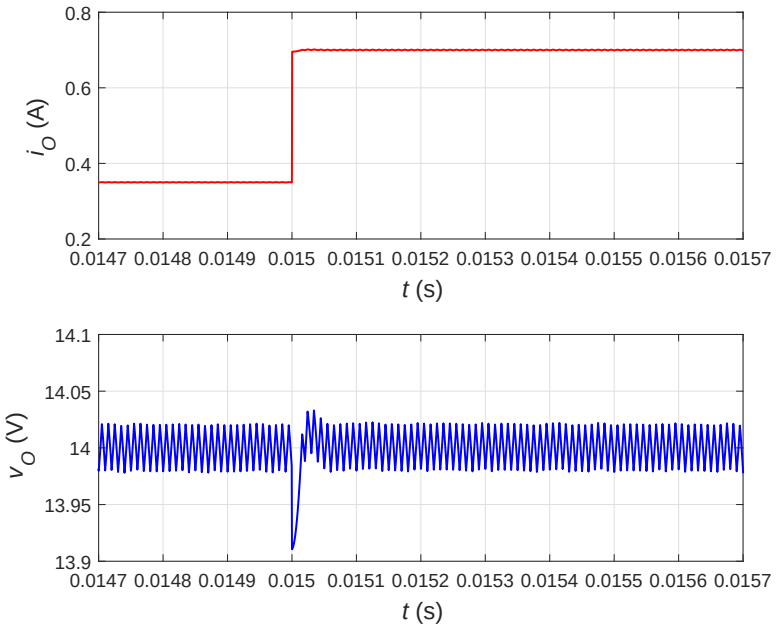
different from the transient response obtained using MATLAB. This is due to the non-ideality of the switching elements and analogue components in SaberRD, which are not included in MATLAB/SIMULINK model. However, MATLAB results provide a good prediction for the analogue control circuit behavior in SaberRD and the practical implementation.

The load current i_O and output voltage v_O waveforms during abrupt increase and decrease in load current are depicted in Figs. 4.5 and 4.6, respectively. Based on SaberRD results, it can be noticed that when i_O changes from 0.35 A to 0.7 A, the output voltage has an undershoot around 0.7 % and recovers the steady-state value after 80 µs. On the other hand, when i_O deceases from 0.35 A to 0.08 A, v_O exhibits an overshoot of 0.5 %. After 80 µs, the output voltage settles at the steady-state value.

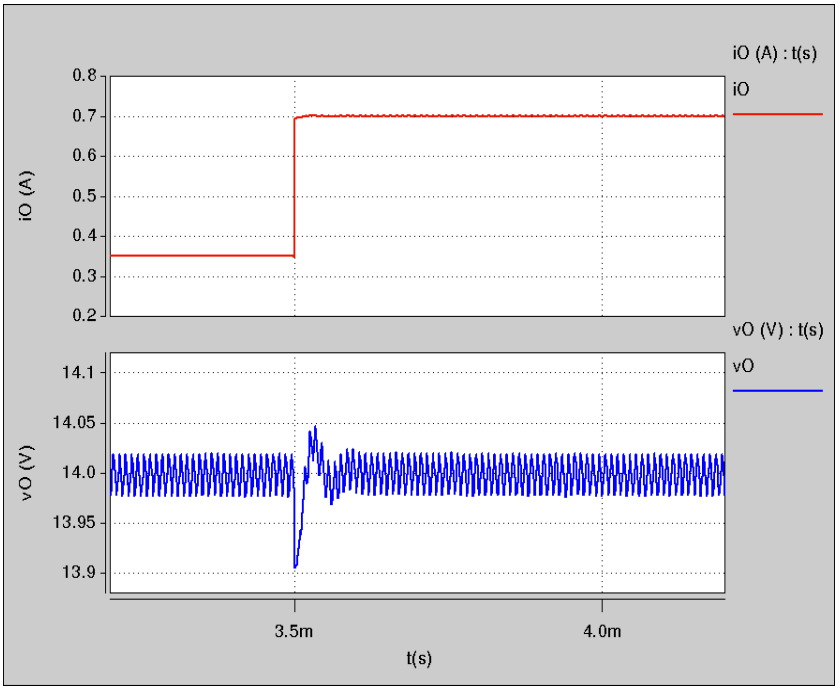
The input voltage v_I and output voltage v_O waveforms during abrupt increase and decrease in input voltage are shown in Figs. 4.7, and 4.8, respectively. As shown in Fig. 4.7, the output voltage response exhibits an overshoot and a settling time of 0.36 % and 400 µs, respectively, while Fig. 4.8 shows that the output voltage response has an undershoot and a settling time of 0.36 % and 400 µs, respectively. Hence, the disturbance rejection property of the control system works well, and the output voltage is maintained within the desired level in the presence of large line and load disturbances. Moreover, the output voltage response exhibits a consistent transient response and tracks the reference voltage.

4.4.3 Line and Load Regulation Performance

The line and load regulation performance of the proposed controller is investigated. The dc output voltage V_O versus dc load resistance R at different dc input voltage levels is depicted in Fig. 4.9. The range of dc quantities of load resistance and input voltage considered in this study is within 20 Ω to 190 Ω and 20 V to 42 V, respectively.

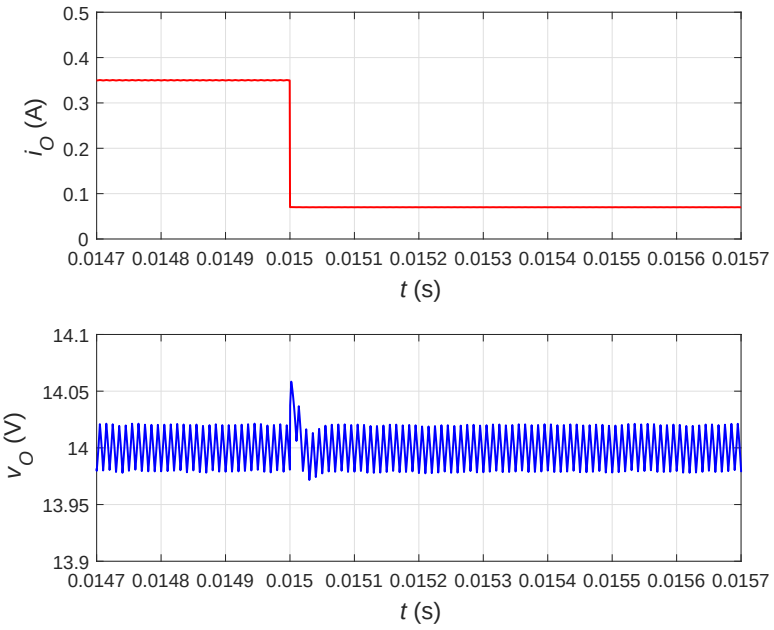


(a)

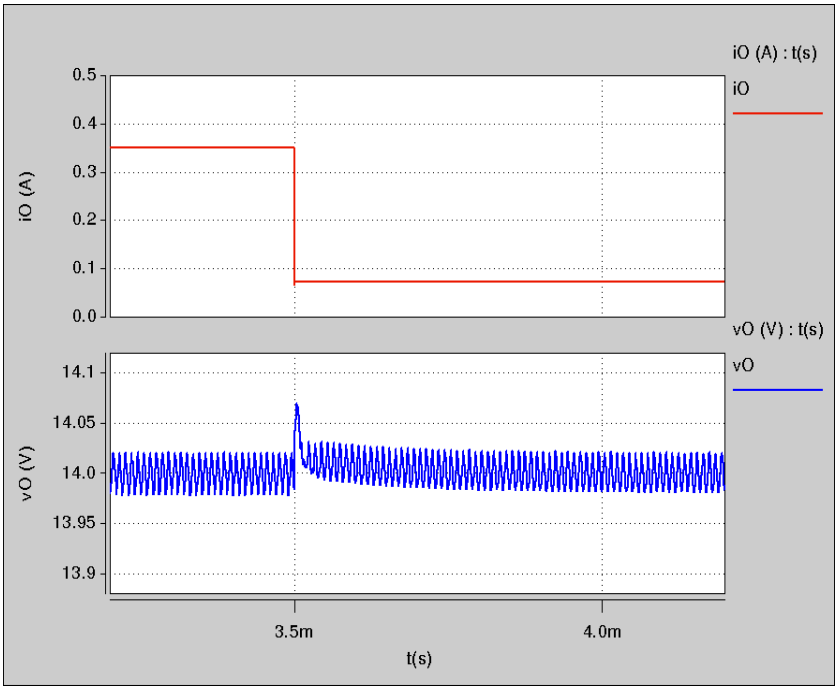


(b)

Figure 4.5: The PI-SSMVC system response during abrupt increase in load current. a) MATLAB results b) SaberRD results.

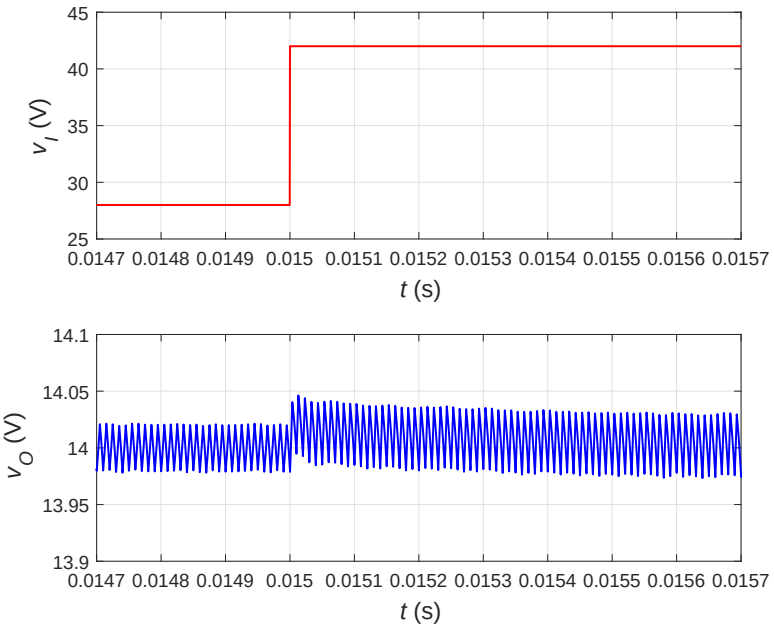


(a)



(b)

Figure 4.6: The PI-SSMVC system response during abrupt decrease in load current. a) MATLAB results b) SaberRD results.



(a)

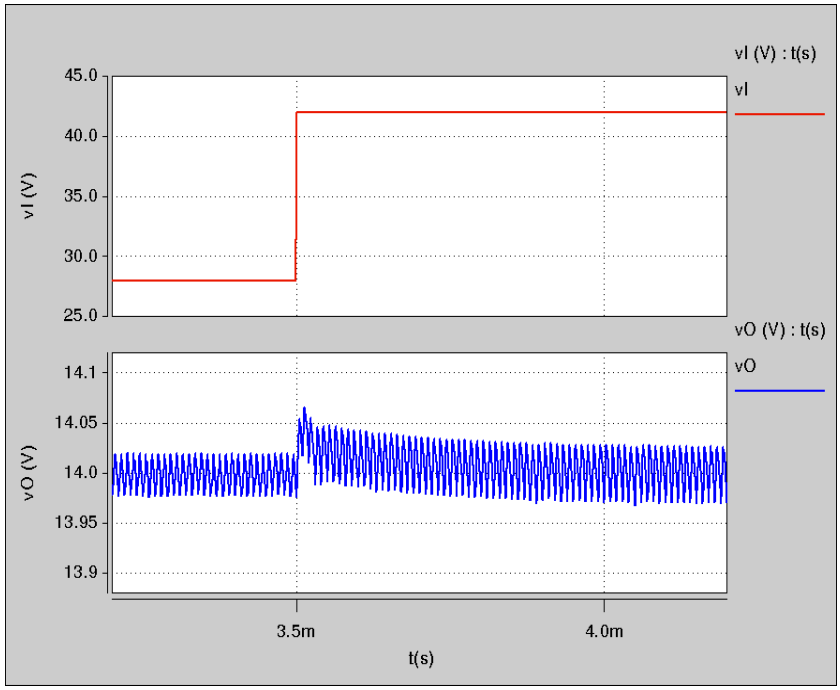


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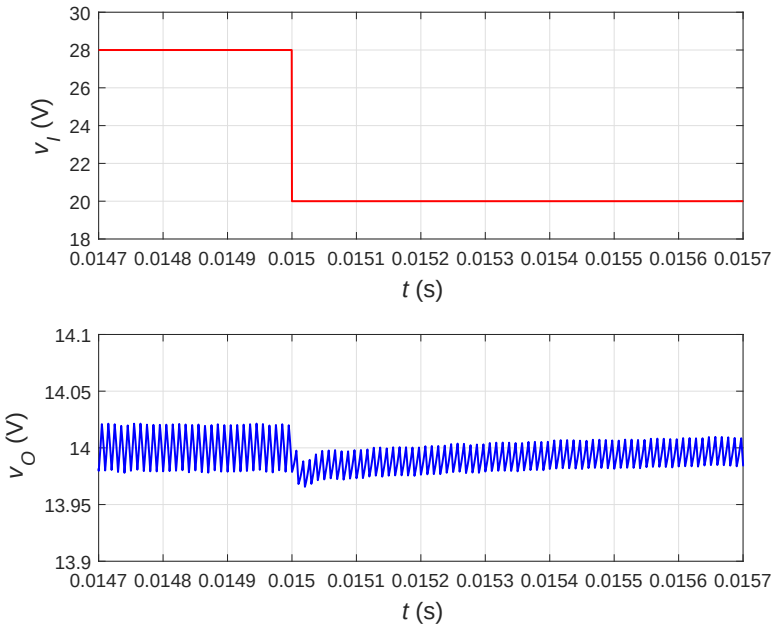
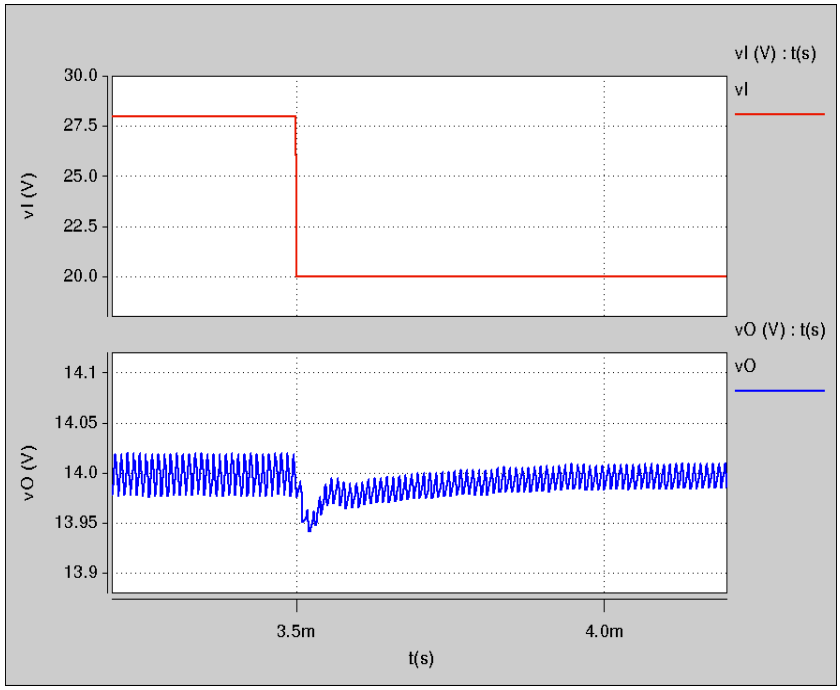
Figure 4.7: The PI-SSMVC system response during abrupt increase in input voltage. a) MATLAB results b) SaberRD results.



(a)



(b)

Figure 4.8: The PI-SSMVC system response during abrupt decease in input voltage. a) MATLAB results b) SaberRD results.

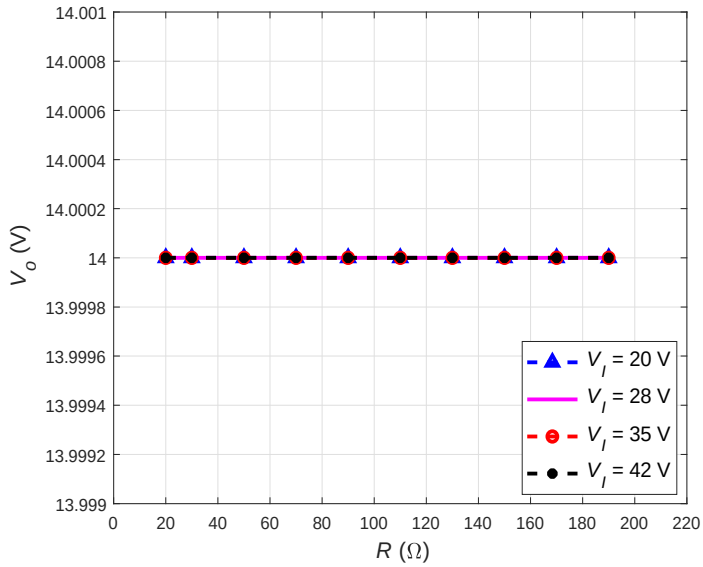


Figure 4.9: The output voltage V_O versus load resistance R at different input voltages V_I.

It can be noticed that the output voltage is maintained at the desired value 14 V during the entire range of operation. Therefore, the percentage line regulation $PLNR$ and percentage load regulation $PLOR$ of the PWM-based PI-SSMVC of dc-dc buck converter are 0 %/V and 0 %, respectively.

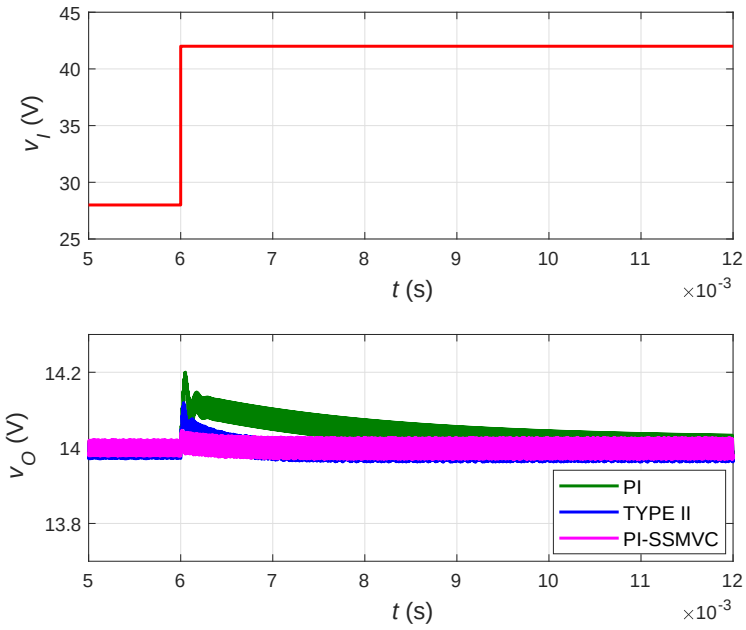
4.4.4 Comparison with Other PWM-Based Voltage-Mode Controllers

The PI-SSMVC system has been compared with the PI and Type II control systems under large disturbances. The transfer functins of the PI and Type II controllers are given in Chapter 3, which are designed to achieve the desired transient response and stability margins. The response of the proposed, PI, and Type II controllers during large line and load disturbances are shown in Figs. 4.10 and 4.11, respectively. It can be noticed that the transient response of the linear PWM-based voltage control system is degraded due to the large deviation from the nominal operating condition. In contrast, the proposed PI-SSMVC system shows the best transient response, while the worst response is exhibited by the PI controller. Table IX summarizes the percentage

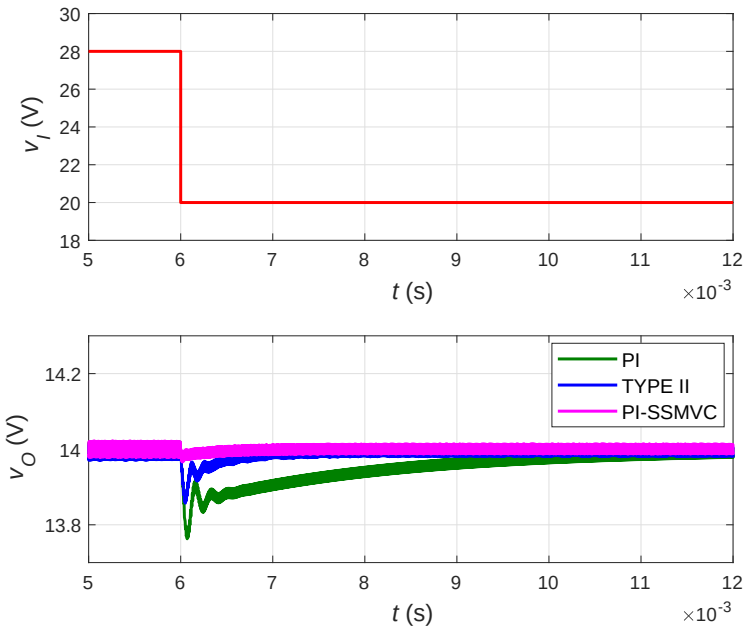
overshoot (PO), undershoot (PU), and settling time (t_s) of the three control systems response during the large disturbance conditions. Obviously, the PWM-based PI-SSMVC system exhibits a lower PO or PU and a shorter t_s as compared to the PI and Type II control systems.

Table IX: Transient Response Characteristics of PI-SSMVC, Type II, and PI Controllers during Large Disturbance

Disturbance	**PI-SSMVC**		**TYPE II**		**PI**	
	PO/PU (%)	t_s (ms)	PO/PU (%)	t_s (ms)	PO/PU (%)	t_s (ms)
$\Delta V_I = 28 \rightarrow 42$ (V)	0.36	0.40	0.70	0.50	1.30	5.00
$\Delta V_I = 28 \rightarrow 20$ (V)	0.36	0.40	0.90	1.50	1.60	6.00
$\Delta R = 60 \rightarrow 15$ (Ω)	1.30	0.08	1.40	0.20	1.60	0.20
$\Delta R = 15 \rightarrow 200$ (Ω)	1.30	0.08	1.60	0.15	2.00	0.20

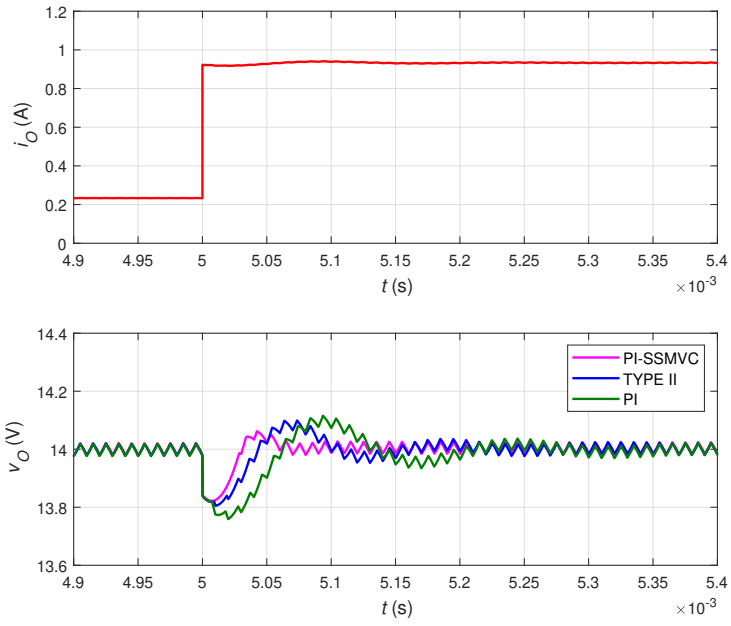


(a)

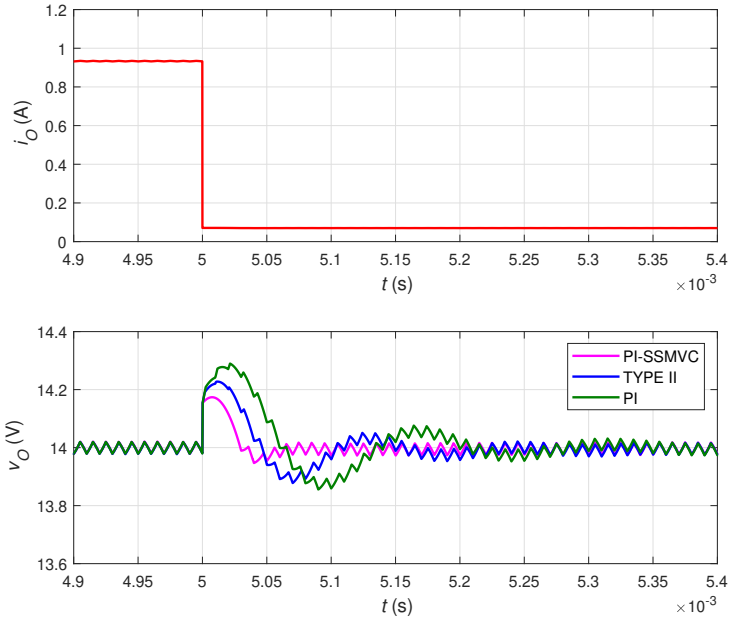


(b)

Figure 4.10: The output voltage response v_O of the proposed, PI, and Type II control systems under large (a) increase and (b) decrease in input voltage v_I.



(a)



(b)

Figure 4.11: The output voltage response v_O of the proposed, PI, and Type II control systems under large (a) increase and (b) decrease in load current i_O.

5 Closed-Loop PI-SSMCC of PWM DC-DC Boost Converter

5.1 Introduction

In this chapter, a proportional-integral simplified sliding-mode current control (PI-SSMCC) of PWM dc-dc boost converter for CCM is designed. The behavioral model is used to derive the averaged control-oriented model of the boost converter. A nonlinear sliding surface is constructed using four control state variables. The equivalent control law along with the existence and stability conditions are derived. The designed procedure and analogue realization of the control circuit are presented. The proposed nonlinear controller is simulated using MATLAB/SIMULINK and SaberRD. The line and load regulation performance is also studied. The tracking performance is investigated using MATLAB/SIMULINK and SaberRD. Finally, the proposed current-mode controller is compared with the linear Type III controller under large disturbances.

5.2 Sliding-Mode Current Control

The sliding-mode voltage control systems of dc-dc buck converter have been discussed in Chapters 3 and 4. According to [4], the buck converter is considered as a minimum phase system, i.e the control-to-output transfer function does not contain a right-half plane zero (RHPZ). Thus, the voltage-mode control of the buck converter is preferred due to the simplicity in the design and implementation. However, in the case of the non-minimum phase systems such as the boost and buck-boost converters, the voltage-mode control results in a slow response due to the presence of the RHPZ that limits the system bandwidth. Therefore, the current-mode control is recommended for these power converters in order to obtain a fast transient response. In the sliding-mode current control (SMCC) design, an instantaneous reference current i_R is generated,

which can be defined as

$$i_R = K(V_r - \beta v_O), \tag{5.1}$$

where K is a constant gain. Next, the reference current i_R is compared with the sensed inductor current i_L. If the difference between i_L and i_R is approximately zero at steady-state, then it can be concluded that the sensed output voltage βv_O tracks the desired reference voltage V_r.

5.2.1 PI-Simplified Sliding-Mode Current Control

As discussed in the PWM-based SSMVC design, the steady-state error is generated during the large disturbances due to the implementation of the pulse-width modulator. In contrast, the double-integral or PI-SSMVC system eliminates the dc error. Similarly, in order to assure a precise tracking by the PWM-based SSMCC of PWM dc-dc boost converter, the PI-SSMCC design approach is applied to the dc-dc boost converter.

5.2.2 Control-Oriented Model of DC-DC Boost Converter

The ideal switched model of the dc-dc boost converter in CCM is derived in Chapter 2 as

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} \frac{1}{L} v_I - \frac{1}{L} v_O \overline{u} \\ \frac{1}{C} i_L \overline{u} - \frac{1}{rC} v_O \end{bmatrix}, \tag{5.2}$$

where $\overline{u}$ is the complement of the switching control input u.

The control state variables x_1, x_2, x_3, and x_4 of the PI-SSMCC system are defined as an inductor current error, an integral of output voltage error, an integral of inductor current error, and a double integral of output voltage error, respectively. Hence,

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} i_R - i_L \\ \int (V_r - \beta v_O) dt \\ \int x_1 dt \\ \int x_2 dt \end{bmatrix}. \tag{5.3}$$

The fourth state in (5.3) contains a double integral term, which is added to improve the tracking performance. It should be noticed that the choice of the control state variables shapes the SMC scheme and affects the controller performance.

Now, if the switched model is reflected by (5.3), then the time derivative of the control state variables gives

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} -\frac{\beta K}{C} i_C - \frac{v_I - v_O \overline{u}}{L} \\ V_r - \beta v_O \\ K(V_r - \beta v_O) - i_L \\ \int (V_r - \beta v_O) dt \end{bmatrix}. \tag{5.4}$$

Thus, the averaged control-oriented model is obtained via averaging the dynamics (5.4), yielding

$$\begin{bmatrix} \dot{\overline{x}}_1 \\ \dot{\overline{x}}_2 \\ \dot{\overline{x}}_3 \\ \dot{\overline{x}}_4 \end{bmatrix} = \begin{bmatrix} -\frac{\beta K}{C} \overline{i}_C - \frac{\overline{v}_I - \overline{v}_O \overline{u}_e}{L} \\ V_r - \beta \overline{v}_O \\ K(V_r - \beta \overline{v}_O) - \overline{i}_L \\ \int (V_r - \beta \overline{v}_O) dt \end{bmatrix}, \tag{5.5}$$

where $\overline{u}_e$ is the averaged quantity of the switching control input complement $\overline{u}$.

5.2.3 Equivalent Control Law

To satisfy the hitting condition, a proper switching control law is selected

$$u = \frac{1}{2}\Big[1 + sign(\psi)\Big], \tag{5.6}$$

where the sliding surface ψ is given by

$$\psi = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4. \tag{5.7}$$

As discussed previously, the direct implementation of the switching control law in (5.6) with the pulse-width modulator is not possible. In contrast, an averaged control

law u_e should be derived based on the invariance conditions and mapped onto a duty cycle [7]. Thus, equating the time derivative of (5.7) to zero yields

$$\dot{\psi} = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 + \alpha_4 \dot{x}_4 = 0. \tag{5.8}$$

Next, the averaged control-oriented model in (5.5) is substituted into (5.8), yielding

$$\alpha_1\Big(-\frac{\beta K}{C}\bar{i}_C - \frac{\overline{v}_I - \overline{v}_O\overline{u}_e}{L}\Big) + \alpha_2\Big(V_r - \beta\overline{v}_O\Big) + \alpha_3\Big[K(V_r - \beta\overline{v}_O) - \bar{i}_L\Big] + \alpha_4\Big[\int (V_r - \beta\overline{v}_O)dt\Big] = 0. \tag{5.9}$$

Now, ignoring $\bar{i}_C$ from (5.9) gives

$$\alpha_1\Big(-\frac{\overline{v}_I - \overline{v}_O\overline{u}_e}{L}\Big) + \alpha_2\Big(V_r - \beta\overline{v}_O\Big) + \alpha_3\Big[K(V_r - \beta\overline{v}_O) - \bar{i}_L\Big] + \alpha_4\Big[\int (V_r - \beta\overline{v}_O)dt\Big] = 0, \tag{5.10}$$

and the equivalent control equation becomes

$$u_e = 1 - \frac{\overline{v}_I}{\overline{v}_O} + L\frac{\alpha_2}{\alpha_1}\Big(\frac{V_r - \beta\overline{v}_O}{\overline{v}_O}\Big) + L\frac{\alpha_3}{\alpha_1}\Big[\frac{K(V_r - \beta\overline{v}_O) - \bar{i}_L}{\overline{v}_O}\Big] + L\frac{\alpha_4}{\alpha_1}\Big[\frac{\int (V_r - \beta\overline{v}_O)dt}{\overline{v}_O}\Big], \tag{5.11}$$

which can also be expressed as

$$u_e = 1 - \frac{\overline{v}_I}{\overline{v}_O} + K_1\Big(\frac{V_r - \beta\overline{v}_O}{\overline{v}_O}\Big) - K_2\Big(\frac{\bar{i}_L}{\overline{v}_O}\Big) + K_i\Big[\frac{\int (V_r - \beta\overline{v}_O)dt}{\overline{v}_O}\Big] + K_p\Big(\frac{V_r - \beta\overline{v}_O}{\overline{v}_O}\Big). \tag{5.12}$$

The controller gains K_1, K_2, K_i, and K_p are defined by

$$\begin{cases} K_1 = L\frac{\alpha_2}{\alpha_1} \\ K_2 = L\frac{\alpha_3}{\alpha_1} \\ K_i = L\frac{\alpha_4}{\alpha_1} \\ K_p = KL\frac{\alpha_3}{\alpha_1}. \end{cases} \tag{5.13}$$

Finally, the equivalent control equation u_e is mapped onto a duty cycle d_T, which results in

$$\hat{u}_e = \gamma(\overline{v}_O - \overline{v}_I) + \gamma K_1(V_r - \beta\overline{v}_O) - \gamma K_2\bar{i}_L + \gamma K_p(V_r - \beta\overline{v}_O) + \gamma K_i\int (V_r - \beta\overline{v}_O)dt \tag{5.14}$$

and

$$V_T = \gamma \overline{v}_{O(nom)}, \tag{5.15}$$

where $\overline{v}_{O(nom)}$ is the nominal output voltage and γ is a scaling factor ($0 < \gamma < 1$) to scale down the control equation parameters and fit the practical implementation. The block diagram of the PI-SSMCC of PWM dc-dc boost converter is shown in Fig. 5.1.

5.2.4 Remarks

1) It can be observed that the derivation the equivalent control equation gives the term $(\overline{v}_O - \overline{v}_I)$, which is not available in the linear current-mode control scheme. This term contributes with the other terms of the proposed control equation to improve the nonlinear control system performance.

2) As shown in (5.14), the gains K_p and K_i construct a PI controller at the outer voltage loop, which eliminates the stead-state error at the output voltage during the large disturbance condition.

5.2.5 Existence and Stability Conditions

Based on the local reachability condition [4], the existence condition for steady-state operation is derived, yielding

$$\begin{cases} K_1(V_r - \beta V_O) + K_2 x_{1(max)} + K_i x_{2(max)} < V_{I(min)} \\ -K_1(V_r - \beta V_O) - K_2 x_{1(min)} - K_i x_{2(min)} < V_O - V_{I(max)}. \end{cases} \tag{5.16}$$

Note that the minimum and maximum quantities are included to take the full-load operating conditions into account. The existence condition ensures that all the state trajectories remain within the vicinity of the sliding surface ψ.

The next step is to analyze the stability of the closed-loop dynamics of the boost converter around the desired equilibrium point. The closed-loop boost converter

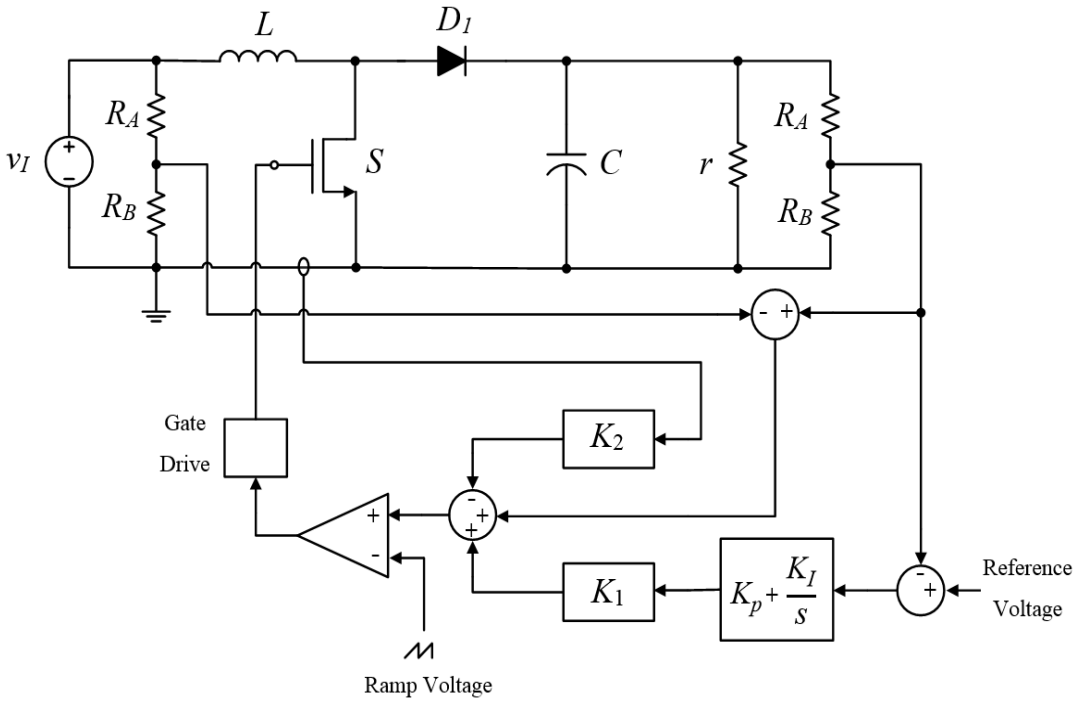


Figure 5.1: The block diagram of the SSMCC of PWM dc-dc boost converter.

dynamics are given by

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} \frac{1}{L}v_I - \frac{1}{L}v_O\overline{u}_e \\ \frac{1}{C}i_L\overline{u}_e - \frac{1}{rC}v_O \end{bmatrix}, \tag{5.17}$$

where $\overline{u}_e$ is the complement of the equivalent control law given in (5.12). Hence, linearizing (5.17) around the equilibrium point given in (2.27) results in

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_O}{dt} \\ \frac{d[\int \tilde{v}_O dt]}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{K_2}{L} & -\frac{(K_1+K_p)\beta}{L} & -\frac{K_i\beta}{L} \\ \frac{V_I}{V_O C} + \frac{2K_2V_O}{V_I CR} & \frac{K_1\beta V_O}{V_I CR} + \frac{K_p\beta V_O}{V_I CR} - \frac{K_2{V_O}^2}{{V_I}^2CR^2} - \frac{2}{CR} & \frac{K_i\beta V_O}{V_I CR} \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix}, \tag{5.18}$$

which can also be written as

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_O}{dt} \\ \frac{d[\int \tilde{v}_O dt]}{dt} \end{bmatrix} = \begin{bmatrix} j_{11} & j_{12} & j_{13} \\ j_{21} & j_{22} & j_{23} \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix}. \tag{5.19}$$

The linearized model has been obtained assuming that $v_I = V_I$, $r = R$, $V_r - \beta V_O = 0$,

and $I_r - I_L = 0$. It has also been assumed that $I_L \gg \tilde{i}_L$ and $V_O \gg \tilde{v}_O$.

The characteristic equation of the linearized model in (5.19) is

$$\begin{vmatrix} \lambda - j_{11} & -j_{12} & -j_{13} \\ -j_{21} & \lambda - j_{22} & -j_{23} \\ 0 & -1 & \lambda \end{vmatrix} = \lambda^3 + P_1\lambda^2 + P_2\lambda + P_3 = 0, \tag{5.20}$$

where

$$\begin{cases} P_1 = -j_{11} - j_{22} \\ P_2 = j_{11}j_{22} - j_{12}j_{21} - j_{23} \\ P_3 = j_{11}j_{23} - j_{13}j_{21}. \end{cases} \tag{5.21}$$

Hence, the stability conditions of the characteristic equation in (5.20) can be determined using Routh-Hurwitz criterion, which yields

$$\begin{cases} P_1 > 0 \\ P_3 > 0 \\ P_2 > \frac{P_3}{P_1}. \end{cases} \tag{5.22}$$

The controller gains K_1, K_2, K_p, and K_i must satisfy the existence and stability conditions given in (5.16) and (5.22) to ensure a proper sliding-mode control operation.

5.3 Analogue Implementation of PI-SSMCC Scheme

The MATLAB/SIMULINK model of the PI-SSMCC of PWM dc-dc boost converter for CCM is introduced in this section. Furthermore, the analogue realization and the design procedure of the control circuit are presented.

5.3.1 Control Equation Parameters

The PWM dc-dc boost converter parameters have been given in Table I. The feedback network gain β is defined as $\beta = V_r/V_O$. If V_r and V_O are 2.5 V and 20 V, respectively,

then β is 0.125. Based on the existence and stability conditions, the controller gains K_1, K_2, K_p, and K_i are set to 6.744, 12, 204, and 588000, respectively. Furthermore, a scaling factor γ of 0.125 is selected to scale down the peak ramp voltage and other control parameters within the practical range, which yields K_1, K_2, K_p, K_i, and V_T to 0.843, 1.5, 25.5, 73500, and 2.5 V, respectively. Hence, the PI-SSMCC equations become

$$\begin{cases} u_e = 0.125(\overline{v}_O - \overline{v}_I) + 0.843(V_r - \beta\overline{v}_O) - 1.5\bar{i}_L + 25.5(V_r - \beta\overline{v}_O) + 73500\int(V_r - \beta\overline{v}_O)dt \\ V_T = 2.5\text{V}. \end{cases} \tag{5.23}$$

The MATLAB/SIMULINK model of the control system is depicted in Fig. 5.2. The s-function template is coded inside the *Boost Converter* subsystem, which contains the nonlinear dynamics of the dc-dc boost converter for CCM. The pulse-width modulator and the equivalent control equation are coded inside the *PWM* and *SMC* subsystems, respectively.

5.3.2 Control Circuit Structure

The mathematical expression of the PI-SSMCC law should be converted into an analogue circuit, simulated on SaberRD, and compared with the corresponding design in MATLAB to validate the design approach. The control equation in (5.23) requires differential, summing, and inverting operational amplifiers. An op-amp is also required to build the PI controller. The input and output voltages can be sensed via a voltage divider, while the inductor current can be sensed via sensing the MOSFET current using a sensing resistor. The analogue realization of the closed-loop control system is shown in Fig. 5.3.

5.3.3 Design Procedure

The design procedure of the control circuit parameters is summarized as follows:

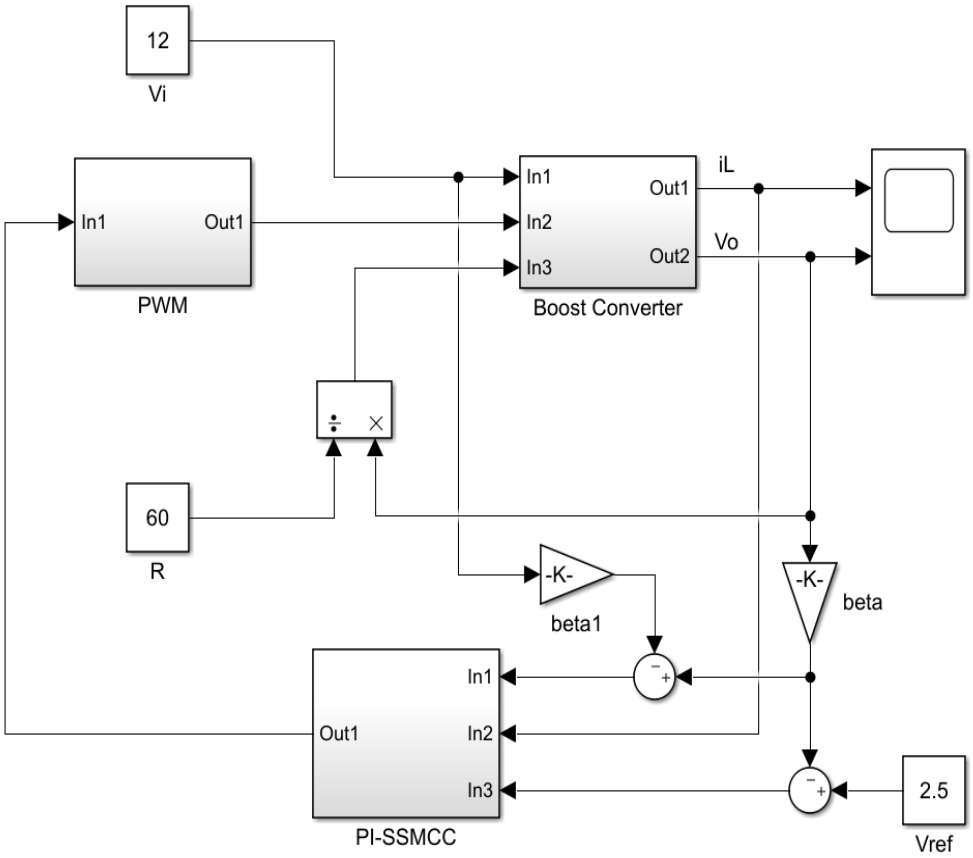


Figure 5.2: MATLAB/SIMULINK model of the PI-SSMCC controlled PWM dc-dc boost converter.

1. Input and output voltage sensor: The voltage sensor gain β is set to 0.125, where $\beta = V_r/V_O = R_B/(R_A + R_B)$. If R_A is assumed to be 4.3 kΩ/1 %/0.25 W, then R_B is 620 Ω/1 %/0.25 W.

2. Inductor current sensor: The inductor current is sensed using a sensing resistor R_s with a low resistance value, which is connected in series with the MOSFET with respect to the ground.

3. Differential amplifier: A differential op-amp with a unity gain is required to subtract the input voltage from the output voltage. Hence, the resistors R_{F1} and R_{F2} can be chosen as 39 kΩ/5 %/0.25 W.

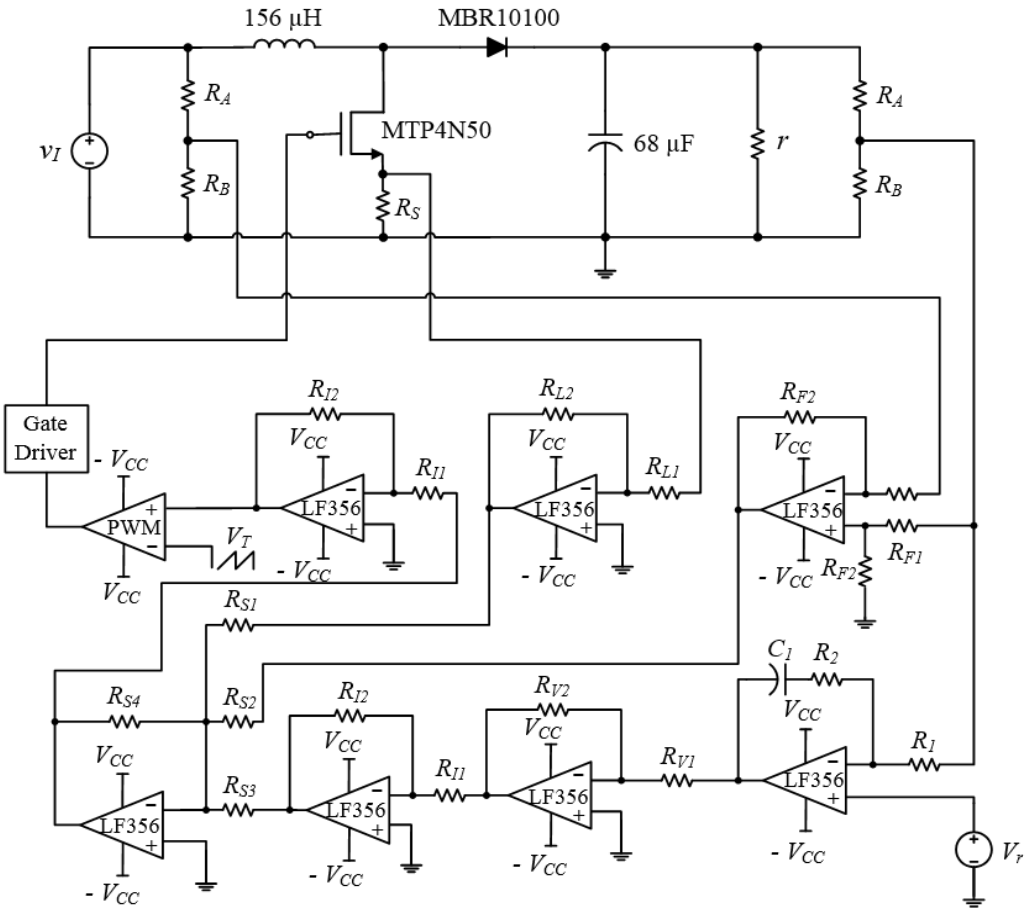


Figure 5.3: Analog realization of PI-SSMCC controlled PWM dc-dc boost converter for CCM.

4. Summing and inverting amplifiers: The resistors R_{S1}, R_{S2}, R_{S3}, and R_{S4} for the summing op-amp and R_{I1} and R_{I2} for the inverting op-amps can be set to 5.1 kΩ/5 %/0.25 W.

5. PWM generator: Since the nominal output voltage is 20 V, the peak ramp voltage V_T without a scaling gain is 20 V. The switching frequency, on the other hand, is set to 100 kHz.

6. Scaling factor: A scaling factor γ is required to scale V_T down for the practical range of the pulse-width modulator. Hence, if γ is 0.125, then V_T becomes 2.5 V.

7. Output voltage error gain K_1: The value of γK_1 is chosen as 0.843 in the previous section, where $\gamma K_1 = R_{V2}/R_{V1}$. If R_{V1} is assumed to be 5.1 kΩ/5 %/0.25 W, then R_{V2} is 4.3 kΩ/5 %/0.25 W.

8. Inductor current gain K_2: The value of γK_2 is chosen as 1.5 in the previous section, where $\gamma K_2 = R_{L2}/R_{L1}$. If R_{L1} is assumed to be 10 kΩ/5 %/0.25 W, then R_{L2} is 15 kΩ/5 %/0.25 W.

9. Proportional gain K_p: According to [72], the proportional gain of the PI controller is defined as $\gamma K_p = R_2/R_1$. Thus, if γK_p is 25.5 and R_1 is selected as 20 kΩ/5 %/0.25 W, then R_2 becomes 510 kΩ/5 %/0.25 W.

10. Integral gain K_i: In [72], the integral gain of the PI controller is defined as $\gamma K_i = 1/(R_1 C_1)$. If the value of γK_i is set to 73500, then C_1 can be selected as 680 pF/12 V .

It should be emphasized that the choice of the controller gains is not unique. The designer can choose various values within the practical range as long as they meet both the existence and stability conditions to assure a proper SMC operation. It should also be noticed that the feedback resistors values must be selected such that $R_A + R_B >> R_{(max)}$ in order to minimize the loading effect of the control circuit.

5.4 Simulation Results and Discussions

5.4.1 Steady-State Performance

The PI-SSMCC circuit given in Fig. 5.3 has been constructed using SaberRD simulator. The control circuit is developed using LF356 op-amps along with their corresponding components. In addition, the power stage is created using an MTP4N50 power MOSFET, a MBR10100 Schottky diode, a 156 µH/0.19 Ω inductor, a 68 µF/0.10 Ω capacitor, and a 60 Ω/20 W load resistor. The supply voltage, ramp voltage, and switching frequency are 12 V, 2.5 V, and 100 kHz, respectively.

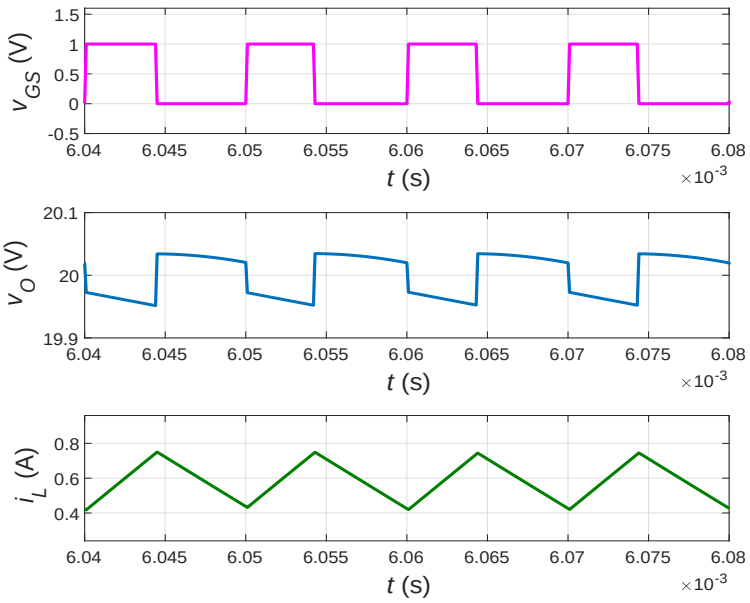
The steady-state waveforms of the analogue control scheme in SaberRD have been compared with the corresponding waveforms of MATLAB/SIMULINK model as shown in Fig. 5.4. It can be noticed form Fig. 5.4(a) that the steady-state values of d_T, v_O, and i_L using MATLAB are 0.44, 19.99 V, and 0.600 A, respectively. As for the results of SaberRD, which are given in Fig. 5.4(b), the steady-state values of d_T, v_O, and i_L are 0.454, 20 V, and 0.631 A, respectively. It can be noticed that the theoretical and simulated results are in good agreement, which verify the proposed design approach. Moreover, the control system provides an excellent tracking performance, while the switching frequency is maintained constant during steady-state operation.

5.4.2 Tracking Performance under Large Disturbances

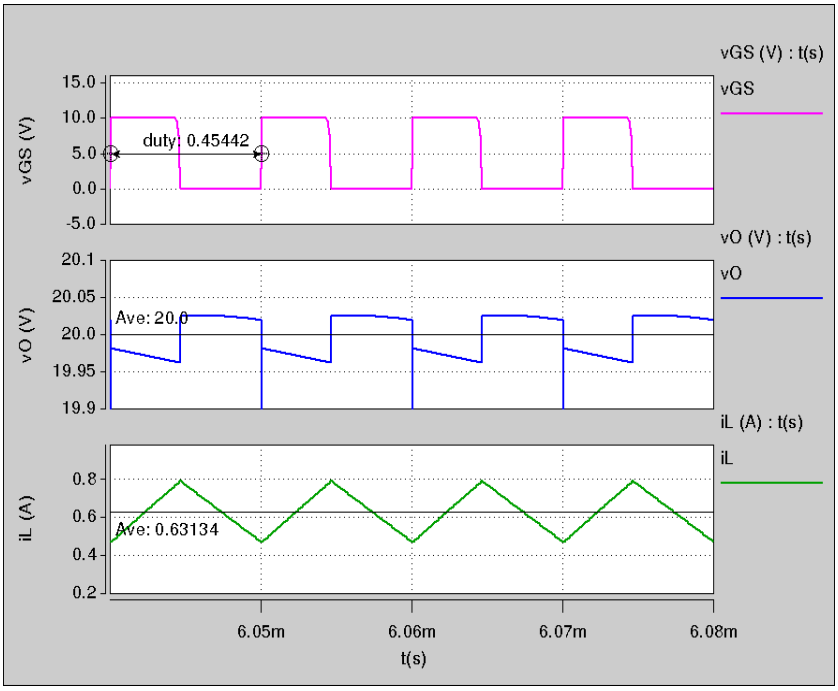
The response of the PI-SSMCC of PWM dc-dc boost converter during large line and load disturbances are shown in Figs. 5.5 - 5.8. The comparison between MATLAB/SIMULINK and SaberRD shows that the results are in good agreement. However, the slight difference in the transient response characteristics of the results obtained from the two platforms are due to the non-ideality of the switching elements and analogue components in SaberRD, which are not included in MATLAB/SIMULINK model.

The load current i_O and output voltage v_O waveforms during abrupt increase and decrease in load current are depicted in Figs. 5.5 and 5.6, respectively. In Fig. 5.5, it can be noticed that when i_O changes from 0.333 A to 1 A, the output voltage exhibits an undershoot around 3 % and then reaches the desired steady-state value after 1 ms. On the other hand, Fig. 5.6 shows that when i_O deceases from 0.333 A to 0.1 A, the output voltage exhibits an overshoot of 0.9 % and a settling time of 1 ms.

The input voltage v_I and output voltage v_O waveforms during abrupt increase and decrease in input voltage are shown in Figs. 5.7 and 5.8, respectively. As shown in Fig. 5.7, when the input voltage increases abruptly from 12 V to 18 V, the output



(a)



(b)

Figure 5.4: Steady-state waveforms of PI-SSMCC of PWM dc-dc boost converter for CCM. a) MATLAB results b) SaberRD results.

voltage response has an overshoot of 0.5 % and a settling time of 800 µs. In Fig. 5.8, however, when v_I decreases from 12 V to 7 V, the percentage undershoot and settling time are about 2 % and 3 ms, respectively.

The simulation results from MATLAB and SaberRD show the excellent tracking performance and large disturbance rejection capability of the PI-SSMCC system. The transient response of the closed-loop control system has significantly been improved as compared to the open-loop boost converter response in Chapter 2.

5.4.3 Line and Load Regulation Performance

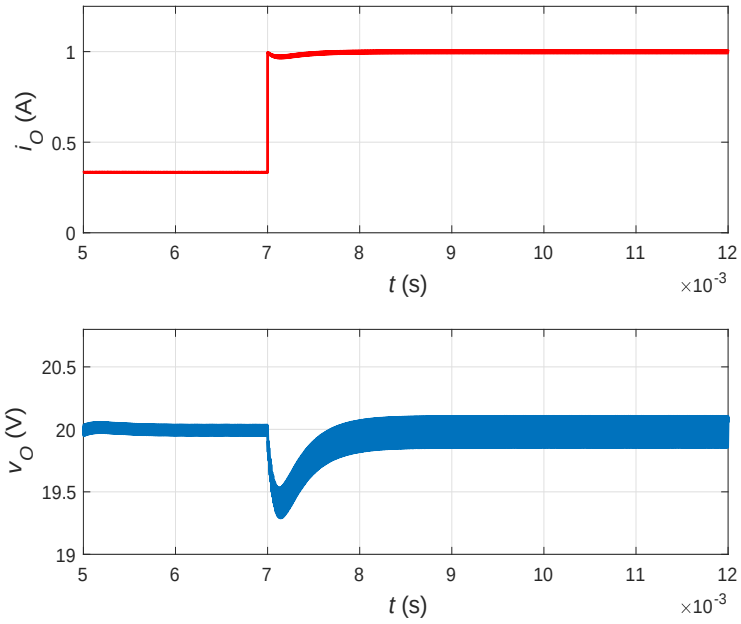
The regulation performance of the PI-SSMCC of PWM dc-dc boost converter for CCM have been investigated. Fig. 5.9 shows the dc output voltage V_O versus the dc load resistance R at different dc input voltage V_I levels. In this study, the range of R and V_I is within 26 Ω to 200 Ω and 10 V to 16 V, respectively. It has been noticed that the control system maintains a constant dc output voltage V_O within the entire range of operation. In other words, the steady-state output voltage is regulated at 20 V despite the load and line variations. Based on Fig. 5.9, it can be concluded that the percentage line regulation $PLNR$ and percentage load regulation $PLOR$ of the PI-SSMCC system for the entire operating range are 0 %/V and 0 %, respectively.

5.4.4 Comparison with PWM-Based Controller

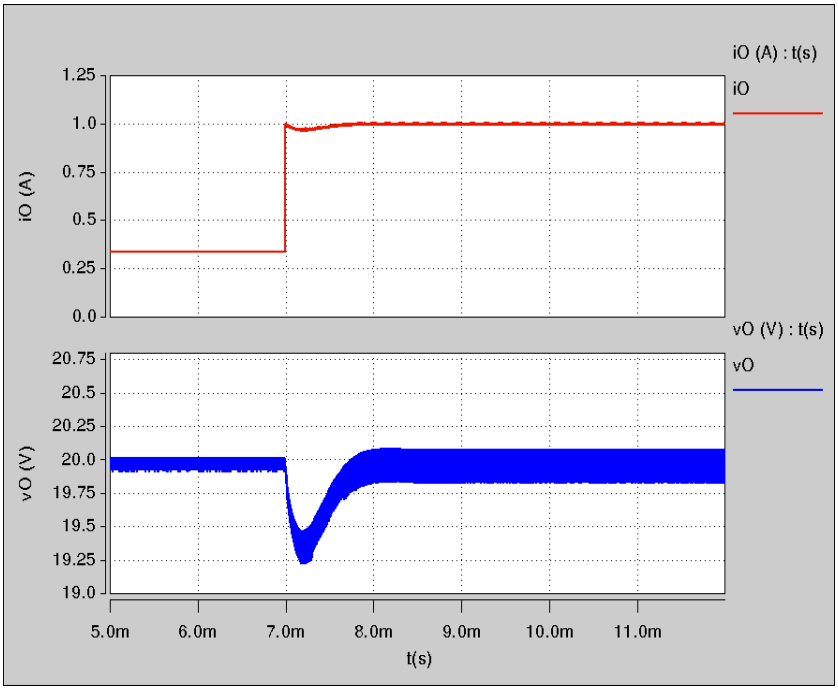
The tracking performance of the proposed controller is compared with a Type III controller during large disturbances. An integral double-lead controller is designed to achieve a phase margin of 60°, where the controller transfer function is [72]

$$T_c = 2.7095 \times 10^6 \frac{(s + 2078)^2}{s(s + 7.599 \times 10^4)^2}. \tag{5.24}$$

The output voltage response of the two control systems during large load disturbance is shown in Fig. 5.10. Obviously, both of them regulate v_O to the desired level. However, the linear Type III control system exhibits larger peak overshoot/undershoot

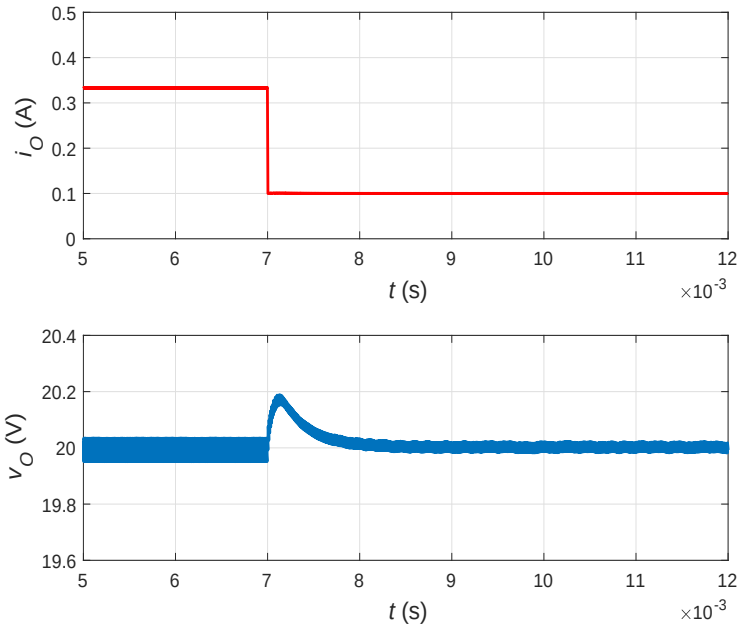


(a)

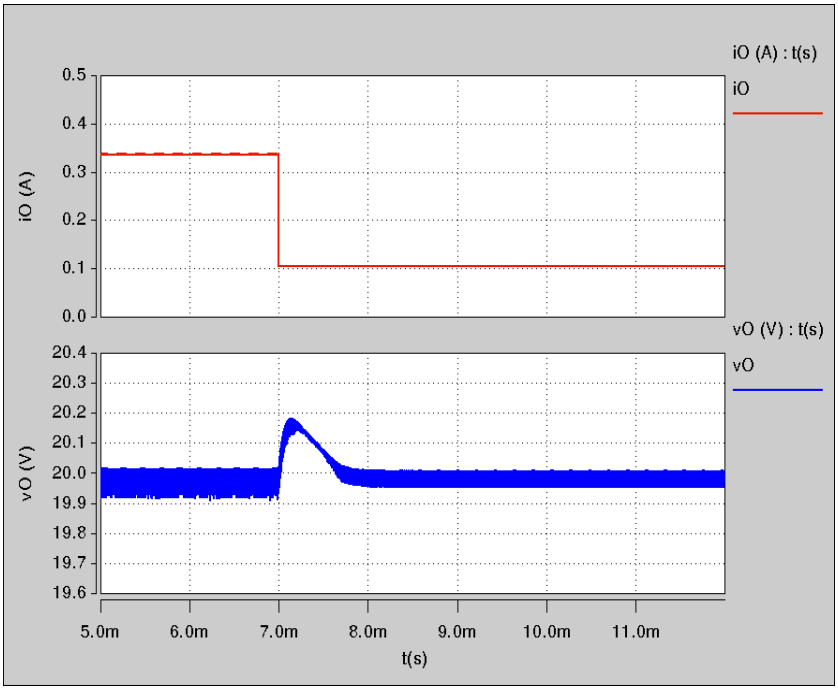


(b)

Figure 5.5: The PI-SSMCC system response during abrupt increase in load current. a) MATLAB results b) SaberRD results.

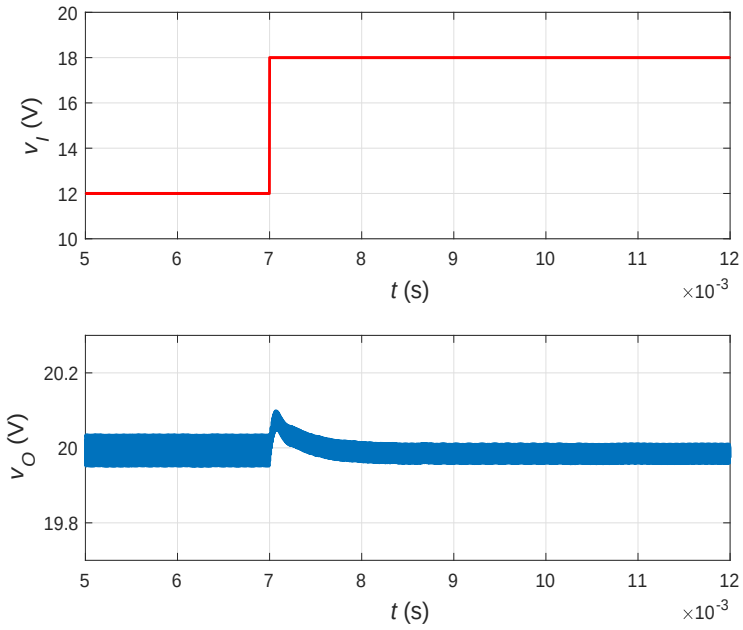


(a)

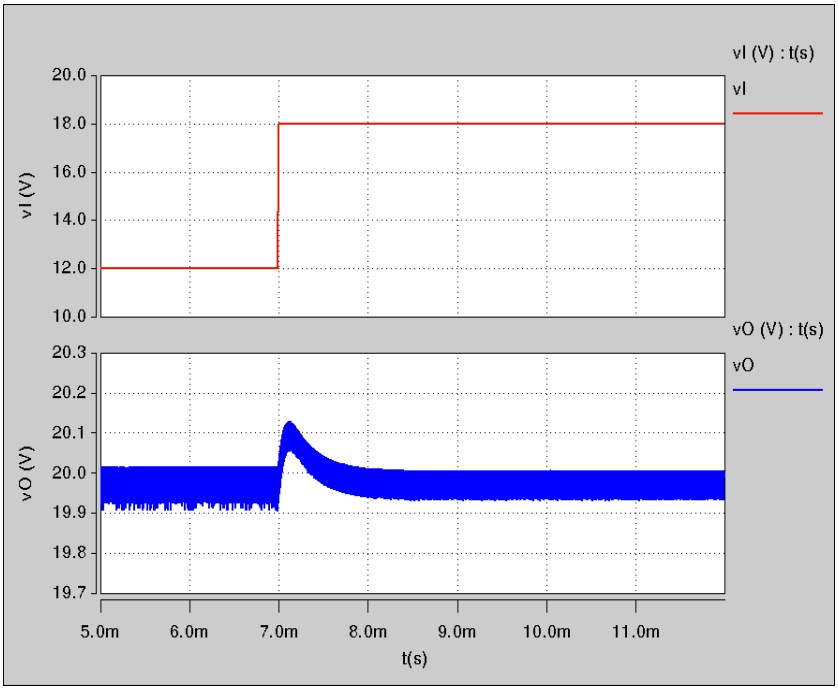


(b)

Figure 5.6: The PI-SSMCC system response during abrupt decrease in load current. a) MATLAB results b) SaberRD results.

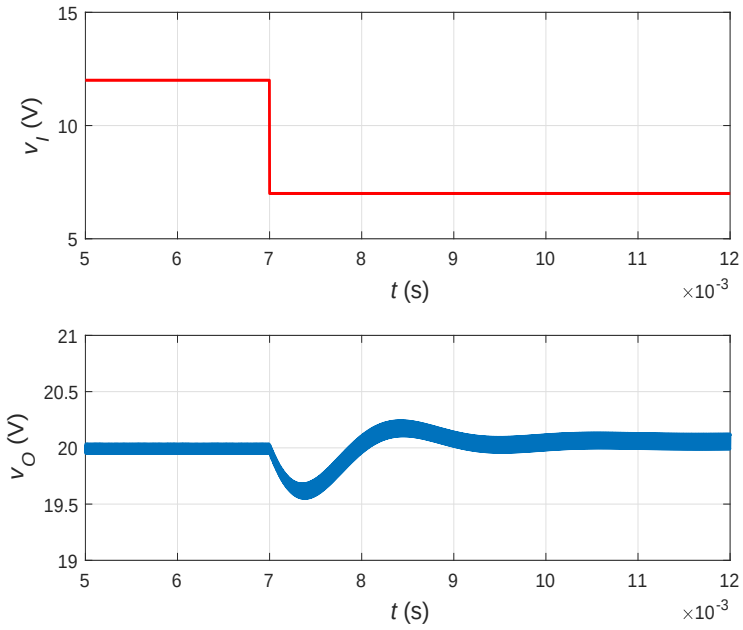


(a)

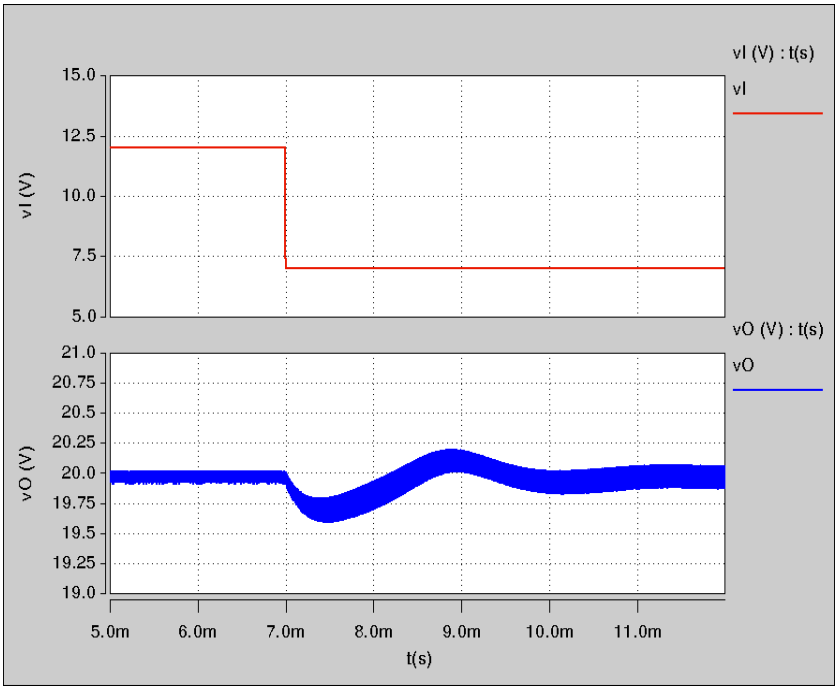


(b)

Figure 5.7: The PI-SSMCC system response during abrupt increase in input voltage. a) MATLAB results b) SaberRD results.



(a)



(b)

Figure 5.8: The PI-SSMCC system response during abrupt decease in input voltage. a) MATLAB results b) SaberRD results.

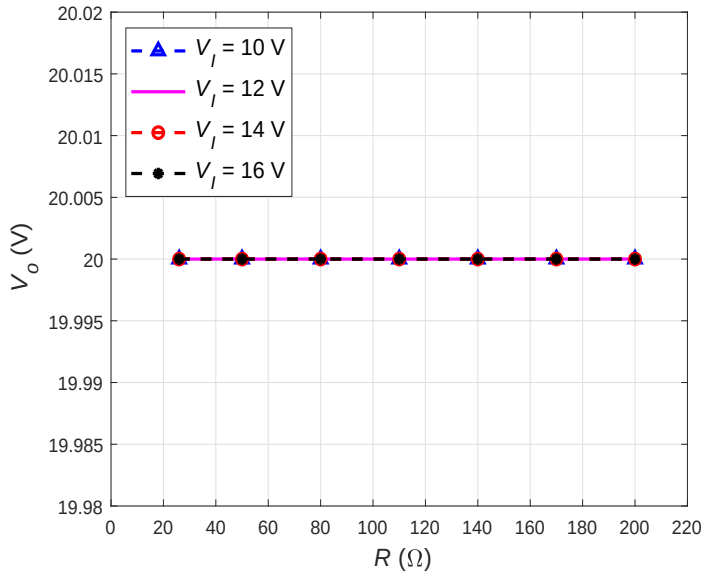
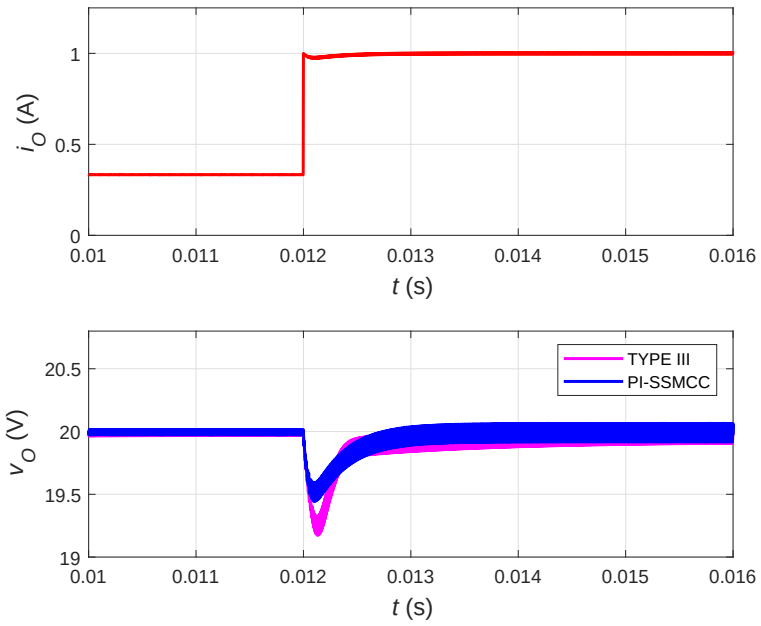


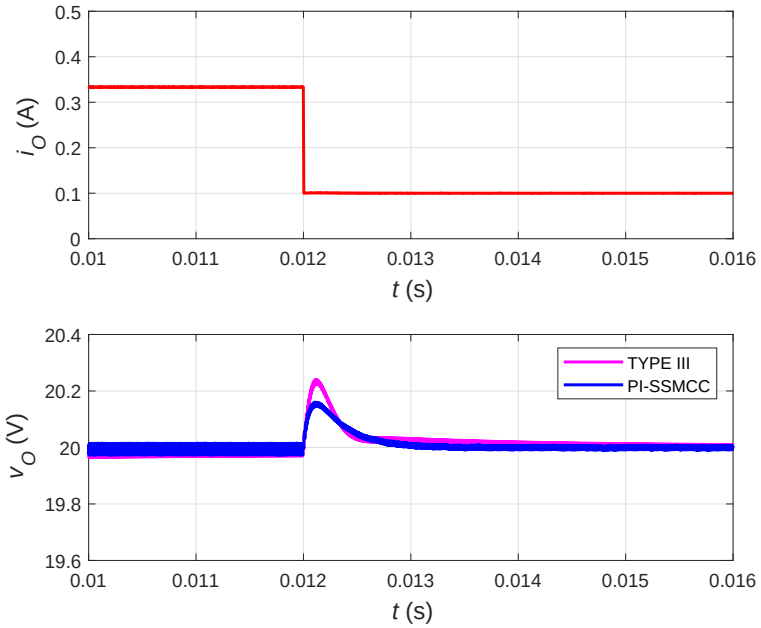
Figure 5.9: The output voltage V_O versus load resistance R at different input voltages V_I.

and longer settling time as compared to the nonlinear PI-SSMCC system. It can be noticed that the nonlinear controller provides consistent dynamical response and large-signal stability.

On the other hand, the tracking performance of the two controllers during large line disturbances is shown in Fig. 5.11. It can be seen that Type III controller response exhibits undesirable transient characteristics. In Fig. 5.11(a), the percentage peak overshoot and settling time of Type III controller response are 17.5 % and 8 ms, respectively, while the percentage undershoot and settling time in Fig. 5.11(b) are about 20 % and 5 ms, respectively. This is the main drawback of the linear control system, which is only valid for a small deviation around the equilibrium point.

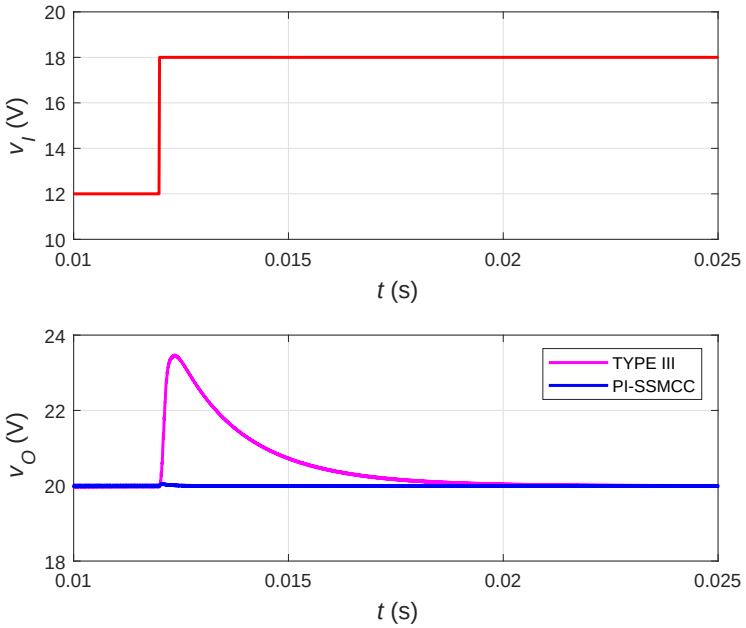


(a)

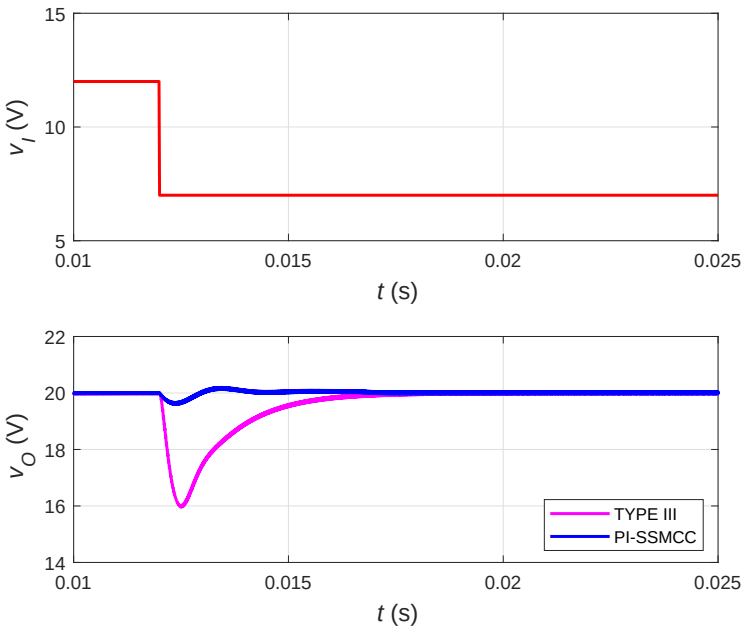


(b)

Figure 5.10: The output voltage response of the PI-SSMCC and Type III control of PWM dc-dc boost converter during abrupt a) increase and b) decrease in load current.



(a)



(b)

Figure 5.11: The output voltage response of the PI-SSMCC and Type III control of PWM dc-dc boost converter during abrupt a) increase and b) decrease in input voltage.

6 PCB Prototype of Closed-Loop SSMV Controlled PWM DC-DC Buck Converter

6.1 Introduction

The practical design and analogue implementation of the SSMVC of the PWM dc-dc buck converter in CCM have been discussed in this chapter. The closed-loop control system is implemented on a printed circuit board (PCB) and tested under steady-state and large disturbance conditions. The experimental and simulated results are compared together to verify the design approach.

6.2 Circuit Description

The design procedure in Chapter 3 is applied to design the the PWM-based SSMV controlled buck converter in CCM. The power converter parameters are defined in Table X. The components of the power stage include an IRF530 N-MOSFET, an MBR10100 Schottky diode, an inductor of 330 µH, an electrolytic output capacitor of 56 µF, and an electrolytic input filter capacitor of 330 µF. On the other hand, the control circuit components are summarized below

1. Output voltage sensor: The feedback network resistors R_A and R_B are 9.1 kΩ/1 %/0.25 W and 5.1 kΩ/1 %/0.25 W, respectively.

2. Differential amplifier: An LF357 op-amp is selected. The resistors R_F and R_D are chosen to be 680 kΩ/5 %/0.25 W and 1.568 kΩ/5 %/0.25 W, respectively. Additionally, R_{V1} and R_{V2} are set to 1 kΩ/5 %/0.25 W. Note that values of R_F and R_D are adjusted based on SaberRD simulator to eliminate the steady-stat error at v_O.

3. Summing and inverting amplifiers: LF356 op-amps are selected. The resistors R_{S1}, R_{S2}, R_{S3}, and R_{I2} are 5.1 kΩ/5 %/0.25 W, whereas R_{I1} is 2.5 kΩ/5 %/0.25

W.

4. PWM generator: The peak ramp voltage V_T is set to 4 V, while switching frequency is chosen to be 100 kHz. An LTC6992-2 is utilized as a pulse-width modulator. The supporting circuitry is designed based on the data sheet and LTspice simulation.

5. Gate driver: An LTC4440-5 high-side gate driver is selected to drive the MOSFET, where the supporting circuitry is developed using the data sheet and LTspice simulation.

Table X: Experimental Buck Converter Parameters

Description	**Parameter**	**Value**
Inductor	L	330 µH
Capacitor	C	56 µF
Load Resistor	r	$(20 - 100)$ Ω
Inductor ESR	r_L	0.05 Ω
Capacitor ESR	r_C	0.200 Ω
Inductor ESR	r_L	0.050 Ω
Capacitor ESR	r_C	0.200 Ω
MOSFET On-Resistance	r_{DS}	0.180 Ω
Diode Forward Resistance	r_F	0.022 Ω
Diode Threshold Voltage	V_F	0.700 V
Input Voltage	v_I	28 ± 4 V
Output Voltage	V_O	14 V
Switching Frequency	f_s	100 kHz

The schematic diagram of the PWM-based SSMV controlled buck converter circuit is shown in Fig. 6.1

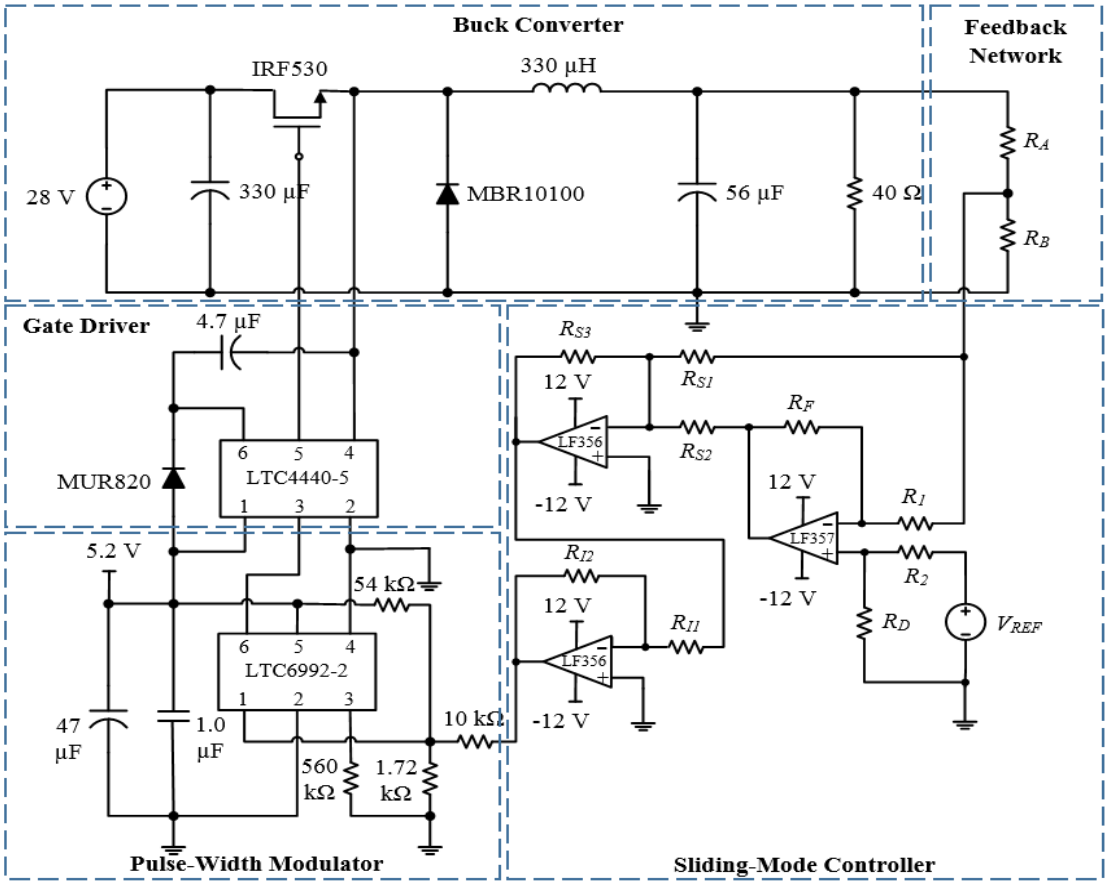


Figure 6.1: Schematic diagram of SSMV controlled PWM dc-dc buck converter circuit for CCM.

6.3 Experimental Prototype

The schematic diagram of the proposed control circuit has been implemented on a 2-layer PCB. The first step is to draw the schematic diagram given in Fig. 6.1 using AUTODESK EAGLE 8.2.2. Next, the schematic diagram is converted to a PCB layout. Once the layout is printed, it can then be utilized to mount and solder the analogue components.

6.3.1 Schematic Diagram

The schematic diagram of the SSMVC PWM dc-dc buck converter is drawn using EAGLE 8.2.2 software as shown in Fig. 6.2. The diagram contains all the relevant

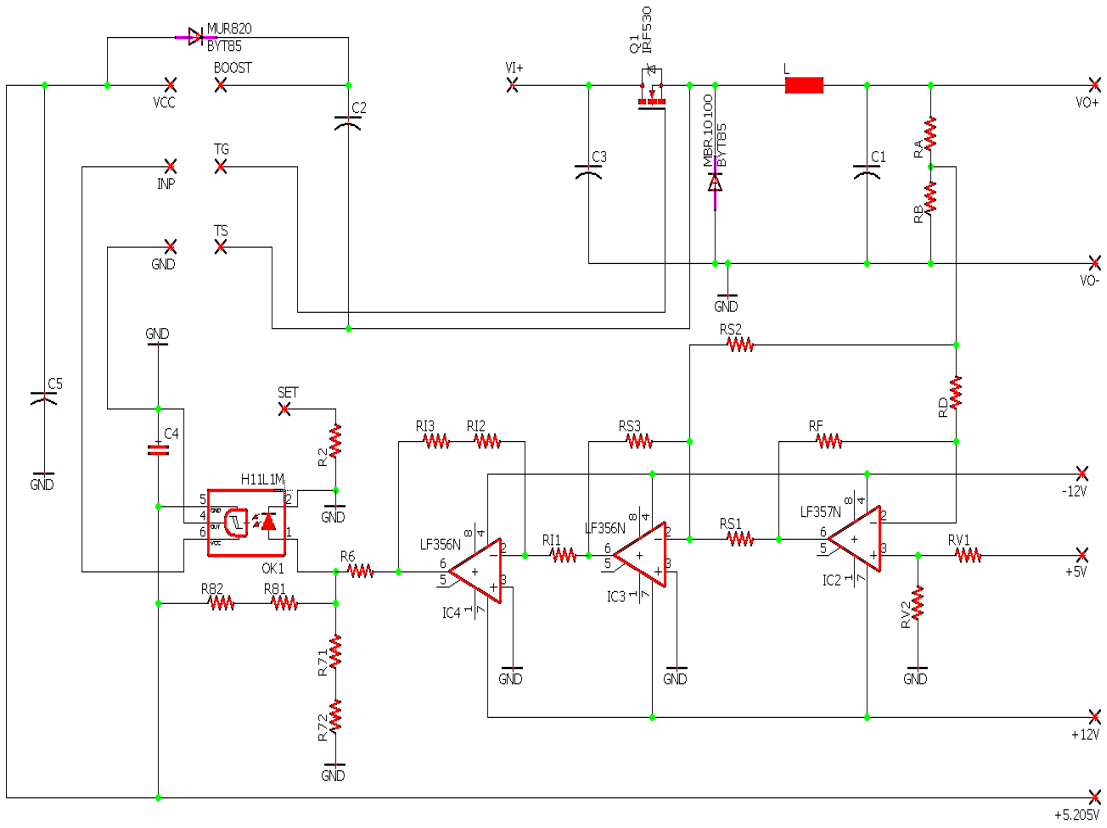
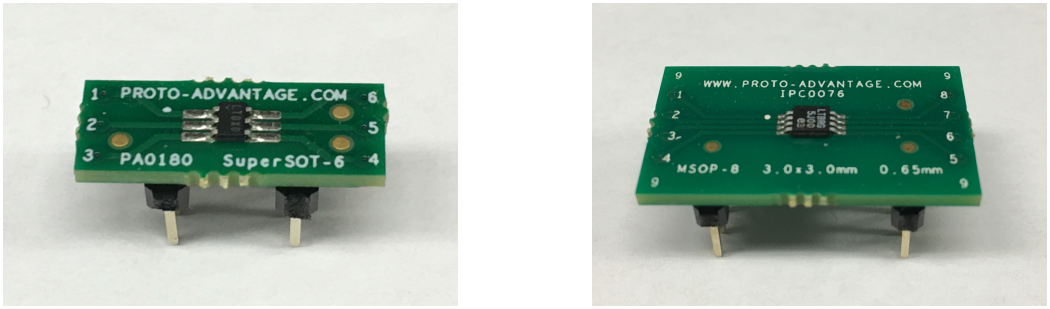


Figure 6.2: EAGLE-based schematic diagram of closed-loop control system.

components of the power stage, feedback network, control circuit, LTC6992-2 pulse-width modulator, and LTC4440-5 high-side gate driver. The ICs LTC6992-2 and LTC4440-5 are mounted on adapters as shown in Fig. 6.3 to fit in the PCB. The supporting components of the two ICs are set based on the data-sheets and LTspice simulations.

6.3.2 PCB Layout

The schematic diagram in Fig. 6.2 is converted to a basic layout using EAGLE software. The layout should be modified by the designer to place the components in order and use the minimum PCB area. In such a hard-switching circuit, standard design guidelines are recommended, which include the design of large ground plane. Additionally, traces are made wide and short, especially those that carry a high current



(a) (b)

Figure 6.3: The (a) pulse-width modulator and (b) high-side gate driver mounted on their adapters.

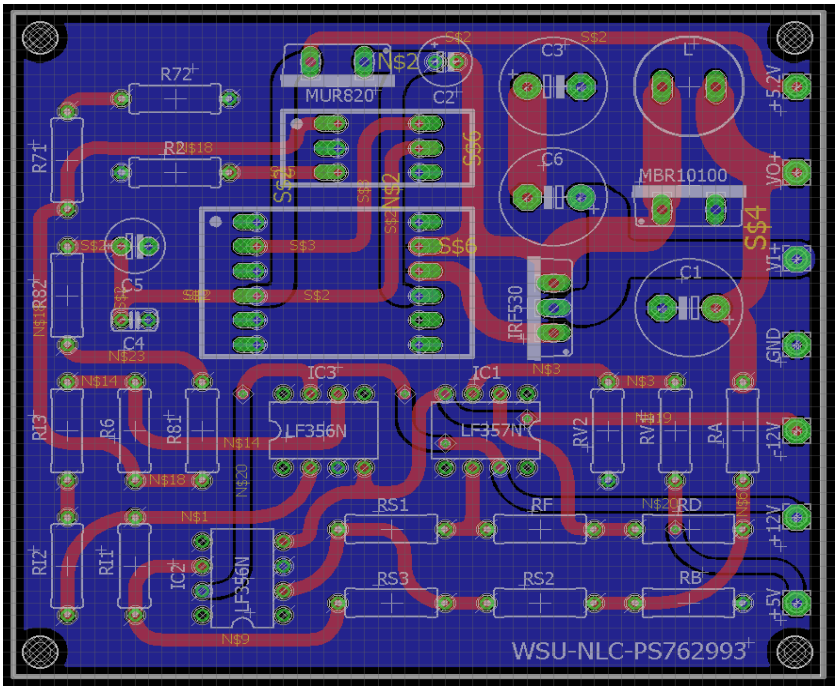


Figure 6.4: PCB layout of closed-loop control system.

at the power stage. The final layout is shown in Fig. 6.4.

6.3.3 PCB Prototype

Once the the layout is printed, the circuit components can be mounted on the PCB and soldered as shown in Fig. 6.5. The prototype can also be redesigned and optimized based on the designer's discretion. However, the purpose of designing the closed-loop

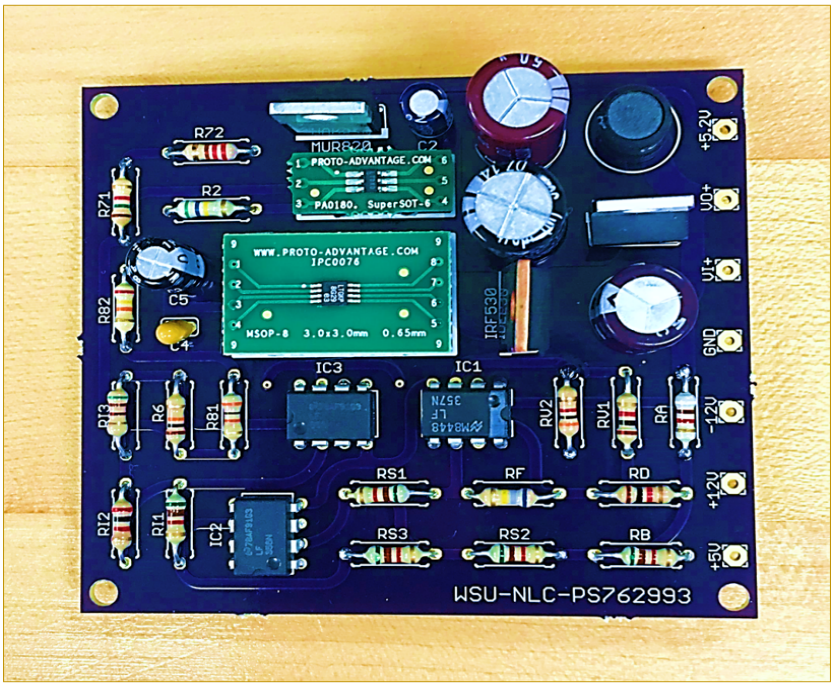


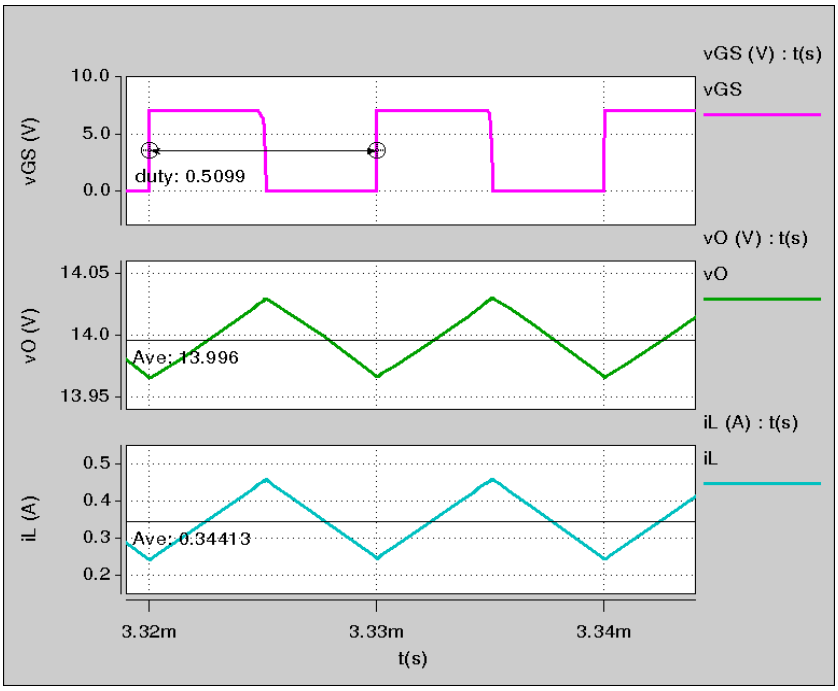
Figure 6.5: PCB prototype of closed-loop control system.

power converter on PCB is to show the feasibility of the design approach and conduct experimental tests.

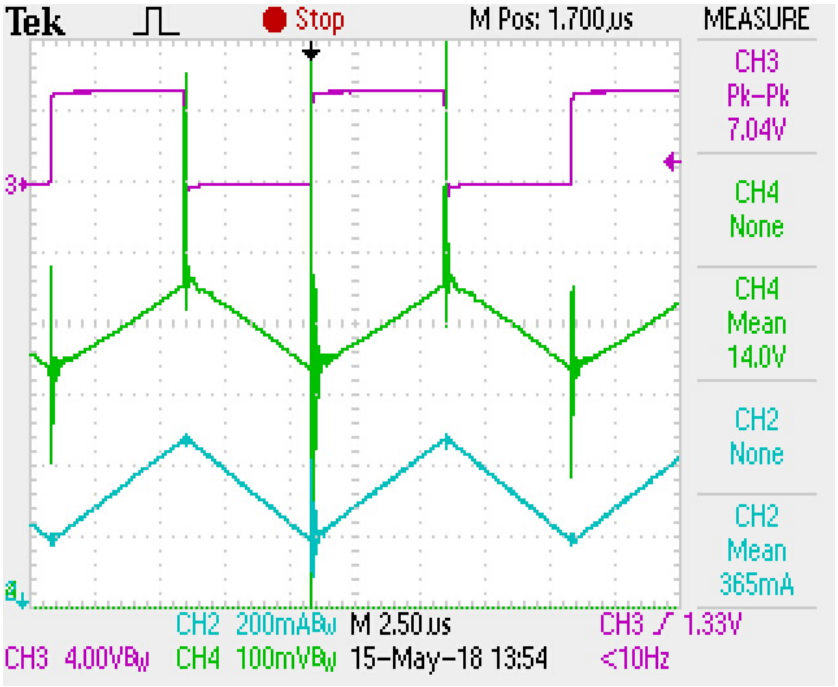
6.4 Simulation and Experimental Results

6.4.1 Steady-State Performance

The steady-state waveforms of the PCB prototype are compared with the corresponding results obtained from SaberRD as shown in Fig. 6.6. The power converter operates at steady-state condition, where v_I and r are 28 V and 40 Ω, respectively. It can be seen that the simulated results are in good agreement with the experimental results. In Fig. 6.6(a), the steady-state values of duty cycle, output voltage, and inductor current are 0.5099, 13.996 V, and 0.344 A, whereas the corresponding experimental results are 0.5, 14.00 V, and 0.365 A, respectively. Moreover, the switching frequency of v_{GS} is kept constant at 100 kHz.



(a)



(b)

Figure 6.6: (a) Simulated and (b) experimental waveforms of gate-to-source voltage v_{GS}, output voltage v_O, and inductor current i_L during steady-state condition.

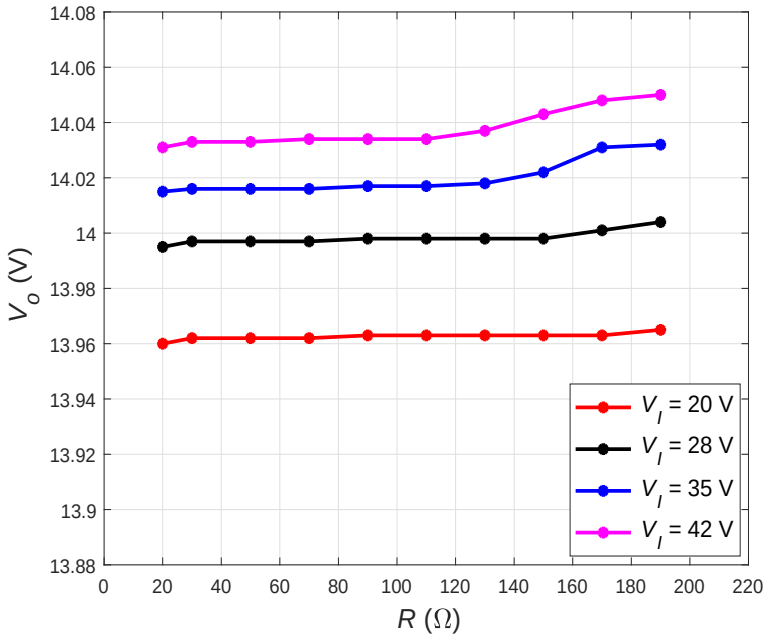
6.4.2 Regulation Performance

Fig. 6.7 shows the output voltage of the proposed control system with respect to the line and load variation. The discrepancies between the simulated and experimental results are due to the tolerances of resistors and the non-ideality of the analogue components in the actual control circuit, which are not modeled in SaberRD simulation. The graphs show that as the load changes from 20 Ω to 190 Ω, the output voltage remains close to the desired value 14 V. From the experimental results, it can be seen that the maximum ΔV_O occurs at $V_I = 42$ V when $R = 190$ Ω and at $V_I = 20$ V when $R = 20$ Ω, where V_O values are 14.060 V and 13.938 V, respectively. Hence, there is about ±60 mV deviation in the desired V_O at maximum operating conditions.

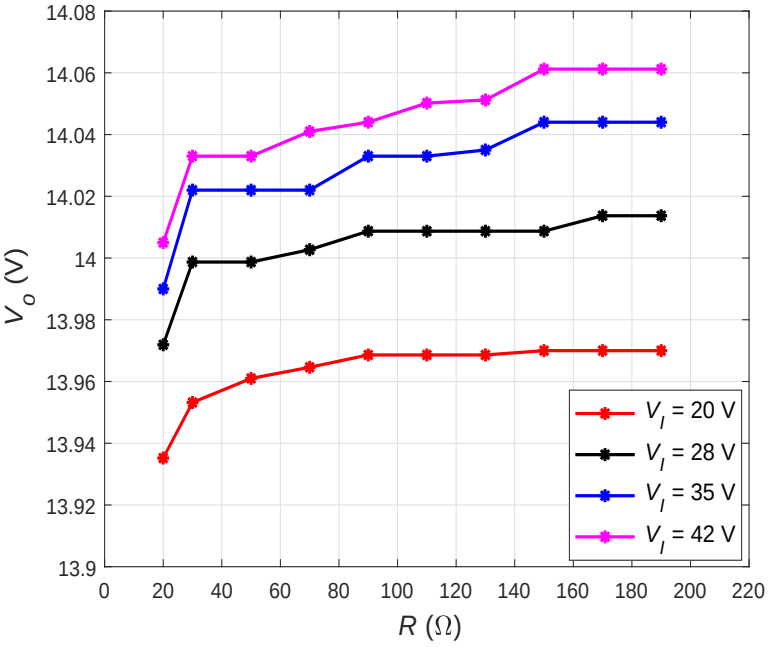
The $PLOR$ and $PLNR$ have been calculated for several cases as shown in Tables XI and XII, respectively. Despite the discrepancy between the simulated and experimental results, it can be noticed that the maximum $PLNR$ is less than 0.1 %/V, and the maximum $PLOR$ is less than 1 %. The experimental results given in Table XI show that when V_I is 42 V, the maximum experimental $PLOR$ is 0.399 %. At this operating condition, if R varies from 20 Ω to 190 Ω, the maximum deviation in V_O is about 56 mV. On the other hand, the maximum experimental $PLNR$ in Table XII is 0.039 %/V, which occurs when V_I changes from 28 V to 20 V at 190 Ω load resistance. Thus, the tabulated results show that the proposed control system maintains an output voltage close to the desired value under a wide operating range.

6.4.3 Tracking Performance

The tracking performance during large disturbances is investigated using MATLAB simulations and compared with the corresponding experimental results. The waveform of v_O during abrupt increase and decrease in v_I is shown in Figs. 6.8 and 6.9, respectively. As shown in Fig. 6.8(b), when v_I increases from 28 V to 42 V, v_O increases about 36.25 mV. Furthermore, if v_I decreases from 28 V to 20 V as depicted



(a)



(b)

Figure 6.7: (a) Simulated and (b) experimental plots of output voltage V_O versus load resistor R at different input voltages V_I.

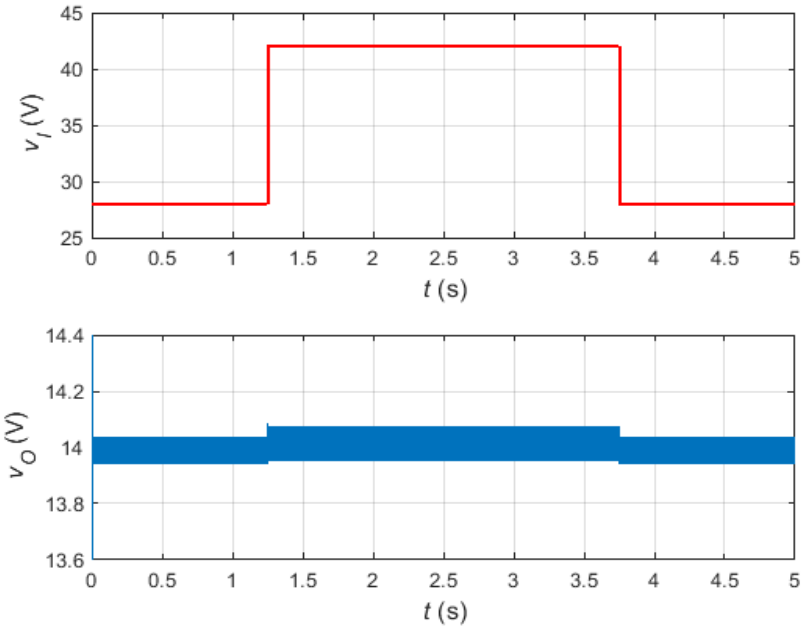
Table XI: Simulated and Experimental Percentage Load Regulation of SSMVC System

V_I (V)	$\Delta V_O = V_{O_{R_{(max)}}} - V_{O_{R_{(min)}}}$ (V)		$PLOR$ (%)	
	Simulated	Experimental	Simulated	Experimental
20	0.005	0.035	0.036	0.249
28	0.010	0.042	0.072	0.298
35	0.019	0.054	0.156	0.386
42	0.022	0.056	0.157	0.399

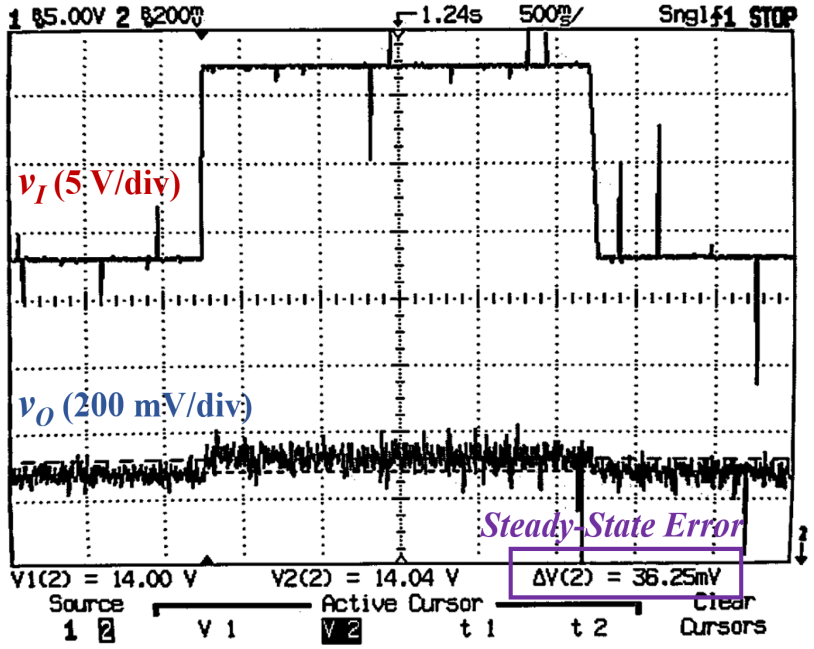
Table XII: Simulated and Experimental Percentage Line Regulation of SSMVC System

R (Ω)	$PLNR$ (%/V)					
	$\Delta V_I = 28 \rightarrow 20$ (V)		$\Delta V_I = 28 \rightarrow 35$ (V)		$\Delta V_I = 28 \rightarrow 42$ (V)	
	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.
20	0.031	0.033	0.018	0.019	0.017	0.017
50	0.032	0.034	0.019	0.024	0.018	0.018
90	0.032	0.036	0.020	0.025	0.018	0.018
130	0.033	0.036	0.020	0.027	0.019	0.022
190	0.036	0.039	0.028	0.031	0.023	0.024

in Fig. 6.9(b), v_O decreases 45 mV. Next, the tracking performance during an abrupt increase and decrease in load current i_O is shown in Figs. 6.10 and 6.11, respectively. Load current was measured using a current probe-to-voltage amplifier scaled 1:1 with the voltage display setting of the oscilloscope. When i_O changes from the nominal value 0.35 A to 0.7 A, v_O decreases 28.13 mV. However, if i_O decreases from 0.35 A to 0.15 A, v_O decreases 15.62 mV. It can be seen that the simulated and experimental results are close to each other, and the disturbance effect is rejected within 40 µs. However, a small steady-state error at v_O is noticed, especially during line disturbance. As mentioned in Chapter 3, the slight deviation in v_O is due to the implementation of the equivalent control equation via a pulse-width modulator with a constant ramp



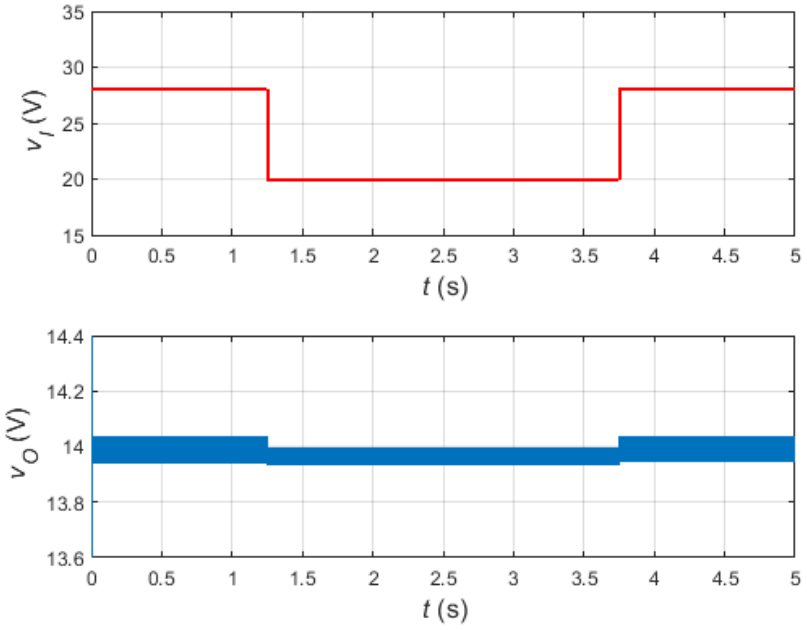
(a)



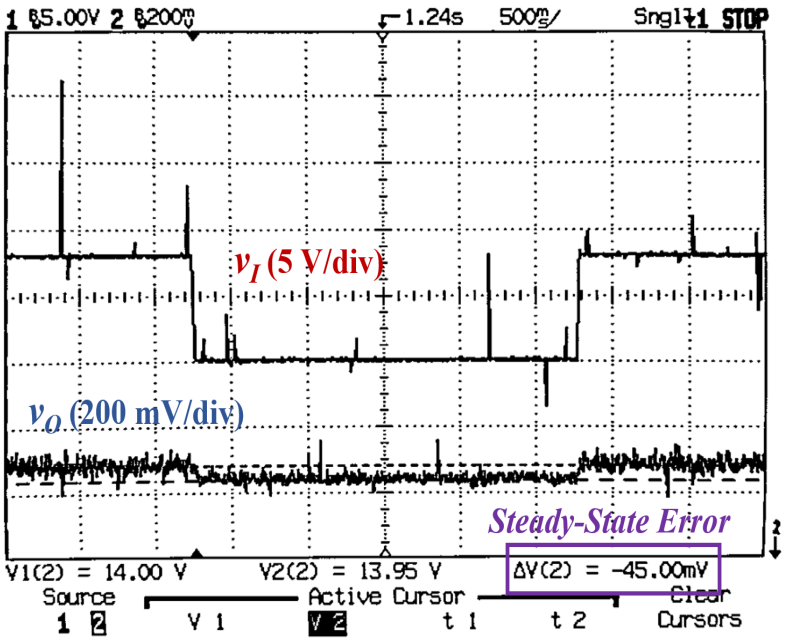
(b)

Figure 6.8: (a) Simulated and (b) experimental waveforms of output voltage v_O when input voltage v_I increases from 28 V to 42 V.

voltage V_T.

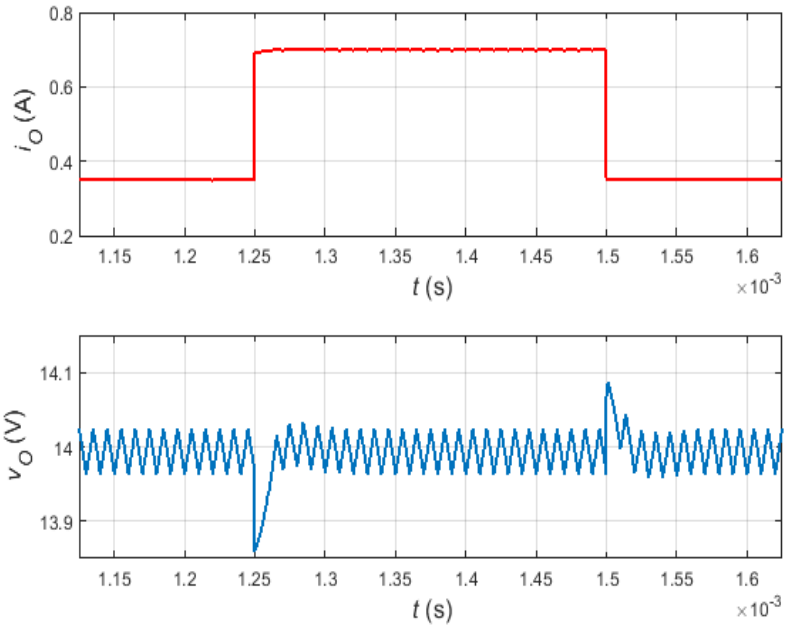


(a)

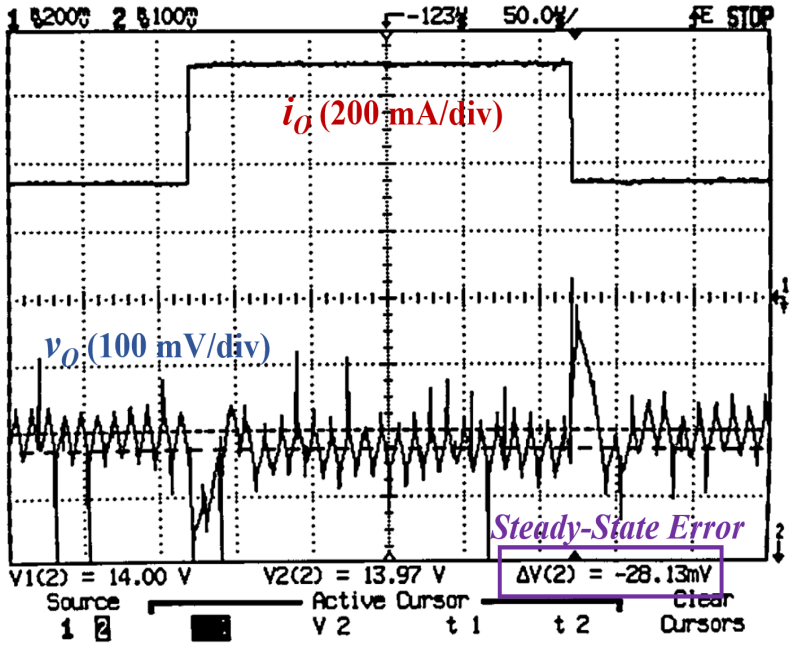


(b)

Figure 6.9: (a) Simulated and (b) experimental waveforms of output voltage v_O when input voltage v_I decreases from 28 V to 20 V.

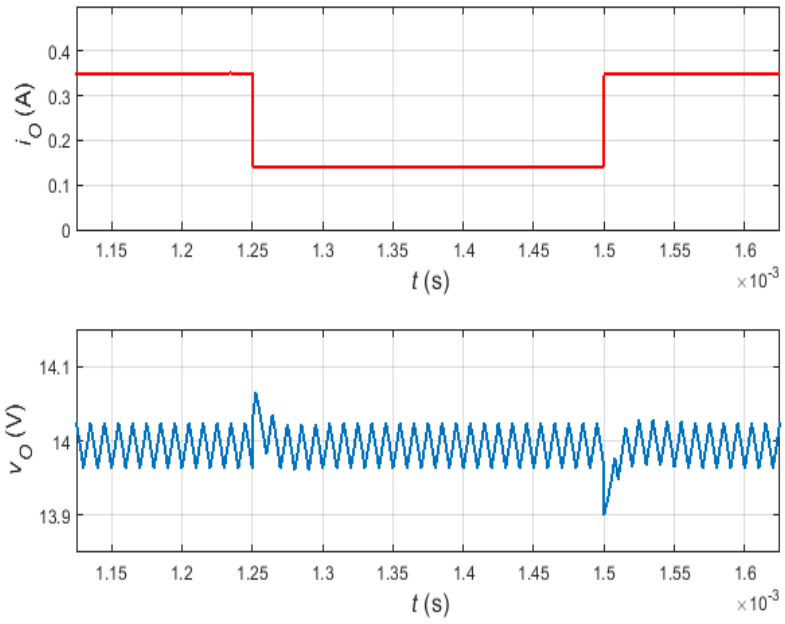


(a)

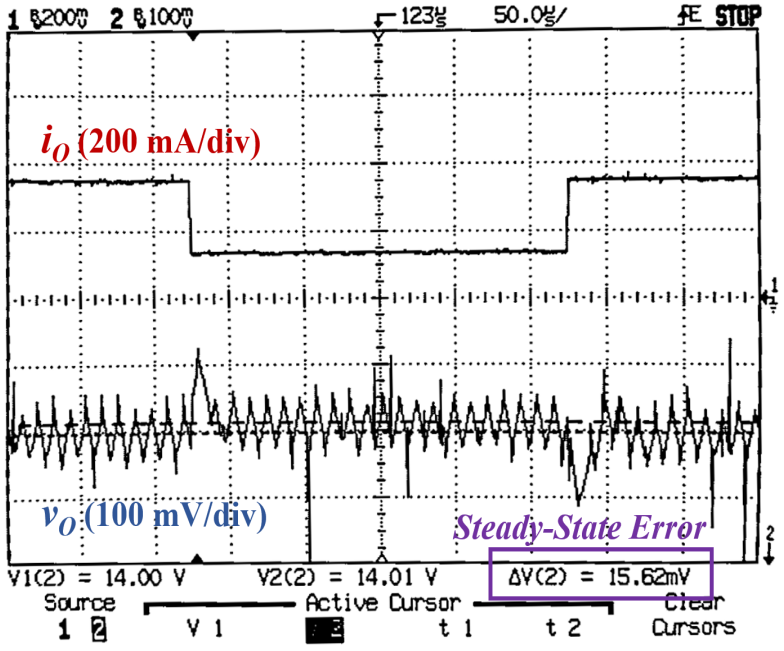


(b)

Figure 6.10: (a) Simulated and (b) experimental waveforms of output voltage v_O when load current i_O increases from 0.35 A to 0.70 A.



(a)



(b)

Figure 6.11: (a) Simulated and (b) experimental waveforms of output voltage v_O when load current i_O decreases from 0.35 A to 0.15 A.

7 Conclusions and Future Work

7.1 Summary

The nonlinear modeling and the design of the simplified sliding-mode control of PWM dc-dc converters in CCM have been discussed. In Chapter 2, the nonlinear models of the buck and boost converters are

- Developed using Kirchhoff's circuit laws and averaging technique.
- Validated via MATLAB/SIMULINK and SaberRD simulations.
- Studied under large line and load disturbances.

The single- and double-integral simplified sliding-mode voltage controlled PWM dc-dc buck converter have been introduced in Chapters 3 and 4, respectively. Additionally, the double-integral simplified sliding-mode current controlled PWM dc-dc boost converter has been explored in Chapter 5, where

1) The equivalent control laws are derived based on the invariance conditions.
2) The existence and stability conditions are derived to set the criteria of choosing the controller gains.
3) The design procedure and analogue realization of the control circuits are given in details.
4) The proposed control circuits are simulated in MATLAB/SIMULINK and SaberRD.
5) The tracking performance under large disturbances and regulation performance are investigated.

The practical implementation of the simplified sliding-mode voltage controlled PWM dc-dc buck has been presented in Chapter 6, in which

- The design aspects of the PCB prototype are explained.
- The experimental results are obtained under large line and load disturbances.
- The simulated and experimental results are compared to validate the design approach.

7.2 Conclusions

1) The nonlinear dynamics of the switched-mode power converters in CCM can easily be derived using Kirchhoff's circuit laws and simulated in MATLAB/SIMULINK using s-function. The models include all the parasitic components and can be simulated without the need of Simscape.

2) The simulation results from SaberRD and MATLAB have showed that the nonlinear models reflect the power converters behavior properly and can be used to investigate the control system performance.

3) The PWM-based simplified sliding-mode voltage and current control schemes exhibit more consistent transient response and better disturbance rejection as compared to the linear control systems.

4) The PWM-based SMC circuits maintain a constant and low switching frequency, thus the EMI issues and switching losses are reduced significantly. In contrast, the HM-based SMC circuits operates at variable and high switching frequency.

5) The proposed control design approach results in simpler control schemes that can be implemented with fewer added components as compared to the sliding-mode control schemes in the previous literatures.

6) The sliding-mode current control method enhances the transient response of the non-minimum phase systems such as the boost and buck-boost converters. In

contrast, the sliding-mode voltage control method is suited for the buck converter because it is a minimum phase system.

7) The proposed double integral simplified sliding-mode voltage and current control circuits eliminate the steady-state error at the output voltage and ensure a precise tracking in the presence of the large disturbances.

8) The simplified sliding-mode control design can be extended to the other types of the basic power converters in CCM such as the buck-boost converter and the dynamic power supplies. Interested readers can refer to [75], [77].

7.3 Contributions

The main contributions in this research are:

1) Large-signal non-ideal averaged models of basic switched-mode power converters in CCM have been developed, simulated in MATLAB/SIMULINK, and validated using SaberRD simulator.

2) Single- and double- integral simplified sliding-mode voltage control circuits for PWM dc-dc buck converter have been designed along with the derivation of the existence and stability conditions.

3) Double integral simplified sliding-mode current controlled PWM dc-dc boost converter has been designed. The existence and stability conditions have also been derived.

4) The design procedure and analogue realization of the PWM-based simplified sliding-mode control systems have been introduced in detail.

5) The control equations and the corresponding analogue circuits have been simulated in MATLAB/SIMULINK and SaberRD during steady-state and large disturbance conditions.

6) The line and load regulation performance of the proposed control systems has been analyzed.

7) A PCB prototype of a simplified sliding-mode voltage controlled PWM dc-dc buck converter has been designed and tested under various operating conditions.

7.4 Future Work

The following topics will be investigated in the future:

1) Discontinuous Conduction Mode (DCM)

   The application of the simplified sliding-mode control design approach to the PWM dc-dc converters in DCM. Modeling of power converter, derivation of equivalent control law, and study of control system performance.

2) Complex Typologies

   The investigation of the simplified sliding-mode control with more complex power converters such as the Cuk, Zeta, Sepic, and cascaded power converters.

3) Constant Power Load

   Solving the constant power load and relevant instability issues of tightly regulated power converters using the simplified sliding-mode control systems.

4) Optimal Control Gains

   The optimization of the simplified sliding-mode voltage and current control gains that yield the optimal transient response and the widest operating range.

5) Isolated Power Converters

   The application of the simplified sliding-mode control method to the isolated power converters such as the flyback converters.

7.5 Publications

1. H. Al-Baidhani and M. K. Kazimierczuk, "PWM-based proportional-integral sliding-mode current control of DC-DC boost converter," *IEEE Conference on TPEC*, pp. 1-6, 2018.

2. H. Al-Baidhani and M. K. Kazimierczuk, "Nonlinear modeling and PWM-based sliding-mode control of DC-DC buck converter for CCM," *IEEE Conference on ISGT*, pp. 1-5, 2018.

3. H. Al-Baidhani, M. K. Kazimierczuk, and Alberto Reatti, "Nonlinear Modeling and Voltage-Mode Control of DC-DC Boost Converter for CCM," *IEEE Symposium on ISCAS*, pp. 1-5, 2018.

4. H. Al-Baidhani, M. K. Kazimierczuk, and R. Ordóñez, "Nonlinear Modelling and Control of PWM DC-DC Buck-Boost Converter for CCM," *Proceedings of the 44th Annual Conference of the IEEE Industrial Electronics Society (IECON-2018)*, pp. 1374-1379, 2018.

5. H. Al-Baidhani, M. K. Kazimierczuk, T. Salvatierra, A. Reatti, and F. Corti, "Sliding-Mode Voltage Control of Dynamic Power Supply for CCM," *IEEE Symposium on ISCAS*, pp. 1-5, 2019.

8 References

References

[1] Z. Chen, W. Gao, and X. Ye, "Frequency domain closed-loop analysis and sliding mode control of a nonminimum phase buck-boost converter," *Control and Intelligent Systems*, vol. 38, no. 4, pp. 245-255, 2010.

[2] G. Spiazzi, P. Mattaelli, and L. Rossetto, "Sliding mode control of DC-DC converters," *Proc. 4th Congresso Brasileiro de Elettronica de Potencia*, pp. 59-68, 1997.

[3] V. Utkin, J. Guldner, and J. Shi, *Sliding Mode Control in Electromechanical Systems*, 2nd ed., Taylor & Francis, Boca Raton, FL: CRC Press, 2009.

[4] S. Tan, Y. Lai, and C. K Tse, *Sliding Mode Control of Switching Power Converters: Techniques and Implementation*, Boca Raton, FL: CRC Press, 2012.

[5] F. Bilalovic, O. Music, and A. Sabanovic, "Buck converter regulator operating in the sliding mode," *Proc. 7th Int. Conf. PCI*, pp. 331-340, Apr. 1983.

[6] S. C. Tan, Y. M. Lai, and C. K. Tse, "General design issues of sliding-mode controllers in DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1160-1174, Mar. 2008.

[7] S. C. Tan, Y. M. Lai, C. K. Tse, and M. K. H. Cheung, "A fixed-frequency pulsewidth modulation based quasi-sliding-mode controller for buck converters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1379-1392, Nov. 2005.

[8] C. Edwards and S. K. Spurgeron, *Sliding Mode Control: Theory and Applications*, London, U.K.: Taylor and Francis, 1998.

[9] V. Utkin, "Sliding mode control of DC/DC converters," *Journal of the Franklin Institute*, vol. 350, no. 8, pp. 2146-2165, 2013.

[10] H. W. Whittington, B. W. Flynn, and D. E. Macpherson, *Switched Mode Power Supplies: Design and Construction*, 2nd ed., New York: Wiley, 1997.

[11] R. Venkataramanan, A. Sabanoivc, and S. Cuk, "Sliding mode control of DC-to-DC converters," *Proc. IEEE Conf. Industrial Electronics, Control Instrumentations (IECON)*, pp. 251-258, 1985.

[12] P. Mattavelli, L. Rossetto, and G. Spiazzi, "Small-signal analysis of DC-DC converters with sliding mode control," *IEEE Trans. Power Electron.* , vol. 12, no. 1, pp. 96-102, Jan. 1997.

[13] E. Vidal-Idiarte, C. E. Carrejo, J. Calvente, and L. Martínez-Salamero, "Two-loop digital sliding mode control of dc-dc power converters based on predictive interpolation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2491-2501, Jun. 2011.

[14] B. B. Naik and A. J. Mehta, "Sliding mode controller with modified sliding function for DC-DC buck converter," *ISA Transactions*, vol. 70, pp. 279-287, Sep. 2017.

[15] Y. Jeung and D. Lee, "Voltage and current regulations of bidirectional isolated dual-active-bridge dc-dc converters based on a double-integral sliding mode control," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6937-6946, July 2019.

[16] J. Wu and Y. Lu, "Adaptive backstepping sliding mode control for boost converter with constant power load," *IEEE Access*, vol. 7, pp. 50797-50807, 2019.

[17] S. Lee, Y. Jeung, and D. Lee, "Voltage balancing control of IPOS modular dual active bridge DC/DC converters based on hierarchical sliding mode control," *IEEE Access*, vol. 7, pp. 9989-9997, Jan. 2019.

[18] Y. Yin et al., "Observer-based adaptive sliding mode control of NPC converters: An RBF neural network approach," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3831-3841, Apr. 2019.

[19] X. Zheng, Y. Feng, F. Han, and X. Yu, "Integral-type terminal sliding-mode control for grid-side converter in wind energy conversion systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3702-3711, 2019.

[20] H. Komurcugil, S. Biricik, and N. Guler, "Indirect sliding mode control for DC–DC SEPIC converters," *IEEE Trans Ind. Informat.*, vol. 16, no. 6, pp. 4099-4108, Jun. 2020.

[21] R. J. Wai and L. C. Shih, "Design of voltage tracking control for dc-dc boost converter via total sliding-mode technique," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2502-2511, Jun. 2011.

[22] E. Vidal, L. Martine, F. Guinjoan, J. Calvente, S. Gomariz, "Sliding and fuzzy control of a boost converter using an 8-bit microcontroller," *Proc. Inst. Elect. Eng. Electr. Power Appl.*, vol. 151, no. 1, pp. 5-11, Jan. 2004.

[23] M. Oettmeier, J. Neely, S. Pekarek, R. DeCarlo, S. Uthaichana, "MPC of switching in a boost converter using a hybrid state model with a sliding mode observer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 9, pp. 3453-3466, Sep. 2009.

[24] R. Ling, D. Maksimovic, and R. Leyva, "Second-order sliding-mode controlled synchronous buck DC-DC converter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2539-2549, Mar. 2016.

[25] R. Ling, Z. Shu, Q. Hu. and Y. Song, "Second-order sliding-mode controlled three-level buck DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 898-906, Jan. 2018.

[26] V. Repecho, D. Biel, R. Ramos-Lara, and P. G. Vega, "Fixed-switching frequency interleaved sliding mode eight-phase synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 676-688, Jan. 2018.

[27] P. Z. Lin et al., "Type-2 fuzzy controller design using a sliding mode approach for application to dc-dc converters," *Proc. Inst. Elect. Eng. Elect. Power Appl.*, vol. 152, no. 6, pp. 1482-1488, Nov. 2005.

[28] K. H. Cheng, C. F. Hsu, C. M. Lin, T. T. Lee, and C. Li, "Fuzzy–neural sliding-mode control for DC-DC converters using asymmetric gaussian membership functions," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1528-1536, Jun. 2007.

[29] S. Oucheriah and L. Guo, "PWM-based adaptive sliding-mode control for boost DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3291-3294, Aug. 2013.

[30] S. M. RakhtAla, M. Yasoubi, and H. HosseinNia, "Design of second order sliding mode and sliding mode algorithms: a practical insight to DC-DC buck converter," *IEEE/CAA Journal of Automatica Sinica*, vol. 4, no. 3, pp. 483-497, July 2017.

[31] J. X. Wang, S. H. Li, J. Yang, B. Wu, and Q. Li, "Extended state observer-based sliding mode control for PWM-based dc-dc buck power converter systems with mismatched disturbances," *IET Control Theory Appl.*, vol. 9, no. 4, pp. 579-586, Feb. 2015.

[32] J. X. Wang, S. H. Li, and J. Yang, "Finite-time disturbance observer based non-singular terminal sliding-mode control for pulse width modulation based DC-DC

buck converters with mismatched load disturbances," *IET Power Electronics*, vol. 9, no. 9, pp. 1995-2002, Jul. 2016.

[33] R. Frasca, L. Iannelli, and F. Vasca, "Dithered sliding-mode control for switched systems," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 53, no. 9, pp. 872-876, Sep. 2006.

[34] C. Wang, H. Xia, Y. Wang , Y. Mai, and S. Ren, "Discretisation performance analysis of sliding mode controlled dc-dc buck converter via zero-order holder," *IET Control Theory Appl.*, vol. 13, no. 16, pp. 2583-2594, Sep. 2019.

[35] Y. Zhao, W. Qiao, and D. Ha, "A sliding-mode duty-ratio controller for DC/DC buck converters with constant power loads," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1448-1458, Mar./Apr. 2014.

[36] P. R. Mohanty and A. K. Panda, "Fixed-frequency sliding-mode control scheme based on current control manifold for improved dynamic performance of boost PFC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 576-586, Mar. 2017.

[37] Z. Wang, S. Li , and Q. Li, "Discrete-time fast terminal sliding mode control design for dc-dc buck converters with mismatched disturbances," *IEEE Transactions on Industrial Informatics*, vol. 16, no. 2, pp. 1204-1213, Feb. 2020.

[38] S. Pandey, S. L. Patil, U. M. Chaskar, and S. B. Phadke, "State and disturbance observer-based integral sliding mode controlled boost dc-dc converters," *IEEE Trans. Circuits Syst. II Exp. Briefs.*, vol. 66, no. 9, pp. 1567-1571, Sep. 2019.

[39] I. Yazici and E. K. Yaylaci, "Fast and robust voltage control of DC-DC boost converter by using fast terminal sliding mode controller," *IET Power Electron.*, vol. 9, no. 1, pp. 120-125, Jan. 2016.

[40] I. Yazici, "Robust voltage-mode controller for DC-DC boost converter," *IET Power Electronics*, vol. 8, no. 3, pp. 342-349, 2015.

[41] S. Singh, D. Fulwani, and V. Kumar, "Robust sliding-mode control of DC/DC boost converter feeding a constant power load," *Power Electron. IET.*, vol. 8, no. 7, pp. 1230-1237, 2015.

[42] A. Merabet, L. Labib, A. M. Y. M. Ghias, C. Ghenai, and T. Salameh, "Robust feedback linearizing control with sliding mode compensation for a grid-connected photovoltaic inverter system under unbalanced grid voltages," *IEEE J. Photovolt.*, vol. 7, no. 3, pp. 828-838, May 2017.

[43] A. R. Gautam, K. Gourav, J. M. Guerrero, and D. M. Fulwani, "Ripple mitigation with improved line-load transients response in a two-stage DC-DC-AC converter: Adaptive SMC approach," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3125-3135, Apr. 2018.

[44] Q. Tabart, I. Vechiu, A. Etxeberria, and S. Bacha, "Hybrid energy storage system microgrids integration for power quality improvement using four-leg three-level NPC inverter and second-order sliding mode control," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 424-435, Jan. 2018.

[45] E. Alarcon, A. Romero, A. Poveda, S. Porta, L. Martinez-Salamero, "Current-mode analog integrated circuit for sliding-mode control of switching power converters," *Electron. Lett.*, vol. 38, no. 3, pp. 104-106, Jan. 2002.

[46] B. Labbe, B. Allard, X. Lin-Shi, and D. Chesneau, "An integrated sliding-mode buck converter with switching frequency control for battery-powered applications," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4318-4326, Sep. 2013.

[47] B. Labbe, B. Allard, and X. Lin-Shi, "Design and stability analysis of a frequency controlled sliding-mode buck converter," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 61, no. 9, pp. 2761-2770, Sep. 2014.

[48] A. Dashtestani and B. Bakkaloglu, "A fast settling oversampled digital sliding-mode DC-DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1019-1027, Feb. 2015.

[49] S. Maity, "Dynamics and stability issues of a discretized sliding-mode controlled dc-dc buck converter governed by fixed-event-time switching," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 60, no. 6, pp. 1657-1669, Jun. 2013.

[50] L. Martínez-Salamero, G. Garcia, M. Orellana, C. Lahore, and B. Estibals, "Start-up control and voltage regulation in a boost converter under sliding-mode operation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4637-4649, Oct. 2013.

[51] A. Leon-Masich, H. Valderrama-Blavi, J. M. Bosque-Moncusi, J. Maixe-Altes, and L. Martínez-Salamero, "Sliding-mode-control-based boost converter for high-voltage-low-power applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 229-237, Jan. 2015.

[52] O. Lopez-Santos, L. Martinez-Salamero, G. Garcia, H. Valderrama-Blavi, and T. Sierra-Polanco, "Robust sliding-mode control design for a voltage regulated quadratic boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2313-2327, Apr. 2015.

[53] S. H. Chincholkar, W. Jiang, and C.-Y. Chan, "A normalized output error-based sliding-mode controller for the DC-DC cascade boost converter," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 67, no. 1, pp. 92-96, Jan. 2020.

[54] S. C. Tan, Y. M. Lai, M. K. H. Cheung, C. K. Tse, "On the practical design of a sliding mode voltage controlled buck converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 425-437, Mar. 2005.

[55] V. M. Nguyen and C. Q. Lee, "Tracking control of buck converter using sliding-mode with adaptive hysteresis," *IEEE Electron. Specialists Conf.*, vol. 2, pp. 1086-1093, Jun. 1995.

[56] S. C. Tan, Y. M. Lai, C. K. Tse, and M. K. H. Cheung, "Adaptive feedforward and feedback control schemes for sliding mode controlled power converters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 182-192, Jan. 2006.

[57] P. Mattavelli, L. Rossetto, G. Spiazzi, and P. Tenti, "General-purpose sliding-mode controller for dc-dc converter applications," in *Rec. IEEE Electron. Specialists Conf. (PESC'93)*, pp. 609-615, Jun. 1993.

[58] F. Mendez-Diaz, B. Pico, E. Vidal-Idiarte, J. Calvente, and R. Giral, "HM/PWM seamless control of a bidirectional buck-boost converter for a photovoltaic application," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2887-2899, 2019.

[59] M. A. Qureshi, I. Ahmad, and M. F. Munir, "Double integral sliding mode control of continuous gain four quadrant quasi-Z-source converter," *IEEE Access*, vol. 6, pp. 77785-77795, 2018.

[60] H. N. Jazi, A. Goudarzian, R. Pourbagher, and S. Y. Derakhshandeh, "PI and PWM sliding mode control of POESLL converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 53, no. 5, pp. 2167-2177, Mar. 2017.

[61] S. C. Tan, Y. M. Lai, and C. K. Tse, "Indirect sliding mode control of power converters via double integral sliding surface," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 600-611, Mar. 2008.

[62] S. C. Tan, Y. M. Lai, and C. K. Tse, "A unified approach to the design of PWM based sliding mode voltage controller for basic DC-DC converters in continuous conduction mode," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 8, pp. 1816-1827, Aug. 2006.

[63] T. Siew-Chong, Y. M. Lai, K. T. Chi, M. Luis, and W. Chi-kin, "A fast-response sliding-mode controller for boost-type converters with a wide range of operating conditions," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 3276-3286, 2007.

[64] S. C. Tan, Y. M. Lai, and C. K. Tse, "Implementation of pulse-width based sliding-mode controllers for boost converters," *IEEE Power Electron Lett.*, vol. 3, no. 4, pp. 130-135, Dec. 2006.

[65] S. C. Tan and Y. M. Lai, "Constant-Frequency Reduced-State Sliding Mode Current Controller for Cuk Converters," *IET Power Electronics*, Vol. 1, No.4, 2008, pp. 466-477.

[66] S. C. Tan, Y. M. Lai, C. K. Tse, and L. Martinez-Salamero, "Special family of PWM-based sliding-mode voltage controllers for basic DC-DC converters in discontinuous conduction mode," *IEE Proc. Electr. Power Appl.*, vol. 1, no. 1, pp. 64-74, Jan. 2007.

[67] H. Sira-Ramirez and M. Ilic, "A geometric approach to the feedback control of switch mode DC-to-DC power supplies," *IEEE Trans. Circuits Syst.*, vol. 35, no. 10, pp. 1291-1298, Oct. 1988.

[68] H. Sira-Ramirez, "A geometric approach to pulsewidth modulated control in nonlinear dynamical systems," *IEEE Trans. Autom. Contr.*, vol. 34, no. 3, pp. 184-187, Feb. 1989.

[69] V. M. Nguyen and C. Q. Lee, "Indirect implementations of sliding mode control law in buck-type converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC'96)*, Mar. 1996, vol. 1, pp. 111-115.

[70] J. Mahdavi, A. Emadi, and H. A. Toliyat, "Application of state-space averaging method to sliding-mode control of PWM DC/DC converters," in *Proc. IEEE Conf. Ind. Appl.* (IAS'97), Oct. 1997, vol. 2, pp. 820-827.

[71] J. Mahdavi, M. R. Nasiri, A. Agah, and A. Emadi, "Application of neural networks and state-space averaging to a DC/DC PWM converter in sliding-mode operation," *IEEE/ASME Trans. Mechatron.*, vol. 10, no. 1, pp. 60-67, Feb. 2005.

[72] M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*, 2nd ed., John Wiley & Sons, Chichester, West Sussex: United Kingdom, 2016.

[73] H. K. Khalil, *Nonlinear Systems*, 3rd ed., Prentice-Hall, Upper Saddle River: NJ, 1996.

[74] H. Al-Baidhani, M. K. Kazimierczuk, and Alberto Reatti, "Nonlinear Modeling and Voltage-Mode Control of DC-DC Boost Converter for CCM," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1-5.

[75] H. Al-Baidhani, M. K. Kazimierczuk, and R. Ordóñez, "Nonlinear Modelling and Control of PWM DC-DC Buck-Boost Converter for CCM," *Proceedings of the 44th Annual Conference of the IEEE Industrial Electronics Society (IECON-2018)*, 2018, pp. 1374-1379.

[76] A. Reatti, F. Corti, A. Tesi, A. Torlai, and M. K. Kazimierczuk, "Effect of Parasitic Components on Dynamic Performance of Power Stages of DC-DC PWM Buck and Boost Converters in CCM," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1-5.

[77] H. Al-Baidhani, M. K. Kazimierczuk, T. Salvatierra, A. Reatti, and F. Corti, "Sliding-Mode Voltage Control of Dynamic Power Supply for CCM," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1-5.