Defects induced by solid state reactions at the tungsten-silicon carbide interface

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Defects introduced by the solid state reactions between tungsten and silicon carbide have been studied using deep level transient spectroscopy (DLTS) and Laplace DLTS. W/4*H*-SiC Schottky barrier diodes were isochronally annealed in the 100–1100 °C temperature range. Phase composition transitions and the associated evolution in the surface morphology were investigated using x-ray diffraction (XRD) and scanning electron microscopy (SEM). After annealing at 1100 °C, the $E_{0.08}$, $E_{0.15}$, $E_{0.23}$, $E_{0.34}$, $E_{0.35}$, $E_{0.61}$, $E_{0.67}$, and $E_{0.82}$ defects were observed. Our study reveals that products of thermal reactions at the interface between tungsten and n-4*H*-SiC may migrate into the semiconductor, resulting in electrically active defect states in the bandgap. *Published by AIP Publishing*. https://doi.org/10.1063/1.5011242

INTRODUCTION

Tungsten is a contact metal of choice on silicon carbide for high temperature and high voltage electronic applications.[1] This has been attributed to the exceptional chemical, mechanical, and physical properties of the metal and the superior semiconductor and physical properties of SiC. In a comparative study of metal contacts on 4*H*-SiC, Gora *et al.*[2] concluded that the W and 4*H*-SiC couple would be the most suitable for fabrication of devices that can operate at high temperatures. 4*H*-SiC has a bandgap of approximately 3.3 eV at room temperature, and tungsten has the highest melting point of all elemental metals. Furthermore, the W/4*H*-SiC junction has been shown to have remarkable junction properties and great potential in the implementation of high voltage microelectronic devices.[1,3]

In miniature microelectronic devices, the influence of ultra-low contamination from formation of silicides and carbides on metal-semiconductor structures and interfaces becomes highly critical to device fabrication yield and determines their lifetime.[4] In silicon, it has been shown that tungsten contamination can be introduced during dopant implantation processes.[5] The related defects severely degraded device properties.[6] Another possible source of contamination is from the migration of device contact metals and their related compounds during subsequent device processing steps or operation in high temperature environments. The impact of such processes in the bandgap of devices remains largely uninvestigated mainly because of the small scale and slow nature of their reaction kinetics. Deep level transient spectroscopy is one of the most sensitive techniques, which is capable of detecting impurities at such low concentrations and measures their electronic properties. Laplace-deep level transient spectroscopy (L-DLTS) offers up to an order of magnitude higher resolution than conventional DLTS and is therefore efficient in the analysis of very low defect concentrations.[7] In 20 Ω cm silicon, Laplace-DLTS can detect impurities at one part per trillion.[8,9]

Several authors have reported on the metallurgical, electrical characteristics, structural composition, and interface properties of tungsten contacts on silicon carbide.[2,10–16] Using different techniques, it has been proven that interfacial reactions between tungsten and silicon carbide result in the formation of different phases of tungsten carbides and tungsten silicides at particular temperatures depending on the inertness of the environment. Rogowski and Kubaik[10] showed that one of the products, i.e., WC, migrated and reached the 4*H*-SiC substrate at elevated temperatures. Similar results were reported by Goesmann and Schmid-Fetzer.[11] In all these reports, there is not a direct correlation between the physical changes at the interface and the resulting electrical characteristics.

Thabethe *et al.*[17] showed inter-diffusion of W into silicon carbide during thermal treatment in argon in the 700–1000 °C temperature range. At present, the tungsten diffusion coefficient and tungsten diffusion models are not known in silicon carbide. Most models that have been developed for diffusion in several semiconductors are based on the interstitial-substitutional mechanisms, a collective term for the dissociative and the kick-out mechanism. Another model that exists is the defect generation–recombination. Evidence of the kick-out mechanism in silicon carbide has been demonstrated both experimentally and using *ab initio* studies for implanted boron.[18] Luca *et al.*[4] suggested that tungsten, owing to its unique physical properties, used two different diffusion models unlike other metals and proposed simultaneous diffusion of interstitial W atoms and W-Si paired atoms.

This work shows that migration of by-products emanating from thermal reactions at the W/4*H*-SiC interface into silicon carbide is accompanied by lattice distortions which result in the formation of electrically active defect levels in the bandgap. We tracked the interfacial reactions and the various silicide phases and carbide phases that were produced at the interface and surface morphological variations during isochronal annealing. Consequently, we correlated the resulting modifications with the measured electrical characteristics of W/4*H*-SiC Schottky barrier diodes.

EXPERIMENTAL PROCEDURE

Nitrogen doped n-type 4*H*-SiC wafers supplied by Cree Inc. were used. The active layers as specified by the supplier were an epi-layer with a net doping density $7 \times 10^{15}\,\mathrm{cm}^{-3}$ grown on a highly doped substrate of $10^{18}\,\mathrm{cm}^{-3}$. Smaller samples of the wafers were cleaned through a two-step procedure of degreasing by boiling trichloroethylene, acetone, and methanol for 5 min each followed by a 1 min etch in 5% hydrofluoric acid. After each step, the samples were rinsed in de-ionized water with a resistivity of 18.2 MΩ cm. A 3000 Å Ni ohmic contact was deposited by resistive evaporation on the sample backside in an Edwards Auto 306 vacuum chamber. Thereafter, the samples were annealed at 950 °C in argon.

After repeating the degreasing and etching procedure at room temperature in an ultrasonic bath, the samples were mounted in a magnetron sputter system and rf etched for 5 min to make sure that the surface was clean at the atomic level. Circular Schottky contacts of 0.6 mm diameter were deposited by dc magnetron sputtering at room temperature from a tungsten metal target through a metal contact mask. The deposition was carried out under a dc power of 1000 W, an Ar pressure of 2×10^{-2} mbar, and a deposition rate of approximately 2.3 nm s^{-1}. Contact quality was evaluated using *I-V* and *C-V* measurements.

Using a quartz tube with flowing Ar, the samples were isochronally annealed for 15 min in the 100–1100 °C range in 100 °C incremental steps. DLTS spectra were recorded at a scan rate of 2 K/min in the 15–360 K range, and Arrhenius analysis was done according to the following equation:[19]

$$e_n = \sigma_n \langle v_{th} \rangle \frac{g_o}{g_1} N_c \exp\left(-\frac{E_c - E_t}{k_B T}\right). \quad (1)$$

Equation (1) gives the emission rate as a function of temperature T, where v_{th} is the thermal velocity of electrons, $(E_{\mathrm{c}} - E_{\mathrm{t}})$ is the activation energy, N_{c} is the density of conduction band states, g_0 and g_1 are the degeneracy terms referring to the states before and after electron emission, and k_{B} is the Boltzmann constant. The apparent capture cross section σ_{n} is assumed to have a T^2 dependency and hence the log (e_{n}/T^2) versus $1000/T$ plots. L-DLTS was used to investigate the fine structure of all defects observed. The L-DLTS system used was capable of collecting and averaging up to 100 000 transients, each with up to 32 000 points. It used three different mathematical routines to perform Tikhonov's regularization and inverse Laplace transforms to give a spectral distribution function with delta-like peaks that represent each extracted emission rate.

Wide angle X-ray diffraction analysis was performed using a Bruker D8 Advanced diffractometer XRD system with a Cu Ka radiation source (1.54184°A) to identify any phase transformations before and after each annealing step. The 2θ radiation source angle was maintained at 20°, and the detector angle scan was from 20° to 120°. Scanning electron microscopy was carried out using a Zeiss Ultra Plus FEG-SEM to study the evolution of the surface morphology during annealing.

RESULTS

Current voltage (*I-V*) and capacitance-voltage (*C-V*) results

I-V and *C-V* measurements were carried out on the devices as-deposited and after every annealing step. This was done in-order to evaluate the quality of the underlying layers and the device rectification properties. The *C-V* data were also used to monitor the carrier concentration so that the accuracy of the DLTS measurements was not compromised through carrier removal. Changes brought about by the annealing would be noted in the process. Parameters for the *I-V* rectification process were determined using the thermionic emission model, which was assumed to be the dominant current transport mechanism across the Schottky barrier.[20] These were ideality factor n, *I-V* barrier height (ϕ_{IV}), and series resistance (R_{s}). *C-V* data were analysed using the Schottky Mott theory and were used to determine the *C-V* barrier height (ϕ_{CV}) and carrier concentration (N_{D}).[20] A summary of the parameters obtained is listed in Table I. These data are representative of a large number of samples that were measured.

As the isochronal annealing steps progressed, the *C-V* characteristics remained almost unchanged with a diminutive decrease in the ideality factor until 700 °C where there is a spike in the *C-V* barrier height accompanied by an increase in the zero bias capacitance. Thereafter, there is also a gradual increase in the *C-V* barrier height until 1100 °C. There is an increase in Φ_{IV} for annealing between 700 and 1000 °C. Also, a dip in the value of n is observed at 900 °C. At 1100 °C, a sharp decrease in the *I-V* barrier height and an increase in the *C-V* barrier height are noted. There is a major degradation in the diode thermionic emission characteristics at the 1100 °C annealing step with an increase in n and R_{s} and a sharp decrease in the *I-V* barrier height and N_{D}. In all, the *I-V* characteristics showed a gradual trend towards ohmic behavior and a marked increase in reverse leakage current with increasing annealing temperature. The quality of the devices was appropriate for DLTS measurements. DLTS measurements were performed to determine if there is a correlation between the observed *I-V* and *C-V* characteristics and any changes in the defect levels detected in the bandgap.

Isochronal annealing

After annealing at below 300 °C, the DLTS spectra showed only the native defects and sputter deposition induced damage. At 300 °C, the damage due to sputter

TABLE I. Diode *I-V* and *C-V* parameters obtained from as-deposited and annealed W/n-4*H*-SiC Schottky barrier diodes.

Temperature	n	R_{s} (Ω)	$N_{\mathrm{D}} \times 10^{15}$ (cm^{-3})	Φ_{IV} (eV)	Φ_{CV} (eV)
As deposited	1.58	27.3	7.8	0.89	0.57
700	1.10	20.9	5.9	0.82	1.87
800	1.15	60.3	7.7	0.90	1.15
900	1.10	23.7	7.4	0.97	1.32
1000	1.22	24.5	7.3	1.03	1.55
1100	2.37	154.4	6.7	0.82	1.87

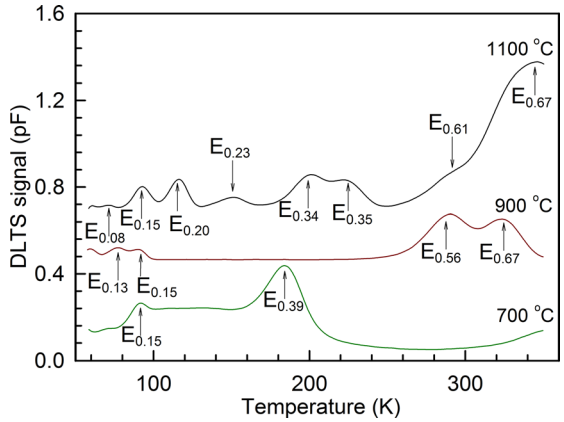

FIG. 1. DLTS spectrum of as-W/4*H*-SiC Schottky barrier diodes observed during isochronal annealing recorded at a quiescent reverse bias (V_R) of −2 V, a filling pulse of 0.5 V, and a pulse width (t_p) of 1 ms.

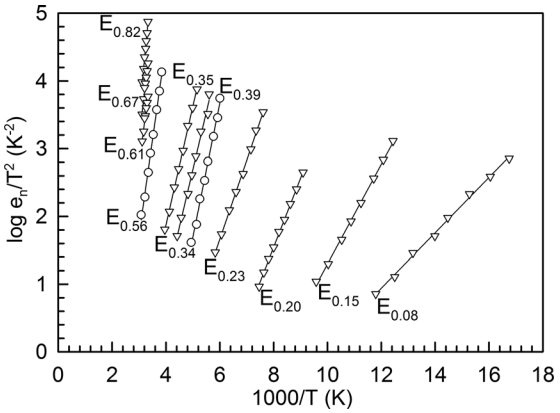

FIG. 2. Arrhenius plots of defects observed during isochronal annealing of W/4*H*-SiC Schottky barrier diodes in the 100–1000 °C temperature range.

deposition annealed out. A detailed account of the sputter deposition induced defects, and their thermal treatment is given elsewhere.[21] Annealing heals pre-existing defects and restores lattice structural order.[22] Figure 1 shows the DLTS spectra obtained after annealing at 700, 900, and 1100 °C. The titanium impurity related $E_{0.15}$ is observed on the three spectra, and the $E_{0.67}$ (Z_1/Z_2) is visible on the 900 and 1100 °C spectra but not on the 700 °C spectrum.[23] The Z_1/Z_2 defect is arguably the most important defect in 4*H*-SiC, and several models have been put forward to describe it with some controversy among researchers. These include the divacancy model, the nitrogen related defect model, and the Ni-carbon interstitial complex model.[24] All the defect properties and Arrhenius plots obtained in this work are shown in Table II and Fig. 2, respectively. The $E_{0.39}$ starts to appear at 400 °C and gradually increases in size as the $E_{0.67}$ decreases in size until it goes completely beyond detection at 700 °C. At this point (700 °C), the $E_{0.39}$ is at the highest concentration. A concurrent increase in zero bias capacitance and *C-V* barrier height is also noticed at 700 °C as stated in the previous section on *I-V* and *C-V* results. At 800 °C, the $E_{0.39}$ was not detectable.

The $E_{0.56}$ appears after annealing at 900 °C. At 1000 °C, $E_{0.20}$ and $E_{0.61}$ were observed in addition to the $E_{0.67}$ defect.

TABLE II. Electronic properties of defects in W/n-4*H*-SiC Schottky barrier diodes observed during isochronal annealing in the 100–1000 temperature range at $V_R = -2.0$ V, $V_P = 0.5$ V, and $t_p = 1$ ms.

Defect label	Energy (meV)	σ_n (cm^{-2})
$E_{0.08}$	81.2	2.7×10^{-18}
$E_{0.13}$	130	2.8×10^{-15}
$E_{0.15}$	146	3.3×10^{-16}
$E_{0.20}$	202	1.2×10^{-15}
$E_{0.23}$	231	6.3×10^{-17}
$E_{0.34}$	336	1.7×10^{-16}
$E_{0.35}$	348	4.2×10^{-17}
$E_{0.39}$	392	4.2×10^{-14}
$E_{0.56}$	559	1.5×10^{-15}
$E_{0.61}$	613	9.2×10^{-16}
$E_{0.67}$	672	3.0×10^{-15}
$E_{0.82}$	818	2.2×10^{-13}

Then, at 1100 °C, the $E_{0.08}$, $E_{0.15}$, $E_{0.20}$, $E_{0.23}$, $E_{0.34}$, $E_{0.35}$, $E_{0.61}$, and $E_{0.67}$ were observed on the spectrum as shown in Fig. 1. Figure 3 shows Laplace DLTS spectra used to obtain the properties of the $E_{0.61}$, $E_{0.67}$, and $E_{0.82}$ defects. The $E_{0.61}$ has been reported as the donor level of the Z_2 center.[25]

We propose that the $E_{0.08}$, $E_{0.20}$, $E_{0.23}$, $E_{0.34}$, and $E_{0.35}$ result from the thermal treatment as their introduction does not appear to be related to the Z_1/Z_2 and other native defects. In-order to determine the spatial distribution of the defects, the fixed bias variable pulse method was used. Depth profiling was done based on the correction proposed by Zohta and Watanabe[26] which gives a defect concentration N_T for an applied DLTS pulse V as

$$\frac{N_T(x_m - \lambda_m)}{N_D(x)} = \frac{1}{\left(1 - \frac{\lambda}{x}\right)^2 - \left(\frac{x_p - \lambda_p}{x}\right)^2} \cdot \frac{2\Delta C}{C}, \quad (2)$$

where ΔC is the change in capacitance due to the pulse (at $t = 0$ just after pulsing), x is the width of the depletion layer ($x = z + \lambda$), and z is a distance measured from the surface into the semiconductor depletion width. The defect levels in the depletion width ($0 \le z \le x$) are empty in the layer $0 \le z \le x\text{-}\lambda$, and $x\text{-}\lambda$ is the plane where the deep levels cross the bulk Fermi level. The subscript p represents variations during the pulse and

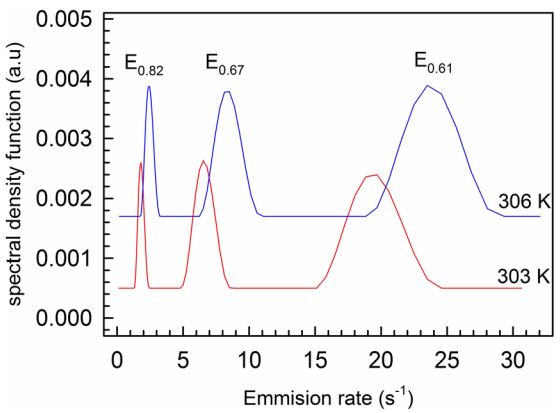

FIG. 3. Laplace DLTS spectrum showing some of the defects observed after annealing W/4*H*-SiC Schottky barrier diodes at 1100 °C.

$$x_m - \lambda_m = \frac{1}{2}\left[(x - \lambda) + (x_p - x_\lambda)\right]. \quad (3)$$

A detailed explanation of the method is given in Ref. 26. We used this method because it has been shown to give a true defect concentration and eliminate limitations of other simpler methods in terms of accuracy. Profiling of the depth distribution of the defects was done at a fixed reverse bias of −2 V. Depth profiles of the $E_{0.20}$, $E_{0.34}$, and $E_{0.35}$ are shown in Fig. 4. The depth profile of the $E_{0.23}$ is not shown because it appeared to be the surface state related due to the inconsistent L-DLTS spectra with multiple peaks. The $E_{0.08}$ was of a very small defect concentration and is also not shown. A comparison of the depth profiles in Fig. 4 shows a similar trend with the concentration that significantly reduces at approximately 0.31 μm.

X-ray diffraction

Tungsten is metastable and undergoes various eutectic reactions with both silicon and carbon during thermal treatment.[27,28] Figure 5 shows the XRD patterns for the W/4*H*-SiC samples before and after annealing in Ar. The as-deposited pattern contained a WO_3 (−1 −1 1) peak at position 30.4°, a SiC (−1 −1 1) peak at 35.7°, and a W (1 1 0) peak at 40.3°. The stability of these phases formed on deposition is a function of kinetics.[29] Previous depositions of tungsten on silicon carbide have also shown trace amounts of tungsten oxide.[16] The oxide could originate from natural oxidation in air as the samples are transferred from the deposition system and between measuring systems. Annealing at 700 °C led to the emergence of two additional W phases (1 0 2) and (2 2 0) at positions 73.2° and 87.4°. At 700 °C, W starts forming the most thermodynamically stable phases. The material becomes more crystalline as evidenced by the narrowing width and the increasing intensity of the W peak at 40.3°. Formation of silicides and carbides were observed, showing that a reaction between W and SiC had taken place. The resulting phases were W_5Si_3 (4 0 0), SiO_2 (2 1 1), WC (1 1 0), and W_2C (2 2 0) at positions 37.4°, 60.4°, 70.5°, and 93.7°, respectively.

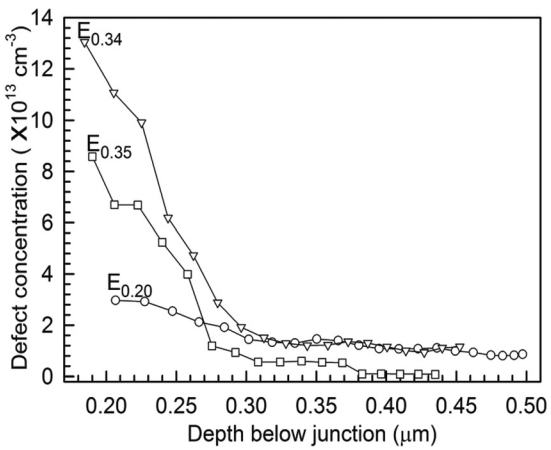

FIG. 4. Depth and concentration of defects observed in 4*H*-SiC Schottky barrier diodes after annealing at 1100 °C.

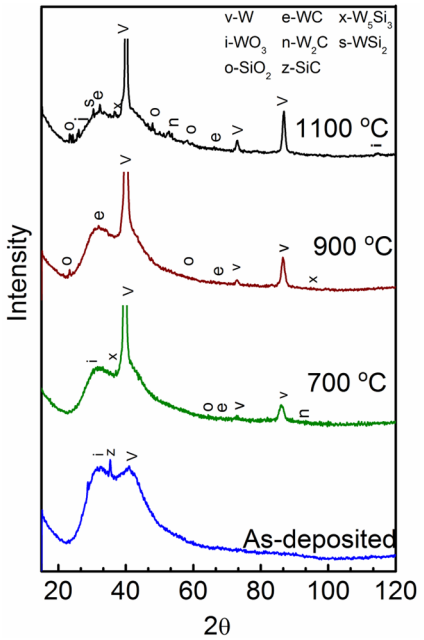

FIG. 5. X-ray diffractograms of the as-deposited W/4*H*-SiC sample and after annealing at 700, 900, and 1100 °C in Ar for 15 min (The tungsten (1 1 0) peak has been cut to magnify other smaller peaks at 700, 900, and 1100 °C).

After annealing at 900 °C, additional SiO_2 (1 0 0) and WC (1 0 0) peaks were observed at positions 23.6° and 36.4°. The formation of these phases was an indication of further reaction of W and WO_3 with SiC. The samples annealed at 1100 °C had the following additional peaks: WO_3 (2 2 1), SiO_2 (3 2 7), W_2C (1 0 2), and WO_3 (5 2 1) at position 24.3°, 47.9°, 52.5°, and 113.0°, respectively. Formation of W_2C confirmed further reaction between W and C.

Scanning electron microscopy

In a previous study where inter-diffusion of tungsten into silicon carbide was confirmed, SEM analysis showed associated morphological changes in the tungsten surface.[17] The SEM micrographs of W deposited on 4*H*-SiC before and after annealing at 700, 900, and 1100 °C showing morphological evolution are depicted in Fig. 6. The as-deposited sample shows a continuous tungsten surface. An uneven patterning is observed on the tungsten film. This could be resulting from the rf etching of 4*H*-SiC which was used to ensure that the surface was atomistically clean before tungsten deposition. It can be seen that the whole surface is covered with the W film.

Annealing at 700 °C resulted in a pronounced change in the surface structure, with the continuous film breaking up into evenly distributed smaller grains of no preferred orientation. The morphological evolution after annealing at 800 and 900 °C shows agglomeration with what appears to be a parasitic growth of larger grains from the smaller ones. Larger crystals appear stacked on the smaller ones, and their formation may represent phase transformations to form other phases as observed in the XRD results in the previous section (Fig. 5). A similar rough surface was observed on a W\6*H*-SiC interface where diffusion was confirmed using Rutherford

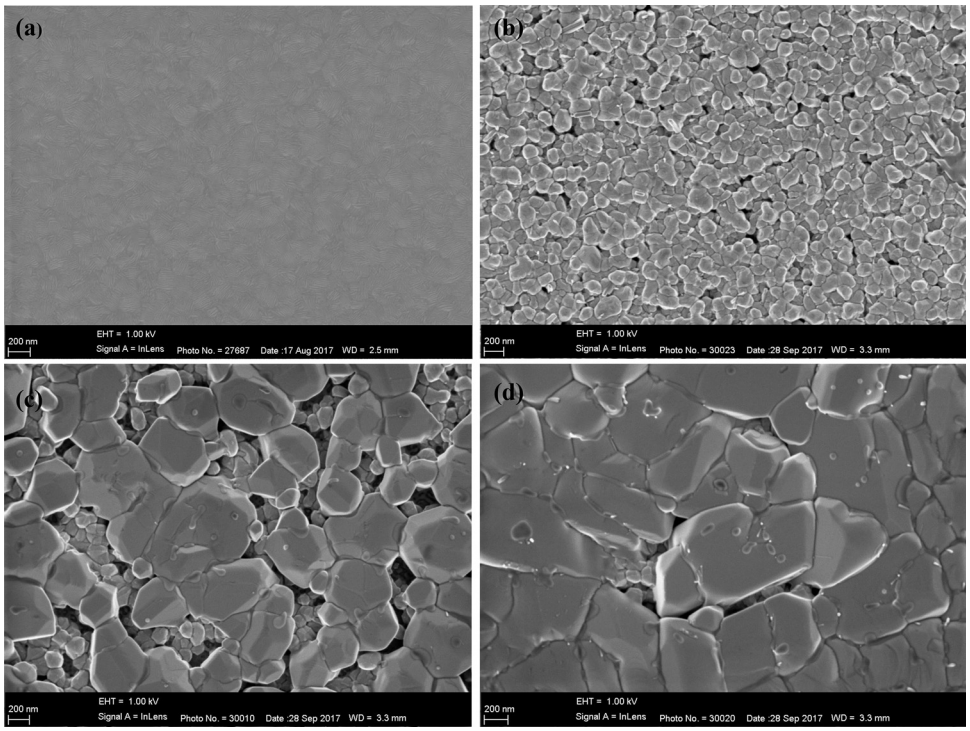

FIG. 6. SEM images for (a) as-deposited W/4*H*-SIC Schottky barrier diodes on the tungsten metal surface. (b)–(d) were obtained after annealing in argon for 15 min at 700, 900, and 1100 °C, respectively.

backscattering spectroscopy after annealing, and it was attributed to stress assisted growth.[17]

Annealing at 1100 °C [Fig. 6(d)] resulted in a larger crystal with some occasional groves in between them. Cavities were also observed and reported when W diffused into Si.[4]

DISCUSSION

The gradual decrease in the concentration of the $E_{0.69}$ (Z_1 center) with the introduction of the $E_{0.39}$ after annealing between 400 and 600 °C suggests that these levels are possibly related or emanating from the same defect. The spike in the *C-V* barrier height at 700 °C was accompanied by the $E_{0.69}$ (Z_1 center) going below the detection limit of DLTS detection and the appearance of the $E_{0.39}$ on the DLTS spectrum (Fig. 1). Ashgar *et al.*[30] also observed the Z_1 center going below detection after annealing at 600 °C for 30 minutes. They attributed the suppression to the annealing out of the silicon vacancy (Z_2) and the capture of the Z_1 by inactive sites such as dislocations and micropipes. Their assertions, however, lacked a plausible explanation on how this related to the nature of the defect or the physical mechanism around the capture.

The Z_1/Z_2 centers are made up of two negative U centers having inverted level ordering.[31] Negative U behavior is when one defect traps two electrons simultaneously with the second one being strongly bound than the first.[24] Processes of the donor level capturing and the acceptor level emitting can be described by the following equations:[32]

$$Z_i^+ + e^- \leftrightarrow Z_i^0, \tag{4}$$

$$Z_i^0 + e^- \leftrightarrow Z_i^-, \tag{5}$$

where the subscript $i = 1$ or 2.

From the above equations, it is found that peaks would be anticipated to appear on the spectrum in a conventional DLTS scan, two for each negative U center. According to Hemmingsson *et al.*,[32] this is not the case because the capture of the binding strengthens when the two electrons are captured by the negative U center during each filling pulse and cannot be subsequently released during a pulse relaxation. In our case, this explains the inability to detect the Z_1 at 700 °C but does not explain concurrent detection of the $E_{0.39}$.

Pulse properties and pulsing conditions have been shown to play a major role on the results of DLTS measurements in negative U centers.[33] The $E_{0.39}$ may result from the donor level of the Z_1 negative U center. This is because we used a lower filing pulse (2.5 V) and shorter pulse length (1 ms) than previous authors who did not see the donor level. The pulse is only long enough to fill the donor defect level with one electron altering the capture cross section in the process. As a result, the defect will not capture the second electron easily. A similar result was observed with the ES1 defect in GaN by Auret *et al.*[34] which is also a negative U center. The DLTS pulse is therefore only sufficient for reaction (4) in an emission of the poorly bound electron only. Gradual introduction of the $E_{0.39}$ seems to point out that the thermal treatment actually influences the first electron to be more loosely bound.

Based on these observations, changes observed in the bandgap below 700 °C can therefore not be correlated with the phase transitions at the surface but can be linked to the Z_1/Z_2 defects undergoing changes during thermal treatment. Although the XRD results verified that there were phase reactions at the interface, by revealing the presence of WC and W_2C and WSi_2, a similar defect behaviour of the Z_1 was observed using gold and nickel contacts on 4*H*-SiC[30], and

therefore, all the observed changes in defects here cannot be correlated with W/4*H*-SiC interfacial reactions.

In our experiments, no new defects were observed after annealing at 800 °C. Lundberg *et al.*[16] also saw that there was no reactions between tungsten and silicon carbide below 800 °C even after annealing for 2 h. However, several defects were observed in the bandgap after thermal treatment in the 900 °C–1100 °C temperature range. Laplace DLTS depth profiles of the $E_{0.23}$, $E_{0.34}$, and $E_{0.35}$ defects, induced by annealing at 1100 °C, were consistent and similar, showing that they might have emanated from the same process. We speculated that they were created by inter-diffusion of a reaction product formed at the metal-semiconductor interface, which was probably a carbide, silicide, or oxide detected by the XRD. According to Kananakova-Georgieva *et al.*,[15] there is a breaking of Si-C bonds, so that the tungsten interacts with liberated carbon atoms, forming tungsten carbide, and with silicon, yielding tungsten silicide.

From the depth profiles for a 15 min annealing interval, the average diffusion rate of the thermal reaction product would be approximately $5.71 \times 10^{-10}\,\mu\text{m s}^{-1}$. The depth profiles in Fig. 4 may be for defects introduced by the diffusion as was observed using time of flight secondary ion mass spectroscopy (ToF-SIMS) by Rogowski and Kubaik[10] after annealing above 1200 °C. We detected it after thermal treatment at a lower temperature than Rogowski and Kubaik because of the high resolution of Laplace DLTS. In the same temperature range in which we carried out DLTS measurements, it has been showed that oxygen related defect centres in 4*H*-SiC occupy shallower levels than what we have observed.[35] We therefore rule out produced oxides as causatives of the observed defects. From the SEM micrographs, the agglomeration of crystals and formation of cavities are consistent with previous morphological observations where tungsten migrated into Si and SiC.[17]

The introduction of the defects after annealing at 1100 °C was accompanied by a major deterioration of the device thermionic emission *I-V* characteristics and modifications in the interfacial composition. Traps act as recombination centers and trapping electrons, and this influences the observed *C-V* and *I-V* characteristics, resulting in poorer diode characteristics. A similar result has also been observed for annealing Al contacts on 4*H*-SiC.[36] The various silicide and carbide phases produced also introduce in-homogeneities in the barrier which also impacts diode *I-V* characteristics.[37] With respect to the nature of the defects observed, we propose that they are interstitials formed by the tungsten occupying vacant sites they encounter during diffusion through the lattice. This is known as the dissociative diffusion mechanism.[38]

CONCLUSIONS

W/n-4*H*-SiC Schottky barrier diodes were fabricated using dc magnetron sputter deposition. Thermal annealing of the SBDs in the 400–700 °C temperature range resulted in changes in *I-V* and *C-V* characteristics which we attributed to the negative U behaviour of the Z_1 center ($E_{0.67}$). The $E_{0.69}$ was undetectable at 700 °C, whereas the $E_{0.39}$ was observed which we speculated to be the shallow donor level of the Z_1 rendered observable by the DLTS pulsing conditions. Furthermore, the results also show that thermally induced physical changes to contacts resulted in the modification of the electronic properties of the W/4*H*-SiC devices. From the depth profiles, it appeared that out-diffusion of silicides and carbides produced during the thermal reactions and phase transitions above 800 °C at the W/4*H*-SiC interface migrates into the silicon carbide, introducing electrically active defects ($E_{0.23}$, $E_{0.34}$, and $E_{0.35}$) in the bandgap. The introduction of the defects was detected at relatively lower annealing temperatures compared to other techniques used in previous studies because of the high sensitivity of Laplace-DLTS. We conclude that exposure of W/4*H*-SiC contacts to temperatures above 800 °C, during operation or thermal treatment, may result in the migration of interfacial reaction products into the semiconductor wafer, contaminating the devices in the process, despite strict cleanliness practice during fabrication. The resulting phase compositions and defects significantly affect the device electrical characteristics.

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