Modelling and Control of a VIENNA Smart Rectifier-I for Wind Power Systems Integrated Under Transient Conditions

Inas M. O. Mohammed[1], Michael Njoroge Gitau[1], Ramesh C. Bansal[2,*] & Kabeya Musasa[3]

[1]Department of Electrical, Electronic and Computer Engineering, University of Pretoria, Pretoria, South Africa

[2]Department of Electrical and Computer Engineering, University of Sharjah, Sharjah, United Arab Emirates

[3]Department of Electrical Power Engineering, Durban University of Technology, Durban, South Africa

*Correspondence to Ramesh C. Bansal email: rcbansal@ieee.org

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Abstract

An improved topology with a fault ride through (FRT) capability when subjected to a DC-link fault-based wind power plant (WPP) employing a Vienna active rectifier-I is proposed in this paper. The proposed system is capable of mitigating fault occurring on the DC-link side using the PWM-controller technique implemented on the Vienna active rectifier. FRT capability analysis is conducted in this paper, simulation results demonstrate the suitability of the control strategy. Actually, use of proposed wind energy conversion unit (WECU) topology has led to the improvement of system stability by maintaining constant output voltage. Furthermore, the WECU integrating Vienna active rectifier-I is also proven as a feasible technology that can be employed in a large-scale WPP or renewable power generations to realize technical and economical efficient grids integration with high voltage direct current (HVDC) transmission systems.

Introduction

Due to the increased demand of electricity nowadays, the world is moving towards the use of renewable energy sources because of high efficiency, resource availability, cost competitiveness and environmental adequateness. In this respect, recent researches have been developed towards the improvement of renewable energy technology [1,2,3]. In fact, for an AC collection grid, each wind energy conversion system (WECS) on a WPP includes: a wind-turbine plus mechanical parts (e.g. gearbox), a generator (e.g. doubly fed induction generator (DFIG), permanent magnet synchronous generator (PMSG), squirrel cage induction generator (SCIG)), and a huge 50- or 60 Hz power transformer including controller circuit. In this paper a wind farm with DC collection grid is considered. For a wind farm employing DC collection grid, the huge power transformers in the WECSs are replaced by the power electronic converters. The power electronic converter is significantly compact and small in size compared to the power transformer of identical features.

Most of studies being done on the design of DC collection grids for wind farm employ the conventional full-bridge active rectifiers as the topology of power converters in WECS. The conventional full-bridge active rectifier contain large numbers of controlled-switches, which increase complexity of controller circuit and affect the system efficiency because of the high switching frequency operation of the controlled switch. The wind DC collection grid in this paper is built out using the parallel connection of Vienna-I active rectifier, and thus reduces the numbers of controlled switches in the power converter compared with conventional active rectifiers.

The DC technology has acquired significant applications in modern distribution systems due to the high penetration levels of DC loads and DC-based distributed generators (DGs) [1]. Unlike conventional AC distribution systems, DC distribution systems have high penetration level of power converters used to interface both DGs and loads [2]. HVDC power transmission and distribution systems have received wide acceptance in power systems and renewable energy resources integration technology. Moreover, DC systems present more advantages over the AC systems. For example, the synchronization of multiple generators, which is flexible because of no frequency sharing than that of AC system, also the absence of reactive power in DC-link increase the system stability [3]. It is also easy to integrate the renewable energy sources into DC grid using simplified control scheme at low cost. As the number of grid-connected wind farms is constantly increasing, the WPPs have to play a considerable function in maintaining the grid stability [4]. This requires that the wind-turbine-generators on wind farm stay connected to the power grid for any fault conditions [3]. The FRT is the capability of WECS to stay connected in short periods of fault conditions. This term can also be used to explain the ability of a wind farm to participate to the voltage stability during grid faults [1]. A WPP generally consists of large number of WECS interconnected together either in series, radial, or series-parallel, and injected to a main bus. The generator in WECS is either the SCIG, mostly used for fixed speed wind-turbine, or a DFIG mostly employed for variable speed wind-turbine (not allow more than 30% speed variation). Fixed speed wind-turbine do not employ power converter in WECS, the control of parameters (e.g. voltage, current, frequency) output of SCIG is done using the STATCOM or FACTS devices installed on the grid side [1]. The drawback of this topology is that no tracking of maximum wind power mechanism is provided. However for the variable speed wind-turbine, power electronic converter is employed in the WECS circuit. DFIG and PMSG are the most considered type of generators for the WECS based variable speed wind-turbine synchronous generators, for many advantages, they can supply constant load for the power consumers, and also can monitoring the power rapidly and flexibly with the help of active power electronic convertors [2, 3]. One of the major challenge in WECS is to handle the discontinuity of wind and to protect the grid stability. The power electronics and energy storage systems are substantial components to maintain continuation of wind power. WECUs are basically grouped into two types.

1. Fixed speed WECU: the wind-turbine with a SCIG.
2. Variable speed WECU: this group is classified into two types:

    (i) PMSG based wind-turbine with a full rating converter.

    (ii) DFIG based wind-turbine with a partial rating converter.

The full rating converters disconnect the synchronous machine speed from the grid frequency and provide adaptable operation over a wide range of speed.

The conventional converters have the following demerits: (i) These are either a buck or a boost converter, (ii) are sensitive to electromagnetic interference (EMI), which reduces the reliability [4, 5]. FRT capability is the ability of WPP to stay connected to the grid while fault is occurring [6,7,8], and the PMSG is a very suitable choice that can integrate with the wind turbine for the following reasons [9].

1. Can ride-through several grid-faults.

2. Able to cut out from the grid immediately in case of a fault and resume rapidly in normal operation after the fault.

3. Has the capability to smooth out the intermittent power fluctuation from the wind.

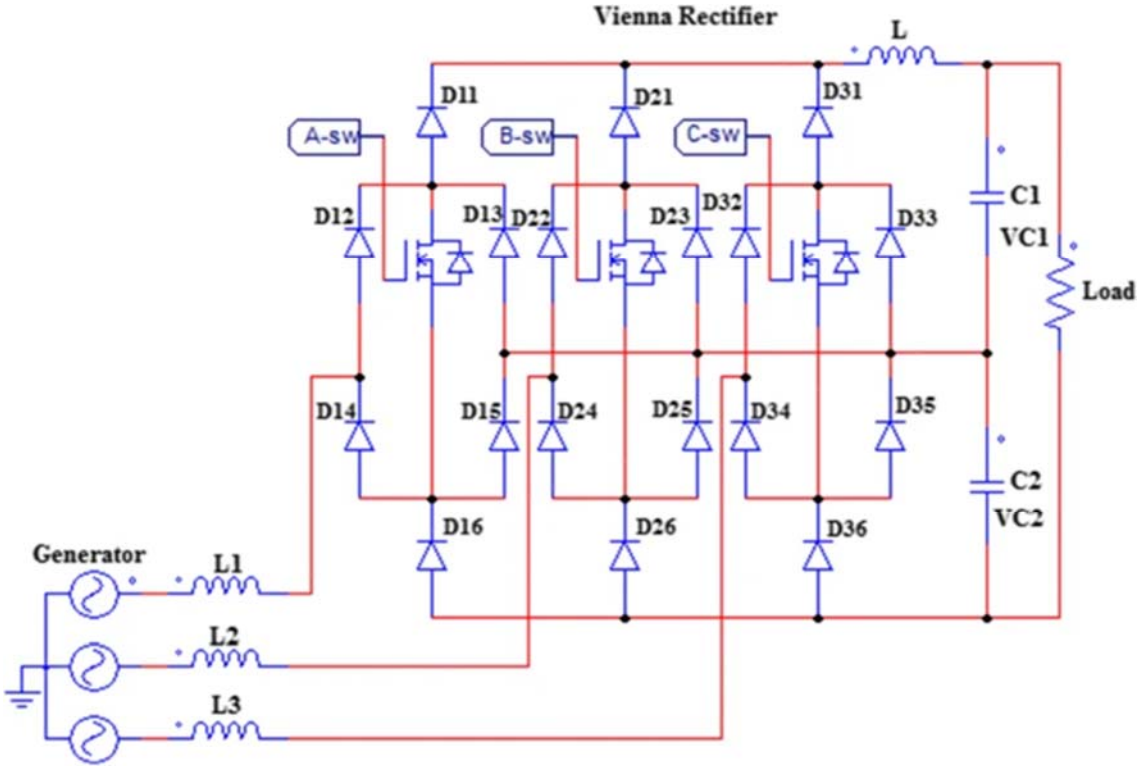


Fig. 1. Three-phase Vienna active Rectifier-I topology

Vienna active rectifier-I, originally introduced by Kolar [10], is one of several types of converters that can be selected as a generator side convertor for wind energy conversion systems. The Vienna active rectifier-I is considered to be a convenient and cost-effective and that recognizes the requirements of power quality and power consistency applications. Also it has less number of active semiconductor devices and less voltage stress compared with conventional rectifiers because the output capacitor is divided in two sections with two equivalent values (C1and C2) as shown in Fig. 1. It has low current total harmonic distortion (THD) and high power density because of three switches which are based on three-level configurations. Therefore, it has been used in several high voltage and high power

applications [10,11,12,13,14]. The schematic diagram of a three-phase Vienna active rectifier-I is shown in Fig. 1.

It consists of three identical power electronic legs, each one connected separately to a phase input. Each power cell includes one active switch (e.g. MOSFET) and six diodes, the output of all the stages are connected to a middle point with output capacitors. The midpoint of the capacitors is practically clamped to a neutral point by connecting it to mid-points of one arm of the diode bridges of all the three phases, by this connection three possibilities of output voltage can be obtained, otherwise it can left free [15,16,17,18]. Vienna active rectifier-I has many advantages over conventional and other types of active rectifiers such as:

1. Capability of double boosting effect because it consists of two inductors, which can improve the rectifier features.

2. Ability of buck-boost operation.

3. Allows transmitting the power to the DC capacitors even if the supply voltage is positive or negative.

4. Involvement of a single switch per power cell that permits to construct a high stable and reliable rectifier.

5. While it is usually used for a three-phase rectification, it can also be used for a single phase applications.

6. Ability of obtaining a two DC-output voltages so that DC-ripples decrease for a given capacitor value.

7. It has the possibility of continuous current and power factor correction operation modes.

However, the disadvantage of using this topology is the difficulty of implementing two inductors [19]. Remaining part of this article is organized as follows. “Modelling and Control of a Vienna Active Rectifier-I” presents modelling and control of Vienna active rectifier-I including rectifier analysis and design of the rectifier input side filter. The AC-bus controller design including design equations and investigation for stability using bode plots have been presented in details in “Design Criteria of the Rectifier Controller”. “Fault Effect Elimination and Analysis” discusses the fault effect elimination and analysis which discusses the type of connection and the controller that has been used for ride through the fault. Simulation results and discussions are presented in “Simulation Results and Discussions” Conclusion of the paper is presented in “Conclusion”.

Modelling and Control of a Vienna Active Rectifier-I

The Rectifier Analysis

The converter topology has been shown in Fig. 1. There are three levels of output voltage, V_{C1} and V_{C2} each is half of the total output voltage. And the third level is the total (V_{C1} + V_{C2}) and should be greater than the maximum supply voltage. It is a boost converter, because

the switching frequency is too high compared with the supply frequency, and the output voltage is always greater than the input voltage. The converter injects ripple in the generator, so ripple filter should be considered in the converter input side design. The operation details of the considered converter have been explained in [11,12,13]. It consists of three active switches (IGBT or MOSFET) and eighteen diodes. The control of the three switches ensures sinusoidal waves input current and desired balanced output DC voltage. The output voltage of the considered rectifier depends on the polarity of the input AC current as well as the switching states [12, 19,20,21].

Filter Design

A filter must be added in the converter input side to attenuate the current harmonics that are produced by the switching converter. The converter injects the input current i_g into the power source V_g as shown in Fig. 2.

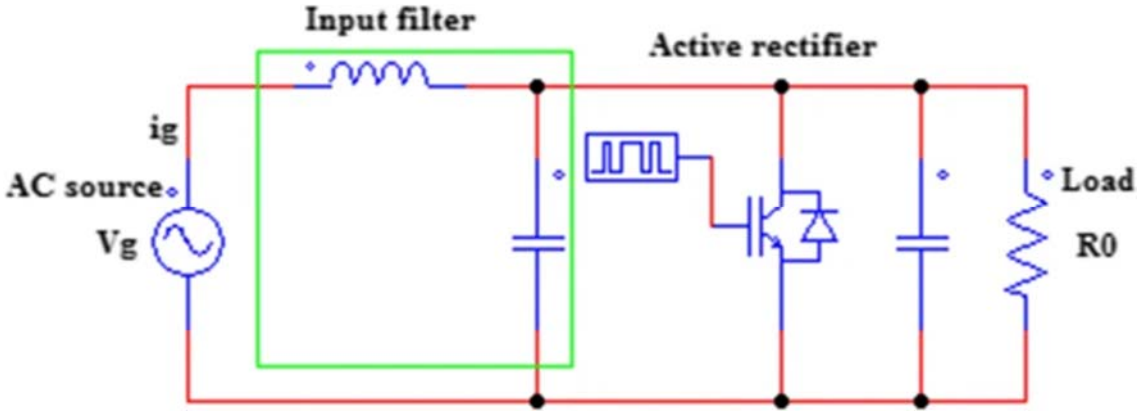


Fig. 2. AC/DC Boost converter circuit [22]

The filter also attenuates the EMI and hence enhances the system stability by protecting the converter from transient voltages and currents [22].

Inductor Design

Inductors are connected in series with a converter input side and can be designed using Eq. 1.

$$L = \frac{V_{in}(V_{out} - V_{in})}{\Delta I_L * f_{sw} * V_{out}} \quad (1)$$

By substituting in Eq. 1 and make use of parameters given in Table 1, the value of inductance will be 82 mH.

Table 1 Parameters used for filter design

Parameter	Description	Value
Generator rms voltage	V_{rms}	500 V
Rectifier output voltage	V_{out}	2400 V
Switching frequency	f_{sw}	4 kHz
Desired output current ripple	ΔI_{out}	1.2 A
Duty ratio	D	0.8
Desired output voltage ripple	ΔV_{out}	48 V
Rectifier output current	I_{out}	50 A

Capacitor Design

The parallel connected capacitors to the rectifier input side can be calculated using Eq. 2 [22].

$$C = \frac{I_{out} \times D}{f_s \times \Delta V_{out}} \tag{2}$$

The total capacitor value can be obtained to 208 *μF* to meet the system filter specifications. The inductor and capacitor have been designed to decrease the rectifier input current and voltage ripples, such that it will affect the output current and voltage wave forms.

Switching Losses

It is a loss of power that occurs instantaneously during ON-OFF transitions of a semiconductor switch. Although the ON- OFF transition is a few of nanoseconds but, power loss may be considerable amount. From Fig. 3.

$$i_a(t) + i_b(t) = i_L(t) \tag{3}$$

The instantaneous power dissipated by the transistor can be given by:

$$v_a(t) \times i_a(t) \tag{4}$$

When the transistor is in OFF state the energy loss is given by:

$$W_{OFF} = 0.5 \times V_g \times i_L(t_2 - t_0), \tag{5}$$

When $v_a = V_g$, then the diode becomes forward biased and when the transistor is in ON state the energy loss can be given by:

$$W_{ON} = 0.5 \times V_g \times i_L \tag{6}$$

The total energy will be dissipated during switching period W_{ON} + W_{OFF}

$$P_{sw} = (W_{ON} + W_{OFF}) \times f_{sw} \quad (7)$$

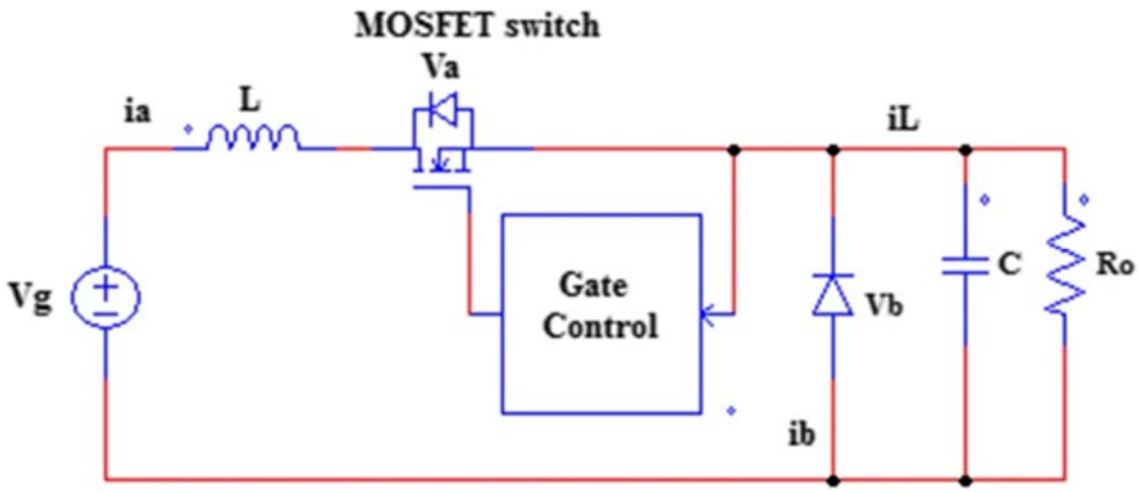


Fig. 3. MOSFET switch representation [22]

Efficiency Versus Switching Frequency

Electrical system efficiency is given by Eq. 8.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (8)$$

Where η is the electrical system efficiency and losses are given by Eq. 9.

$$P_{loss} = P_{cond.} + P_{fixed} + P_{sw} \quad (9)$$

Wh

ere $P_{cond.}$ is conduction losses, P_{fixed} is fixed losses and P_{sw} is switching losses

$$P_{sw} = W_{total} \times f_{sw} \quad (10)$$

$$W_{total} = W_{ON} + W_{OFF} \quad (11)$$

$$P_{sw} \propto f_{sw}$$

The critical frequency can be given by,

$$f_{cri.} = \frac{P_{cond.} + P_{fixed.}}{W_{total}} \tag{12}$$

Switching losses cause the efficiency to decrease at high frequencies, and the Vienna active rectifier has a minimum number of switches comparing with other types of active rectifiers.

Design Criteria of the Rectifier Controller

The controller aims to ensure constant output voltage and current, and the governor of the control circuit is an output voltage and sinusoidal supply input current, the output voltage is sensed and subtracted from the reference voltage to produce the error signal. It is desirable to minimize the error signal, and the current reference is used to maintain the supply sinusoidal current.

Current Loop Controller Design and Analysis

The AC voltages in a rectifier system shown in Fig. 4, can be written as [21, 23,24,25,26]

$$\begin{aligned} V_{sa}(t) &= \hat{V}_s \cos(\omega_0 t + \theta_0) \\ V_{sb}(t) &= \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \tfrac{2\pi}{3}\right) \\ V_{sc}(t) &= \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \tfrac{4\pi}{3}\right) \end{aligned} \tag{13}$$

Where $\hat{V}_s$ is the peak value of phase voltage, ω_o is the AC source frequency and θ_o is the initial rotor angle. The nonlinear system in Fig. 4, can be described by:

$$L\frac{di_d}{dt} = V_{td} + L\omega(t)\, i_q - \hat{V}_s \cos(\omega_0 t + \theta_0 - \rho) - (R + r_{on}) i_d \tag{14}$$

$$L\frac{di_q}{dt} = V_{tq} - L\omega(t)\, i_d - \hat{V}_s \sin(\omega_0 t + \theta_0 - \rho) - (R + r_{on}) i_q \tag{15}$$

Where i_d, i_q and ρ are the state variables. V_{td}, V_{tq} and ω are the control inputs.

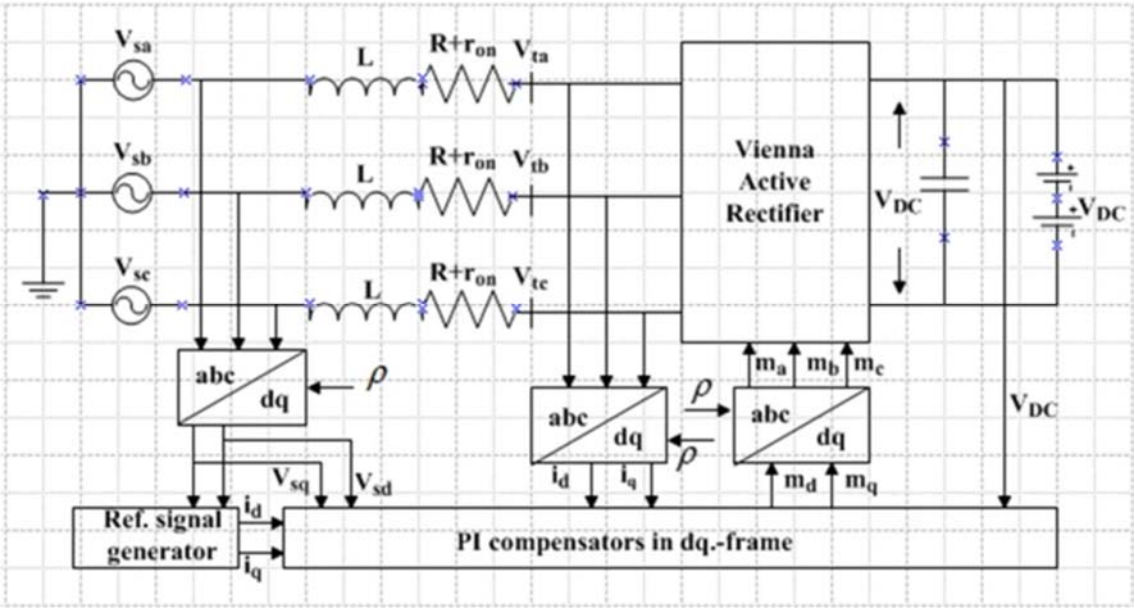


Fig. 4. Graphical scheme of the current-control in a dq-frame

Assume steady state operating conditions and substitute for $\omega(t)=\omega_0$, then Eqs. 14 and 15 can be written as:

$$L\frac{di_d}{dt} = V_{td} + L\omega_0 i_q - (R + r_{on})i_d - V_{sd} \tag{16}$$

$$L\frac{di_q}{dt} = V_{tq} - L\omega_0 i_d - (R + r_{on})i_q - V_{sq} \tag{17}$$

Where V_{sd} and V_{sq} are disturbance inputs. The relationship between a modulating signal and the corresponding AC side terminal voltage can be given by:

$$\vec{V}_t(t) = \frac{V_{DC}}{2}\vec{m}(t) \tag{18}$$

$$V_{td}(t) = \frac{V_{DC}}{2}m_d(t) \tag{19}$$

$$V_{tq}(t) = \frac{V_{DC}}{2}m_q(t) \tag{20}$$

$$m_d = \frac{2}{V_{DC}}(V_{sd}+U_d - L\omega_0 i_q) \tag{21}$$

$$m_q = \frac{2}{V_{DC}}(V_{sq}+U_q + L\omega_0 i_d) \tag{22}$$

Where U_d and U_q are control inputs. By substituting for the m_d and m_q from Eqs. 21 and 22 in Eqs. 19 and 20, yields

$$V_{td}(t) = (V_{sd} + U_d - L\omega_0 i_q) \tag{23}$$

$$V_{tq}(t) = (V_{sq} + U_q - L\omega_0 i_d) \tag{24}$$

Also by substitute $V_{td}(t)$ and $V_{tq}(t)$ Eqs. 23 and 24, respectively in Eq. 16 and 17, yields:

$$L\frac{di_d}{dt} = U_d - (R + r_{on})i_d \tag{25}$$

$$L\frac{di_q}{dt} = U_q - (R + r_{on})i_q \tag{26}$$

Then, Eqs. 25 and 26 depict two separated first order linear systems; i_d and i_q can be controlled by U_d and U_q, respectively, as shown in Fig. 5a and b.

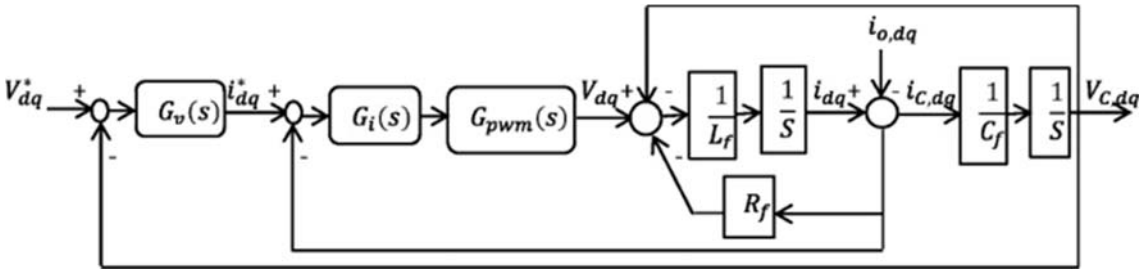


Fig. 5. Closed loop current controller, **a** d-axis controller **b** q-axis controller

The voltage loop controls the converter output voltage by fixing the current reference and the current loop is controlling the converter to track the command, [23]. The control block diagram of the closed loop system is clarified in Fig. 6.

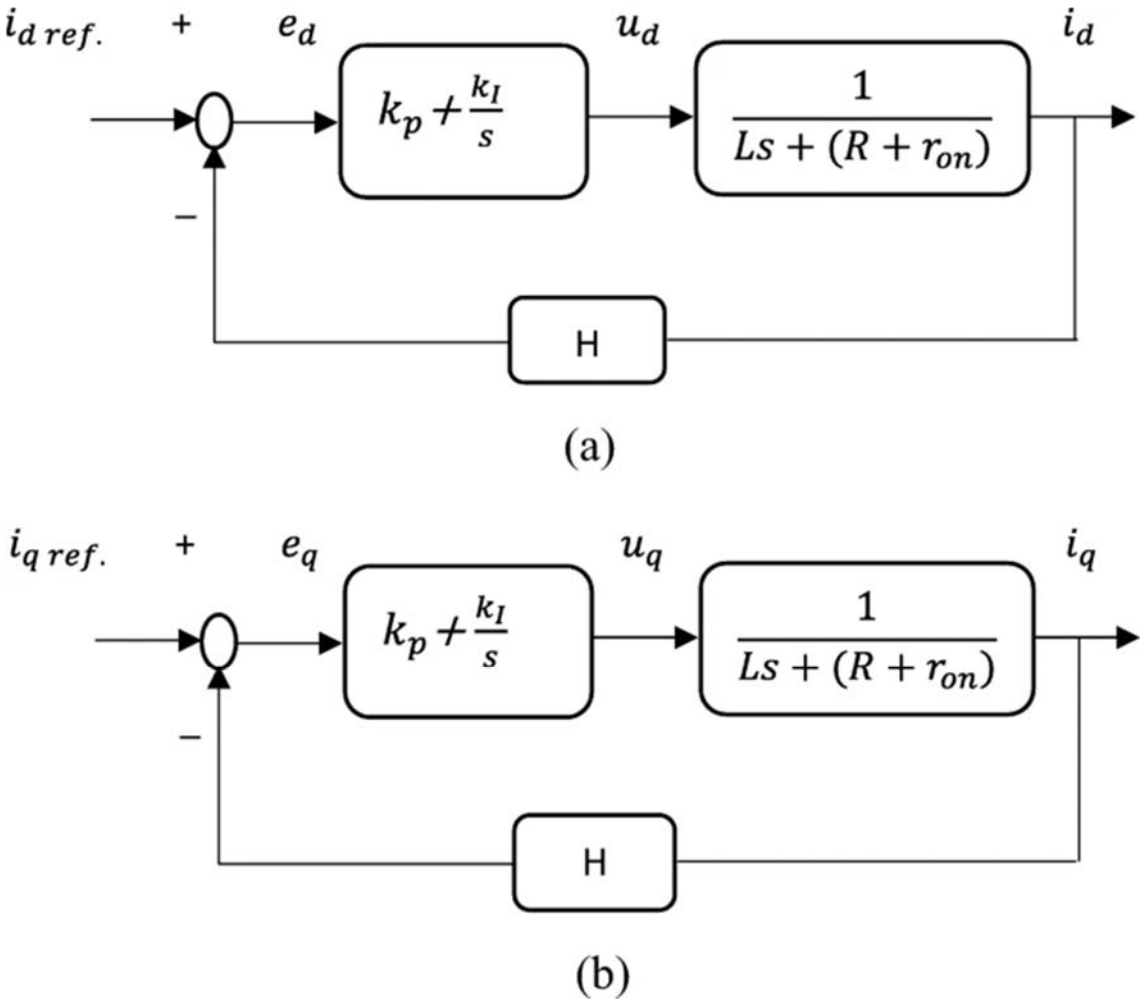


Fig. 6. Block diagram of the closed loop system

Where $G_v(s)$ and $G_i(s)$ and are the voltage and current compensators respectively, V_{dq}^* and i_{dq}^* are the reference voltage and current vectors, L_f is the filter inductor, R_f is the equivalent series resistance of the inductor, C_f is the filter capacitor value. $G_{p\,\mathrm{wm}}(s)$ is the transfer function related to PWM delays, and $= [1 - (T_d/2)]/[1 + (T_d/2)s]$, where T_d is the delay time of the system and $= 1.5\ Ts = 375\ \mu s$.

The current compensator $G_i(s)$ that was designed and analysed is proportional resonance PR compensator and can be given using this equation:

$$G_i(s) = k_p + \frac{2\omega_{c1} k_i S}{S^2 + 2\omega_{c1} S + (h\omega_0)^2} \tag{27}$$

Where, $k_p = 2\pi f_{bw} L$ and $k_i = \frac{R_f}{L_f} k_p$, f_{bw} assumed to be 600 Hz, $\omega o = 2\pi 60 = 377$ rad/s is the fundamental resonant frequency, ω_{C1} is a damping frequency and assumed to be 10 rad/s. The current closed-loop transfer function (TF) Fig. 7, can be determined in Eq. 28

$$i_{dq}(s) = \frac{G_i(s)G_{pwm}(s)C_f(s)}{L_f C_f S^2 + R_f C_f S + G_i(s)G_{pwm}(s)C_f S + 1} i^*_{dq} + \frac{1}{L_f C_f S^2 + R_f C_f S + G_i(s)G_{pwm}(s)C_f S + 1} i_{0,dq} \tag{28}$$

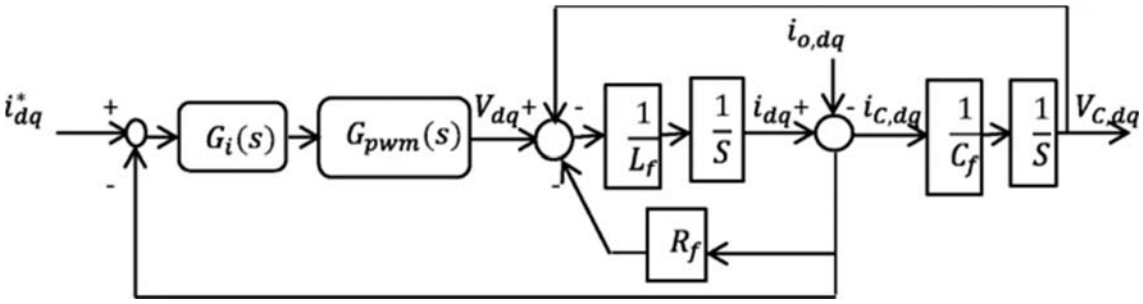


Fig. 7. Block diagram of the designed current loop system

Figure 8 shows the frequency response (FR) of the TF in Eq. 28. The controller has ability to produce zero steady-state error at the desired frequency (600 Hz) which is affected by the proportional gain.

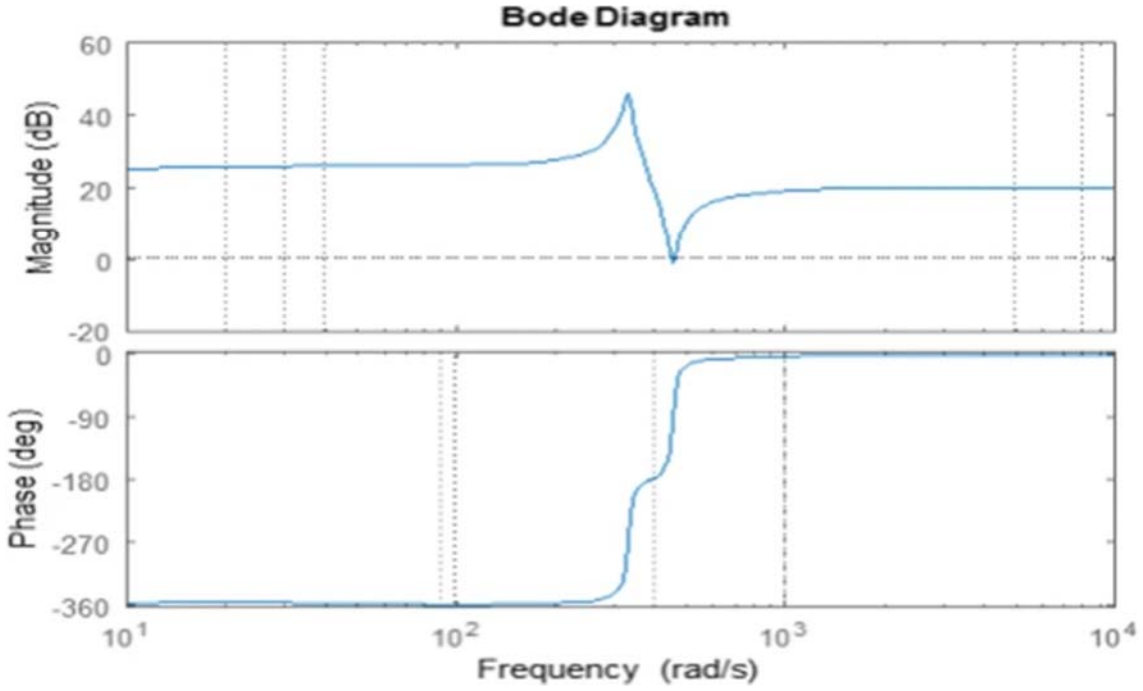


Fig. 8. Closed loop FR of the inner current loop

Voltage-Mode Control Using Phase Locked Loop (PLL)

The AC voltages (13) in a rectifier system shown in Figs. 5 and 9, can be rewritten again as:

$$\begin{aligned} V_{sa}(t) &= \hat{V}_s \cos(\omega_0 t + \theta_0) \\ V_{sb}(t) &= \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \tfrac{2\pi}{3}\right) \\ V_{sc}(t) &= \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \tfrac{4\pi}{3}\right) \end{aligned} \tag{29}$$

Based on the space phasor

$$f_d + j f_q = \vec{f}(t)\, e^{-j\rho(t)} \tag{30}$$

The voltage expressed in a dq-frame can be given by

$$V_{sd} = \hat{V}_s \cos(\omega_0 t + \theta_0 - \rho) \tag{31}$$

$$V_{sq} = \hat{V}_s \sin(\omega_0 t + \theta_0 - \rho) \tag{32}$$

Where ρ is the phase shift and,

$$\frac{\partial \rho}{\partial t} = \omega(t) \tag{33}$$

From Eq. 33, $\omega(t)$ is the input to the voltage controlled oscillator (VCO) as shown in Fig. 9, and it is integrated to produce the desired value of ρ.

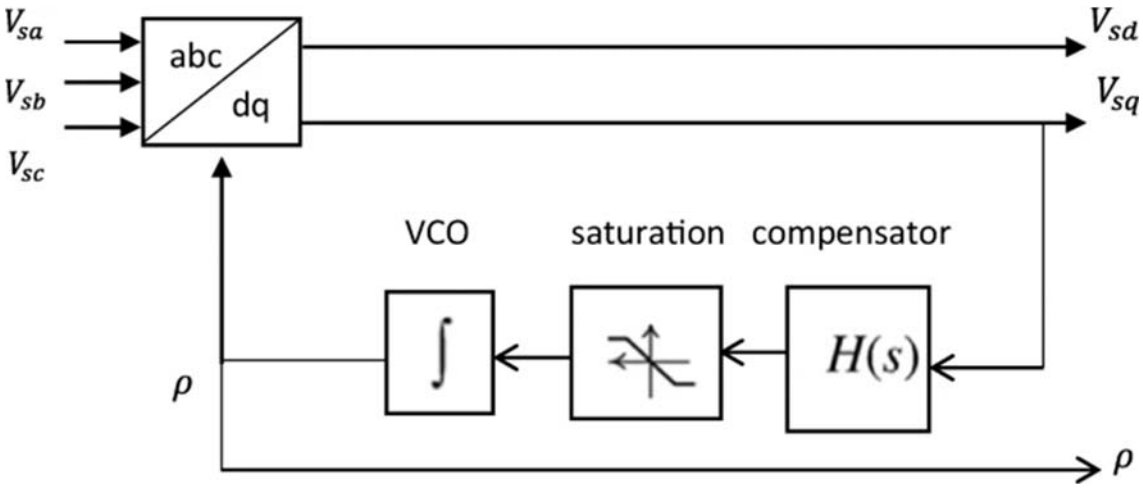


Fig. 9. Graphical representation of the voltage-control in a dq-frame

The compensator output equation can be formulated as,

$$\omega(t) = H(p)\, V_{sq}(t) \tag{34}$$

Where $H(p)$ is a compensator transfer function and p is a differentiation operator

The PLL compensator H(s) in Fig. 10, can be formulated as,

$$H(s) = \left(\frac{h}{\hat{V}_{sn}}\right) \times \frac{S^2 + (2\omega_0)^2}{S(S + 2\omega_0)^2} \times F(s) \tag{35}$$

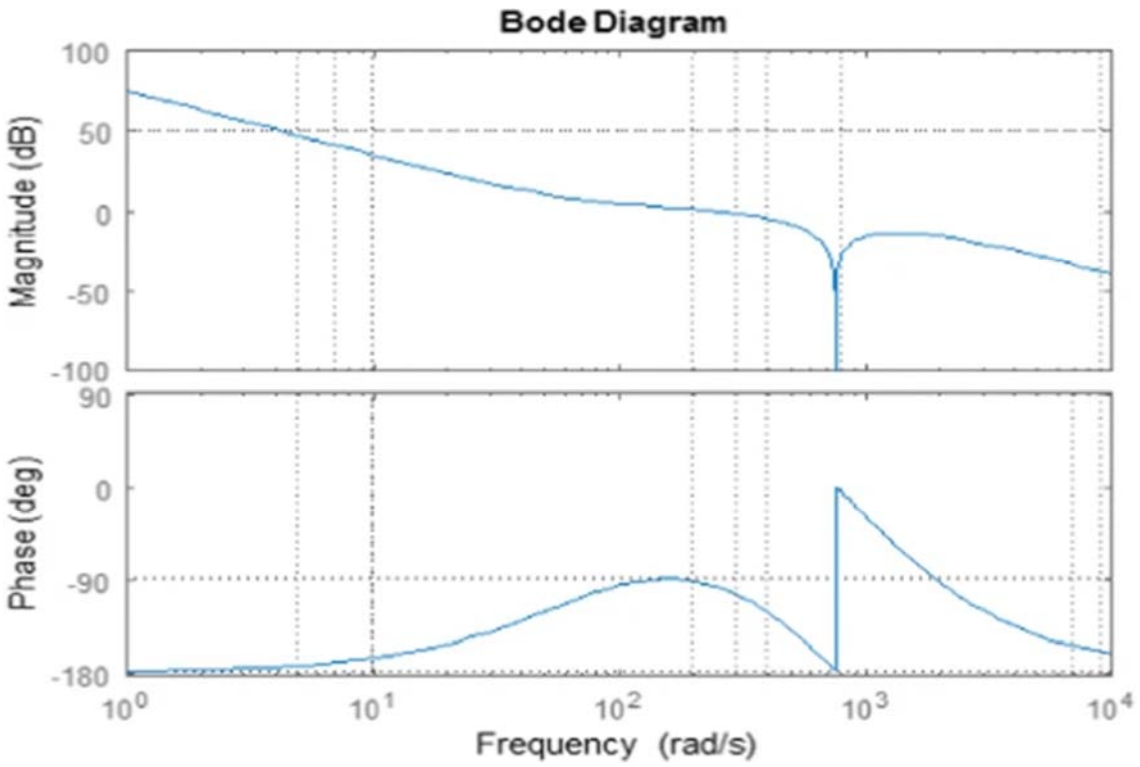


Fig. 10. The frequency response of the PLL for the loop gain L(s)

Where $\hat{V}_{sn}$ is the nominal value of $\hat{V}_s$, h is a constant gain, F(s) is a convenient transfer function with no zero at S = 0, and can be obtained using the Eq. 36.

$$F(s) = \left(\frac{S + (p_1/\alpha)}{S + p_1}\right)^2 \tag{36}$$

Where p_1 is the filter pole, α is a real constant and should be greater than 1. The maximum phase margin of the filter is given by Eq. 37.

$$\delta_m = sin^{-1}\left(\frac{\alpha - 1}{\alpha + 1}\right) \tag{37}$$

The maximum phase margin takes place at the frequency given by Eq. 38.

$$\omega_m = \frac{p_1}{\sqrt{\alpha}} \tag{38}$$

ω_m can be equal to the crossover frequency ω_c. The loop gain can be solved using the equation,

$$l(s) = h \times \frac{S^2 + (2\omega_0)^2}{S^2(s + 2\omega_0)^2} \times F(s) \tag{39}$$

Assume L(s) = 1, and substitute for h, then h = 1.09×10^6. Using parameters given in Table 2, the loop gain can be got and plots to determine the frequency response.

Table 2 Parameters used for compensator design

Parameter	Description	Value
Phase margin	δ_m	60
Crossover frequency	ω_c	250 rad/s
Supply frequency	ω_0	377 rad/s
Peak value of phase voltage	$\hat{V}_s$	577V

From the bode plot Fig. 10, it is found that L(s) declines with the slope of −20 dB when ω is greater than ω_C. The gain margin and the phase margin are 75 dB and 90°

respectively, which is indication of a good stability.

Fault Effect Elimination and Analysis

The wind power plant consists of three parallel connected WECUs as shown in Fig. 11a. DC fault that occurs close to unit 1 terminal will cause large fault currents in its proximity. This type of fault is due to loss or short circuit of one transmission line. The fault is considered to be on DC-link connected to unit 1 as shown in Fig. 11a, the output current will be zero due to the flow of the fault current through the system. Figure 11b, shows the controller that has been used to ride through the fault through D_sw and the fault blocking diode which blocks the fault by reverse bias and FRT components.

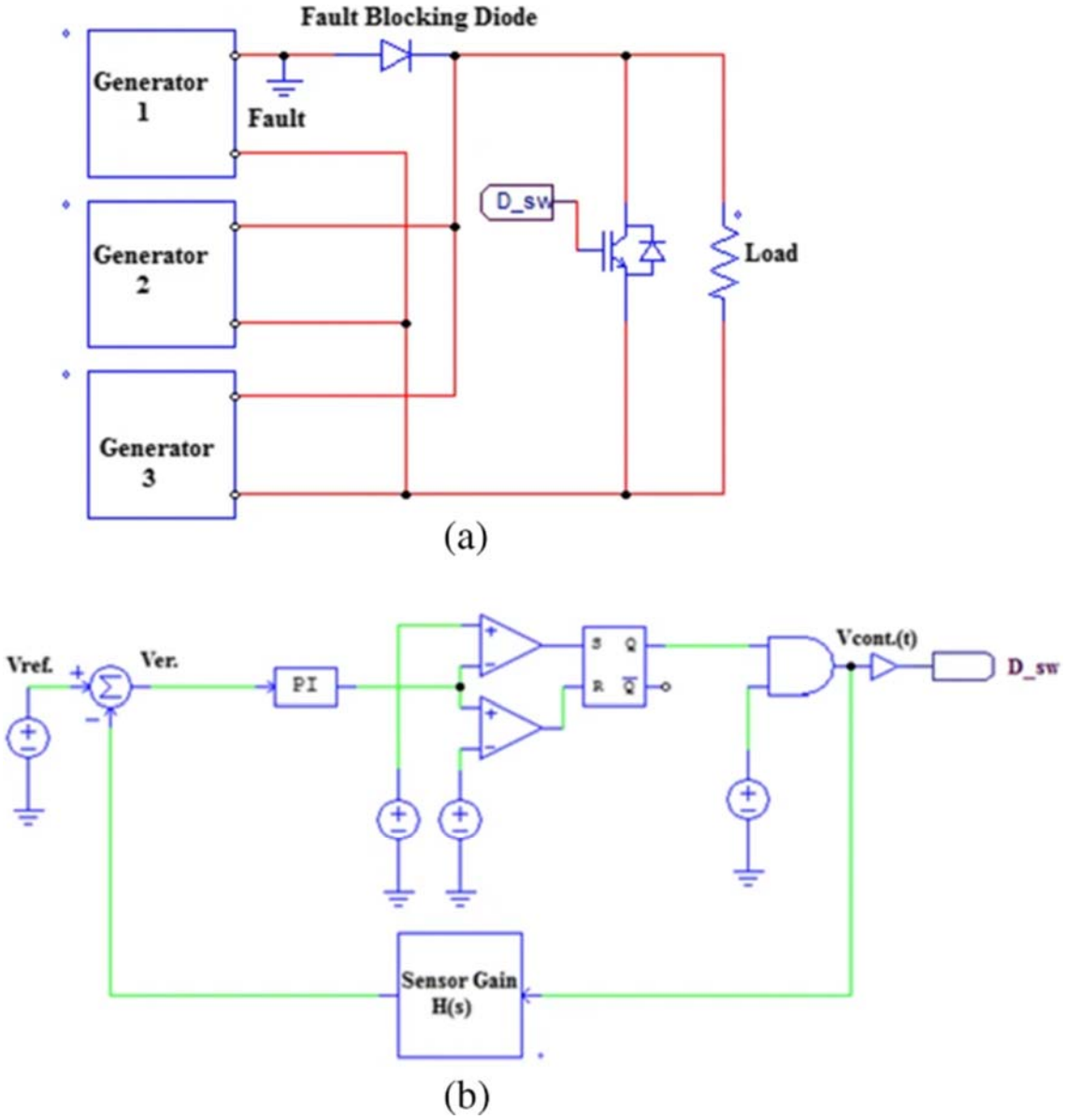


Fig. 11. Connection of three units and the controller, **a** Three units connected in parallel and the fault and fault blocking diode are placed at unit 1, **b** FRT controller

The controller output voltage $V_{cont.}(t)$ is sensed with H(s), the sensor output will be H(s) × $V_{cont.}(s)$ and is compared with a reference input voltage $V_{ref.}$, the aim is to let H(s)×$V_{cont.}(s)$ closer to V_{ref}. The variation between the reference input $V_{ref.}$, and the sensor output H(s)×$V_{out}(s)$ is an error signal. If the feedback system is perfect then the error signal will be zero. In practice, the error signal is commonly not zero but none the less very small. In any case of disturbance the compensator should compensate the error signal to the desired signal.

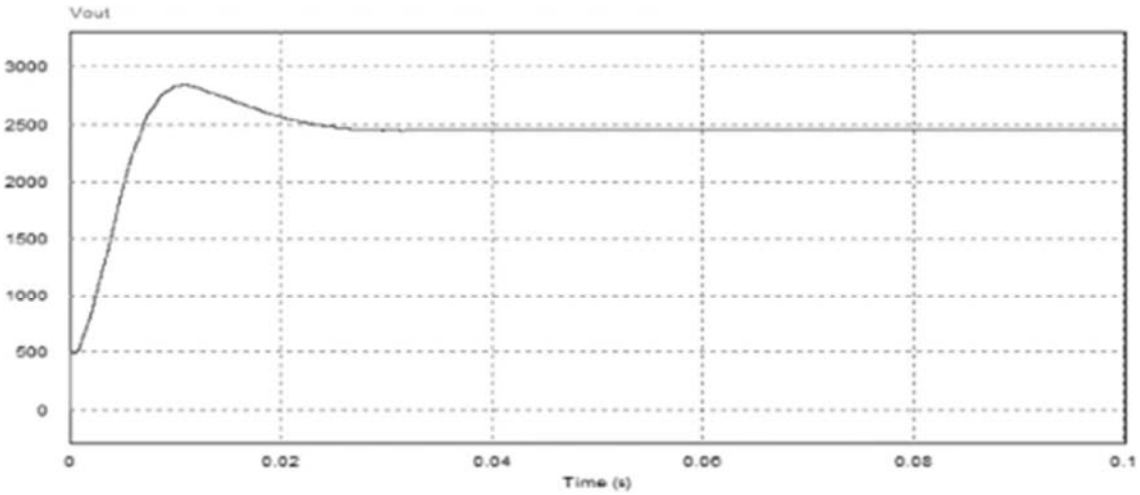
Simulation Results and Discussions

Simulations have been carried out using PSIM programme and the values of parameters used have been shown in Table 3. Three WECUs are connected in parallel, so that the parallel connection is the strongest type of connections and if one unit collapses the system remains in synchronism.

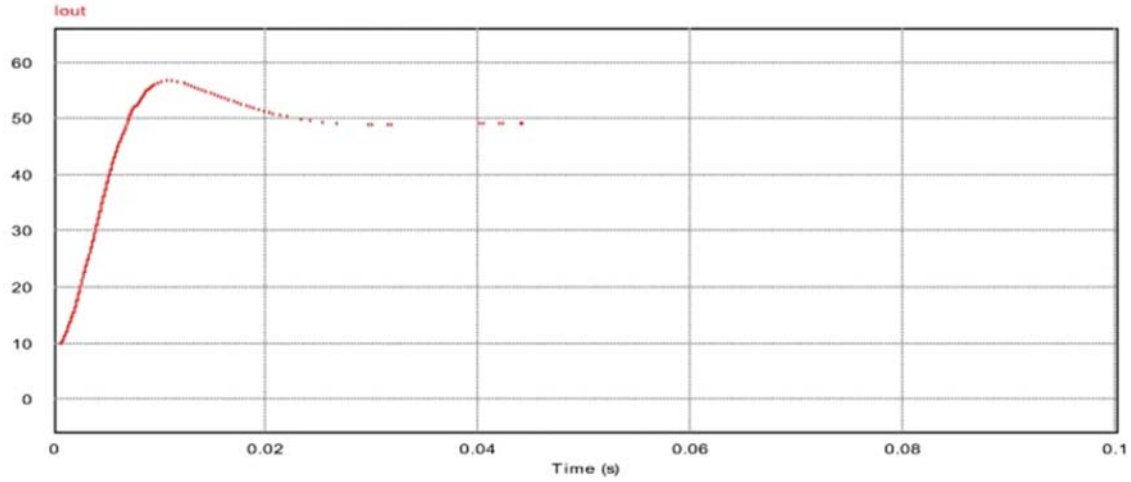
Table 3 Parameters used for simulation

Parameter	Description	Value
Generator voltage rating	V_g	500 V
Generator current rating	I_g	20 A
Turbine voltage rating	V_t	500 V
Turbine current rating	I_t	20 A
Generator filter capacitance	C_F	208 μF
Generator filter inductance	L_F	82mH
DC link capacitance	C_1,C_2	1000 μF
Load	R	50 Ω

In normal operation conditions, the switch will be locked for a long time, so that voltage and current waves are in stable operation. Figure 12a and b, shows the output voltage and current wave forms in the steady state operation. The output voltage as shown in Fig. 12 is in steady state condition and is stable at 2400 V after small overshooting due to system start up.



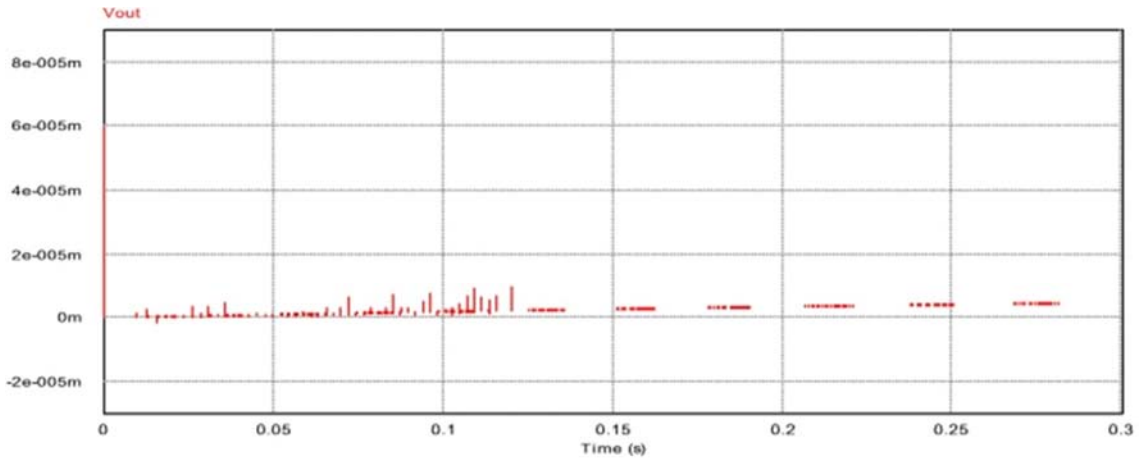
(a)



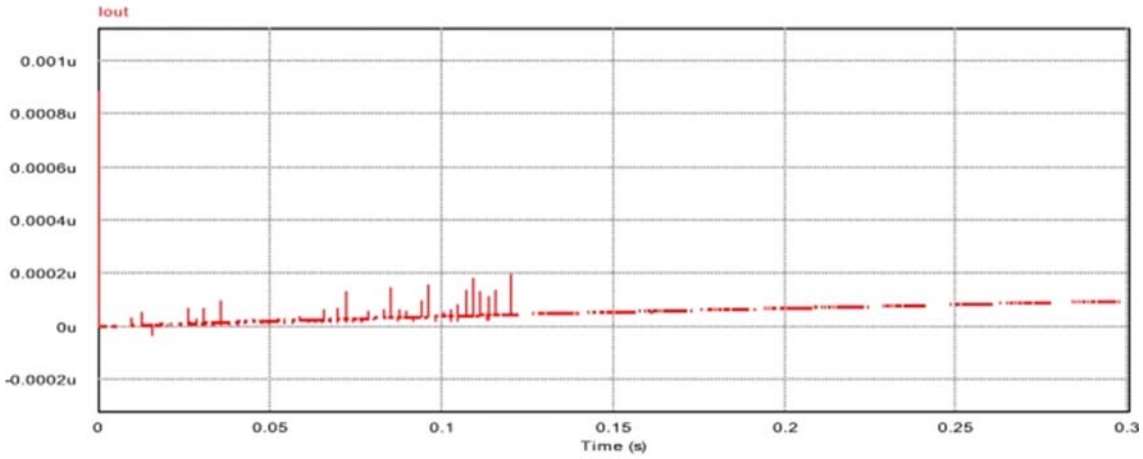
(b)

Fig. 12. Steady state operation, voltage and current wave forms, **a** output voltage, **b** output current

Similar to output voltage, the output current as shown in Fig. 12b, is in a normal operation and stable at 50 A after some overshooting. The collapsed output voltage and current wave forms which represent the faulted system are shown in Fig. 13a and b, when the fault applied in unit 1, the fault current will flow through the system and will result of a damage, but by connecting the controller that has been designed the fault can ride through, as shown in Fig. 14.

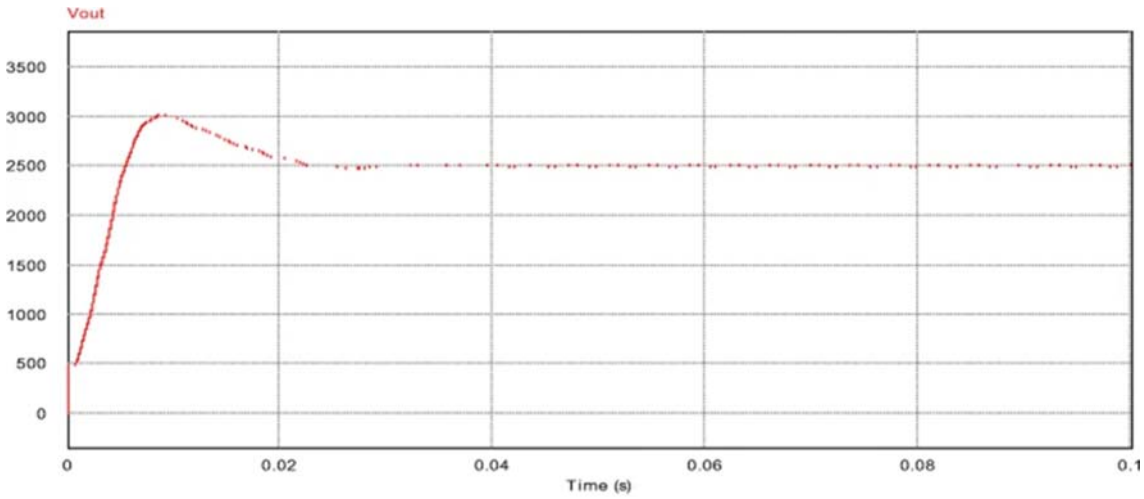


(a)

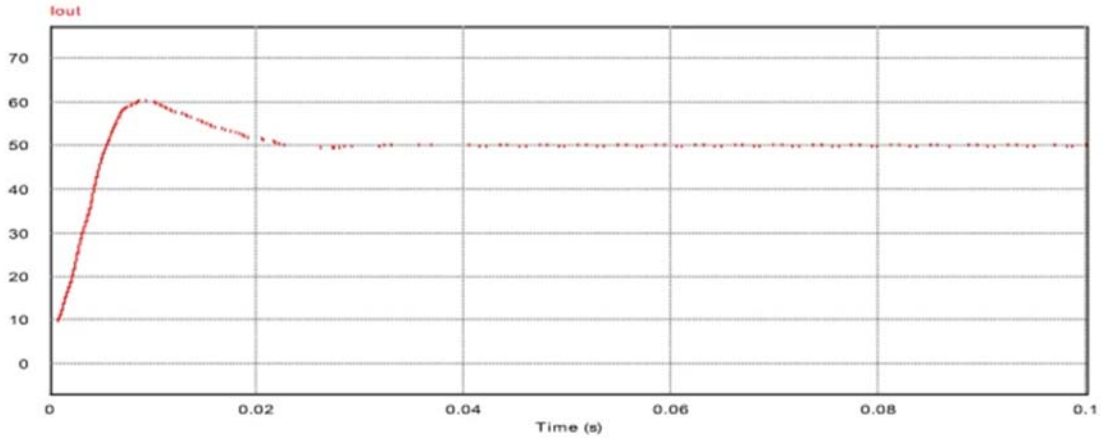


(b)

Fig. 13. Output voltage and current wave forms when applying the fault, **a** output voltage, **b** output current



(a)



(b)

Fig. 14. Output voltage and current wave forms when applying FRT controller, **a** output voltage, **b** output current

Figure 14, shows the output voltage and current wave forms after applying FRT controller the fault blocking diode, and simulation result shows that the controller can ride through the fault very well, because the output voltage and current wave forms are similar as steady state operation “before applying the fault”. The voltage across the fault blocking diode shown in Fig. 15a has the same peak inverse value of load voltage, and the current wave Fig. 15b has zero value because of diode reverse bias.

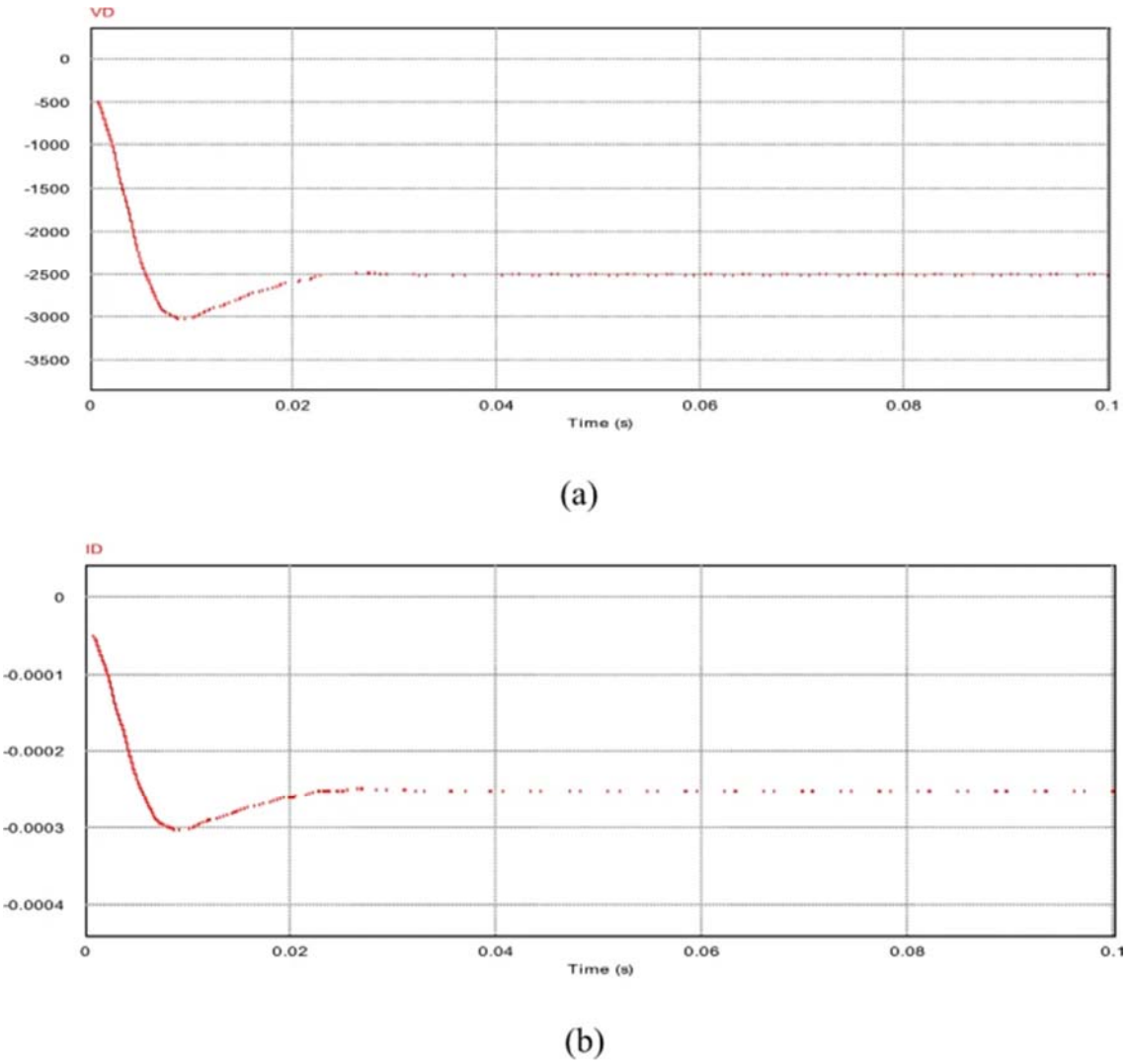


Fig. 15. Fault blocking diode characteristics, **a** voltage characteristics **b** current characteristics

Howell et al. [27] they did a similar work of using a fault blocking diode in a DC transmission line to block the fault current and they built a HVDC system topology to transmit unidirectional power into weak AC system while retaining the ability to clear DC faults. They discussed Control strategies including fault blocking diode and its performances under DC and AC faults using electromagnetic transient simulations, and they concluded that the topology is viable candidate. The difference between this work and their work is they used a line commutated converter LCC and a modular multilevel converter MMC as a rotor side converter RSC and a grid side converter GSC, respectively. Furthermore, this control strategy using fault blocking diode was performed in [28,29,30,31,32] and they concluded and recommended that it is a practical and effective controller that participate in the power system stability.

Conclusion

This paper has presented DC-link fault analysis to ride through the transient faults. The simulation results have shown the superiority of the proposed FRT capability controller, which involving sub-models consisting of controller and fault blocking diode. The fault blocking diode has detected the fault very fast and protected power tools from thermal over stresses with the controller assistance by creating new current path to eliminate the fault current effect. This paper proved that the unidirectional HVDC scheme is able to protect the transmission DC line from the transient faults that can occur due to short circuit. The current and voltage loop controllers have been designed to maintain constant voltage at steady state conditions. Also, the supply side filter that consists of inductor and capacitor has been designed to decrease the input voltage and current ripple values It has been concluded that the power transmission is found to be rapid and continual for the non-permanent faults and the controller has improved the stability and reliability of the wind power HVDC system.

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