

Unified Approach for Synthesis and Analysis of Non-Isolated DC-DC Converters

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ABSTRACT Transformational techniques unifying synthesis of two-state DC-DC converters and analytical synthesis techniques allowing generation of all possible converters meeting a certain criteria already exist. The analysis of a family of converters derived from a single converter cell has also been unified. Current waveforms generated by the family of converters were shown to be related. However, a concept or basic building blocks that facilitate unified synthesis, analysis, prediction of current waveforms and assignment of switch states over a very wide range of DC-DC converters is still lacking. This study will propose three 3-terminal basic building blocks and one 3-terminal filter block. It will be shown that between them, they are sufficient for realizing all non-isolated DC-DC converters excluding those with coupled inductors. The various DC-DC converters fall into those realized through cascade, stacked, stacked plus cascade, interleaved/paralleled or differential connection of the basic building blocks. A systematic approach for evaluating input-output current gains will be presented. Moreover, a basic building block will be shown to have fixed switching states for proper operation. This gives rise to the generation of a unique set of current waveforms at the three terminals irrespective of where a basic building block is embedded. It has been shown that the effort and time needed to design DC-DC converters can be reduced as switching device stresses can be estimated without the need for tedious first principle derivations.

INDEX TERMS Basic building blocks, converter cells, current waveforms, non-isolated DC-DC converters, steady-state gains, unified analysis of DC-DC converters, unified synthesis of DC-DC converters.

I. INTRODUCTION

Much effort has been devoted towards the development of techniques for synthesizing DC-DC converters over the last five decades [1]–[29]. Techniques for synthesizing two-state or single active switch DC-DC converters [1]–[12] and those for synthesizing multiple-switch, multiple-inductor converters [13]–[29] have been developed. The synthesis techniques fall into two broad groups: transformational [1], [3]–[16], [18]–[23] and analytical [2], [17]. The transformational techniques are further categorized into: duality principle [6], [7], bilateral inversion [2], [6], [7], paralleling and cascading [2], [8], [13], [16], [18]–[23], stacking [18], [20], [21], [23], extension of the canonical switching cell [1], [4], [5]–[7], rules based [3], [19], [21], [23], graphical [3], layer and graft schemes [10]–[12] and systematic

rearrangement of the three- and five-element circuits [3], [15], [16]. Analytical techniques to obtain steady-state input-output voltage and current gains include those that treat converters or converter cells as three-port terminal devices [5]–[7], [14], [15], [20], one that treated a third-order cell as a four-port device [20] and those based on conventional analytical techniques [1], [2], [9]–[12], [16]–[18]. The analytical technique in [17] builds on that in [2]. It allows the generation of multiple-switch, multiple-inductor and multiple-capacitor converters which is not the case with [2]. Both [2] and [17] facilitate the derivation of input-output steady-state voltage gains. Despite allowing the generation of all possible converters for a given set of performance specifications, they are analytically intensive. Moreover, they are not suited to analyzing existing converters. In [14], [15], it was shown that the functionality of all DC-DC converters falls into three categories: buck, boost and buck-boost whilst [5]–[7] had shown this to be true for all two-state

The associate editor coordinating the review of this manuscript and approving it for publication was Yue Zhang¹.

DC-DC converters. The layer and graft schemes [10]–[12] synthesize converters using transfer gains as a starting point.

A converter cell was defined as a DC-DC converter minus source and load [1], [14], [15]. The three-element canonical switching cell was the first converter cell to be proposed [1], [10]. Three-element converter cells referred to as Tee canonical cell and Pi canonical cell were proposed in [7]. Five-element converter cells were proposed in [6], [14], [15] while [4] proposed two two-element P-cell and N-cell. These were considered as the basic building blocks (BBBs) for various types of DC-DC converters using transformational techniques. Other researchers saw the basic buck, boost and buck-boost converters as the BBBs for more complex converters [5], [8], [13], [16], [21]–[29].

In [7], [14], [15] 14 different types of 3-terminal switching converter cells were identified. These included: 1st order 2-switch and 4-switch converter cells plus 3rd order 2-switch and 4-switch converter cells. The switching converter cells can be categorized into three groups ($u=1,2,3$), each group has members ($v=1,2,3,..,4/6$) and each group member gives rise to a family of up to 6 converters ($w=1, 2, 3,..,6$). Group 1 members (1- $v.w$) generate a continuous current signal with triangular ripple at one terminal and pulsed signals at the other two terminals. Group 2 members (2- $v.w$) generate pulsed current signals at all three terminals while the group 3 members (3- $v.w$) generate continuous current signals at all three terminals.

The study in [14] unified the derivation of converters' steady-state input-output DC gains as well as small-signal analysis for a family of converters obtained from the same converter cell. Further, [14], [15] suggested that voltage and current waveforms of the family of converters obtained from a given converter cell are related. However, no attempt was made to extend this concept to cover all converters from the various converter cells. For example, no attempt was made to establish why seemingly unrelated switching converter cells generate current signals that share certain characteristics and why these converter cells are all capable of buck, boost or buck-boost functionalities. Moreover, the study did not develop a structured technique for deriving their current gains, predicting current signals generated or determining the required gate signals for control purposes. This would make analysis and design of various DC-DC converters more structured.

Some of the most commonly used DC-DC converters (basic buck, boost and buck-boost, Cuk, Zeta and Sepic) are derived directly from the 14 converter cells considered in this study. However, there are many other DC-DC converters that are not derived directly from the 14 converter cells. These include the non-isolated current-fed [11], [12], [18] and voltage-fed [11], [12], [18] full-bridge DC-DC converters. There are also interleaved [9], [22] DC-DC converters that are used in various applications. Other commonly used DC-DC converters topologies are the impedance sourced converters also referred to as Z-sourced and quasi-Z-sourced

DC-DC converters [30]–[32]. In the available literature, there is no evidence of studies that have been carried out to try and develop a structured approach to predict current signals generated by these DC-DC converters.

This study will propose three 3-terminal BBBs and one 3-terminal filter block. The BBBs can be considered as the most elementary 3-terminal sub-circuits that any non-isolated DC-DC converter can be broken down into. The 3 BBBs and 1 filter block are together sufficient for realizing any of the 14 converter cells proposed in the literature [7], [14], [15] as well as other non-isolated DC-DC converters excluding those with coupled inductors. This study will show that DC-DC converter structures fall into one of the following categories: cascaded, stacked, cascaded plus stacked, parallel/interleaved, or differential connection of BBBs. Converter current gains will be obtained in a more intuitive, less analytically intense technique and hence simpler than currently available techniques. The BBBs will be shown to have unique sets of switch states that guarantee proper operation. These in turn give rise to unique sets of current waveforms at the BBBs' terminals. The switch states of converters and current waveforms generated are thus dictated by the BBBs used to realize them. Similarities between converters currently presented as unique will be easy to identify as will identification of redundant sub-circuits or components in DC-DC converters. The quasi-Z-source DC-DC converter will be shown to belong to the same family as the Zeta converter. In [33] a very comprehensive method to design interleaved step-up DC-DC converters was presented. This study will demonstrate that for non-isolated DC-DC converters, BBBs allow switching device stress to be estimated without the need for tedious first principle derivations. The study will also show that sizing of passive components is dictated by the BBBs irrespective of where the BBB is embedded in a more complex converter.

The remainder of the paper is structured as follows: Section II will propose three 3-terminal BBBs and one 3-terminal filter block needed to build non-isolated DC-DC converters. Key analyses for each basic building block (BBB) will be presented. Section III will demonstrate that all converter cells previously proposed [7], [10], [14], [15] are realized using one or a combination of the 3 BBBs and filter block proposed in this study. Furthermore, it will be shown that gate signals, current signals and current gains of DC-DC converters are dictated upon by those of BBBs used to realize these converters. Section IV will extend the concept of BBBs to commonly used DC-DC converters. Section V will demonstrate that the BBBs are suitable for predicting semiconductor devices' current and voltage stresses. Moreover, it will also show that, sizing of passive components is dictated by the BBB even in complex converters. Section VI will present simulated waveforms to validate that converter current signals are predetermined once the BBBs to realize a converter are selected. Waveforms and data to validate derivations for the BBBs and generated using PSIM software will be presented. Section VII will present concluding remarks.

II. CONCEPT OF BASIC BUILDING BLOCKS FOR DC-DC CONVERTERS

Conventionally, DC-DC converters are treated as single unique unrelated entities or the relationship between them is not well established as there is no solid analytical foundation for the relationship. This section will introduce the concept of a BBB or converter sub-topology. It will demonstrate that DC-DC converters without transformer isolation or coupled inductors can be broken down into three-terminal sub-topologies. These sub-topologies are seen as the most basic building blocks for realizing DC-DC converters, for example, those reported in [7], [14], [15]. In fact, DC-DC converters can be realized using one or a combination of the three types of basic building blocks referred to as type-1, type-2 and type-3 plus the 3-terminal filter block. The proposed technique applies to both continuous and discontinuous conduction modes (CCM and DCM). However, only CCM operation is considered in this study and DCM will be the subject of a separate study.

A. TYPE-1 BASIC BUILDING BLOCK

A type-1 BBB is shown in Fig. 1. It comprises three components: an inductor, L , and two semiconductor devices, S_1 and S_2 connected to node N_1 . To comply with circuit laws and avoid damaging dv/dt , inductor current, i_L , cannot be forcedly switched. The switches S_1 and S_2 cannot be “on” or “off” at the same time. At any one given time, one of the switches has to conduct to provide a path for inductor current. At the same time, during steady-state operation, average voltage across the inductor must be zero. This requires an inductor to be provided with a charging interval (associated with a conducting active switch) as well as an interval for the inductor to discharge (associated with a conducting diode) within each switching period. Hence, the only allowable switch states combinations and the corresponding currents are as shown in Table 1. These switch state combinations are independent of converter functionality and are the basis on which current signals shown in Fig. 1 are obtained. When power flow is unidirectional, S_1 is a self-controlled switch, and S_2 must be

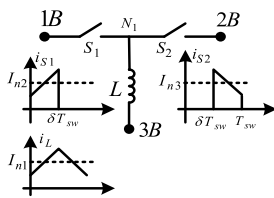


FIGURE 1. Type-1 basic building block.

TABLE 1. Allowable switch states and corresponding switch currents for type – 1 BBB.

S_1	S_2	I_{S1}	I_{S2}
0	1	0	I_L
1	0	I_L	0

a diode, with the two devices operating as a complimentary pair. When switch S_1 conducts ($S_1 = 1$ and $S_2 = 0$), inductor current and hence current through S_1 , i_{s1} , increases linearly to charge the inductor. Similarly, when S_2 conducts ($S_1 = 0$ and $S_2 = 1$), inductor current and hence current through S_2 , i_{s2} , decreases linearly, thus discharging the inductor. When the switching-period is much shorter than inductor electrical time-constant, the above switching actions lead to trapezoidal switch and diode current waveforms and triangular inductor current waveform irrespective of where the basic building block is embedded in a DC-DC converter. In other words, continuous inductor current.

The following relations are derived with reference to Fig. 1, for a type-1 BBB, assuming CCM. The derivations assume S_1 is a self-controlled switch and S_2 is a diode. Further, in Fig. 1, I_{n1} , I_{n2} , and I_{n3} are the nominal magnitudes of the inductor, active switch and diode currents respectively. Self-controlled switch duty-ratio is δ .

$$I_{L,ave} = I_{n1} = I_{n2} = I_{n3} \tag{1}$$

$$I_{S1,ave} = \delta I_{n2} \tag{2}$$

$$I_{S2,ave} = (1 - \delta) I_{n3} \tag{3}$$

$$I_{L,ave} = I_{S1,ave} + I_{S2,ave} = \delta I_{n2} + (1 - \delta) I_{n3} \tag{4}$$

Define input-output current gain as follows

$$G_{I_{in,ave} \rightarrow I_{o,ave}} \equiv G_{I_{in} \rightarrow I_o} = \frac{I_{o,ave}}{I_{in,ave}}$$

From (1)-(4), expressions for current gains between any two of the three terminals (i.e. gains of the various BBB’s stages) are obtained as

$$G_{I_L \rightarrow I_{S2}} = \frac{I_{L,ave}}{I_{S2,ave}} = 1 - \delta \tag{5}$$

$$G_{I_{S1} \rightarrow I_{S2}} = \frac{I_{S1,ave}}{I_{S2,ave}} = \frac{1 - \delta}{\delta} \tag{6}$$

$$G_{I_L \rightarrow I_{S1}} = \frac{I_{L,ave}}{I_{S1,ave}} = \frac{1}{\delta} \tag{7}$$

Equations (5)-(7) show that functionality of the BBB (based on current gains) is dependent on the terminals that are designated as input and output. When the active switch is connected to input and inductor to output, boost functionality is obtained as seen in (5). Buck-boost functionality requires the active switch to be connected to input and diode to output as seen in (6). When the inductor is connected to the input terminal and diode to the output terminal, buck functionality is obtained. It is evident from (5)-(7) that these connections of type-1 BBB, yield the three distinct DC-DC converters. The functionality based on voltage gain is the inverse of that based on current gain. Swapping S_1 and S_2 cause the functionality to change from buck (boost) to boost (buck). The derivations, switch states and terminal waveforms are independent of the position of a BBB in a converter. If a positive current gain coincides with output current flow out of the positive rail, then the gain in (6) should have a negative sign to cater for polarity.

B. TYPE-2 BASIC BUILDING BLOCK

A type-2 BBB is shown in Fig. 2. It consists of three terminals and three components: semiconductor switch, inductor and capacitor. The type-2 are unique BBBs that can be used to realize various DC-DC converters. Two variants of type-2 BBBs can be synthesized depending on, whether an active or passive semiconductor device is employed. Proper steady-state circuit operation in CCM dictates that the inductor current must be unidirectional or DC, average inductor voltage and average capacitor current must be zero. The permissible switch states combinations and corresponding switch and capacitor currents for each BBB variant are as shown in Table 2. If S_1 is an active switch, L_1 charges when $S_1 = 1$ and discharges when $S_1 = 0$. Given that capacitor current, i_{C11} , is bidirectional and AC, it flows in one direction when $S_1 = 1$ and in the opposite direction when $S_1 = 0$. Changing S_1 to a diode would cause i_{L1} and i_{S1} to reverse in polarity and L_1 to charge and discharge when diode is off and on respectively. However, Table 2 would still be applicable.

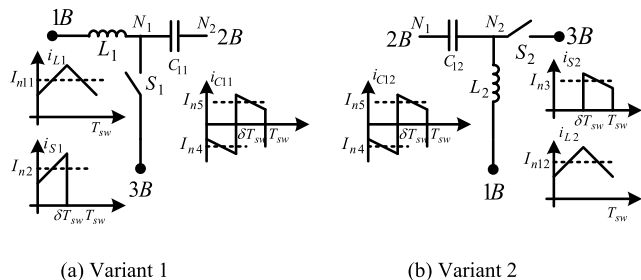


FIGURE 2. Variants of type-2 BBB and associated current signals.

TABLE 2. Permissible switch states and corresponding currents in the components of type - 2 BBBs.

S_1	I_{S1}	I_{C11}	S_2	I_{S2}	I_{C12}
0	0	I_{L1}	0	0	I_{L2}
1	$I_{L1} + I_{C11}$	I_{N2}	1	$I_{L2} + I_{C12}$	I_{N1}

It is evident that a single type-2 BBB cannot guarantee charge and discharge intervals for the inductor and capacitor. This is necessary to ensure zero average inductor voltage and capacitor current and hence proper steady-state converter operation. Moreover, a practical DC-DC converter must have DC currents at all three terminals, which is not the case in type-2 BBBs. Unlike type-1 BBBs, a single type-2 BBB does not constitute a viable DC-DC converter on its own. Therefore, at least two type-2 BBBs, type-1 and type-2 BBBs, or type-1, type-2 and type-3 BBBs must be connected together to realize a practical viable DC-DC converter as will be elaborated later. Assuming S_1 is an active switch and S_2 a diode, when S_1 conducts, L_1 charges from the source, causing i_{L1} to rise. At the same time, C_{11} discharges through S_1 . When S_1 is off, L_1 discharges through C_{11} , causing i_{L1} to decrease. Similarly, when S_2

conducts, L_2 discharges causing i_{L2} to decrease while C_{12} charges. And when S_2 is off, L_2 is charged by C_{12} and hence C_{12} discharges. Thus the nature of current signals is easily determined.

From Fig. 2(a), the following relations are derived considering the type-2 BBB associated with node N_1 and having S_1 as an active switch. Further, I_{n11} , I_{n12} , I_{n2} and I_{n3} are the nominal magnitudes of i_{L1} , i_{L2} , i_{S1} and i_{S2} respectively. Additionally, I_{n4} and I_{n5} are the nominal magnitudes of capacitor current when S_1 and S_2 conduct respectively.

$$I_{L1,ave} = I_{n11} = I_{S1,ave} = \delta I_{n2} \xrightarrow{\text{yields}} G_{I_{L1} \rightarrow I_{S1}} = \frac{I_{S1,ave}}{I_{L,ave}} = 1 \tag{8}$$

$$I_{n5} = I_{n11} \tag{9}$$

$$\delta I_{n4} = (1 - \delta) I_{n5} = (1 - \delta) I_{n11} \tag{10}$$

Nominal capacitor current when S_1 conducts and nominal current for S_1 are then obtained in terms of nominal current for L_1 as

$$I_{n4} = I_{n2} - I_{n11} = \frac{I_{n11}}{\delta} - I_{n11} = I_{n11} \left(\frac{1 - \delta}{\delta} \right) \tag{11a}$$

$$I_{n2} = I_{n11} \left(\frac{1}{\delta} \right) \tag{11b}$$

Equation (11) shows that it is possible to predict the amplitude of capacitor current when S_1 conducts even though at this stage the circuit connecting to the second terminal of the capacitor is not necessarily known. The expressions applicable to type-2 BBB associated with node N_2 shown in Fig. 2(b) utilizing a diode, are obtained in a similar manner as follows:

$$I_{L2,ave} = I_{S2,ave} \xrightarrow{\text{yields}} G_{I_{L2} \rightarrow I_{S2}} = \frac{I_{S2,ave}}{I_{L2,ave}} = 1 \tag{12}$$

A DC current gain can only be defined for terminals 1B and 3B and it is always unity as seen in (8) and (12).

$$\therefore I_{n12} = (1 - \delta) I_{n3} = I_{n4} \tag{13}$$

$$I_{n3} = I_{L2,ave} + I_{n5} = I_{n12} + I_{n5} = \frac{I_{n12}}{1 - \delta} \tag{14}$$

$$\therefore I_{n5} = I_{n12} \frac{\delta}{1 - \delta} \tag{15}$$

From (9), (11), (14) and (15),

$$I_{n2} = I_{n11} + I_{n12} = I_{n3} = I_{n12} + I_{n11} \tag{16}$$

Equation (16) shows that the nominal current for S_1 is the same as for S_2 . Thus, the active switch and diode in the two variants of type-2 BBBs behave as if they are a pair.

C. TYPE-3 BASIC BUILDING BLOCK

A type-3 BBB is shown in Fig. 3. It has three terminals and comprises three components: an active switch, a diode and a capacitor. The type-3 is a unique BBB, which can be used to realize various DC-DC converters. Proper steady-state operation of type-3 BBB requires that average capacitor current to be zero. The corresponding switch states and capacitor

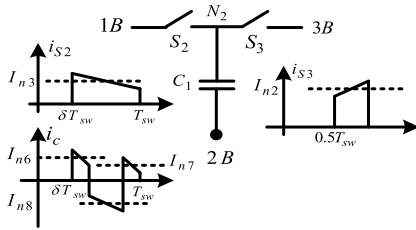


FIGURE 3. Type-3 BBB and associated current waveforms.

TABLE 3. Permissible switch states and corresponding currents in the components of type – 3 BBBs.

S ₂	S ₃	I _{C1}
0	0	0
0	1	I _{S3}
1	0	I _{S2}
1	1	0

current are as shown in Table 3. Given that average capacitor current is zero, average current through the two switches must be identical and capacitor current must be the difference between switches S₂ and S₃ currents. Also, it is evident that a single type-3 BBB does not have DC currents at all three terminals. It is thus, not a viable DC-DC converter on its own. A type-3 combines with at least a type-1 or type-2 BBBs to realize a practical viable DC-DC as discussed later.

The relevant expressions for a type-3 BBB are obtained with reference to Fig. 3 as

$$I_{S2,ave} = I_{S3,ave} \xrightarrow{\text{yields}} G_{I_{S2} \rightarrow I_{S3}} = \frac{I_{S3,ave}}{I_{S2,ave}} = 1 \quad (17)$$

$$I_{C1,ave} = 0 \quad (18)$$

$$I_{n6} + I_{n7} = 2I_{n3} \quad (19)$$

$$I_{n8} = I_{n3} - I_{n2} \quad (20)$$

$$\delta I_{n8} = \left(\frac{1}{2} - \delta\right) (I_{n6} + I_{n7}) \quad (21)$$

Equation (17) shows that for a type-3 BBB, a DC gain (of unity) is only possible between the terminals connecting to semiconductor devices i.e. 1B and 3B.

D. FILTER BLOCK

A 3-terminal filter block shown in Fig. 4 comprises three components: two inductors and a capacitor. This filter block is sometimes combined with some of the BBBs to realize various DC-DC converters. Proper steady-state circuit operation requires that inductor current is continuous, average voltage across the inductor and average current through the capacitor must be zero. The corresponding inductors' and capacitor currents are as shown in Table 4. Given that average capacitor current is zero, average current through the two inductors must be identical and capacitor current must be the difference between the ripple of inductors 1 and 2 currents.

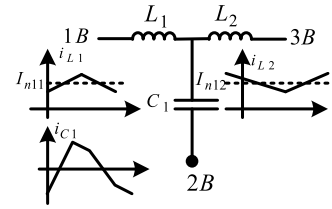


FIGURE 4. Filter block and associated current waveforms.

TABLE 4. Currents in the components of filter block.

L ₁	L ₂	I _{C1}
I _{L1}	I _{L2}	I _{L1} + I _{L2}
I _{L1}	I _{L2}	I _{L1} + I _{L2}

Moreover, inductor currents will be dictated by those of the stage connecting to the filter block.

The relevant expressions for the 3-terminal filter block are obtained with reference to Fig. 4 as

$$I_{L1,ave} = I_{L2,ave} \xrightarrow{\text{yields}} G_{I_{L1} \rightarrow I_{L2}} = \frac{I_{L2,ave}}{I_{L1,ave}} = 1 \quad (22)$$

$$I_{L1,ave} = I_{L2,ave} \rightarrow I_{n11} = I_{n12} \quad (23)$$

$$I_{C1,ave} = 0 \quad (24)$$

It is seen from (22) that for the filter block a DC gain (of unity) is only possible between the terminals connecting to inductors i.e. 1B and 3B. It is thus not a viable converter cell on its own.

III. SYNTHESIS OF DC-DC CONVERTERS FROM BASIC BUILDING BLOCKS

This section presents DC-DC converters synthesis from different combinations of the BBBs discussed in the preceding section. Moreover, it demonstrates that the analyses developed in the preceding section, for the various BBBs, remain applicable to the complex converters to be synthesized. Further, switch states and current waveforms will still be dictated by the type of BBBs used to realize a DC-DC converter and the waveforms in Figs. 1-4 apply.

A. CONVERTERS BASED ON TYPE-1 BBBs

There are six different ways of orientating a 3-terminal type-1 BBB to realize converter cells [14], [15], [17]. This section will present several converters cells that utilize type-1 BBBs, and complex converters synthesized from these converter cells.

1) CONVERTER CELL 1-1.w REALIZED USING A SINGLE TYPE-1 BBB

A 3-terminal converter cell gives rise to 6 DC-DC converters. Fig. 5 shows the three unique DC-DC converters obtained from a single type-1 BBB, with the remaining three converters being not unique. These three DC-DC converters are commonly referred to as buck, boost and buck-boost in

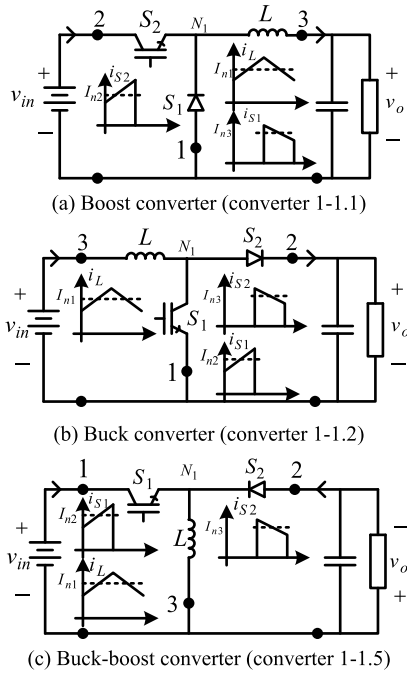


FIGURE 5. Three unique DC-DC converters obtained from a single type-1 basic building block.

the literature. Equations (1)-(7) and Table 1 apply to these converters. Moreover, for a given DC-DC converter, interchanging source and load leads to the inverse of the gain of the converter with the initial source and load connection. Hence, interchanging the position of source and load in Figs. 5(a), 5(b) and 5(c) leads to the inverse of the gains in (5), (6) and (7) respectively. The converter waveforms are essentially those for the BBB.

2) CONVERTER CELL 2-1.w REALIZED USING TWO TYPE-1 BBBS

Any two 3-terminal BBBS can be cascaded, stacked, paralleled or differentially connected to realize more complex converters. Fig. 6(a) shows a 3-terminal switching converter cell 2-1.w comprising two type-1 BBBS. Table 5 is obtained from Table 1 by recognizing that there are two type-1 BBBS. It shows the permissible switch state combinations and currents through various components. Figs. 6(a)-(b) show three converters derived from the converter cell 2-1.w. Fig. 6(b) shows the current path from source to load is through two cascaded type-1 BBBS' stages (S_1 to L and L to S_4). Figs. 6(c)-(d) on the other hand show converters obtained by stacking together two type-1 BBBS. The stacking of the BBBS creates two parallel current paths between input and output. This section will present the derivation of the current gains between the input and output terminals for the three converters using the expressions previously derived for type-1 BBBS. From (1)-(7) and Figs. 1 and 6, the following expressions are obtained:

$$I_{S1,ave} = \delta I_{n1} = \delta I_{L,ave} \tag{25}$$

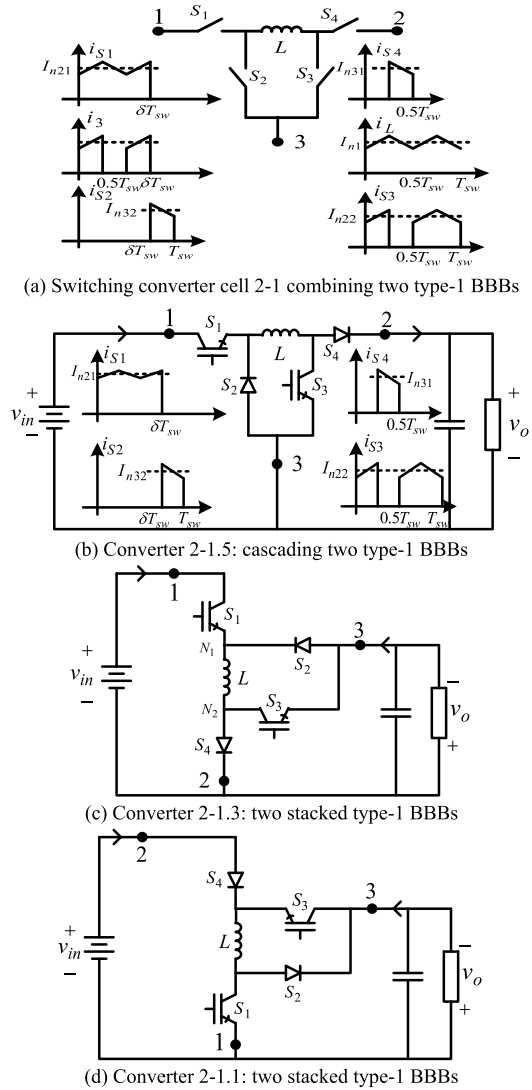


FIGURE 6. Switching converter cell by cascading or stacking two type-1 basic building blocks.

TABLE 5. Permissible switch states and currents flowing through the switches and capacitor in converter cell.

Interval	S_1	S_2	S_3	S_4	I_{S1}	I_{S2}	I_{S3}	I_{S4}
(i)	1	0	1	0	I_L	0	I_L	0
(ii)	1	0	0	1	I_L	0	0	I_L
(iii)	1	0	1	0	I_L	0	I_L	0
(iv)	0	1	1	0	0	I_L	I_L	I_L

$$I_{S4,ave} = (1 - \delta) I_{L,ave} = I_{o,ave} \tag{26}$$

$$I_{3,ave} = I_{S2,ave} - I_{S3,ave} = (1 - \delta) I_{L,ave} - \delta I_{L,ave} = I_{L,ave} (1 - 2\delta) \tag{27}$$

From (25)-(27) and Figs. 6(b)-(d), current gains of the three converters are obtained as

$$G_{I_{S1} \rightarrow I_{S4}} = \frac{I_{S4,ave}}{I_{S1,ave}} = \frac{I_{S4,ave}}{I_{L,ave}} \times \frac{I_{L,ave}}{I_{S1,ave}} = (1 - \delta) \times \frac{1}{\delta} = \frac{1 - \delta}{\delta} \tag{28a}$$

$$G_{I_{S1} \rightarrow I_3} = \frac{I_{3,ave}}{I_{S1,ave}} = \frac{I_{S2,ave}}{I_{S1,ave}} - \frac{I_{S3,ave}}{I_{L,ave}} \times \frac{I_{L,ave}}{I_{S1,ave}}$$

$$G_{I_{S1} \rightarrow I_3} = \frac{1-\delta}{\delta} - \delta \times \frac{1}{\delta} = \frac{1-2\delta}{\delta} \quad (28b)$$

$$G_{I_{S4} \rightarrow I_3} = \frac{I_{3,ave}}{I_{S4,ave}} = \frac{I_{S2,ave}}{I_{L,ave}} \times \frac{I_{L,ave}}{I_{S4,ave}} - \frac{I_{S3,ave}}{I_{S4,ave}}$$

$$G_{I_{S4} \rightarrow I_3} = (1-\delta) \times \frac{1}{1-\delta} - \frac{1}{1-\delta} = \frac{1-2\delta}{1-\delta} \quad (28c)$$

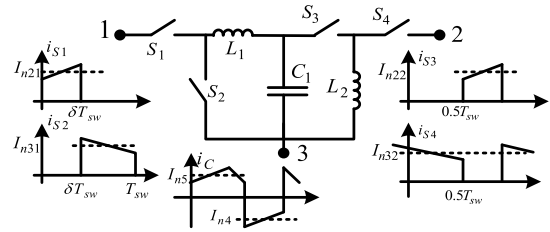
Fig. 6(b) and (28a) reveal that the input-output current gain is the product of the gains of the two cascaded BBBs' stages (i.e. S_4 to L and L to S_1). The BBBs' stages contribute buck and boost current gains respectively, and overall gain corresponding to buck-boost functionality. Fig. 6(c) and (28b) show that stacking the BBBs creates two parallel current paths from source to load. The first current path is through a single type-1 BBB stage (S_3 to S_4) and it contributes a buck-boost gain. The second current path gain is the product of the two type-1 BBBs' stages (S_2 to L and L to S_4), and it contributes boost and buck gains respectively. The currents in the two paths are in opposite directions. Consequently, the overall current gain is the difference between the two parallel paths' gains, and buck (boost) functionality for current (voltage) is achieved. Fig. 6(d) and (28c) show that the gain of the first current path with two cascaded stages (L to S_2 and S_4 to L) is the product of stage gains, and for the second path it is that of the single type-1 BBB stage. Overall gain is the difference between the two current paths' gains, and boost (buck) functionality for current (voltage) is achieved. Similar reasoning is applicable to all converters comprising type-1 BBBs.

3) CONVERTER CELL 2-2.w REALIZED USING TWO TYPE-1 BBBs

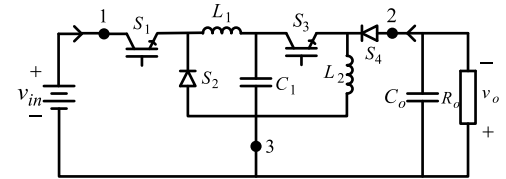
Fig. 7(a) shows a switching converter cell 2-2.w comprising of two type-1 BBBs and an inter-stage capacitor connected at node N_2 . Node N_2 could also be associated with a type-3 BBB made up of S_2 , S_3 and C_1 . The inter-stage capacitor acts as an intermediate output and input (sink and source), for the first and second stage, so its role is no more than a filtering stage. Table 6 is obtained from Tables 1 and 2, and it presents switch state combinations and currents through various components in converter cell 2-2.w. The gate signals for the two active switches S_1 and S_2 are manipulated in such a way to realize 180° out of phase operation of the cascaded converter cells to improve current and voltages. This type of gate control is applicable to all converters with 2 active switches studied in this paper. The restrictions on the possible switch state combinations for type-1 BBBs and the 180° phase-shift between the signals of the two type-1 BBBs dictate the switching pattern in Table 6. Moreover, for the active switches $\delta < 0.5$ but if $\delta > 0.5$ switch states are determined from Table 5.

From (1)-(7) and Figs. 1, 2 and 7, the following expressions are obtained

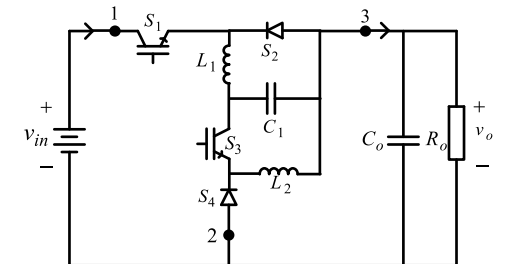
$$I_{n12} = I_{L2,ave} \quad (29)$$



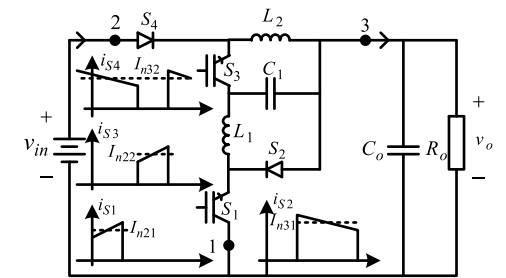
(a) Switching converter 2-2 comprising two type-1 BBBs



(b) Converter 2-2.5: two cascaded type-1 BBBs



(c) Converter 2-2.3: two stacked type-1 BBBs



(d) Converter 2-2.1: two stacked type-1 BBBs

FIGURE 7. Switching converter cell 2-2.w comprising two type-1 BBBs plus an inter-stage capacitor and three converters based on it.

TABLE 6. Switch states combinations and currents flowing through the switches and capacitor in Cell 2-2.w.

Interval	S_1	S_2	S_3	S_4	I_{S1}	I_{S2}	I_{S3}	I_{S4}	I_{C1}
(i)	1	0	0	1	I_{L1}	0	0	I_{L2}	0
(ii)	0	1	0	1	0	I_{L1}	0	I_{L2}	I_{L1}
(iii)	0	1	1	0	0	I_{L1}	I_{L2}	0	$I_{L1} - I_{L2}$
(iv)	0	1	0	1	0	I_{L1}	0	I_{L2}	I_{L1}

$$I_{S3,ave} = I_{L1,ave} = I_{n11} \quad (30)$$

$$I_{3,ave} = I_{L2,ave} - I_{S2,ave} = I_{L2,ave} - (1-\delta)I_{L1,ave} = I_{L2,ave} (1-\delta-\delta^2) \quad (31)$$

From (29)-(31) and Figs. 1, 2 and 7, current gains of converters in Figs. 7(b)-(d) are obtained as

$$\frac{I_{S4,ave}}{I_{S1,ave}} = \frac{I_{S4,ave}}{I_{S3,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}} = \frac{1-\delta}{\delta} \times \frac{1}{\delta} = \frac{1-\delta}{\delta^2} \quad (32a)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{S1,ave}} &= \frac{I_{L2,ave}}{I_{S3,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}} - \frac{I_{S2,ave}}{I_{S1,ave}} = \frac{1}{\delta} \times \frac{1}{\delta} - \frac{1-\delta}{\delta} \\ &= \frac{1-\delta+\delta^2}{\delta^2} \end{aligned} \quad (32b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{S4,ave}} &= \frac{I_{L2,ave}}{I_{S4,ave}} - \frac{I_{S2,ave}}{I_{L1,ave}} \times \frac{I_{S3,ave}}{I_{S4,ave}} = \frac{1}{\delta} - \delta \times \frac{1-\delta}{\delta} \\ &= \frac{1-\delta+\delta^2}{\delta} \end{aligned} \quad (32c)$$

For cascade BBBs connection, (32a) shows that overall gain is the product of path stage gains. For stacked BBBs connections in Figs. 7(c) and (d) there are two parallel current paths in each case. Equations (32b) and (32c) show the overall gain as the difference between the gains of the two parallel current paths. The waveforms are again dictated by the BBBs. The type-3 BBB associated with the inter-stage capacitor is not necessary for gain evaluation but does play a useful role in predicting current waveforms.

4) CONVERTER CELL 2-3.w REALIZED USING TWO TYPE-1 BBBs

Fig. 8(a) shows switching converter cell 2-3.w comprising two type-1 BBBs and an inter-stage capacitor connected at node N_2 . Node N_2 could also be associated with a type-3 BBB made up of S_2 , S_3 and C_1 . Table 6 is applicable to converter cell 2-3.w as well for operation with $\delta < 0.5$.

From (1)-(7) and Figs. 1, 3 and 8, the following expressions are obtained

$$I_{n11} = I_{n21} = I_{n31} = I_{L1,ave} \quad (33)$$

$$I_{n12} = I_{n22} = I_{n32} = I_{L2,ave} \quad (34)$$

$$I_{S3,ave} = I_{S2,ave} \rightarrow \delta I_{L2,ave} = (1-\delta) I_{L1,ave} \quad (35)$$

$$I_{3,ave} = I_{L2,ave} - I_{L1,ave} = I_{L1,ave} \frac{(1-2\delta)}{\delta} = I_{L2,ave} \frac{(1-2\delta)}{1-\delta} \quad (36)$$

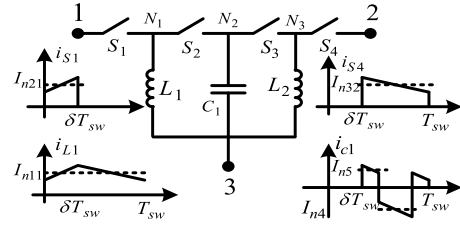
From (33)-(36) and Figs. 1, 3 and 8, current gains for converters in Figs. 8(b)-(d) are obtained as

$$\frac{I_{S4,ave}}{I_{S1,ave}} = \frac{I_{S4,ave}}{I_{S3,ave}} \times \frac{I_{S2,ave}}{I_{S1,ave}} = \frac{1-\delta}{\delta} \times \frac{1-\delta}{\delta} \quad (37a)$$

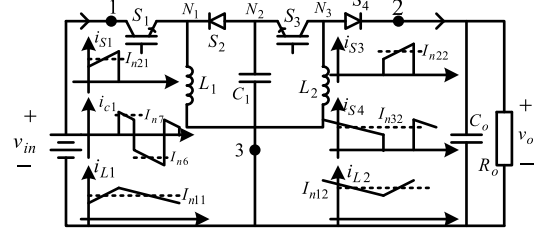
$$\begin{aligned} \frac{I_{3,ave}}{I_{S1,ave}} &= \frac{I_{L2,ave}}{I_{S3,ave}} \times \frac{I_{S2,ave}}{I_{S1,ave}} - \frac{I_{L1,ave}}{I_{S1,ave}} = \frac{1}{\delta} \times \frac{1-\delta}{\delta} - \frac{1}{\delta} \\ &= \frac{1-2\delta}{\delta^2} \end{aligned} \quad (37b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{S4,ave}} &= \frac{I_{L2,ave}}{I_{S4,ave}} - \frac{I_{L1,ave}}{I_{S2,ave}} \times \frac{I_{S3,ave}}{I_{S4,ave}} = \frac{1}{1-\delta} - \frac{1}{1-\delta} \\ &\times \frac{\delta}{1-\delta} = \frac{1-2\delta}{(1-\delta)^2} \end{aligned} \quad (37c)$$

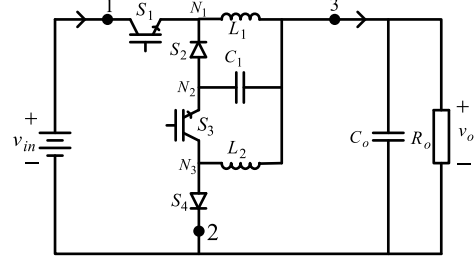
Fig. 8(b) shows cascade connection of two type-1 buck-boost stages and (37a) gives the overall gain as the product of two buck-boost stages' gains. Figs. 8(c) and (d) on the other hand show stacked connections of two boost stages. Equations (37b) and (37c) give an overall gain as the difference of the two parallel current paths' individual gains. The contributions towards a path gain by the BBBs' stages in a given current paths are clearly evident.



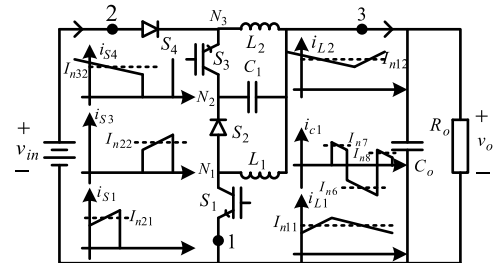
(a) Switching converter 2-3 comprising two type-1 BBBs



(b) Converter 2-3.5: two type-1 BBBs cascaded



(c) Converter 2-3.3: two stacked type-1 BBBs



(d) Converter 2-3.1: two stacked type-1 BBBs

FIGURE 8. Switching converter cell 2-3.w comprising two type-1 BBBs plus an inter-stage capacitor and three converters based on it.

5) CONVERTER CELL 2-4.w REALIZED USING TWO TYPE-1 BBBs

Fig. 9 shows switching converter cell 2-4.w comprising two type-1 BBBs and an inter-stage capacitor, C_1 . Node N_2 can also be associated with a type-4 BBB made up of L_1 , L_2 and C_1 . Currents through C_1 are therefore a combination of currents from the two type-1 BBBs. Table 6, obtained by recognizing that there are two type-1 BBBs is applicable to converter cell 2-4.w when $\delta < 0.5$. Table 5 applies for operation with $\delta > 0.5$.

From (1)-(7) and Figs. 1, 4 and 9, the following expressions are obtained

$$I_{n11} = I_{n21} = I_{n31} = I_{L1,ave} \quad (38)$$

$$I_{n12} = I_{n22} = I_{n32} = I_{L2,ave} \quad (39)$$

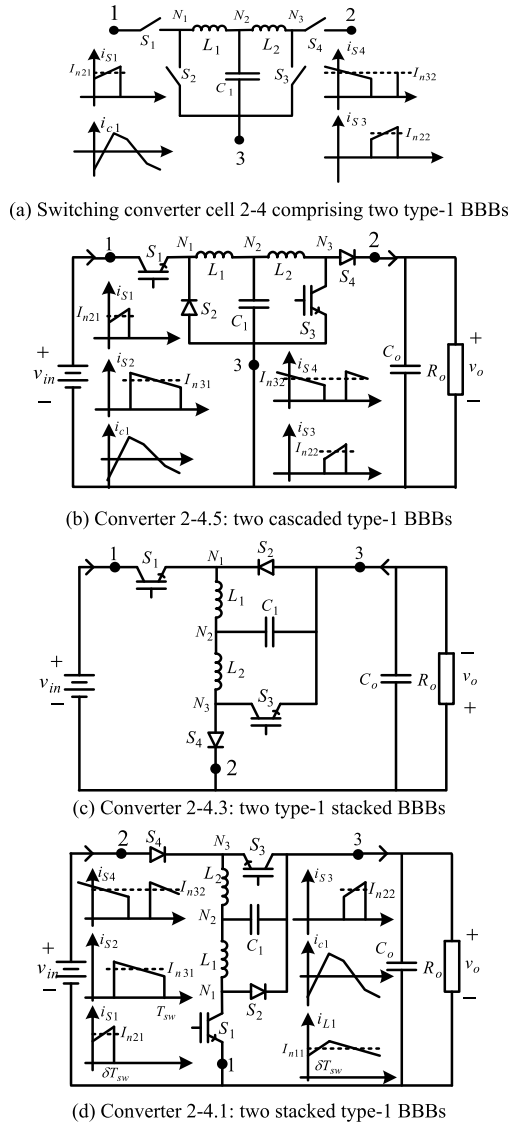


FIGURE 9. Switching converter cell 2-4.w comprising two type-1 BBBs plus an inter-stage capacitor and three converters derived from it.

$$I_{L1,ave} = I_{L2,ave} \tag{40}$$

$$I_{3,ave} = I_{S2,ave} - I_{S3,ave} = I_{L1,ave} (1 - 2\delta) = I_{L2,ave} (1 - 2\delta) \tag{41}$$

From (38)-(41) and Figs. 1, 4 and 9 current gains for the converters in Figs. 9(b)-(d) are obtained as

$$\frac{I_{S4,ave}}{I_{S1,ave}} = \frac{I_{S4,ave}}{I_{L2,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}} = (1 - \delta) \times \frac{1}{\delta} = \frac{1 - \delta}{\delta} \tag{42a}$$

$$\frac{I_{3,ave}}{I_{S1,ave}} = \frac{I_{S2,ave}}{I_{S1,ave}} - \frac{I_{S3,ave}}{I_{L2,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}} = \frac{1 - \delta}{\delta} - \delta \times \frac{1}{\delta} = \frac{1 - 2\delta}{\delta} \tag{42b}$$

$$\frac{I_{3,ave}}{I_{S4,ave}} = \frac{I_{S2,ave}}{I_{L1,ave}} \times \frac{I_{L2,ave}}{I_{S4,ave}} - \frac{I_{S3,ave}}{I_{S4,ave}} = (1 - \delta) \times \frac{1}{1 - \delta} - \frac{\delta}{1 - \delta} = \frac{1 - 2\delta}{1 - \delta} \tag{42c}$$

Expression (42a) shows that the buck-boost functionality is realized by the cascading of boost and buck BBBs stages. Equations (42b) and (42c) yield respectively buck (boost) and buck-boost (buck-boost) functionalities for current (voltage) as a result of stacked connection of buck and buck-boost stages.

6) CONVERTER CELL 3-2.w REALIZED USING TYPE-1 AND TYPE-2 BBBs

Fig. 10(a) shows a 3-terminal switching converter cell 3-2.w combining a type-1 and a type-2 BBBs. The permissible switch states are similar to those in Table 1. From (1)-(7), (8)-(16), Figs. 1, 2 and 10 the following expressions are obtained:

$$I_{S2,ave} = I_{L2,ave} \quad \& \quad I_{3,ave} = I_{S1,ave} \tag{43}$$

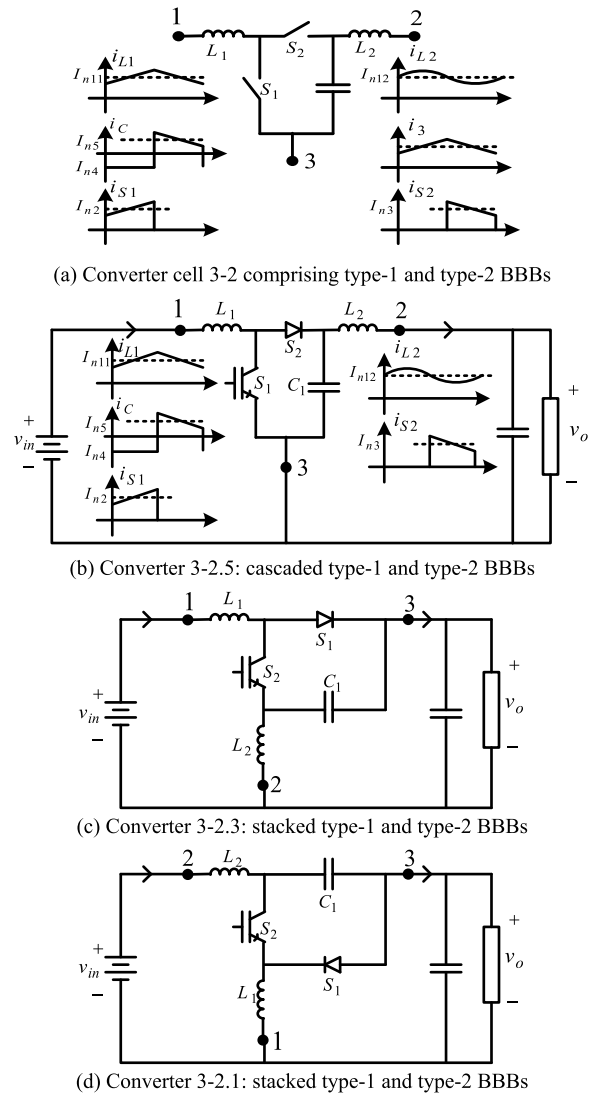


FIGURE 10. Switching converter cell 3-2.w comprising type-1 and type-2 BBBs and three converters derived from it.

From (43) and Figs. 1 and 9, current gains for the converters in Figs. 10(b)-(d) are obtained as

$$\frac{I_{L2,ave}}{I_{L1,ave}} = \frac{I_{L2,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{L1,ave}} = 1 \times (1 - \delta) = 1 - \delta \quad (44a)$$

$$\frac{I_{3,ave}}{I_{L1,ave}} = \frac{I_{S1,ave}}{I_{L1,ave}} + \frac{I_{C,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{L1,ave}} = 1 - \delta + 0 = 1 - \delta \quad (44b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L2,ave}} &= \frac{I_{C,ave}}{I_{L2,ave}} + \frac{I_{S1,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{L2,ave}} = 0 + \frac{1 - \delta}{\delta} \times 1 \\ &= \frac{1 - \delta}{\delta} \end{aligned} \quad (44c)$$

From (44a) and Fig. 10(b), the gain from source to load is the product of a type-1 BBB stage (L_1 to S_2) and a type-2 BBB stage (S_2 to L_2) gains. The type-1 and type-2 BBBs contribute buck and unity gains respectively, and overall buck functionality. Figs. 10(c) and 10(d) show two parallel paths between source and load due to stacking of BBBs. However, a capacitor blocks DC current flow in one of the paths. From (44b) the gain is therefore obtained as that of type-1 BBB (L_1 to S_1) buck functionality. From (44c), the overall gain is the product of type-1 (S_1 to S_2) and type-2 (L_2 to S_2) BBB stages contribute buck-boost and unity gains respectively, and hence overall buck-boost functionality. Converter cell 3-2.w could also be viewed as a type-1 BBB plus a CL-filter. Compared with converter cell 1-1.w, including the CL-filter leads to significant benefits as continuous current waveform are generated at all three terminals.

7) CONVERTER CELL 1-2.w REALIZED USING TYPE-1 AND BBB AND A FILTER BLOCK

Fig. 11(a) shows a 3-terminal switching converter cell 1-2.w comprising a type-1 BBB and a filter block. The permissible switch states combinations are similar to those in Table 1. From (1)-(7), (8)-(16), Figs. 1, 4 and 11 the following expressions are obtained:

$$I_{n11} = I_{L1,ave} = I_{L2,ave} = I_{n12} \quad (45)$$

$$I_{3,ave} = I_{S2,ave} = (1 - \delta) I_{L1,ave} = (1 - \delta) I_{L2,ave} \quad (46)$$

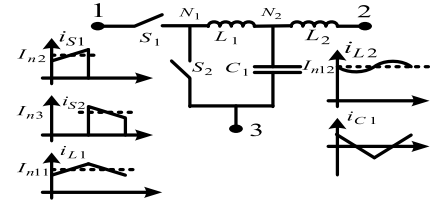
From (45)-(46) and Figs. 1, 4 and 11 current gains for the converters in Figs. 11(b)-(d) are obtained as

$$\frac{I_{L2,ave}}{I_{S1,ave}} = \frac{I_{L1,ave}}{I_{S1,ave}} \times \frac{I_{L2,ave}}{I_{L1,ave}} = \frac{1}{\delta} \times 1 = \frac{1}{\delta} \quad (47a)$$

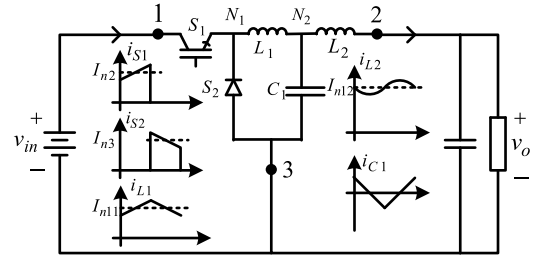
$$\begin{aligned} \frac{I_{3,ave}}{I_{S1,ave}} &= \frac{I_{C,ave}}{I_{L1,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}} + \frac{I_{S2,ave}}{I_{S1,ave}} = 0 \times \frac{1}{\delta} + \frac{1 - \delta}{\delta} \\ &= \frac{1 - \delta}{\delta} \end{aligned} \quad (47b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L2,ave}} &= \frac{I_{S2,ave}}{I_{L1,ave}} \times \frac{I_{L1,ave}}{I_{L2,ave}} + \frac{I_{C,ave}}{I_{L2,ave}} = (1 - \delta) \\ &\times 1 + 0 = 1 - \delta \end{aligned} \quad (47c)$$

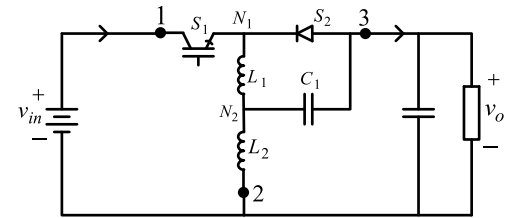
Equations 47(a)-47(c) show that cascading or stacking a type-1 BBB and a filter block yields a gain identical to that of the employed BBB. Converter cell 1-2.w could also be viewed as a type-1 BBB plus a CL-filter. Compared with



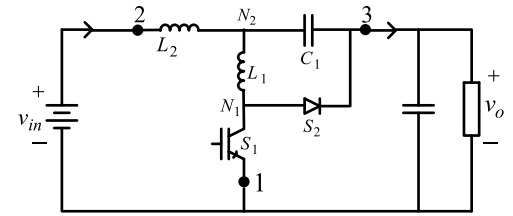
(a) Converter cell 1-2: 1 type-1BBB and filter block



(b) Converter 1-2.5: cascaded type-1 BBB and filter block



(c) Converter 1-2.3: stacked type-1 BBB and filter block



(d) Converter 1-2.1: stacked type-1 BBB and filter block

FIGURE 11. Switching converter cell comprising type-1 and filter block BBBs and three DC-DC converters based on the converter cell.

converter cell 1-1.w, including the CL-filter does not lead to any significant benefits as both generate a continuous current waveform at one terminal and pulsed current at the other two terminals.

B. CONVERTER CELLS BASED ON TYPE-2 BBBs

There are several possibilities of connecting two variants of type-2 BBB to realize a converter cell. The primary goal is to ensure charge and discharge intervals for both inductor and capacitor such that average inductor voltage and average capacitor current are zero. Additionally, guarantee DC currents at all three converter-cell terminals. Cascaded and stacked connections will meet all the above requirements. This section will present two such converter cells and the converters obtained from them.

1) CONVERTER CELL 1-4.w REALIZED USING THE TWO VARIANTS OF TYPE-2 BBB

Fig. 12(a) shows a converter switching cell 1-4.w comprising two type-2 BBBs. Figs. 12(b)-(d) show three DC-DC

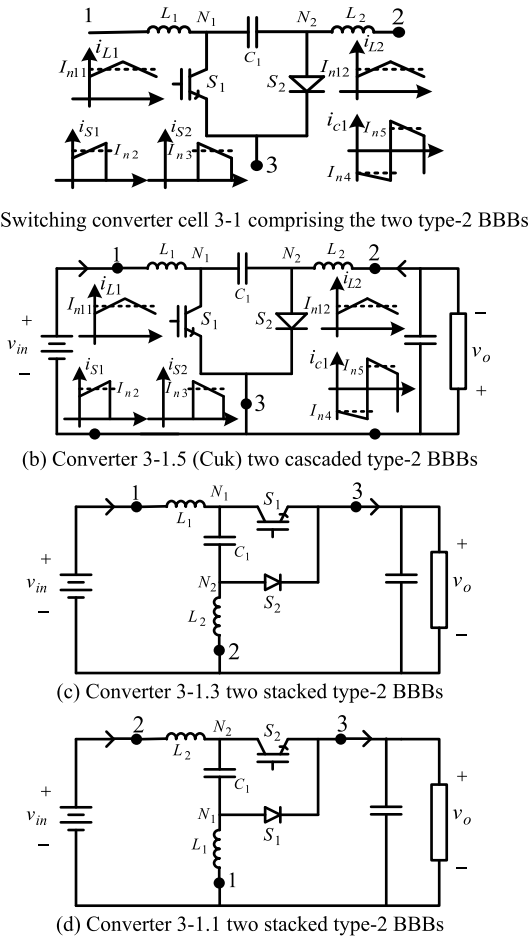


FIGURE 12. Converter cell 1-4.w: three of its DC-DC converters and current waveforms for various components.

TABLE 7. Permissible switch states and current flowing through the switches and capacitor of the converter cell.

S_1	S_2	I_{S1}	I_{C1}	I_{S2}
0	1	0	$I_{N3} = I_{L1}$	$I_{N3} = I_{L2} + I_{C1}$
1	0	$I_{L1} + I_{C1}$	$-I_{N1} = -I_{L2}$	0

converters realized using cell 1-4.w. Table 7 is obtained from Table 2 and shows the permissible switch states combinations and currents through the various components.

From (8)-(16), Figs. 1 and 12 the following expressions are obtained

$$I_{S1,ave} = I_{L1,ave} = I_{n11} \quad (48)$$

$$I_{n4} = I_{L2,ave} \quad \& \quad I_{n5} = I_{L1,ave} \quad (49)$$

$$I_{n2} = I_{L1,ave} + I_{L2,ave} = I_{n3} \quad (50)$$

$$I_{S2,ave} = I_{L2,ave} = I_{n12} \quad (51)$$

$$I_{3,ave} = I_{L2,ave} - I_{S1,ave} = I_{L2,ave} - I_{L1,ave} \quad (52)$$

From Figs. 1 and 12 and (48)-(52), current gains for the converters in Figs. 12(b)-(d) are obtained as

$$G_{I_{L1} \rightarrow I_{S2}} = \frac{I_{S2,ave}}{I_{L1,ave}} = \frac{(1 - \delta) (I_{L1,ave} + I_{L2,ave})}{\delta (I_{L1,ave} + I_{L2,ave})} = \frac{1 - \delta}{\delta} \quad (53a)$$

$$G_{I_{L1} \rightarrow I_3} = \frac{I_{3,ave}}{I_{L1,ave}} = \frac{I_{L1,ave}}{I_{L1,ave}} - \frac{I_{L2,ave}}{I_{L1,ave}} = 1 - \frac{\delta (I_{L1,ave} + I_{L2,ave})}{(1 - \delta) (I_{L1,ave} + I_{L2,ave})}$$

$$G_{I_{L1} \rightarrow I_3} = 1 - \frac{\delta}{1 - \delta} = \frac{1 - 2\delta}{1 - \delta} \quad (53b)$$

$$G_{I_{S2} \rightarrow I_3} = \frac{I_{3,ave}}{I_{S2,ave}} = \frac{I_{L2,ave}}{I_{S2,ave}} - \frac{I_{L1,ave}}{I_{S2,ave}} = 1 - \frac{\delta (I_{L1,ave} + I_{L2,ave})}{(1 - \delta) (I_{L1,ave} + I_{L2,ave})}$$

$$G_{I_{S2} \rightarrow I_3} = 1 - \frac{\delta}{1 - \delta} = \frac{1 - 2\delta}{1 - \delta} \quad (53c)$$

Fig. 12(b) shows a cascade connection of the two type-2 BBBs variants. Unlike in the case of type-1 BBBs cascade, there is no direct path for DC current between source and load. Energy transfer is through the capacitor and buck-boost functionality. Equation (53a) shows that the gain for converter in Fig. 12(b) is equal to the ratio of $I_{L1,ave}$ to $I_{L2,ave}$ yielding a buck-boost functionality is obtained. From Figs. 12(c) and (d), stacking of the two type-2 BBBs variants creates one direct path of DC current flow between source and load and a second indirect path. The direct path comprises a single unity gain stage while the second path entails energy transfer through the capacitor and contributes buck-boost functionality. From (53b) and (53c), the gains are obtained as the difference between unity gain and ratio of $I_{L2,ave}$ to $I_{L1,ave}$ and $I_{L1,ave}$ to $I_{L2,ave}$. Actually, the overall gains are the differences between the gains of the two parallel current paths. In all instances gains are obtained in terms of ratios between inductor currents. This is a feature of converters employing type-2 BBBs.

2) CONVERTER CELL 3-1.w REALIZED USING THE TWO VARIANTS OF TYPE-2 BBB

Fig. 13(a) shows switching converter cell 3-1.w comprising the two type-2 BBBs variants. Tables 2 and 7 show the applicable switch state combinations and currents through various components.

From (8)-(16) and Figs. 2 and 13 the following expressions are obtained

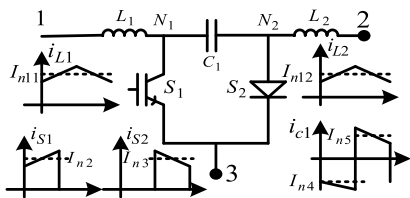
$$I_{S1,ave} = I_{L1,ave} \quad (54)$$

$$I_{S2,ave} = I_{L2,ave} \quad (55)$$

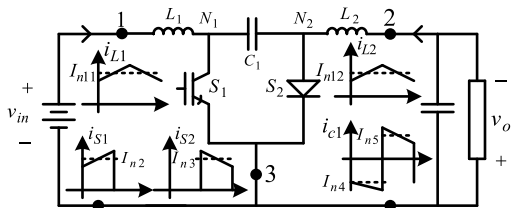
$$I_{n4} = I_{L2,ave} \quad \& \quad I_{n5} = I_{L1,ave} \quad (56)$$

$$I_{n2} = I_{L1,ave} + I_{L2,ave} = I_{n3} \quad (57)$$

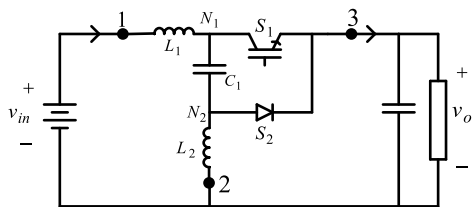
$$I_{3,ave} = I_{L1,ave} + I_{L2,ave} \quad (58)$$



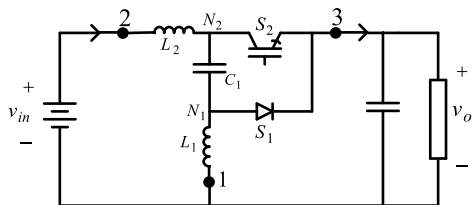
(a) Switching converter cell 3-1 comprising the two type-2 BBBs



(b) Converter 3-1.5 (Cuk) two cascaded type-2 BBBs



(c) Converter 3-1.3 two stacked type-2 BBBs



(d) Converter 3-1.1 two stacked type-2 BBBs

FIGURE 13. Switching converter cell 3-1.w comprising the two type-2 BBBs and three converters derived from it.

From (54)-(58) and Figs. 13, current gains for the converters in Figs. 13(b)-(d) are obtained as

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{L2,ave}}{I_{L1,ave}} = \frac{(1 - \delta) (I_{L1,ave} + I_{L2,ave})}{\delta (I_{L1,ave} + I_{L2,ave})} = \frac{1 - \delta}{\delta} \quad (59a)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L1,ave}} &= \frac{I_{S1,ave}}{I_{L1,ave}} + \frac{I_{S2,ave}}{I_{L1,ave}} \\ &= 1 + \frac{(1 - \delta) (I_{L1,ave} + I_{L2,ave})}{\delta (I_{L1,ave} + I_{L2,ave})} = 1 + \frac{1 - \delta}{\delta} = \frac{1}{\delta} \end{aligned} \quad (59b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L2,ave}} &= \frac{I_{L1,ave}}{I_{L2,ave}} + \frac{I_{L2,ave}}{I_{L2,ave}} = 1 + \frac{\delta (I_{L1,ave} + I_{L2,ave})}{(1 - \delta) (I_{L1,ave} + I_{L2,ave})} \\ &= 1 + \frac{1 - \delta}{\delta} = \frac{1}{\delta} \end{aligned} \quad (59c)$$

Again, cascade connection of the two type-2 BBBs variants does not yield a direct path between source and load for DC current. Energy transfer is purely through the capacitor as an intermediate storage yielding buck-boost functionality.

Equations (59a) to (59c) express the functionalities (in terms of current gains) of the DC-DC converters synthesized using two type-2 BBBs. These are all functions of ratios of the currents in the two inductors. Despite the complexities of the DC-DC converters in Fig. 13 (b)-(d), their functionalities and control range and order are identical to that of the simplest type-1 BBBs.

C. DC-DC CONVERTERS REALIZED USING TYPE-1, TYPE-2 AND TYPE-3 BBBs

Fig. 14 shows switching converter cell 3-4.w comprising 1 type-1, 1 type-2 and 1 type-3 BBBs associated with three nodes (N_1 , N_2 and N_3). This is an example of a converter cell utilizing three types of BBBs. Node N_1 links up 4 components (L_1 , S_1 , C_1 , S_4) and this sub-circuit comprises 1 type-2 (L_1 , S_4 , conductor) and 1 type-3 (conductor, S_1 , C_1) BBBs. The doubling of ripple frequency in i_{L2} and the peculiar shapes of i_3 and i_{C1} resembling doubling of ripple frequency are due to active switches' gate signals being 180° out of phase. Tables 1, 3 and 7, (1)-(7) and Figs. 1, 3 and 14 are applicable.

From (1)-(7) and Figs. 1, 3 and 14 the following expressions are obtained

$$I_{S1,ave} = I_{cond,ave} \quad (60)$$

$$I_{S3,ave} = I_{S2,ave} \quad (61)$$

$$I_{S4,ave} = I_{cond,ave} + I_{L1,ave} \quad (62)$$

$$I_{N21} = I_{N31} = I_{L2,ave} \quad (63)$$

$$I_{N22} = I_{N11} + I_{N12} = I_{L1,ave} + I_{L2,ave} = I_{N32} \quad (64)$$

$$I_{N3,ave} = I_{S3,ave} + I_{S4,ave} = I_{L1,ave} + I_{L2,ave} \quad (65)$$

From Figs. 1, 3 and 14 and (60)-(65) current gains for the converters in Figs. 14(b)-(d) are obtained as

$$\frac{I_{L2,ave}}{I_{L1,ave}} = \frac{I_{L2,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{cond,ave}} \times \frac{I_{cond,ave}}{I_{L1,ave}} = \frac{1 - \delta}{2\delta - 1} \quad (66a)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L1,ave}} &= \frac{(I_{L1,ave} + I_{L2,ave})}{I_{L1,ave}} = \frac{I_{S4,ave}}{I_{L1,ave}} + \frac{I_{S3,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{S1,ave}} \\ &\quad \times \frac{I_{S1,ave}}{I_{cond,ave}} \times \frac{I_{cond,ave}}{I_{L1,ave}} \\ &= 1 + \frac{1 - \delta}{2\delta - 1} = \frac{\delta}{2\delta - 1} \end{aligned} \quad (66b)$$

$$\begin{aligned} \frac{I_{3,ave}}{I_{L2,ave}} &= \frac{I_{L1,ave}}{I_{L2,ave}} + \frac{I_{L2,ave}}{I_{L2,ave}} = \frac{I_{S3,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{L2,ave}} + \frac{I_{S4,ave}}{I_{cond,ave}} \\ &\quad \times \frac{I_{cond,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{L2,ave}} + 1 \\ &= \frac{(2\delta - 1)}{\delta} + 1 = \frac{1 - \delta}{\delta} \end{aligned} \quad (66c)$$

Fig. 14(b) shows a converter realized through cascade connection of 3 BBBs. Overall gain is the product of the contribution from the three stages as seen in (66a). Figs. 14(c) and (d) on the other hand show a combination of stacked and cascaded BBBs to realize DC-DC converters. Overall gain is buck-boost functionality obtained as the sum of the parallel paths gains. The contributions of the various stages in a given

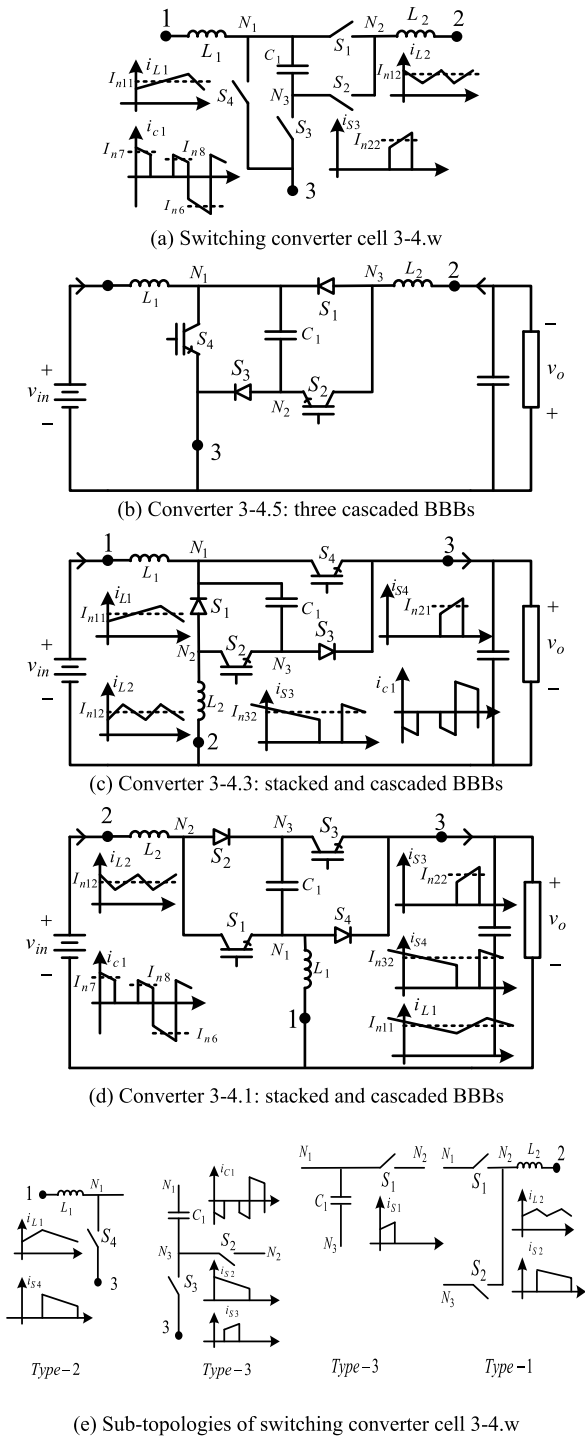


FIGURE 14. Switching converter cell comprising a type-1, type-2 and type-3 BBBs plus some family members of DC-DC converters based on the cell.

current path towards path gain are clearly evident. Converters in Figs. 14(b) and (c) have limited control range.

IV. EXTENDING THE TECHNIQUE TO DC-DC CONVERTERS NOT DERIVED FROM ANY OF THE 14 CONVERTER CELLS

The technique developed in section III for predicting current signals and gains can be applied to converters not derived

directly from the 14 converter cells that were considered in the first part of this study. Sample groups of converters that include non-isolated full-bridge DC-DC converters, interleaved and 3-level DC-DC converters as well as Z-source and quasi-Z-source DC-DC converters will be considered.

Non-isolated full-bridge DC-DC converters are commonly used in high power applications. Figures 15 (a)-(b) present voltage-fed and current-fed full-bridge DC-DC converters [11], [12], [18] while Fig. 15(c) shows a three-level boost DC-DC converter [9]. Each of the three DC-DC converters can be broken up into two type-1 BBBs associated with nodes N_1 (T_1, D_1, L) and N_2 (T_2, D_2, L), as shown in Figs. 15(a)-(c). Those in Figs. 15(a) and (b) are differentially connected while stacked in Fig. 15(c). From Table 1, the applicable switch states combinations and currents through various components are shown in Table 6 for $\delta < 0.5$ and Table 5 for $\delta > 0.5$. They are applicable to the different converter topologies and were used to predict the current waveforms shown in Fig. 15(d).

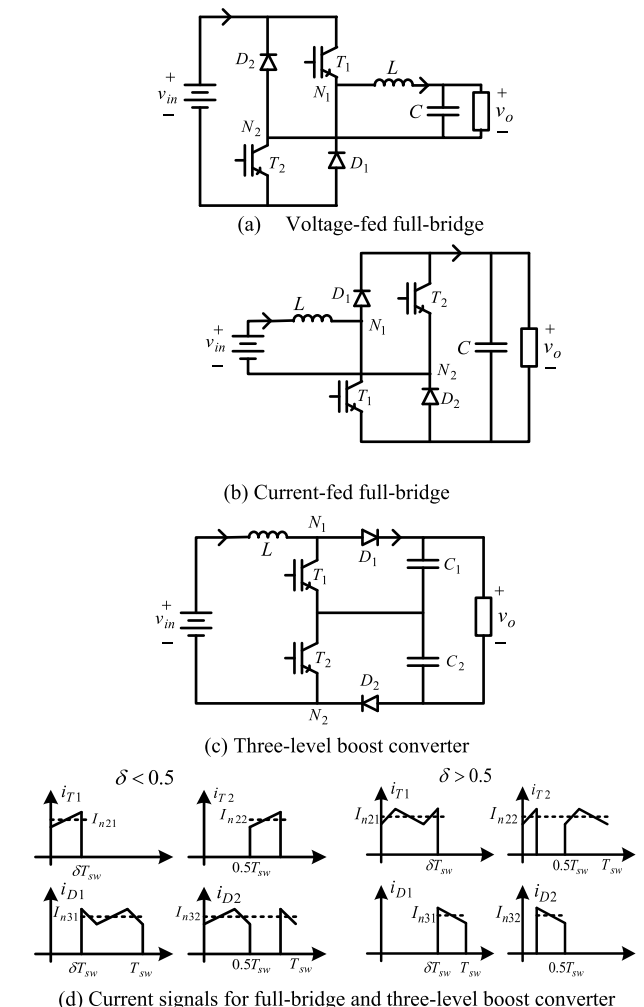


FIGURE 15. Non-isolated full-bridge DC-DC converters and three-level boost converter and associated current signals.

As with other converters with two active switches, gate signals for active switches T_1 and T_2 are 180° out of phase.

Consequently, at any one given time, current flows in a loop that includes one diode (switch) from each of the two BBBs when $\delta < 0.5$ ($\delta > 0.5$). This interaction between the two BBBs gives rise to doubling of ripple frequency in the inductor current. The 180° phase-shift between gate signals of T_1 and T_2 also creates a situation where inductor charging and discharging currents flow through a loop that includes both an active switch and a diode. This is unlike in converters with single active switches where inductor charging current is always through a loop with just an active switch and the discharging current through a diode. For the non-isolated full-bridge DC-DC converters $\delta < 0.5$ is employed for buck functionality while $\delta > 0.5$ is employed in a boost converter. In the case of the three-level boost converter, $\delta < 0.5$ is used when $v_o < 2v_{in}$ and $\delta > 0.5$ is required to obtain $v_o > 2v_{in}$.

Interleaved or multiphase DC-DC converters are modular in construction and offer additional benefits of lower input and output ripple, lower losses, smaller magnetic components and faster inductor current dynamics. Figs. 16(a)-(b) show a 2-phase boost DC-DC converter [9] and associated current signals. This converter comprises two interleaved type-1 BBBs associated with nodes N_1 (T_1, D_1, L_1) and N_2 (T_2, D_2, L_2) shown in Fig. 16(a). Tables 5 and 6 are applicable to this converter too. Unlike in the case of non-isolated full-bridge and three-level boost DC-DC converters, current loops formed do not entail switches from the two separate BBBs. As a result, a switch in one BBB does not provide a path for current flowing in the second one. It is only in the input circuit and output filter capacitor where currents from the two BBBs combine giving rise to doubling of the ripple frequency. Figs. 16(c) presents a Z-source DC-DC converter comprising two stacked type-2 BBBs and cascaded with a third type-2 BBB. Fig. 16(d) shows a quasi-Z-source DC-DC converter, comprising a stacking of the two type-2 BBBs variants. The signals in Fig. 16 (e) are predicted using Tables 2 and 7 and are similar to those shown in Figs. 2, 12 and 13.

Referring to (1)-(7) and Fig. 15(a), voltage-fed full-bridge DC-DC converter current gain is obtained as shown in (67). It is clear from (67) that $\delta > 0.5$ for a voltage-fed converter.

$$I_{in,ave} = I_{T1,ave} - I_{D2,ave} = \delta I_{L,ave} - (1 - \delta) I_{L,ave} \quad (67a)$$

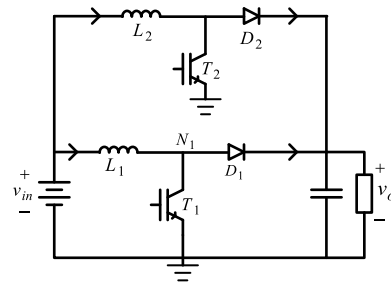
$$I_{D1,ave} = I_{D2,ave} \quad \& \quad I_{T1,ave} = I_{T2,ave} \quad (67b)$$

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{L,ave}}{I_{T1,ave}} \times \frac{I_{T1,ave}}{I_{T1,ave} - I_{D1,ave}} = \frac{1}{\delta} \times \frac{\delta}{2\delta - 1} = \frac{1}{2\delta - 1} \quad (67c)$$

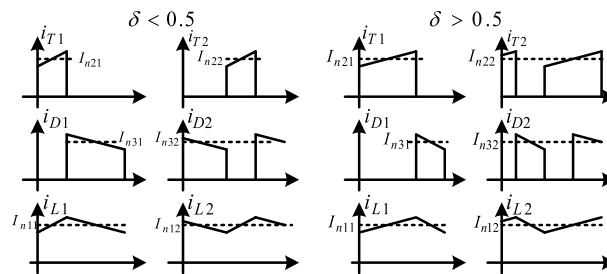
From Fig. 15(a) and (67c), the overall gain is boost. It is obtained as the product of two boost stages' gains (input conductor to T_1 and T_1 to L) and $\delta > 0.5$. Referring to (1)-(7) and Fig. 15(b), current-fed full-bridge DC-DC converter current gain is obtained as shown in (68). It is clear from (68) that $\delta < 0.5$ for a current-fed full-bridge DC-DC converter.

$$I_{o,ave} = I_{D1,ave} - I_{T2,ave} = (1 - \delta) I_{L,ave} - \delta I_{L,ave} \quad (68a)$$

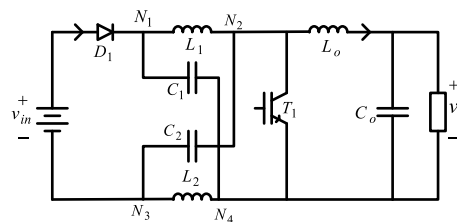
$$I_{D1,ave} = I_{D2,ave} \quad \& \quad I_{T1,ave} = I_{T2,ave} \quad (68b)$$



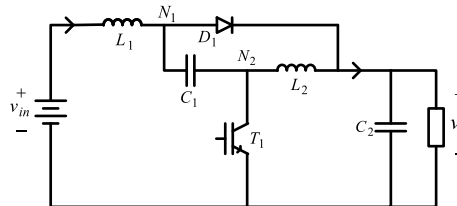
(a) Two-phase boost converter



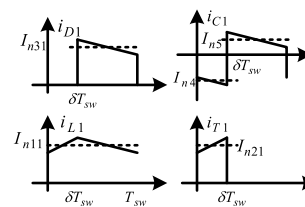
(b) Current signals for two-phase boost converter



(c) Z-source converter



(d) Quasi-Z-source converter



(e) Type-2 BBB waveforms

FIGURE 16. Two-phase boost, Z- and quasi-Z-source converters and associated current signals.

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{o,ave}}{I_{D1,ave}} \times \frac{I_{D1,ave}}{I_{L,ave}} = \frac{1 - 2\delta}{1 - \delta} \times \frac{1 - \delta}{1} = 1 - 2\delta \quad (68c)$$

From Fig. 15(b) and (68c), the overall gain is buck. It is obtained as the product of two buck stages' gains (L to D_1 and D_1 to output terminal conductor) and $\delta < 0.5$. Referring

to (1)-(7) and Fig. 15(c), 3-level boost DC-DC converter current gain is obtained as shown in (69). It is clear from (69) that $0 < \delta < 1$ for a 3-level boost DC-DC converter.

$$I_{o,ave} = I_{D1,ave} = I_{D2,ave} \quad (69a)$$

$$I_{o,ave} = (1 - \delta) I_{L,ave} \quad (69b)$$

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{D1,ave}}{I_{L,ave}} = 1 - \delta \quad (69c)$$

From Fig. 15(c) and (69c), the overall gain is buck. It is obtained as the gain of a single buck stage (L to D₁). From (1)-(7) and Fig. 16(a), 2-phase boost converter current gain is obtained as shown in (70).

$$I_{o,ave} = I_{D1,ave} + I_{D2,ave} \quad (70a)$$

$$I_{D1,ave} = I_{D2,ave} = (1 - \delta) I_{L1,ave} = (1 - \delta) I_{L2,ave} \quad (70b)$$

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{D1,ave}}{I_{L1,ave} + I_{L2,ave}} + \frac{I_{D2,ave}}{I_{L1,ave} + I_{L2,ave}} = \frac{1 - \delta}{2} + \frac{1 - \delta}{2} = 1 - \delta \quad (70c)$$

From Fig. 16(a) and (70c), the overall gain is buck. It is obtained as the sum of two buck stages (L₁ to D₁ and L₂ to D₂). From (8)-(16) and Fig. 16(c), Z-source DC-DC converter current gain is obtained as shown in (71g).

$$I_{S2,ave} = I_{D1,ave} - (1 - \delta) I_{n3} = I_{L1,ave} = I_{cond,ave} \quad (71a)$$

$$I_{cond,ave} = I_{S2,ave} + I_{Lo,ave} = \delta I_{n2} + I_{Lo,ave} \quad (71b)$$

$$I_{n4} = I_{L1,ave} \quad (71c)$$

$$I_{n5} = I_{n3} - I_{L1,ave} \quad (71d)$$

$$\delta I_{n4} = (1 - \delta) I_{n5} \quad (71e)$$

$$I_{n3} = \frac{1}{1 - \delta} I_{L1,ave} = I_{n2} \quad (71f)$$

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{Lo,ave}}{I_{cond,ave}} \times \frac{I_{L1,ave}}{I_{D1,ave}} = \frac{1 - 2\delta}{1 - \delta} \times 1 = \frac{1 - 2\delta}{1 - \delta} \quad (72)$$

Fig.16(c) shows that nodes N₂ and N₄ link up 4 components each. They were thus treated as a combination of 2 3-terminal BBBs as previously discussed for converter cell 3-4.w. From Fig. 16(c) and (71g), the overall gain is buck. It is obtained as the product of three stages' (D₁ to L₁, L₁ to conductor and conductor to L_o) gains and $\delta < 0.5$. From (8)-(16) and Fig. 16(d), quasi-Z-source DC-DC converter current gain is obtained as shown in (73).

$$I_{o,ave} = I_{D1,ave} - I_{L2,ave} = (1 - \delta)(I_{L1,ave} + I_{L2,ave}) - I_{L2,ave} \quad (73a)$$

$$I_{L2,ave} = I_{T1,ave} = \delta (I_{L1,ave} + I_{L2,ave}) \quad (73b)$$

$$\frac{I_{o,ave}}{I_{in,ave}} = \frac{I_{D1,ave}}{I_{L1,ave}} \times \frac{I_{o,ave}}{I_{D1,ave}} = 1 \times \left[(1 - \delta) - \delta \times \frac{\delta}{1 - \delta} \right] = \frac{1 - 2\delta}{1 - \delta} \quad (73c)$$

From Fig. 16(d) and (73c), the overall gain is buck. It is obtained as the product of two stages' (L₁ to D₁ and D₁ to conductor) gains and $\delta < 0.5$. From considering the

connection of the two BBBs, the quasi-Z-source converter is actually derived from converter cell 1-4.w. It is a Zeta converter with position of diode and self-controlled switch interchanged.

V. COMPONENTS' STRESSES

The basic building blocks can also be utilized to determine semiconductor devices' currents and voltage stresses.

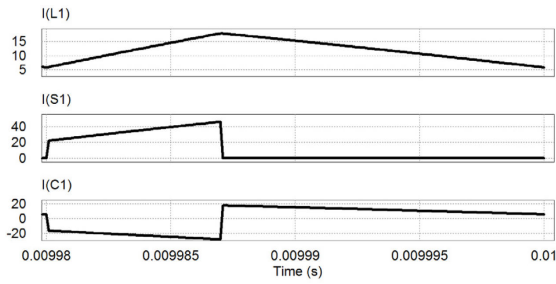
A. CURRENT STRESS

Then nominal magnitude of the current through a component is good measure of the current stress that the component experiences. For the components of a type-1 BBB, Fig. 1 shows the expected current waveforms for the various components. The nominal magnitude of the currents through an active switch and a diode are designated as I_{n2} and I_{n3} respectively. Equation (1) then shows that, for a type-1 BBB the nominal magnitudes of active switch and diode currents are equal to the inductor current. This is true irrespective of the converter in which the BBB is embedded in. The current waveforms generated by a type-2 BBB are shown in Fig. 2. Again, I_{n2} and I_{n3} denote the nominal magnitudes of active switch and diode currents respectively. Equations (11b), (14) and (16) show how to relate semiconductor devices' nominal currents to the two inductor currents. In particular, (16) shows that for a type-2 BBB, semiconductors' devices nominal currents are equal to the sum of the two inductors' currents. For a type-3 BBB, S₂ and S₃ are devices in two separate type-1 BBBs that are interfaced using a capacitor that acts as sink for the preceding BBB and as a source for the BBB that comes after the capacitor. Their current stresses are therefore determined as described for the type-1 BBB.

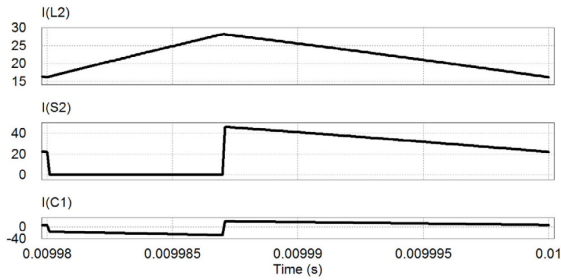
B. VOLTAGE STRESS

The voltage stress experienced by the semiconductor devices of a given BBB is dependent on the terminal of the BBB that is common to both source and load. There are three possible orientations of a BBB. With reference to Fig. 1, one possibility is when terminal 3B is common to both source and load. With this connection, output voltage', v_{2B3B}, has a polarity that is reversed relative to that of the input voltage, v_{1B3B}. This is necessary for proper circuit operation. From Fig. 1, when S₁(S₂) conducts, S₂(S₁) blocks a voltage equal to (v_{1B3B} + v_{2B3B}). If terminal 2B is common to source and load and with source connected across terminals 1B and 2B, device S₁(S₂) blocks a voltage whose magnitude is v_{1B2B} when S₂(S₁) conducts. And when terminal 1B is common to both load and source and with load connected across terminals 3B and 1B, the voltage stress is identical to that for a converter where terminal 2B is common to source and load. However, when source is connected across terminals 3B and 1B, semiconductor device S₁(S₂) block a voltage whose magnitude equal to v_{2B1B} when S₂(S₁) conducts.

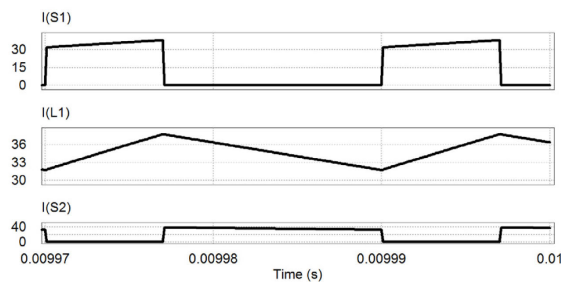
The converter shown in Fig. 12 which employs the two variants of the type-2 BBB will be used to explain how device stresses are evaluated. The evaluation takes advantage



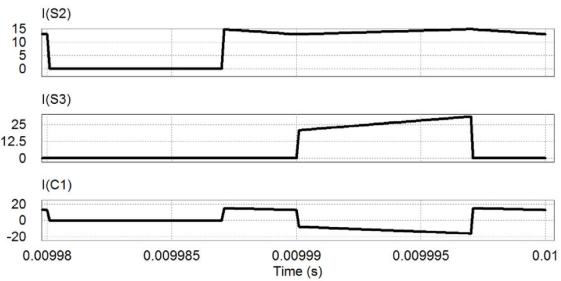
(a) Converter 1-4.1 type-2 variant 1 BBB waveforms



(b) Converter 1-4.1 type-2 variant 2 BBB waveforms



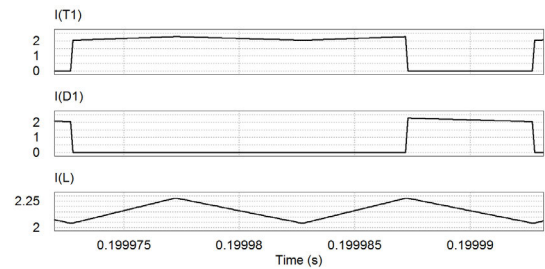
(c) Converter 2-4.1 type-1 BBB waveforms



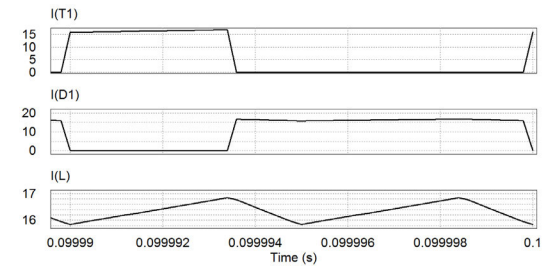
(d) Converter 3-4.1 type-3 BBB waveforms

FIGURE 17. TYPE-1, Type-2 and Type-3 BBBs' current waveforms.

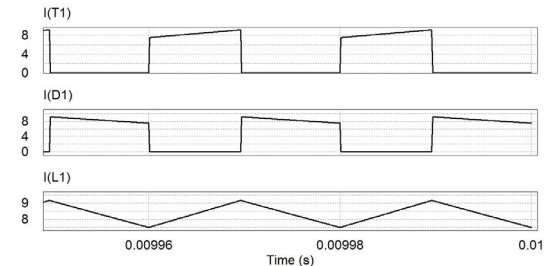
of the fact that the average voltage across an inductor is zero during steady-state operation. First consider operation when terminal 3 is common to both source and load as shown in Fig. 12 (b). Semiconductor device S_1 average voltage is then obtained as v_{13} and v_{32} for S_2 . By considering the interval when the device is conducting or blocking, the blocking voltages are then obtained as $\frac{v_{13}}{1-\delta}$ for S_1 and $\frac{v_{32}}{\delta}$ for S_2 . The average voltage across the BBB's capacitor is obtained as v_{13} . The second scenario is when terminal 2 is common to both source and load as shown in Fig. 12 (b). In this case, the average voltage across S_1 is obtained as $(v_{12} - v_{32})$ and



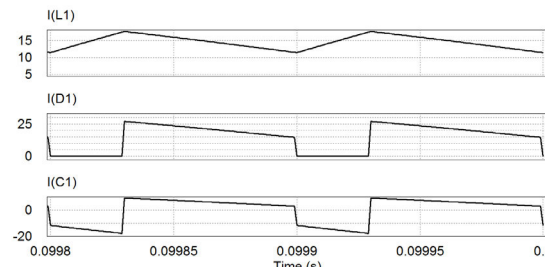
(a) Voltage-fed full-bridge type-1 BBB



(b) Current-fed full-bridge type-1 BBB



(c) Two-phase boost converter type-1 BBB



(d) Voltage-fed quasi-Z-source type-2 BBB

FIGURE 18. Current signals generated by non-isolated full-bridge DC-DC converters as well as two-phase boost converter.

v_{13} for device S_2 . The magnitude of the blocking voltage is then obtained as $\frac{(v_{12}-v_{32})}{1-\delta}$ for S_1 and $\frac{v_{31}}{\delta}$ for S_2 . The average voltage across the BBB's capacitor is then obtained as $(v_{12} - v_{32})$. The third scenario is when terminal 1 is common to both load and source as shown in Fig. 12 (d). The average voltage across S_1 is obtained as v_{31} and $(v_{21} - v_{31})$ for S_2 . The blocking voltages are then obtained as $\frac{v_{31}}{1-\delta}$ for S_1 and $\frac{(v_{21}-v_{31})}{\delta}$ for S_2 . The average voltage across the BBB's capacitor is obtained as v_{31} .

C. SIZING OF COMPONENTS

The sizing of the converters' passive components can also be shown to be essentially dependent on the waveforms generated by a BBB irrespective of where it is embedded

TABLE 8. Validation of (8)-(16) and (48)-(53) for type-2 BBB and converter employing 2 type-2 BBBs.

Converter	$I_{S2,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]	$\frac{I_{3,ave}}{I_{S2,ave}}$	$\frac{I_{L1,ave}}{I_{L2,ave}}$
Cell 1-4.1	22.266	11.977	22.326	10.298	0.4621	0.53646
	$\frac{I_{3,ave}}{I_{S2,ave}} = 1 - \frac{I_{L1,ave}}{I_{L2,ave}}$		$\frac{I_{3,ave}}{I_{S2,ave}} = \frac{1 - 2\delta}{1 - \delta}$		$I_{n4} = \frac{I_{n11}(1 - \delta)}{\delta}$	
	0.46354		0.46154		22.243A	
	$I_{n2} = \frac{I_{n11}}{\delta}$		$I_{n2} = I_{n3} = I_{n11} + I_{n12}$		$I_{n5} = \frac{I_{n12}\delta}{1 - \delta}$	
	34.22A		34.303A		12.022A	
Converter	$I_{S1,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]	$\frac{I_{3,ave}}{I_{L1,ave}}$	$\frac{I_{L2,ave}}{I_{L1,ave}}$
Cell 1-4.3	12.943	12.884	23.993	11.05	0.85765	1.86223
	$\frac{I_{3,ave}}{I_{L1,ave}} = \frac{I_{L2,ave}}{I_{L1,ave}} - 1$		$\frac{I_{3,ave}}{I_{L1,ave}} = \frac{1 - 2\delta}{\delta}$		$I_{n4} = \frac{I_{n11}(1 - \delta)}{\delta}$	
	0.86223		0.85714		23.927	
	$I_{n2} = \frac{I_{n11}}{\delta}$		$I_{n2} = I_{n3} = I_{n11} + I_{n12}$		$I_{n5} = \frac{I_{n12}\delta}{1 - \delta}$	
	36.811A		36.877A		12.919A	
Converter	$I_{S2,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]		$\frac{I_{S2,ave}}{I_{L1,ave}}$	$\frac{I_{L2,ave}}{I_{L1,ave}}$
Cell 1-4.5	12.821	6.878	12.852		1.86406	1.86857
	$\frac{I_{S2,ave}}{I_{L1,ave}} = \frac{I_{L2,ave}}{I_{L1,ave}}$		$\frac{I_{S2,ave}}{I_{L1,ave}} = \frac{1 - \delta}{\delta}$		$I_{n4} = \frac{I_{n11}(1 - \delta)}{\delta}$	
	1.86857		1.85714		12.773A	

TABLE 9. Validation of (1)-(7) and (38)-(42) for type-1 BBB and converter employing 2 type-1 BBBs.

Converter	$I_{S2,ave}$ [A]	$I_{S3,ave}$ [A]	$I_{S4,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]
Cell 2-4.1	22.539	12.153	22.555	34.708	34.708	10.378
	$\frac{I_{S3,ave}}{I_{S4,ave}} = G_{IS4 \rightarrow IS3}$		$\frac{I_{S2,ave}}{I_{L2,ave}} = G_{IL2 \rightarrow IS2}$		$\frac{I_{L1,ave}}{I_{S4,ave}} = G_{IS4 \rightarrow IL1}$	
	0.53882		0.64939		1.53882	
	$\frac{I_{3,ave}}{I_{S4,ave}} = \frac{I_{S2,ave}}{I_{L2,ave}} \times \frac{I_{L1,ave}}{I_{S4,ave}} - \frac{I_{S3,ave}}{I_{S4,ave}}$				$\frac{I_{3,ave}}{I_{S4,ave}} = \frac{1 - 2\delta}{1 - \delta}$	
	0.46047		0.46154			
Converter	$I_{S1,ave}$ [A]	$I_{S2,ave}$ [A]	$I_{S3,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]
Cell 2-4.3	13.116	24.297	13.116	37.413	37.413	11.181
	$\frac{I_{3,ave}}{I_{S1,ave}}$		$\frac{I_{3,ave}}{I_{S1,ave}} = \frac{I_{S2,ave}}{I_{S1,ave}} - \frac{I_{S3,ave}}{I_{L2,ave}} \times \frac{I_{L2,ave}}{I_{L1,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}}$			
	0.85247		1.85247-1=0.85247			
	$\frac{I_{3,ave}}{I_{S1,ave}} = \frac{1 - 2\delta}{\delta}$		$I_{n12} = I_{n22} = I_{n32} = I_{L2,ave}$		$I_{3,ave} = I_{S2,ave} - I_{S3,ave}$	
	0.85714		37.413A		11.181A	
Converter	$I_{S1,ave}$ [A]	$I_{S4,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$\frac{I_{S2,ave}}{I_{L1,ave}}$	$\frac{I_{L2,ave}}{I_{L1,ave}}$
Cell 2-4.5	13.858	25.744	39.575	39.575		
	$\frac{I_{S4,ave}}{I_{S1,ave}}$		$\frac{I_{S4,ave}}{I_{S1,ave}} = \frac{I_{S4,ave}}{I_{L2,ave}} \times \frac{I_{L2,ave}}{I_{L1,ave}} \times \frac{I_{L1,ave}}{I_{S1,ave}}$			
	1.8577		1.8577			
	$\frac{I_{S4,ave}}{I_{S1,ave}} = \frac{1 - \delta}{\delta}$		$I_{n11} = I_{n21} = I_{n31} = I_{L1,ave}$		$I_{L1,ave} = I_{L2,ave}$	
	1.85714		39.575A		39.575A	

in a more complex converter. For the inductor, the ripple is shown to be always triangular in nature. For the type-1 BBB, the inductance required to maintain a given peak-peak

ripple $\Delta i_{L,pk-pk}$ is given by $L = \frac{v_L \Delta t}{\Delta i_{L,pk-pk}}$. When terminal 3B is common to load and source, the required inductance is given by $L = \frac{v_{1B3B} \delta T_{sw}}{\Delta i_{L,pk-pk}}$. When terminal 2B is common

TABLE 10. Validation of (17)-(21) and (66a)-(66c) for converters employing 1 type-1, 1 type-2 and 1 type-3 BBBs.

Converter	$I_{S1,ave}=I_{cond,ave}$ [A]	$I_{S2,ave}$ [A]	$I_{S3,ave}$ [A]	$I_{S4,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]
Cell 3-4.1	4.896	9.061	9.092	16.791	11.926	13.957	25.883
	$\frac{I_{3,ave}}{I_{L2,ave}}$		$\frac{I_{3,ave}}{I_{L2,ave}} = 1 + \frac{I_{L1,ave}}{I_{L2,ave}}$		$\frac{I_{3,ave}}{I_{L2,ave}} = \frac{(1-\delta)}{\delta}$		
	1.85448		1.85448		1.85714		
	$\frac{I_{3,ave}}{I_{L2,ave}} = \frac{I_{3,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{L2,ave}} + \frac{I_{S4,ave}}{I_{cond,ave}} \times \frac{I_{cond,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{L2,ave}}$						
	0.65142939+1.203052232=1.85448						
Cell 3-4.3	$I_{S1,ave}=I_{cond,ave}$ [A]	$I_{S2,ave}$ [A]	$I_{S3,ave}$ [A]	$I_{S4,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	$I_{3,ave}$ [A]
	8.353	15.496	15.465	28.768	20.384	23.849	44.233
	$\frac{I_{3,ave}}{I_{L1,ave}}$		$\frac{I_{3,ave}}{I_{L1,ave}} = 1 + \frac{I_{L2,ave}}{I_{L1,ave}}$		$\frac{I_{3,ave}}{I_{L2,ave}} = \frac{\delta}{2\delta - 1}$		
	2.17		2.17		2.167		
	$\frac{I_{3,ave}}{I_{L1,ave}} = \frac{I_{S4,ave}}{I_{L1,ave}} + \frac{I_{S3,ave}}{I_{S2,ave}} \times \frac{I_{S2,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{cond,ave}} \times \frac{I_{cond,ave}}{I_{L1,ave}}$						
1.411302983+0.758683281=2.17							
Cell 3-4.5	$I_{S1,ave}=I_{cond,ave}$ [A]	$I_{S2,ave}$ [A]	$I_{S3,ave}$ [A]	$I_{S4,ave}$ [A]	$I_{L1,ave}$ [A]	$I_{L2,ave}$ [A]	
	7.177	13.329	13.279	24.753	20.507	17.525	
	$\frac{I_{L1,ave}}{I_{L2,ave}}$		$\frac{I_{L1,ave}}{I_{L2,ave}} = \frac{1-\delta}{2\delta-1}$		$\frac{I_{L2,ave}}{I_{L1,ave}}$		
	1.17016		1.16667		0.8545862		
	$\frac{I_{L1,ave}}{I_{L2,ave}} = \frac{I_{L1,ave}}{I_{S1,ave}} \times \frac{I_{S1,ave}}{I_{cond,ave}} \times \frac{I_{cond,ave}}{I_{L2,ave}}$						
1.17016							

to both source and load, the required inductance is $L = \frac{(v_{12}-v_{32})\delta T_{sw}}{\Delta i_{L,pk-pk}}$. When terminal 1B is common to both source and load, the required inductance is $L = \frac{v_{3B1B}\delta T_{sw}}{\Delta i_{L,pk-pk}}$.

For the type-2 BBB, the inductance for L_1 is given by $L_1 = \frac{v_{13}\delta T_{sw}}{\Delta i_{L,pk-pk}}$ and that for L_2 is given by $L_2 = \frac{v_{23}(1-\delta)T_{sw}}{\Delta i_{L,pk-pk}}$. For a given capacitor peak-peak voltage ripple, $\Delta v_{C,pk-pk}$ the capacitor for the type-2 BBB is sized referring to capacitor current waveform in Fig. 2 as $C = \frac{I_{n4}\delta T_{sw}}{\Delta v_{C,pk-pk}}$. For the inter-stage capacitor, the required capacitance is obtained with reference to Fig. 3 as $C = \frac{I_{n8}\delta T_{sw}}{\Delta v_{C,pk-pk}}$.

VI. SIMULATED WAVEFORMS

PSIM software package is used to simulate various circuits to validate the analytical predictions including current waveforms for the BBBs.

A. CONVERTERS FROM SOME OF THE 14 CONVERTER CELLS REPORTED IN THE LITERATURE

This section presents simulated waveforms and data to validate those for the proposed BBBs. Figs. 17(a) and (b) show the waveforms for the two type-2 BBB variants in Figs. 2(a) and (b). There is good correspondence between these waveforms and those in Figs. 2(a) and (b) thus

validating the theoretical basis used to analyze converters with type-2 BBBs (i.e. (8)-(16)). These waveforms were generated using converter 1-4.1 that employs two type-2 BBBs shown in Fig. 12 and therefore also to validate the waveforms shown in Fig. 12. Other converters employing two type-2 BBBs are shown in Figs. 13, 16(c) and 16(d) while converters with a single type-2 BBB are shown in Figs. 7, 10, and 14. Fig. 17(c) shows the waveforms of a type-1 BBB. These were used to validate those shown in Fig. 1 and confirm the correctness of the analysis in (1)-(7) for type-1 BBBs. They were generated using converter 2-4.1 that employs 2 type-1 BBBs and therefore also serve to validate the waveforms in Figs. 12(b)-(d). Other converters employing two type-1 BBBs are shown in Figs. 6, 7, 8, 9, 15 and 16(a). Converters with a single type-1 BBB are shown in Figs. 5, 10, 11 and 14. Similarity between the waveforms of type-1 BBBs and those in Fig. 17(c) is evident. Fig. 17(d) shows the waveforms of a type-3 BBB that were generated using converter 3-4.1 that employs 1 type-1, 1 type-2 and 1 type-3 BBBs. These were used to validate those shown in Fig. 3 as well as confirm the correctness of the theoretical basis for the analysis in (17)-(21). Further, validate waveforms for type-3 BBBs in converters in Figs. 8 and 14.

Table 8 presents average currents at the various terminals of the two type-2 BBBs used to realize converters 1-4.1,

TABLE 11. Analytical validation of current and voltage stresses predictions (i.e. (8), (11b), (13), (14), (16), (20)-(21)) in type-2 BBBs.

Converter	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
Cell 1-4.1	104V	34.296A	34.296A
	$V_{s1,block} = \frac{V_{31}}{1-\delta}$	$V_{s2,block} = \frac{V_{21}-V_{31}}{\delta}$	$V_{c1,ave} = V_{s1,ave} = V_{31}$
	160V	-160V	104V
Cell 1-4.3	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
	104V	34.296A	34.296
	$V_{s1,block} = \frac{V_{12}-V_{32}}{\delta}$	$V_{s2,block} = \frac{V_{32}}{1-\delta}$	$V_{c1,ave} = V_{12}-V_{32}$
	-160V	160V	-56V
Cell 1-4.5	$V_o = \frac{V_{in}\delta}{1-\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
	25.846V	19.643A	19.643A
	$V_{s1,block} = \frac{V_{13}}{1-\delta}$	$V_{s2,block} = \frac{-V_{23}}{\delta}$	$V_{c1,ave} = V_{13}$
	73.846V	-73.846V	48V

TABLE 12. Simulated validation of current and voltage stresses predictions in type-2 BBBs.

Converter	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
Cell 1-4.1	103.5V	34.28A	34.25A
	$V_{s1,block} = \frac{V_{31}}{1-\delta}$	$V_{s2,block} = \frac{V_{21}-V_{31}}{\delta}$	$V_{c1,ave} = V_{s1,ave} = V_{31}$
	158V	-157.82V	103.513V
Cell 1-4.3	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
	103.51V	34.07A	34.07A
	$V_{s1,block} = \frac{V_{12}-V_{32}}{\delta}$	$V_{s2,block} = \frac{V_{32}}{1-\delta}$	$V_{c1,ave} = V_{12}-V_{32}$
	-157.88V	157.97V	-55.506V
Cell 1-4.5	$V_o = \frac{V_{in}\delta}{1-\delta}$	$I_{s1,nom} = I_{L1,ave} + I_{L2,ave}$	$I_{s2,nom} = I_{L1,ave} + I_{L2,ave}$
	25.69V	19.495A	19.495A
	$V_{s1,block} = \frac{V_{13}}{1-\delta}$	$V_{s2,block} = \frac{-V_{23}}{\delta}$	$V_{c1,ave} = V_{13}$
	73.11V	-73V	47.78V

1-4.3 (zeta) and 1-4.5 (Sepic) shown in Fig. 12. The currents are partly used to evaluate the input-output current gains of these converters using (53a), (53b) and (53c). Each one of these equations presents several expressions for a given input-output gain. Values obtained using these different expressions are all in very close agreement, validating the accuracy of the proposed technique. Table 8 also presents the nominal magnitudes of the switches' and capacitors' currents. These together with the average BBBs' terminal currents help to validate (8)-(16). Table 9 presents average currents at the various terminals of the two type-1 BBBs used to realize converters 2-4.1, 2-4.3 and 2-4.5 shown in Fig. 9. The currents are used to evaluate the input-output current gains of these converters using (42a), (42b) and (42c). Each one of these equations presents several expressions for a given input-output gain. Values obtained using these different expressions

are essentially identical. These average BBBs' terminal currents also help to validate (1)-(7). Table 10 presents average currents at the various terminals of a type-1, type-2 and type-3 BBBs used to realize converters 3-4.1, 3-4.3 and 3-4.5 shown in Fig. 14. The currents are used to evaluate the converters' input-output current gains using (66a), (66b) and (66c). Values of gains from the different expressions are essentially identical. These average BBBs' terminal currents also help to validate (1)-(7), (8)-16) and (17)-(21). The above demonstrates the accuracy of the technique when converters employ several different types of BBBs.

B. NON-ISOLATED FULL-BRIDGE, TWO-PHASE BOOST AND QUASI-Z-SOURCE DC-DC CONVERTER

Figs. 18(a)-(b) show waveforms generated by type-1 BBBs used in non-isolated voltage- and current-fed, half- and

TABLE 13. Analytical validation of current and voltage stresses predictions ((1)-(4)) in type-1 BBBs.

Converter	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
Cell 2-4.1	104V	34.769A	34.769A	36.4V
	$V_{s1,block} = V_{31}$ 104V	$V_{s2,block} = -V_{31}$ -104V	$V_{s3,nom} = V_{31} - V_{21}$ 56V	$V_{s4,nom} = V_{21} - V_{31}$ -56V
Cell 2-4.3	$V_o = \frac{V_{in}\delta}{1-2\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
	56V	37.5A	37.5A	36.4V
	$V_{s1,block} = V_{12} - V_{32}$ 104V	$V_{s2,block} = V_{32} - V_{12}$ -104V	$V_{s3,nom} = V_{23}$ 56V	$V_{s4,nom} = V_{32}$ -56V
Cell 2-4.5	$V_o = \frac{V_{in}\delta}{1-\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
	25.846V	39.583A	39.583A	16.8V
	$V_{s1,block} = V_{13}$ 48V	$V_{s2,block} = -V_{13}$ -48V	$V_{C1,ave} = V_{23}$ 25.846V	$V_{C1,ave} = -V_{23}$ -25.846V

TABLE 14. Simulated validation of current and voltage stresses predictions in type-1 BBBs.

Converter	$V_o = \frac{V_{in}(1-\delta)}{1-2\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
Cell 2-4.1	104.1V	34.735A	34.714A	36.54V
	$V_{s1,block} = V_{31}$ 104V	$V_{s2,block} = -V_{31}$ -104V	$V_{s3,nom} = V_{31} - V_{21}$ 56.19V	$V_{s4,nom} = V_{21} - V_{31}$ -56.19V
Cell 2-4.3	$V_o = \frac{V_{in}\delta}{1-2\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
	56.07V	37.4A	37.42A	36.54V
	$V_{s1,block} = V_{12} - V_{32}$ 104.24V	$V_{s2,block} = V_{32} - V_{12}$ -104.16V	$V_{s3,nom} = V_{23}$ 56.18V	$V_{s4,nom} = V_{32}$ -55.76V
Cell 2-4.5	$V_o = \frac{V_{in}\delta}{1-\delta}$	$I_{s1,nom} = I_{s2,nom} = I_{L1,ave}$	$I_{s3,nom} = I_{s4,nom} = I_{L2,ave}$	$V_{C1,ave} = V_{s2,ave} = \delta V_{s2,nom}$
	25.742V	39.565A	39.581A	16.8V
	$V_{s1,block} = V_{13}$ 48V	$V_{s2,block} = -V_{13}$ -48V	$V_{C1,ave} = V_{23}$ 25.846V	$V_{C1,ave} = -V_{23}$ -25.846V

full-bridge DC-DC converters. Fig. 18(c) presents signals generated by type-1 BBB in 2-phase boost converters. The signals are similar to those generated by type-1 BBB in converter shown in Fig. 17. This confirms that it is the type of BBB that primarily determines the current signals generated in different DC-DC converter topologies. Fig. 18(d) shows current signals generated by type-2 BBB used to build Z- and quasi-Z-source DC-DC converters. They are similar to those predicted for converter cell 1-4 and cell 3-1 in Fig. 7 and Fig. 13 respectively.

Tables 11 and 13 present analytical data for devices' current and voltage stresses. These were obtained using (1)-(7), (8)-(16) for the currents and voltage stress equations from section V part B. Tables 12 and 14 on the other hand present simulated data to validate the usefulness of the BBBs in predicting current voltage stresses for the semiconductor devices and cell capacitors. It is evident that analytical and simulated values are in close agreement.

VII. CONCLUSION

In the literature, several attempts have been made to develop a unified approach for synthesis all two-state DC-DC converters and generation of converters that meet a certain set criteria. For example, two-, three- and five-elements converter cells were proposed as BBBs for DC-DC converters. However, none of these efforts have provided a BBB or a set of BBBs that can generate all non-isolated or coupled inductor DC-DC converters. It has been found that to propose a concept or BBBs that will form the basis for a unified analytical technique and prediction of current waveforms, it is necessary to establish a unified pattern of gate signals in all DC-DC converters. This study has proposed three 3-terminal BBBs and one 3-terminal filter block which together are sufficient to realize all non-isolated DC-DC converters, excluding those with coupled inductors.

The proposed technique uses BBBs to facilitate analysis of DC-DC converters in a structured manner. It shows that all non-isolated DC-DC converters are realized by

connecting BBBs in cascade, stacked, stacked plus cascade, parallel/interleaved or differentially. Cascaded connection of BBBs leads to a single current path between source and load. Stacking or stacking plus cascading on the other hand, creates at least two parallel current paths between source and load. Interleaving gives rise to as many parallel current paths as the number of phases involved. For any given current path, the path gain is obtained as the product of the gains of all the BBBs' stages in that path. When a converter has parallel current paths connecting load and source, the overall gain is obtained as the sum (difference) of the individual path gains when currents are in the same (opposite) directions. The technique for obtaining current gains is intuitive, less analytically intense and hence simpler than currently available techniques. It relies on the analysis developed for the three BBBs and the filter block. This makes the BBBs and the filter block useful tools for both synthesis and analysis of DC-DC converters.

A BBB has unique switch states for proper operation. These in turn cause unique sets of waveforms to be generated at the three terminals irrespective of where a BBB is embedded. Thus, a converter switch states and current waveforms that it generates are dictated by the BBBs used to realize it. It is thus easy to determine similarities between converter cells that are currently treated as unique and identify redundant sub-circuits or components in converter cells. Moreover, it was demonstrated how to represent a node connecting 4 components using 2 3-terminal BBBs. This makes the proposed technique suitable for analyzing a very wide variety of DC-DC converters.

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