A High-Q Second-Order All-Pass Delay Network in CMOS

Piotr Jan Osuch [1], Tinus Stander [2]

[1, 2] Dept. of Electrical, Electronic & Computer Engineering, University of Pretoria, Pretoria, South Africa

Abstract: Analogue signal processing (ASP) is a promising alternative to DSP techniques in future telecommunication and data processing solutions. Second-order all-pass delay networks – the building blocks of ASPs – are currently primarily implemented in off-chip planar media, which is unsuited for volume production. In this work, a novel on-chip CMOS second-order all-pass network is proposed that includes a post-production tuning mechanism. It is shown that automated tuning with a genetic local optimizer can compensate for CMOS process variation and parasitics, which make physical realization otherwise infeasible. Measurements indicate a post-tuning bandwidth of 280 MHz, peak-to-nominal delay variation of 10 ns and magnitude variation of 3.1 dB. This is the first time that measurement results have been reported for an active inductorless on-chip second-order all-pass network with a delay Q-value larger than 1.

1. Introduction

Analogue signal processing (ASP) is a promising alternative to digital signal processing (DSP) techniques in future high-speed telecommunication and data-processing solutions, as analogue devices outperform their digital counterparts in terms of cost, power consumption, and the maximum attainable bandwidth [1]. The fundamental building block of any ASP is a dispersive delay structure (DDS) of prescribed response [2], [3]. For example, DDSs with non-constant linear group delays are used for real-time Fourier transformation, stepped group delays for distortionless frequency discrimination, and Chebyshev delays for distortion-encoding multiple-access communication channels [3], easing the burden on the system DSP [5]. Any of these dispersive responses can be synthesized by cascaded first- and second-order all-pass networks (as is shown in [4]).

In practically implementing a first- or second-order all-pass network [1], [3], [5]–[31], a trade-off is made between the maximum achievable all-pass delay ($\Delta\tau$) and the insertion loss of the network at the resonant frequency. The Q_D-value, defined as $Q_D = \Delta\tau.\omega_0/4$ [7] (where ω_0 is the peak delay frequency) is used as a figure of merit to gauge the maximum achievable $\Delta\tau$ independent of ω_0. A Q_D-value larger than 1 is required for many ASP applications [2]. Real-time spectrum analysis [2] requires $Q_D > 0.79$ for frequency discrimination, while $Q_D > 3.5$ and $Q_D > 10$ results in a resolution of ~0.4f_0 and ~0.2f_0, respectively. In frequency scanning antenna arrays, a Q_D of 2 has been shown to result in a mapping of 60°/GHz [2], with higher Q_D required for finer spatial resolution. In M-ary PPM, a Q_D of 3.14 is required to create a maximum delay of one pulse width. In off-chip media, microwave DDSs have been proposed that are comprised of cascaded microwave C-sections [1], [3]. These have been shown to exhibit Q_D-values larger than 1 with bandwidths of approximately 4 GHz [1] and 15 GHz [5]. However, the high losses of on-chip distributed line elements make these approaches infeasible on-chip [32]. Similarly, passive lumped element configurations on-chip are also vulnerable to resonant loss, due to low attainable inductor Q-factors (not the same as Q_D-values) of typically less than 10 [7], [23], [24], [27]. In [23] an approximation to a second-order all-pass network is proposed based on a single transistor inverter. This design uses an on-chip inductor achieving a Q_D-value of only 0.04. In [24] an analogue two transistor delay circuit using an on-chip inductor achieves a Q_D-value of only 0.047. Similarly, in [27] a simple Padé approximation is implemented achieving a Q_D-value 0.049. In recognition of these difficulties with on-chip inductors numerous active *inductorless* implementations of all-pass networks have been proposed [25], [26], [28], [30], [31]. In [25] an active inductorless approximation to a second-order all-pass network is proposed based on a CMOS inverter, and achieves a Q_D-value of 0.19. In [26] an LC network is implemented by using an active inductor, approximating a second-order delay response with an overall Q_D-value of 0.098. In [28], [30], [31] a special case of a second-order delay network is obtained with the resonant frequency at 0 Hz and therefore a Q_D-value of 0. To avoid an approximation to an ideal second-order all-pass response and to increase the achievable Q_D-value, operational amplifier and CCII-based realizations have been proposed [8]–[22] which can potentially achieve Q_D-values larger than 1. Op-amp based realizations are generally undesirable due to low bandwidths [9], sparking interest in CCII-based implementations. These devices exhibit higher bandwidth, greater linearity and lower power consumption than op-amps, making them better suited for implementation of second-order all-pass networks [8]–[22]. However, CCII non-idealities such as non-unity voltage mirroring (A_v) and current conveying (A_i), non-zero input resistance at port X (R_X), and finite values of output resistance at ports Y and Z (R_Y and R_Z) make many of these designs impractical, even when using high-precision CCIIs [33]. This shortcoming has, however, never been addressed in literature, as most papers assume ideal CCII elements. For example, implementing the all-pass network in [8] using a CCII with an R_X of 5 Ω and a 2% deviation in A_v results in a ~3 dB magnitude peak at resonance, whereas a similar deviation in A_i results in a ~2 dB notch, as will be shown in section II. An R_X of 10 Ω results in an even larger 8 dB magnitude notch. It is, therefore, crucial to practical on-chip implementation to use all-pass circuits which can account for the above CCII non-idealities through appropriate selection of RC components. Furthermore, since both the CCII parameters and the RC components themselves change with process parameter variation, post-production

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tunability of the circuit is also necessary in practice, yet has never been implemented in a CCII-based second-order all-pass network.

In this work, the synthesis approach presented in [12], based on partial fraction decomposition, is applied to the general CCII configuration in [13] to synthesize an inductorless second-order all-pass network with a Q_D-value larger than 1. The proposed network is then adapted for post-production tunability to concurrently account for non-unity A_v and A_i, as well as a non-zero R_X. The effects of remaining CCII non-idealities on the all-pass response are further considered and it is shown that the proposed design is sufficiently insensitive to them for practical consideration in this work. The proposed design is implemented in the 0.35 µm CMOS technology node using CCIIs based on [34], with the surrounding RC network implemented in the form of varactors and NMOS transistors operating in the triode region to provide post-production tunability. A post-production automated tuning method is further proposed, whereby measured data from a VNA is used in a real-time genetic local optimizer on a PC (which controls various bias voltages using a DAC card) to tune the physical all-pass network. It is shown that this step is crucial to realizing a practical system, leading to the first ever measured results of an active inductorless on-chip CMOS second-order all-pass network with a Q_D-value larger than 1.

This paper makes the following contributions to the state-of-the-art (SOTA), in synthesis of second-order all-pass networks with CCIIs.

1. An RC network extending on the design in [13] is synthesized, resulting in a novel inductorless second-order all-pass network. The network is shown to be uniquely insensitive to a non-unity CCII A_v and A_i, as well as a non-zero CCII R_X.
2. A post-production tuning mechanism is proposed and an automated tuning method is developed, to account for CCII non-idealities and CMOS process tolerances.
3. The first ever measured results of an active inductorless on-chip CMOS second-order all-pass network with a Q_D-value larger than 1 are presented.

2. Second-order all-pass network synthesis

In this section, we will synthesize a new second-order all-pass network using the generalized CCII configuration proposed in [13]. The synthesis will take into account various CCII non-idealities. Next, the effect of variation of these non-ideal parameters on our proposed, as well as other, second-order all-pass networks will be illustrated.

2.1. Synthesis

A generalized CCII-based second-order transfer function is proposed in [13], as shown in Fig. 1.

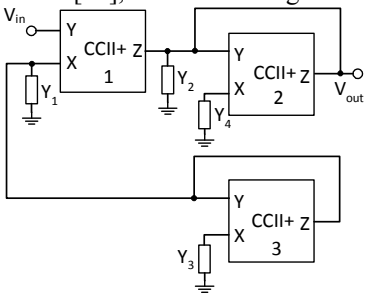


Fig. 1. *CCII+ based general second-order implementation.*

The transfer function, considering non-unity A_i and A_v, is:

$$\frac{V_o}{V_i} = \frac{A_i A_v \cdot \left[Y_1 - Y_3 \cdot A_i A_v\right]}{Y_2 - Y_4 \cdot A_i A_v}. \tag{1}$$

Extending on the work in [13], the desired second-order all-pass transfer function can be written as:

$$\frac{V_0}{V_i} = \frac{s_n^2 - s_n / Q_D + 1}{s_n^2 + s_n / Q_D + 1} = \frac{Y_N}{Y_D}, \tag{2}$$

where $s_n = s/\omega_0$, $Q_D = \Delta\tau.\omega_0/4$, $\omega_0 = 2\pi f_0$ is the center frequency of the second-order all-pass delay function, and $\Delta\tau$ is the corresponding peak-to-nominal group delay. Following the approach in [12], from (2):

$$\frac{Y_N}{s_n\left(s_n+1\right)} = \frac{s_n^2 - s_n / Q_D + 1}{s_n\left(s_n+1\right)}. \tag{3}$$

After division and partial fraction decomposition this becomes

$$\frac{Y_N}{s_n+1} = s_n + 1 - \frac{s_n\left(2+1/Q_D\right)}{s_n+1}. \tag{4}$$

Similarly, for the denominator, we can state that

$$\frac{Y_D}{s_n+1} = s_n + 1 - \frac{s_n\left(2-1/Q_D\right)}{s_n+1}. \tag{5}$$

Equating terms in (4) and (5) with (1) and introducing a real scaling unknown α, the following set of equations can be derived:

$$A_i A_v Y_1 = \left(s_n+1\right)\alpha, \tag{6}$$

$$Y_2 = \left(s_n+1\right)\alpha, \tag{7}$$

$$A_i^2 A_v^2 Y_3 = \frac{s_n \alpha\left(2+1/Q_D\right)}{s_n+1}, \tag{8}$$

$$Y_4 A_i A_v = \frac{s_n \alpha\left(2-1/Q_D\right)}{s_n+1}. \tag{9}$$

Y_1 and Y_2 can be realized as a parallel RC network, and Y_3 and Y_4 as a series RC network, with:

$$\begin{aligned} R_1 &= \frac{A_i A_v}{\alpha}, & C_1 &= \frac{\alpha}{A_i A_v \omega_0}, \\ R_2 &= \frac{1}{\alpha}, & C_2 &= \frac{\alpha}{\omega_0}, \\ R_3 &= \frac{A_i^2 A_v^2}{\alpha\left(2+1/Q_D\right)}, & C_3 &= \frac{\alpha\left(2+1/Q_D\right)}{\omega_0 A_i^2 A_v^2}, \\ R_4 &= \frac{A_i A_v}{\alpha\left(2-1/Q_D\right)}, & C_4 &= \frac{\alpha\left(2-1/Q_D\right)}{\omega_0 A_i A_v}, \end{aligned} \tag{10}$$

where the subscripts of Y correspond to that of the R and C components. The proposed network is shown in Fig. 2.

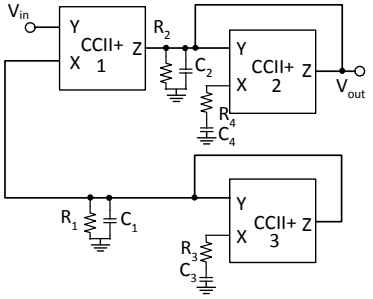


Fig. 2. *Proposed CCII-based second-order all-pass network.*

In the preceding derivation, CCII non-idealities other than A_i and A_v (specifically the critical parameter R_X) are not

considered, since equating terms in (4) and (5) with (1) then becomes impossible without applying an approximation. It is evident in Fig. 1 that R_X of both the 2nd and 3rd CCIIs can be incorporated into the series R_4 and R_3, respectively, thus effectively compensating for its non-ideal effect. Perfect compensation for R_X in the 1st CCII is not possible; however, as will be shown later in this section, this is not necessary for many practical cases (R_X < 30 Ω). Perfect compensation of practical R_Z values in all the CCIIs is also not possible, however this is not necessary, as will be also shown later in this section.

2.2. Effects of CCII non-idealities on the all-pass response

Next, the effects that CCII non-idealities have on the proposed design, as well as on other all-pass networks in the literature [8], [14], [15], [17]–[21], are investigated and compared. In each case, the transfer function of the all-pass network is derived, including the effect of the non-ideal constituent CCII parameters, and the numerical transfer response computed for variable values of different CCII non-idealities. In all cases, identical non-ideality is assumed for all CCIIs in the second-order network, with only one non-ideality varied at a time.

It is also important to consider, in this comparison, to what degree the synthesis of the network (selection of R and C values) can be adapted to *a priori* known CCII non-idealities. It is evident from their respective transfer functions that non-ideal A_i can be compensated for in this work, as well as in [8], [14], [18], [19], [21] through appropriate selection of R and C values. Similarly, non-ideal A_v can be compensated for in this work and in [20] and non-zero R_X in circuits [18]–[21] (partially in this work as described earlier). In all cases R_Z and R_Y cannot be perfectly compensated, but as will be shown, this is often not necessary for practical cases.

From each numerical transmission response calculation over frequency, two performance metrics are extracted. These are the magnitude response variation ($\Delta|H|$) and the group delay similarity, defined as:

$$\tau_s = \int_0^{2\omega_0} \left|\tau_{ideal} - \tau_{net}\right| d\omega \Big/ \int_0^{2\omega_0} \left|\tau_{ideal}\right| d\omega \,, \qquad (11)$$

where τ_{ideal} is the delay response with ideal CCIIs and τ_{net} the non-ideal network response. A $\tau_s = 0$ indicates that the two responses are identical whereas a $\tau_s > 0$ indicates dissimilarity between the group delays. This definition captures both $\Delta\tau$ and ω_0 deviations, as well as deviations from the ideal group delay curve *shape*. This is important to consider, as CCII non-idealities can disrupt the network response to such an extent that the network's delay no longer resembles that of a second-order all-pass network at all.

Finally, as all the considered networks are underdetermined (fewer bounding equations than R and C unknowns) the following component choices are made to ensure a fair comparison between the circuits, as shown in Table 1. In all cases $C_1 = C_2 = C$.

The parameter β represents a constant and is chosen as 10^3 (as this leads to a realizable resistance on-chip), Q_D is set as 2 and ω_0 as $2.\pi.200.10^6$ rad/s (corresponding to design choices made later in this paper). It is, however, reasonable to expect the general conclusions using these parameters to hold for other design choices as well.

Table 1. Component choices for inter-circuit comparison.

All-pass network	IMPOSED CONDITION	Design eq. 1	Design eq. 2	Design eq. 3
[14]	$R_2 = R_3 = R_4 = R$	$R_2 = \beta$	$R_1 = \beta / \left(Q_D^2 \cdot A_i\right)$	$C = \frac{\left(A_i^2 \cdot Q_D\right)}{\left(\omega_0 \cdot \beta\right)}$
[15]	--	$R_1 = \beta$	$R_2 = \beta / Q_D^2$	$C = Q_D / \left(\omega_0 \cdot \beta\right)$
[17]	$R_1 = R_2$	$R_1 = \beta$	$R_3 = \beta / Q_D^2$	$C = Q_D / \left(\omega_0 \cdot \beta\right)$
[18]	--	$R_1 = \beta$	$R_2 = A_i \beta / Q_D^2$	$C = Q_D / \left(\omega_0 \cdot \beta\right)$
[19]	$R_2 = R_3$	$R_1 = \beta$	$R_2 = A_i \beta / Q_D$	$C = Q_D / \left(\omega_0 \cdot \beta\right)$
[20]	$R_2 = 2R_3$	$R_3 = \beta$	$R_1 = 4\beta / Q_D^2$	$C = Q_D / \left(2\omega_0 \cdot \beta\right)$
[21]	$R_2 = R_3$	$R_1 = \beta$	$R_2 = A_i \beta / Q_D$	$C = Q_D / \left(\omega_0 \cdot \beta\right)$

For the proposed circuit, as well as the network in [8], the design choices $C_1 = \alpha/\omega_0$, $C_2 = \alpha(2 + 1/Q_D)/\omega_0$, $C_3 = 2\alpha/\omega_0 Q_D$, $R_1 = 1/\alpha$, $R_2 = 1/(\alpha \cdot (2 + 1/Q_D))$, and $R_3 = Q_D/2\alpha$ are made. In both cases α is chosen as 10^{-3}, to ensure agreement to the component values in Table 1 for the other networks.

Fig. 3 shows $\Delta|H|$ and τ_s over the various CCII non-idealities. In each sub-figure, the solid curve represents the best-case response, where all the non-idealities are known beforehand and compensated for (if possible) in the selection of R and C values. The dotted curves on the other hand represent the response without any compensation for non-idealities (even if compensation is possible). In all cases * denotes the network proposed in this work.

From Fig. 3 (a-b), the proposed circuit and the design in [20] are the only designs in which A_v can be compensated for. For $\Delta|H| < 0.5$ dB, designs [8], [15], [17] require A_v precisions within 1.4 % of unity, designs [18], [19], [21] A_v precisions within 2.7 % of unity, and design [14] an A_v precision within 6 % of unity (making it the design most resilient to CCII A_v variation without explicit compensation applied). Achieving even this level of precision, however, requires a high-precision CCII with feedback which complicates the design and reduces the achievable bandwidth [33]. This point is further illustrated later with a Monte Carlo analysis.

Fig. 3 (c-d) shows the benefit of the proposed design over the circuit in [20], since it allows for ideal compensation of A_i variation. In [20], A_i precision within 3 % of unity is required for $\Delta|H| < 0.5\,dB$ – a value that is difficult to guarantee with CMOS CCIIs – again illustrated later with a Monte Carlo analysis. In Fig. 3 (e-f), the proposed design is shown to require R_X < 30 Ω for $\Delta|H| < 0.5$ dB, which is easily achievable with most CCIIs presented in the literature. In contrast, design [14] requires R_X < 13 Ω and design [8] R_X < 4 Ω for $\Delta|H| < 0.5\,dB$. This, again, necessitates high-precision CCIIs. Even though designs [18]–[21] can compensate for non-zero R_X, as was shown in Fig. 3 (a-d), they still require high-precision CCIIs to achieve the required A_v and A_i precisions.

Fig. 3 (g-h) indicates that for $\Delta|H| < 0.5$ dB, the proposed design requires R_Z > 100 kΩ, circuit [14] an R_Z > 66 kΩ, designs [8], [19], [21] an R_Z > 50 kΩ, and designs [15], [17], [18] an R_Z > 33 kΩ. An $R_Z \approx$ 100 kΩ can be achieved with a cascode current mirror. Even though current conveying bandwidth is reduced by a low R_Z, its effect on CCII bandwidth is much smaller compared to the bandwidth reduction incurred by the feedback required in high-precision CCII designs.

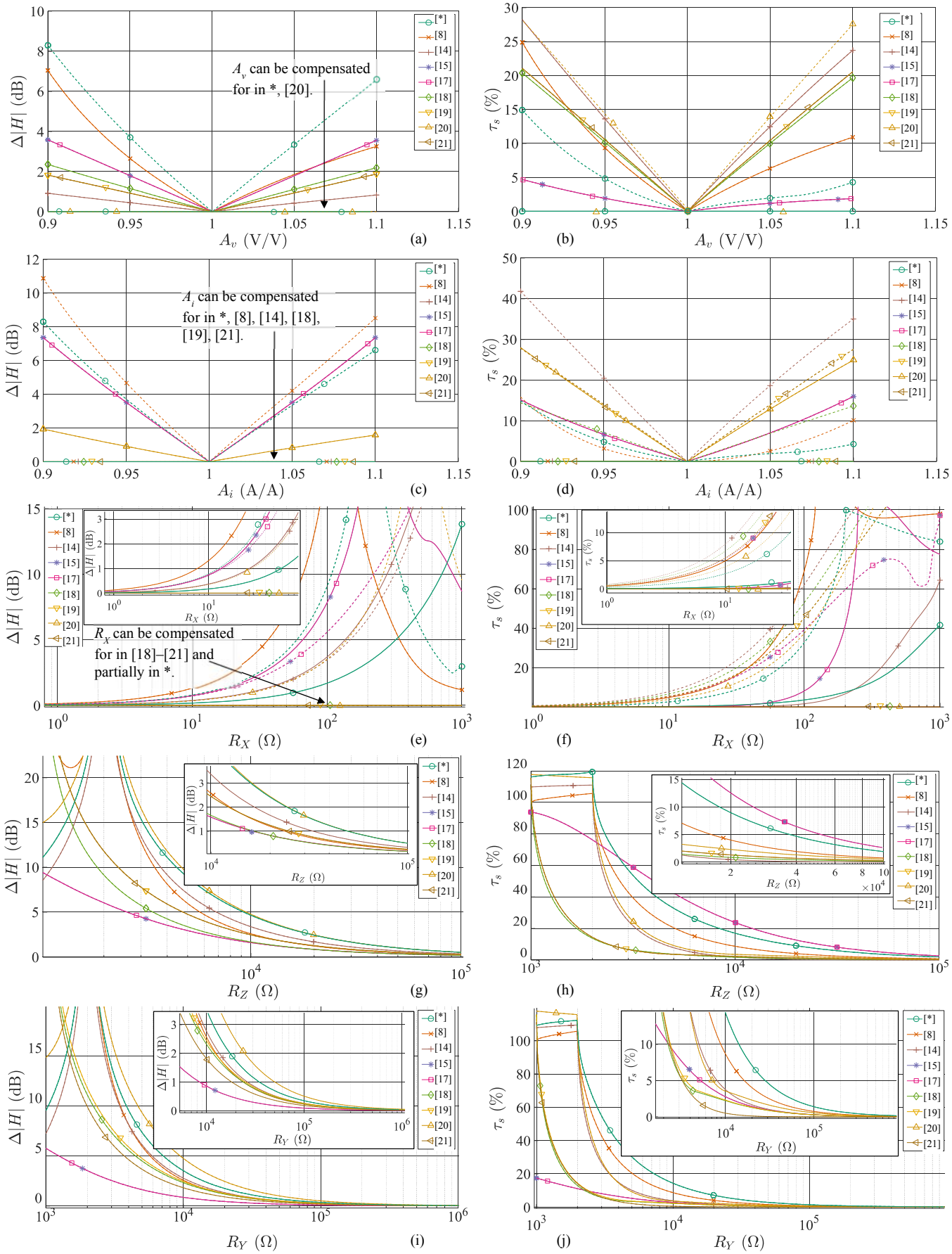


Fig. 3. *Effects of CCII non-idealities on all-pass network response characteristics:* ***(a)*** *non-unity Av vs.* $\Delta|H|$, ***(b)*** *non-unity Av vs.* τ_s, ***(c)*** *non-unity Ai vs.* $\Delta|H|$, ***(d)*** *non-unity Ai vs.* τ_s, ***(e)*** *non-zero* R_X *vs.* $\Delta|H|$, ***(f)*** *non-zero* R_X *vs.* τ_s, ***(g)*** *finite* R_Z *vs.* $\Delta|H|$, ***(h)*** *finite* R_Z *vs.* τ_s, ***(i)*** *finite* R_Y *vs.* $\Delta|H|$, ***(j)*** *finite* R_Y *vs.* τ_s.

Finally, Fig. 3 (i-j) indicates that a $\Delta|H| < 0.5\ dB$ requires $R_Y > 100$ kΩ for all the designs, a value achievable with many CCIIs. Given the ability to compensate for known non-ideal A_i and A_v, as well as the acceptable sensitivity to R_X, R_Y and R_Z without the need for bandwidth-limiting high-precision CCIIs, the network proposed in this work is more suitable for second-order delay network implementation than others analyzed from literature. Fig. 3 also illustrates the importance of post-production tunability of the R and C components to account for *a postiori* knowledge of CCII non-idealities. This need is exacerbated by other circuit non-idealities not captured by the above analysis, such as process variation and parasitic capacitances.

Finally, the effects of varying Q_D (and therefore $\Delta\tau$) on the response of the proposed network, with values of R and C chosen in aid of compensation, are shown in Fig. 4, for different values of R_X, R_Y and R_Z. There is clearly scope for trade-off consideration in the choice of Q_D given a requirement for $\Delta|H|$ (for instance R_Y can be increased by decreasing the bias current through the current mirror). Such a tradeoff is difficult to achieve in passive soft-substrate designs without the use of active enhancement techniques.

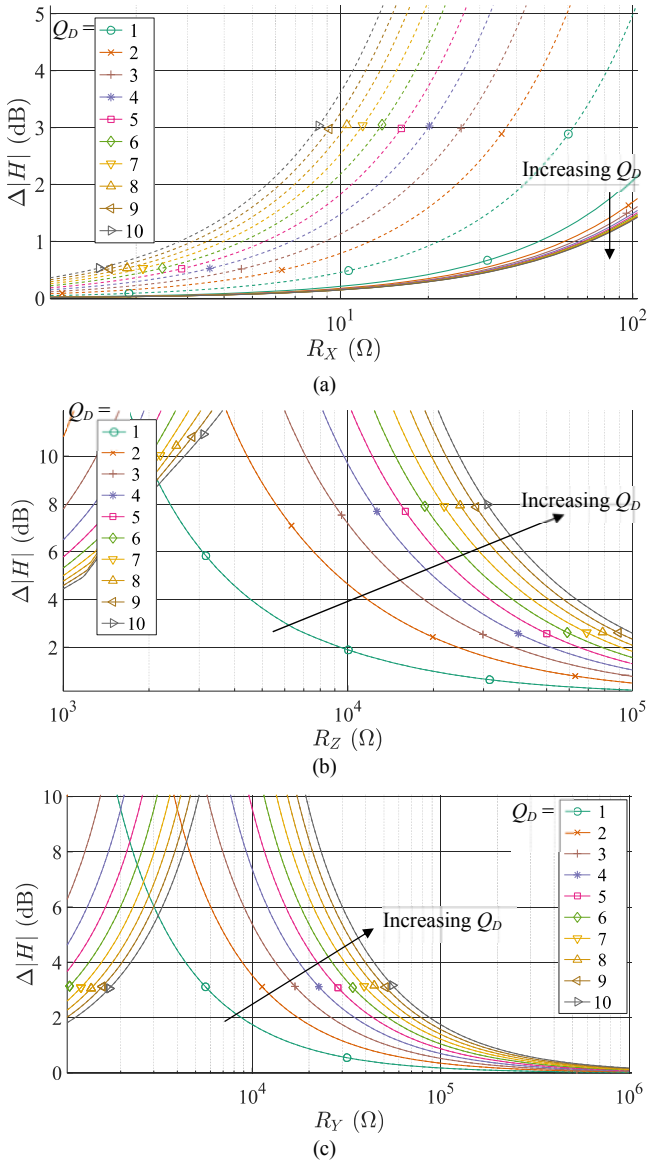


Fig. 4. *Tradeoff between the second-order all-pass Q_D-value and $\Delta|H|$ for various CCII R_X, R_Z and R_Y non-idealities. As in the previous figures the solid curve represents the best-case response, and the dotted curves responses without any compensation for non-idealities (even if compensation is possible).*

3. CMOS implementation of second-order all-pass network

Having proposed a second-order all-pass network suitable for monolithic integration in CMOS, and verifying its improvement on the SOTA w.r.t. resilience to CCII parametric variation, we can proceed with the detailed implementation of the all-pass network in a 0.35 µm CMOS technology node using the synthesis in section II.

3.1. CCII implementation

The high-bandwidth, low-R_X CCII presented in [34] is used as the basis of the CCII design in this work. Even though higher-precision CCIIs have been reported, their design is complicated by necessary stability analyses and compensation networks [33]. Furthermore, the higher precision comes at the expense of lower bandwidth. As per the discussion in section II, the non-idealities of the chosen CCII lie within acceptable bounds and a bandwidth-precision tradeoff is not necessary. A minimum theoretical magnitude variation of ~2 dB can be achieved after compensation using our network, which is attributed mostly to R_Y and R_Z as per Fig. 3(e-j). The CCII used in this work is presented in Fig. 5 with bias currents and transistor aspect ratios as given in Table 2.

Table 2. Transistor sizes chosen for devices in Fig. 5.

Device	W/L (µM/µM)	Device	W/L (µm/µm)	Device	W/L (µm/µm)
M0	11/0.5	M8	10/1.95	M16	40/0.35
M1	10/1.95	M9	10/1.95	M17	40/0.35
M2	5/1.95	M10	20/0.35	M18	10/0.35
M3	18.9/0.75	M11	20/0.35	M19	10/0.35
M4	18.9/0.75	M12	30/0.35	M20	10/0.35
M5	18.9/0.75	M13	30/0.35	M21	10/0.35
M6	25/1.5	M14	30/0.35		
M7	10/1.95	M15	30/0.35		

Resistor R_1 is chosen as 333 Ω to ensure an M_0 bias current of 150 µA with V_{B1} set to 0 V. To establish a range of possible operating conditions of the CCII, a Monte Carlo analysis is performed on the circuit, leading to the performance characteristic range as shown in Table 3.

These simulation results agree well with values presented in the literature. Resistance R_X is well within maximum bounds for successful compensation in most scenarios, as only 3% of the simulated 500 samples have R_X of greater than 20 Ω and only 1.4 % have R_X of greater than 30 Ω. The maximum achievable -3 dB transmission bandwidth (limited by the voltage transfer between ports Y and X) for the nominal corner is ~ 500 MHz.

Table 3. Performance characteristics of the CCII in Fig. 5.

Parameter	MEAN	Standard deviation	Minimum	Maximum
A_v (V/V)	1.083	9.814×10^{-3}	1.062	1.114
A_i (A/A)	0.992	6.306×10^{-3}	0.968	1.009
R_X (Ω)	18.660	8.611	12	161
R_Z (kΩ)	70	26	23	125
R_Y (kΩ)	26	2.4	18	30

3.2. All-pass implementation

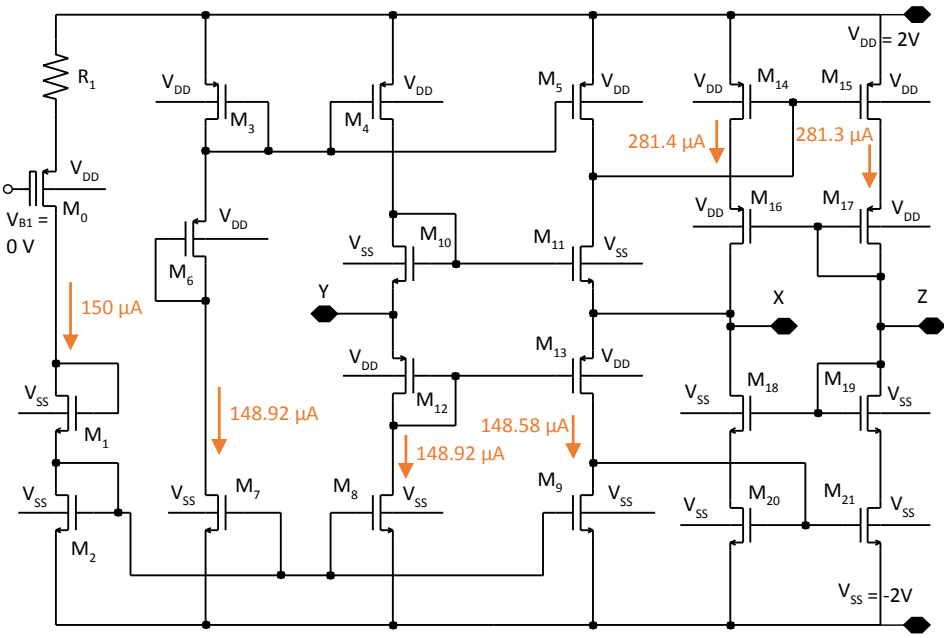


Fig. 5. *CCII+ used for the second-order all-pass network proposed in this work.*

Having designed the CCII as in Fig. 5, the remainder of the proposed all-pass network is implemented as shown in Fig. 6. In this paper we choose f_0 = 200 MHz and $\Delta\tau$ = 7 ns. Component values are then calculated using (10), with α chosen as 10^{-3}. Using the mean A_v and A_i from Table 3, the synthesis results in R_1 = 1074 Ω, R_2 = 1 kΩ, R_3 = 470 Ω, R_4 = 695 Ω, C_1 = 0.74 pF, C_2 = 0.80 pF, C_3 = 1.69 pF, C_4 = 1.15 pF. All resistors are implemented as NMOS devices operating in the triode region, where the bias voltages $V_{R1} - V_{R4}$ are chosen such that the effective channel resistance corresponds to $R_1 - R_4$ above. The NMOS devices in Fig. 6 are chosen as (10 µm/0.5 µm) for $M_{1,2}$ and (20 µm/0.5 µm) for $M_{3,4}$, requiring nominal bias voltages of V_{R1} = 1.94 V, V_{R2} = 1.97 V, V_{R3} = 1.95 V, V_{R4} = 1.83 V.

Capacitors are implemented using accumulation-mode MOS varactors [35] which are tuned with gate bias voltages $V_{C1} - V_{C4}$ such that the effective capacitance values correspond to $C_1 - C_4$ above. The peak capacitances of the varactors are chosen as $C_{1p} = C_{2p}$ = 1.80 pF and $C_{3p} = C_{4p}$ = 2.88 pF, allowing for a sufficient tuning range around the nominal values. Nominal bias voltages V_{C1} = -0.03 V, V_{C2} = -0.06 V, V_{C3} = 0.11 V, V_{C4} = 0.27 V are then required. An 8-bit DAC is required to set and later to fine-tune the bias voltages. In this work, the DAC is implemented off-chip due to prototyping space restrictions. Lastly, the remaining bias values are set as in Fig. 5. The input signal level of the second-order all-pass network must be sufficiently small to ensure that the MOS resistors and varactors operate in the linear region.

A conventional voltage buffer stage (4th CCII+) is added to make the circuit capable of driving a 50 Ω load impedance, as is required for the VNA measurement.

After initial circuit synthesis and layout, a simulation of the proposed all-pass network is performed using accurate non-ideal device models from the AMS foundry as well as extracted layout RC parasitics, as shown in Fig. 7.

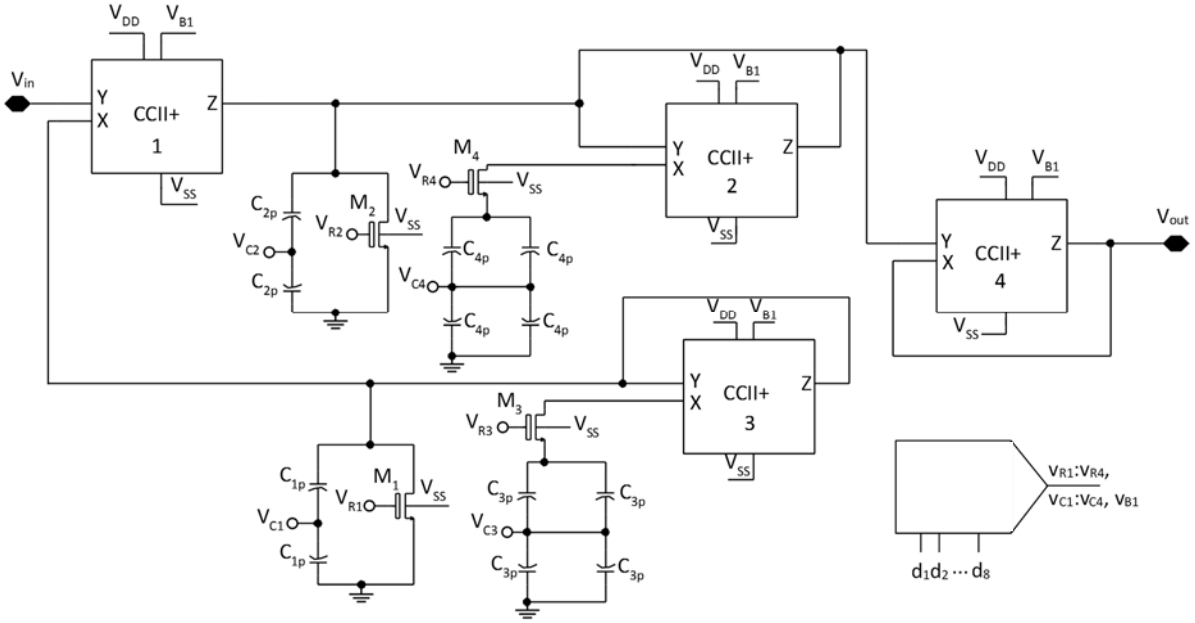


Fig. 6. *Circuit schematic of the proposed second-order all-pass network with post-production tunability compensation.*

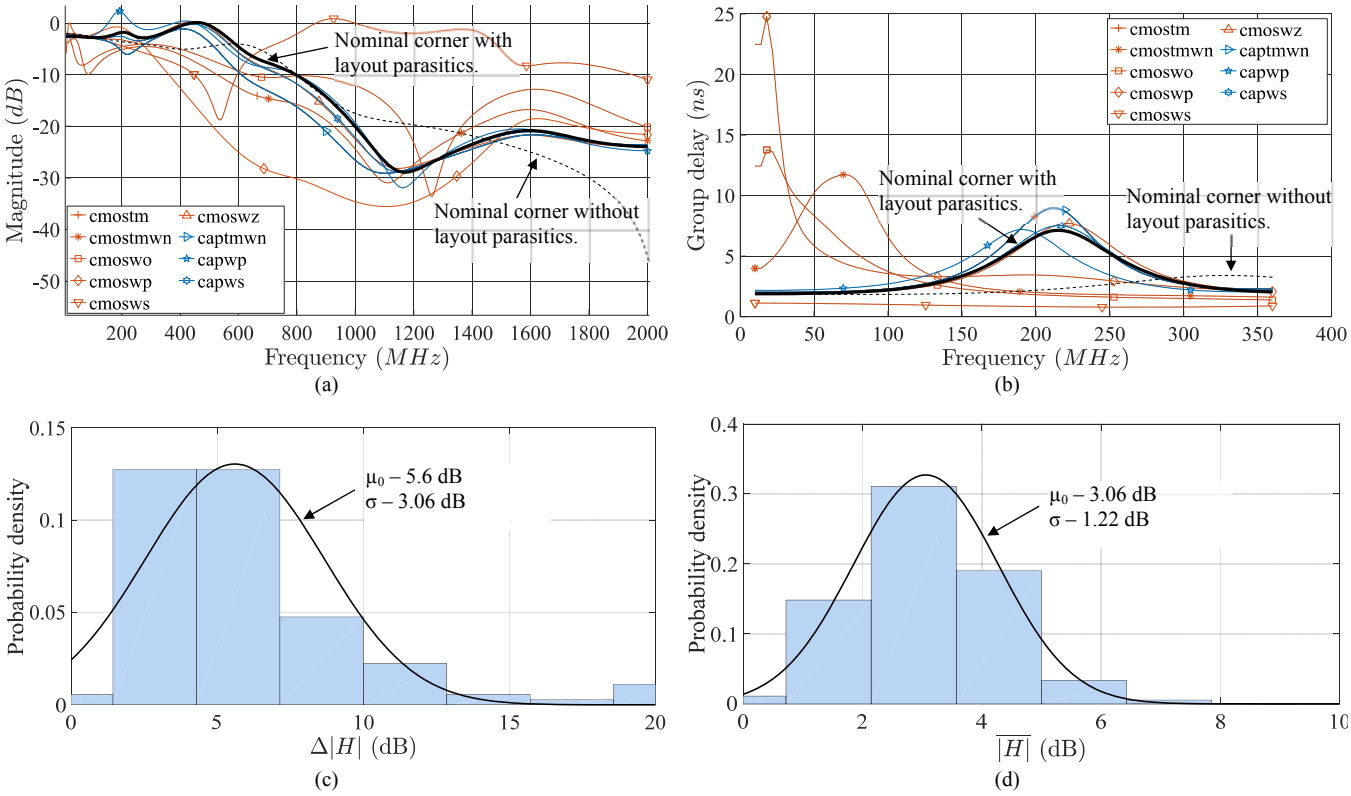


Fig. 7. *Corner and Monte Carlo simulations of the proposed second-order all-pass network.*

To compensate for the resulting change in circuit response, bias voltages are optimized (in simulation) using a global optimizer resulting in the solid black curve, as indicated. The optimizer goals are set to minimize τ_S, $\Delta|H|$ and the deviation of f and $\Delta\tau$ from the desired values of 200 MHz and 7 ns respectively. The optimized bias voltages are V_{R1} = 2.01 V, V_{R2} = 1.98 V, V_{R3} = 2.05 V, V_{R4} = 1.93 V, V_{C1} = 0.03 V, V_{C2} = 0.13 V, V_{C3} = 0.16 V, V_{C4} = 0.40 V, V_{B1} = -0.02 V. These values will serve as the initial values for the automated tuning procedure during measurement. A corner simulation is also performed as indicated in Fig. 7 (a – b). This serves to illustrate the large variation in response characteristics that can be expected without post-production tuning. A description of the corner designations used in the legend of Fig. 7 is given in Table 4 below. A Monte Carlo simulation of the full circuit, analyzing $\Delta|H|$ and $|\overline{H}|$ over 500 samples, indicates that a magnitude flatness of 5.6 dB is most likely, which further justifies the proposed post-production tuning approach.

Table 4. Process corner designations.

Corner designation	DESCRIPTION
cmostm	Typical mean (nominal)
cmostmwn, captmwn	Typical worst noise
cmoswo	Worst case one (fast NMOS and slow PMOS)
cmoswp, capwp	Worst case power (fast NMOS and fast PMOS)
cmosws, capws	Worst case speed (slow NMOS and slow PMOS)
cmoswz	Worst case zero (slow NMOS and fast PMOS)

The power consumption of the second-order all-pass network excluding the DAC is simulated to be 37 mW (15 mW without the voltage buffer). A noise simulation is also performed, as shown in Fig. 8, indicating a nominal output noise of 22 nV/√Hz, peaking at 62 nV/√Hz at resonance.

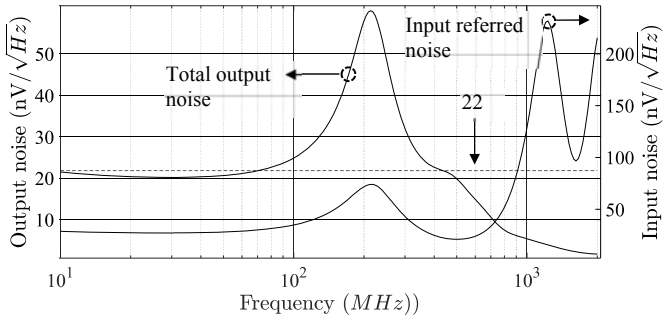


Fig. 8. *Noise simulation of the all-pass network.*

4. Measurement results and post-production automated tuning

The second-order all-pass network of Fig. 6 is manufactured using the C35B4 0.35 µm CMOS process from AMS, as shown in the micrograph of Fig. 9.

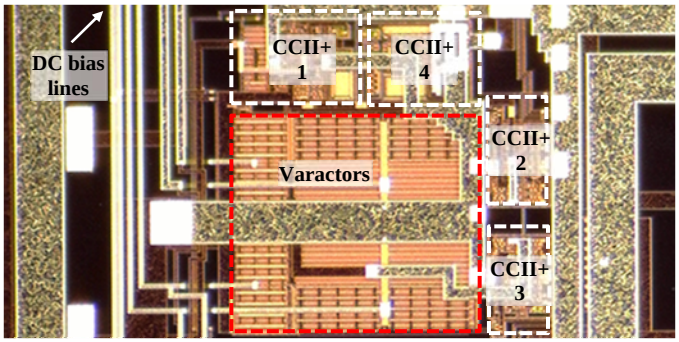


Fig. 9. *Micrograph showing the top view of the all-pass network.*

A PCB is also designed to house the IC and supply the necessary bias voltages and RF test signals, as shown in Fig. 10. Bondwires are used to connect the IC to the PCB pads.

Power supply and DC bias voltages are supplied by the IDC connector as shown. The V_{in} and V_{out} terminals are routed to SMA connectors, which are connected to an Anritsu MS4640A VNA for measurements. To ensure wideband operation, decoupling capacitors are placed as close to the IC as possible (less than λ/10 at 500 MHz).

The overall measurement and post-production automated tuning setup is shown in Fig. 11. The pre-calibrated VNA captures 1001-point two-port S-parameter data and sends it to a PC running a genetic optimizer algorithm in MATLAB®. The optimizer code extracts the transmission magnitude and group delay response from the S-parameters, and calculates the required bias voltage settings for the next measurement iteration. These values are programmed to an Analog Devices AD5370 DAC card connected to the PC via USB, and then applied to the DUT. Only the 8 most significant bits of the 16-bit DAC card are used. A 500 MHz bandwidth digital oscilloscope is also used to monitor the input and output excitations.

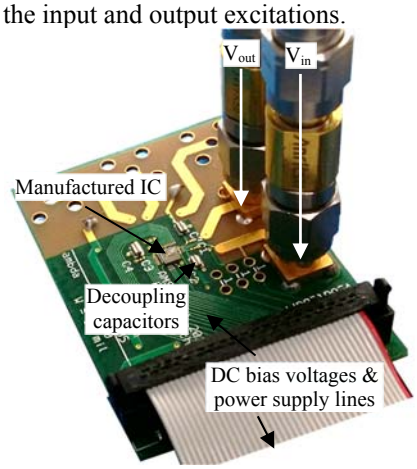


Fig. 10. *Test PCB for housing and testing the proposed all-pass network.*

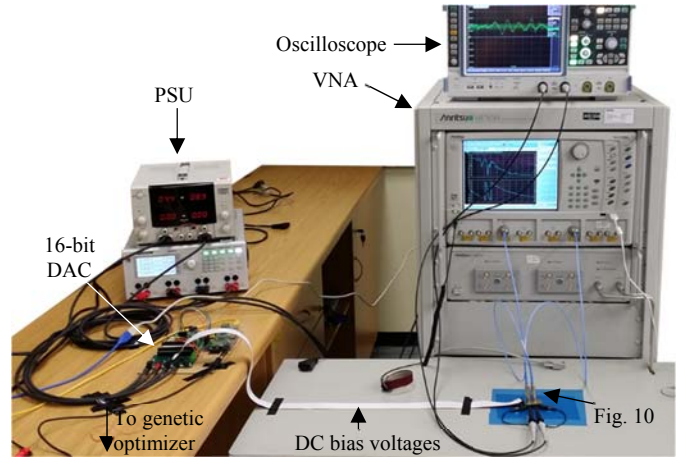
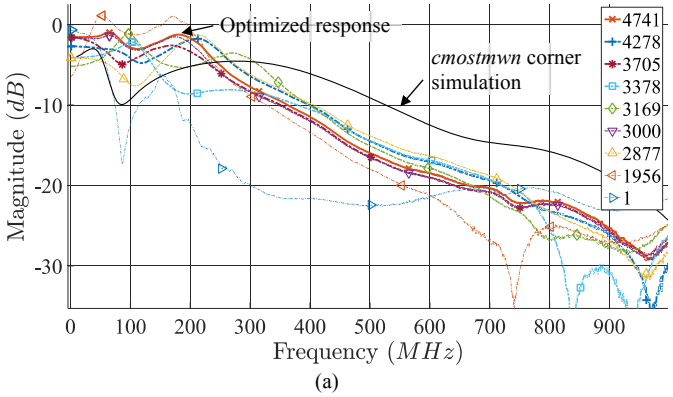


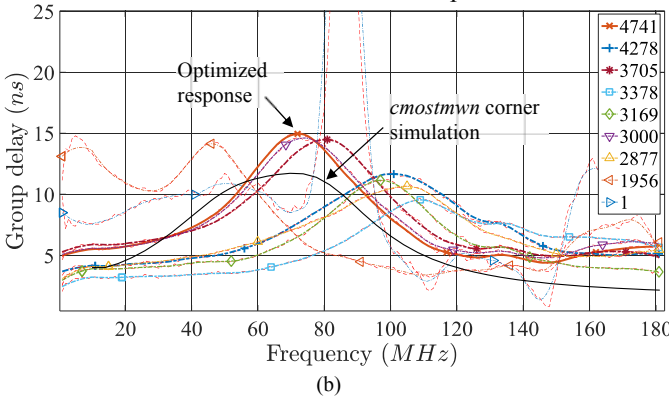
Fig. 11. *Post-production measurement and genetic optimization setup.*

Measured results are shown in Fig. 12 versus the genetic optimizer iteration. As expected from the corner simulations, the initial response is far from the desired all-pass response with a magnitude variation of ~15 dB. After running the optimizer for 4500 iterations (which represents 2.54 sweep points per optimization variable, of which there are 9), the magnitude variation is reduced to 3.1 dB with a -3 dB voltage transfer bandwidth of 280 MHz. The optimized group delay f_0 = 73 MHz and $\Delta\tau$ = 10 ns, giving a Q_D-value of 1.15.

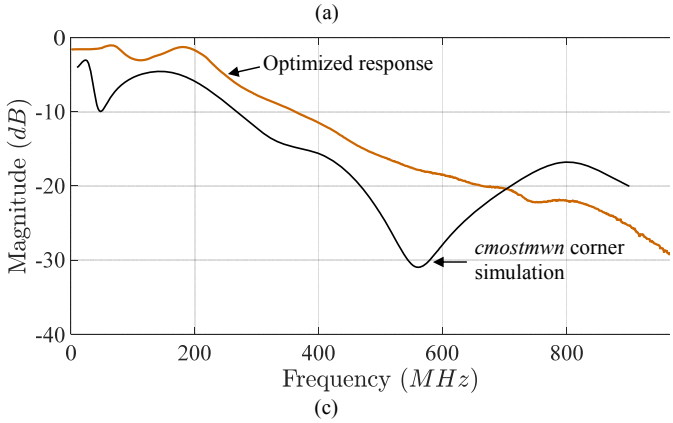
To compare measured results with simulations, the simulation corner which best corresponds to the measured responses is identified as shown in Fig. 12. This is not a trivial task since the bias control voltages in the simulated response are fine-tuned for the nominal corner whereas the control voltages applied in the measured results are optimized for an unknown corner. Therefore, the most-probable corner is identified by choosing a corner simulation which best matches all the measured results in the optimization flow.



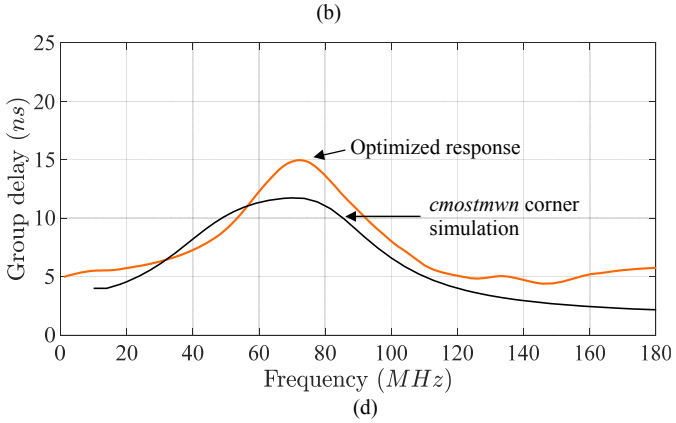
(a)



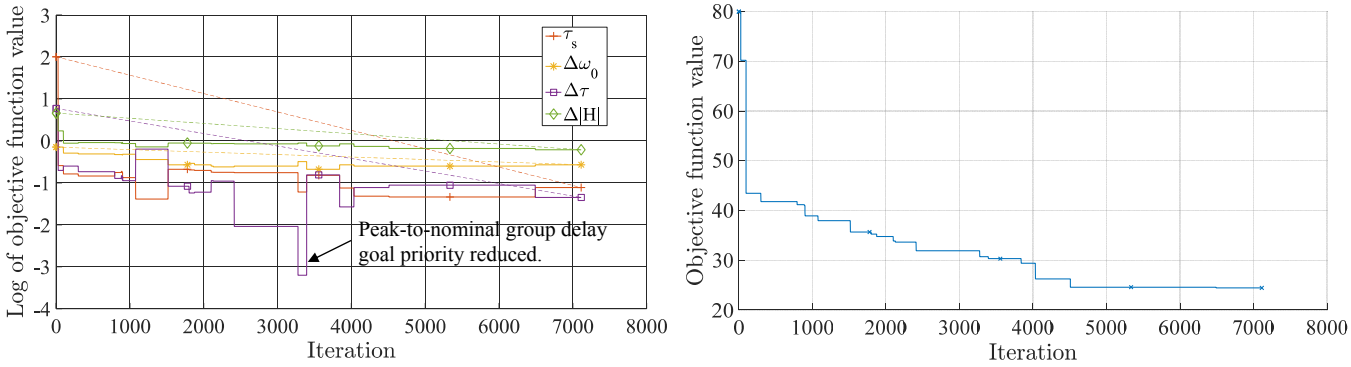
(b)



(c)



(d)



(e) (f)

Fig. 12. ***(a-d)*** *Measured voltage and group delay transfer curve of the proposed CCII.* ***(e)*** *Various metrics used in the calculation of the objective function versus the iteration.* ***(f)*** *Overall objective function versus the iteration.*

This IC is found to fall roughly into the *cmostmwn* corner (as shown in Fig. 12(a-d)) – resulting in a much lower bandwidth than predicted by nominal operating conditions and inability of any combination of applied control voltages to achieve the original design goals for f_0 and $\Delta\tau$.

Fig. 12 (c) shows the metrics used to calculate the overall objective function in Fig. 12 (d). The group delay similarity, τ_s, as defined earlier, turns out to be crucial in correctly guiding the genetic optimizer to the correct minimum. The overall objective function is then a simple linear superposition of these components.

A time-domain measurement of the optimized circuit's output for an input sinusoid of 100 MHz is shown in Fig. 13 (filtered with a digital low-pass filter to remove noise).

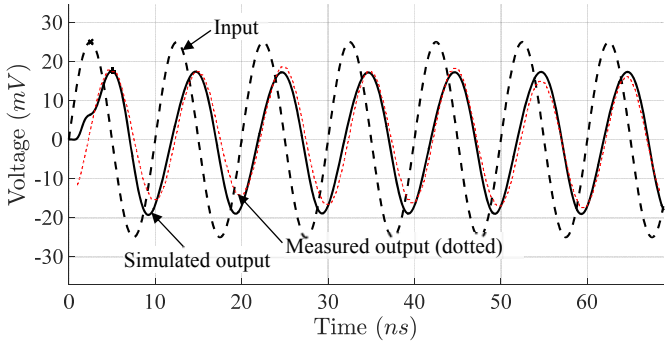


Fig. 13. *Measured input versus output sinusoid signals at 100 MHz.*

The input to the all-pass network must satisfy the small-signal condition to ensure that all active devices operate within permissible ranges. The input signal level is limited by the NMOS resistors to ensure operation in the triode region. The benefits of the proposed design over existing implementations are summarized in Table 5. A Q_D-value larger than 1 is measured for the first time in literature for an inductorless on-chip implementation. As discussed in the introduction this is necessary for many ASP applications.

5. Conclusion

A novel on-chip active second-order all-pass network is proposed, with post-production tunability to account for CCII non-idealities as well as CMOS process tolerances. The method is implemented in a 0.35 µm CMOS prototype design, and subjected to automated post-production tuning using a genetic local optimizer to realize a practical all-pass network. This represents the first measured results of an active inductorless on-chip second-order all-pass network with a Q_D-value larger than 1 in published literature and therefore presents the first step of implementing ASPs on-chip in silicon. Future work should focus on increasing achievable bandwidth and reducing sensitivity to process variation.

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Table 5. Comparison with published measured work.

Ref.	ORDER	Q_D	f_0 *(GHz)*	-3dB Bandwidth (GHz)	Technology	# of L	Size (mm^2)	Power (mW)	Magnitude variation (dB)
This work	2nd	1.15	0.073	0.280	0.35 µm CMOS	0	0.0625	15 (excl. DAC)	3.1
[25]	2nd	0.19 (0.59)***	3	4	0.25 µm CMOS	0	0.085	< 95	1.5 (> 25)
[23]	2nd	0.04 (0.52)	7	13	0.13 µm CMOS	1	0.0627	18.5	0.5 (> 13)
[26]	2nd	0.098	7	16.5	0.09 µm CMOS	0	-	< 27	< 1
[27]	2nd	0.049 (0.61)	6.3	12	0.13 µm CMOS	1	-	16.5	~ 1.5 (> 10)
[24]	2nd	0.047	6	7.5	SiGe BiCMOS HBT (f_T = 95 GHz)	1	0.49*	121	~ 1
[28]	2nd (f_0 = 0)**	0	0	12.2	0.16 µm CMOS	0	0.15	90	1.4
[29]	0th (f_0 = 0)**	0	0	10	SiGeRF HBT (f_T = 80 GHz)	2	0.4197	38.8	2 – 2.5
[30]	2nd (f_0 = 0)**	0	0	4.38	0.18 µm CMOS	0	0.0512	7.88	-
[31]	2nd (f_0 = 0)**	0	0	> 3	0.13 µm CMOS	0	0.29	112	~ 0.75

* Including pads, ** constant delay with frequency, *** values in brackets are computed over the entire bandwidth with the associated magnitude variation also shown in brackets.

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