MODULAR MULTILEVEL CONVERTER WITH EMBEDDED BATTERIES AS A MOTOR CONTROLLER

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ABSTRACT

This thesis details the design of the control system and hardware for a prototype of the new inverter topology the modular multilevel converter with embedded batteries for electric vehicle applications. Within this topology, the battery cells incorporated within the battery pack are directly integrated into the motor controller/ power converter by replacing the individual module capacitors with batteries. Since the batteries are directly connected to the module switching circuit, the batteries can be individually balanced using the same technique as an active battery management system, without the need for external energy-shunting hardware.

A control algorithm for balancing the embedded batteries without affecting the motor control scheme with significantly unbalanced battery cells is presented and discussed. A multilevel space vector modulation scheme using the abc-reference frame for the selection of space vectors is developed.

Initial testing of both the simulation model and prototype was carried out using a static RL load to test the PWM scheme and battery SOC balancing scheme. A Field-oriented control scheme was then designed and implemented for controlling a salient pole surface-mounted PMSM.

The performance of the converter as a motor controller was assessed in terms of ability to balance the SOC of the embedded module batteries and total harmonic distortion over the course of the operating torque-speed range. Simulation of the control system on simulated hardware has been carried out in MATLAB; these simulation results verify the theoretical analysis. Then further verified and analysed using the developed laboratory-scale embedded battery MMC prototype.

ACKNOWLEDGEMENTS

Firstly, it would be remiss of me to not thank my supervisor Dr Paul Gaynor for his guidance, support, and expertise throughout the course of my Master's and undergraduate studies. I am deeply grateful for his patience, passion, and wealth of knowledge.

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GLOSSARY OF TERMS

AC	Alternating current
ADC	Analogue to digital converter
Arm	Connection between one DC bus pole and a single AC phase, made up of one or more semiconductor switches
Battery	Multiple cells connected together in a single package
BLDCM	Brushless DC motor
BMS	Battery management system
Bus	An electrical conductor used to make a common connection between circuits in a system
Cell	A single anode and cathode separated by electrolyte
DC	Direct current
DOD	Depth of discharge
dSPACE controller	Processing unit manufactured by DSPACE for HIL control system development
EMF	Electromotive force
EMI	Electromagnetic interference
EV	Electric vehicle
FOC	Field-oriented control
Galvanic isolation	Electrical decoupling through non-electrical transmission method (e.g. magnetic, optical)
Hil	Hardware-in-the-loop
HV	High voltage (> 1500 V_{DC}, > 1000 $V_{AC,RMS}$)
ICE	Internal combustion engine
Inverter	DC to AC converter
I/O	Input/Output
Leg	Two arms bridging the DC bus with an AC phase connection between the two arms
Li-ion	Refers to the overarching battery cell chemistries featuring lithium based electrolytes
MATLAB	Programming language and computing environment program
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor

OCV	Open-circuit voltage
PCB	Printed circuit board
PMSM	Permanent magnet synchronous motor
PWM	Pulse-width modulation
RMS	Root mean square
Simulink	Graphics based programming environment built into MATLAB
SOC	State of charge
SOH	State of health
SPWM	Sinusoidal PWM
STATCOM	Static Synchronous Compensator
SVM	Space vector modulation
THD	Total harmonic distortion
VSD	Variable speed drive

CHAPTER 1 INTRODUCTION

In late 2019, the New Zealand government passed into legislation the Climate Change Response (Zero Carbon) Amendment Act. The purpose of this amendment act was to affirm New Zealand's commitment to the limitation of global average temperature to less than 2 °C above pre-industrial levels, as outlined in the 2015 Paris Agreement [1]. In particular to define mechanisms for the transition into decarbonising sectors by implementing government policies. The cause of these increases in global temperature is as a result of greenhouse gas production emanating from human activities.

In terms of gross global emissions, the overwhelming majority of emissions are produced by the Energy sector (Figure 1.1). However, in terms of New Zealand's emissions profile in 2019, the largest contributor is from Agriculture (48 %) and Energy is the second largest contributor (42 %) [2]. In terms of changes in emissions, between 1990 and 2019, total gross emissions increased by 26 %, agriculture by only 17 %, but Energy increased by 44 %.

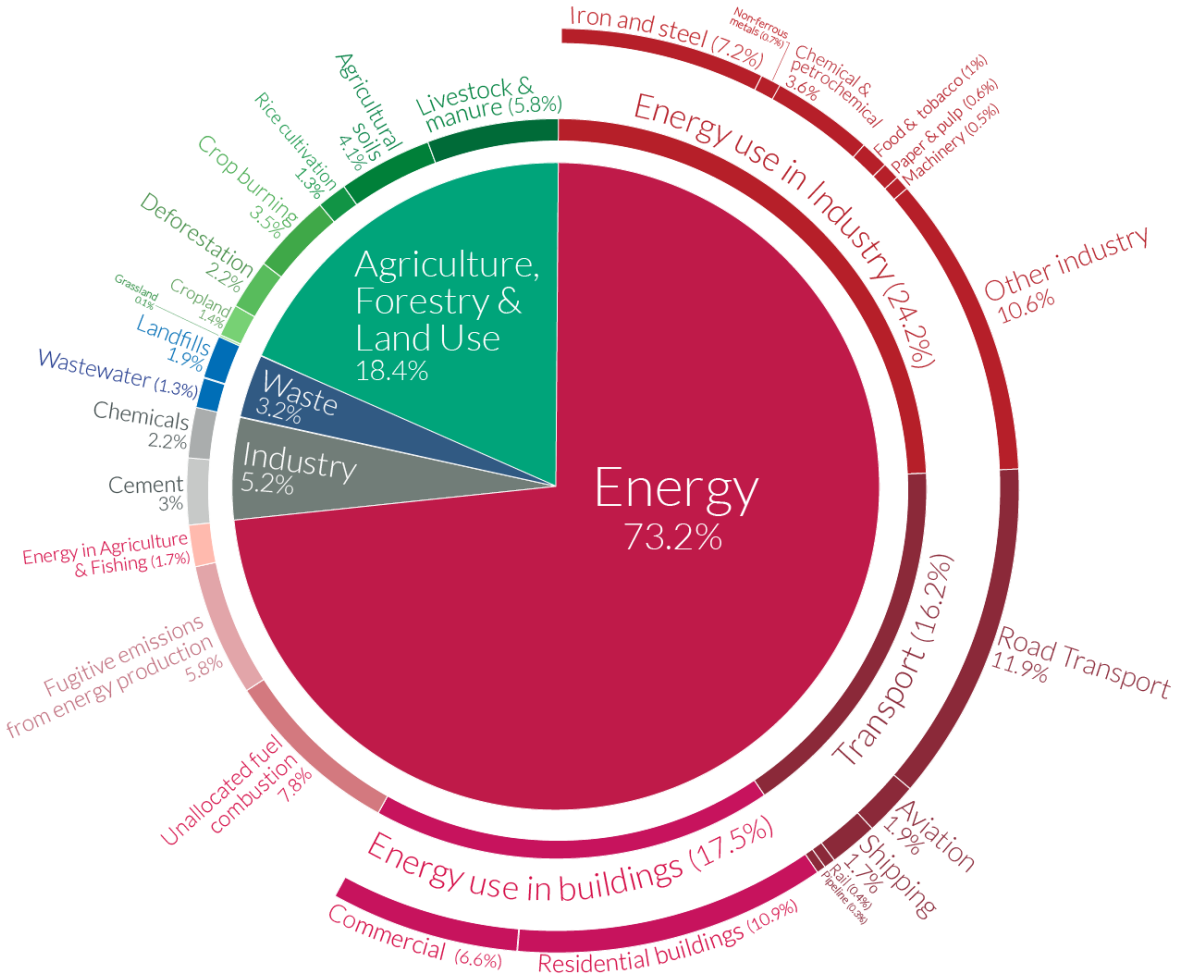


Figure 1.1. Sector contributions to global emissions in 2016 [3]

The Energy sector is comprised of energy industries, manufacturing and construction, transport, and Other. Transport emissions make up 50 % of all Energy sector emissions and have increased by 85 % over the last 30 years, whereas Energy industries have decreased by 23 % and manufacturing by only 44 %.

CHAPTER 1 INTRODUCTION

The transport sector is made up of predominantly Road Transportation, Domestic Aviation, and shipping. Of this, 91 % of emissions are from Road Transportation and have nearly doubled in the past 30 years.

Furthermore, New Zealand's gross carbon emissions are projected to increase by 19.5 %, with the transport sector set to continue to contribute more than the rest of the energy sector. For New Zealand to meet its international carbon emissions reduction targets, decarbonising the transport industry will be a key way of meeting these obligations.

As such, reducing carbon emissions through higher efficiency combustion engines will not have a significant enough impact. Therefore, to meet our obligated carbon levels, alternative powertrain options need to be become commonplace. One such alternative, electric vehicles (EVs) have the distinct advantage of producing no direct carbon emissions through their operation. However, their integration into society is hampered by short-range capacities due to the limited energy storage capabilities of electrochemical battery cells, a lack of charging infrastructure. Some of these deficiencies could be alleviated through the usage of a more compact, flexible, reliable powertrain. The work detailed in this thesis helps tackle some of these issues through exploring the usage of a variation of an inverter topology used for high voltage applications in place of standard traditional EV inverters.

1.1. MOTIVATION AND PROBLEM STATEMENT

As of the end of 2020, the number of EVs operating worldwide exceeded 10 million, doubling that of just three years prior [4]. However, barriers restricting rapid consumer uptake of EVs have been identified by a 2015 report prepared for the Ministry of Transport [5], these include:

- Electric vehicles are significantly more expensive than their internal combustion engine counterparts
- The limited supply of vehicles and little variety in models
- Availability of and access to charging infrastructure
- The perceived limited ranges and long charge periods

This has been spurred on by government policies incentivising purchasing of EVs and construction of infrastructure to support EVs. It is projected that EV energy demand will rise to almost 640 TWh by 2030 (58 TWh in 2018) [6], meaning they will make up a large amount of load on power distribution systems.

The diffusion of EVs into society could be benefited by a redevelopment of the powertrain topology to one better suited to EV applications and integrating with power grids.

Due to EVs being a relatively new technology in modern times, many of the individual systems have yet to mature to a refined degree. One such system is the motor controller/traction drive. Nearly all commercial EVs on the market today operate using a basic two-level half-bridge voltage –fed converter[7]. This design decision is largely driven by the fact that they are basic in design and construction, and are significantly easier to control than many other topologies. Modern EV powertrains are split into several separate systems, these include the HV battery, motor controller/drive, and on-board charger/off-board charger interface. A question to consider is what if all of these systems were a part of a single powertrain unit?

Many DC/AC (inverter) converter topologies exist which have been used as motor controllers for EVs, these include: H bridge inverters, soft-switching inverters, and various resonant converters [7].

To alleviate many of the issues imposed by using these 2-level converters, multilevel converters have been considered and tested. However, although many of the issues imposed by 2-level converters have been mitigated, limitations inherent to multilevel converters have also restricted the proliferation of this technology. To allow for the proliferation of EVs in society, many of these limitations need to be overcome. In recent years, the Modular Multilevel Converter (MMC) has been identified as a possible solution. MMCs are a relatively new technology (circa 2001) used primarily in the electric power industry for high voltage direct current transmission (HVDC) and flexible alternating current transmission systems (FACTS). Experimentation with this topology has yielded the potential of a MMC with embedded batteries. This could allow for the integration of all the major EV electrical systems into a single modular package.

1.2. AIMS AND OBJECTIVES

This research endeavours to study, design, and test a prototype of the new converter concept, the embedded battery MMC. Within this research, high attention is payed to the hardware requirements for such an endeavour. In comparison with other research on this topology, which focus almost exclusively on the control and performance aspects [8-10]. This work was performed in parallel and compliments that of a PhD student at the University of Canterbury Electrical Engineering Department who was studying advanced embedded battery MMC control schemes for motor and charging control.

The objectives of the thesis are as follows:

- Design a MMC with embedded batteries for EV applications
- Use the dSPACE controller hardware available in the Electrical Engineering department as the controller and use the HiL development strategy to develop the required control systems
- Produce and assemble hardware for a prototype version of the proposed converter
- Design a SOC-estimation scheme for monitoring the state of the module batteries
- Create a closed-loop motor control scheme capable of controlling the motor over a variety of speed and torque ranges
- Develop and implement a module SOC balancing system capable of integrating within the motor control
- Define a suitable multilevel modulation technique for the proposed prototype converter
- Experimentally verify the proposed MMC prototype

1.3. OUTLINE OF THESIS

Outside of the introduction, the thesis includes the following eight chapters:

- Chapter 2 introduces important theory related to electric vehicles, in particular the variety of drivetrain setups, selection of motors, and applications.
- Chapter 3 details the requirement and functionality of Battery Management Systems (BMS). The development of a BMS, in particular the creation of a battery SOC estimation algorithm are detailed.
- Chapter 4 presents the theory behind the MMC topology and its applications, then introduces the embedded cell MMC version.
- Chapter 5 outlines the development of the control schemes required for motor control and the balancing of the module batteries.
- Chapter 6 is dedicated to the design and manufacturing of the hardware, the assembly of the MMC, interfacing the hardware with the controller, and the refinement of the hardware.

- Chapter 7 concerns the implementation of the designed control systems in Simulink, then implementing the Simulink model on the dSPACE controller, and the optimising of the model for the hardware.
- Chapter 8 details the simulation of the proposed converter, testing of the hardware prototype, and analysis of the results.
- Chapter 9 concludes this thesis, including future recommendations for improving the hardware and control.

CHAPTER 2 ELECTRIC VEHICLES

In this chapter the relevant theory behind electric vehicles and the various components will be explored. In particular, the options available to act as the energy source, and the interfacing of the energy source with the inverter. This is followed by discussion of the synchronous motor topology options and comparisons between these will be made. The design parameters for a motor for the prototype MMC will be determined and a motor selected based on these. Finally, the motor feedback sensor options and their characteristics will be explored.

2.1. TYPES OF ELECTRIC VEHICLES

Conventional internal combustion engine vehicles utilize a combustion engine for propulsion, while using petroleum or diesel fuel as the energy source. By contrast, EVs employ an electric motor for propulsion and batteries, fuel cells, super-capacitors, or flywheels, for the energy source. However, due to their lack of energy storage capability, super-capacitors and flywheels are unable to act as a sole source of energy. Currently there are four distinct categories of EV system based on a combination of propulsion source and energy source:

- Battery EVs (BEVs) utilize batteries as the sole source of energy, and electric motors as the sole propulsion source (Figure 2.1). BEVs were one solution proposed to help mitigate the energy crisis and global warming. Although, due to high manufacturing costs, short driving range, long recharge time, and minimal passenger or cargo space, their proliferation has been limited.

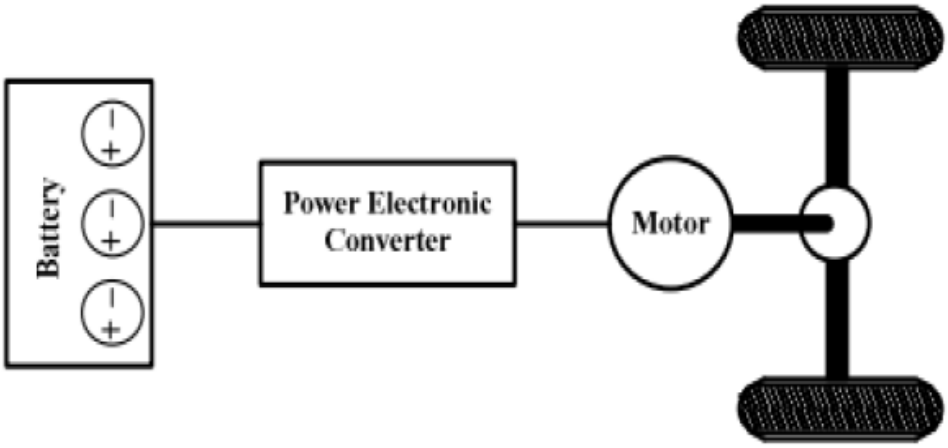


Figure 2.1. Battery EV powertrain structure [11]

- Hybrid EVs (HEVs) utilize an internal combustion engine and electric motor for propulsion (Figure 2.2). Petroleum or diesel fuel act as the main energy source, while batteries act as an auxiliary energy source. HEVs can offer similar driving ranges to solely combustion engine vehicles, while reducing the emissions produced over this range.

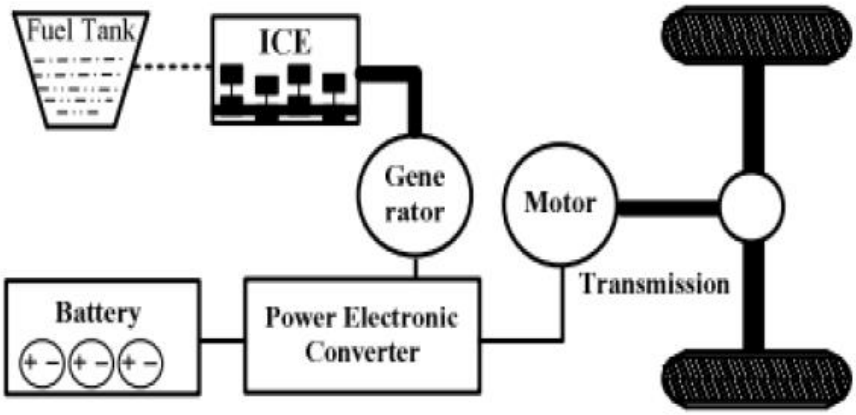


Figure 2.2. Hybrid EV powertrain structure [11]

- Fuel cell EVs (FCEVs) incorporates hydrogen or methanol fuel cells as the main source of energy, and electric motors for propulsion (Figure 2.3). Batteries are commonly used as an auxiliary energy source, due to fuel cells being unable to absorb regenerative energy. The FCEV, like the HEV, offers comparable driving ranges to combustion engine vehicles. However, due to high manufacturing costs and limitations in fuel cell supply, are drastically less commonplace compared with HEVs. A hydrogen fuel cell uses hydrogen and oxygen to produce electricity described by the following reaction equations

$$Overall\ reaction\ 2H_2 + O_2 \rightarrow 2H_20 \tag{2.1}$$

$$Anode\ reaction\ 2H_2 + 4OH^- \rightarrow 4H_2O + 4e^-$$

$$Cathode\ reaction\ O_2 + 2H_2O + 4e^- \rightarrow 4OH^-$$

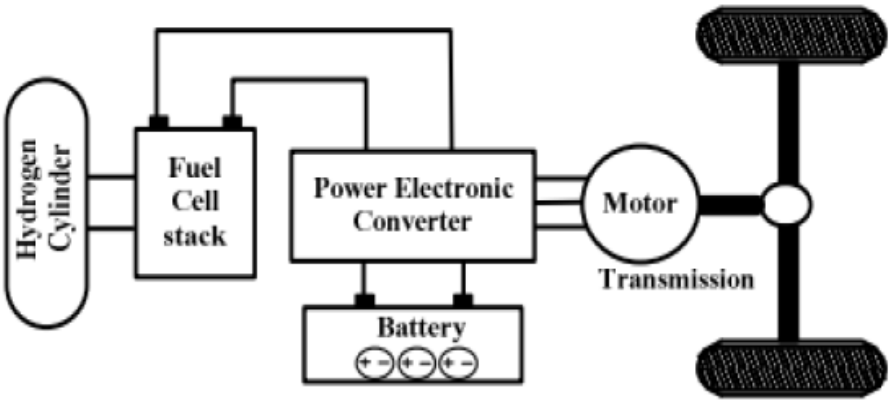


Figure 2.3. Fuel Cell EV powertrain structure [11]

- Plug-in hybrid EVs (PHEVs) refers to vehicles incorporating the usage of both fuel and electricity either independently or in conjunction (Figure 2.4). This technology acts as an intermediary between the BEV and HEV technologies. It can be viewed as wither a BEV with an internal combustion engine for support to increase the driving range or as a HEV where the purely electric powered range is extended as a result of larger battery packs able to be recharged from an external source.

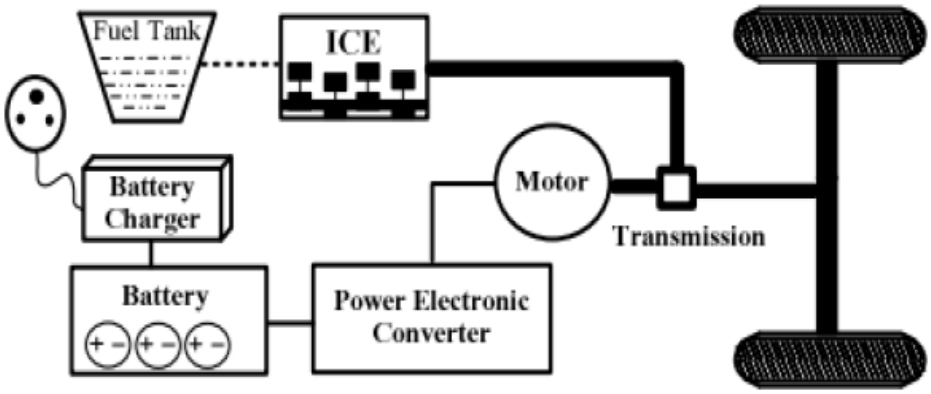


Figure 2.4. Plug-in Hybrid EV powertrain structure [11]

2.2. ELECTRIC VEHICLE OVERVIEW

Figure 2.5 shows a general overview of the electrical configuration for BEVs. Four overarching subsystems are involved: electric powertrain, battery pack, the On/Off-board charger, and low voltage systems.

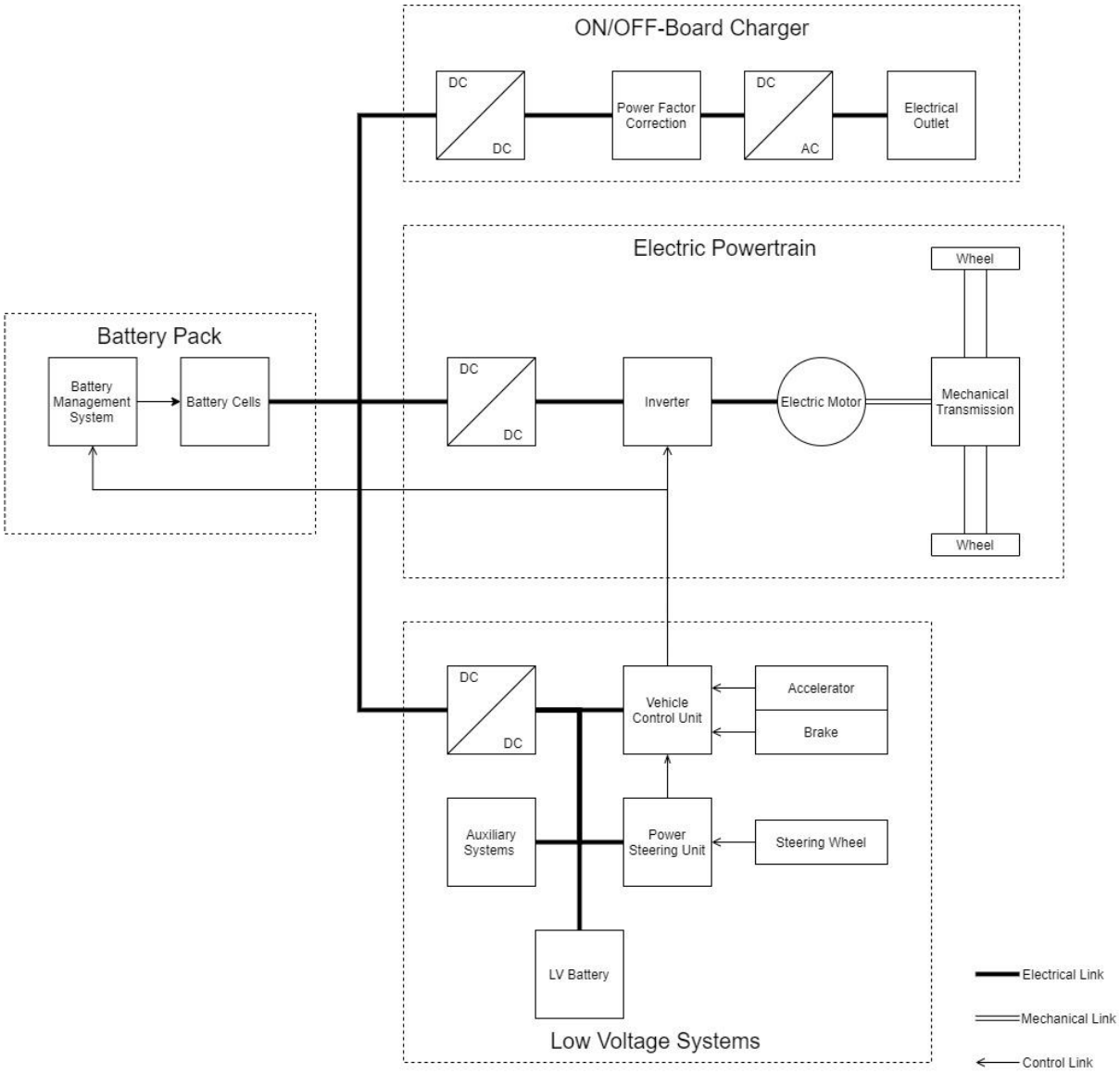


Figure 2.5. Block diagram of basic battery EV structure

Based off the control inputs provided from the driver via the brake and accelerator pedals, the vehicle control unit provides motor control targets for the inverter. Which itself acts as a regulator between the energy source and the drivetrain. The backward energy flow from the motor to the energy source is from regenerative braking. This energy can be stored by most available EV batteries as well as super capacitors and flywheels.

2.2.1. Inverters in Electric Vehicles

For general applications, an inverter converts DC electrical energy to AC through the usage of controlled switching. For EVs, the inverter acts as the bridge between the battery pack (DC) and the electric motor (AC). The most common topology, a form of voltage source converter (VSC), the three-phase full-bridge topology, uses six switches over three-phases to regulate the current through the stator windings of the motor (Figure 2.6). Anti-parallel diodes are placed across the switches to allow for reverse direction current flow. A DC link capacitor, also known as an intermediate capacitor, is responsible for smoothing ripple currents created by the high frequency switching of the inverter. This topology is capable of motor control for both induction motors,

permanent magnet synchronous motors (PMSMs), and brushless DC motors (BLDCMs), just with differing control strategies. The state of the switches shown in Figure 2.6 dictate the direction of current flow through the stator windings. If for example, switches Q_1 and Q_5 were closed, the supply voltage is applied across phases a and b of the motor, with a current drawn from phases a to b.

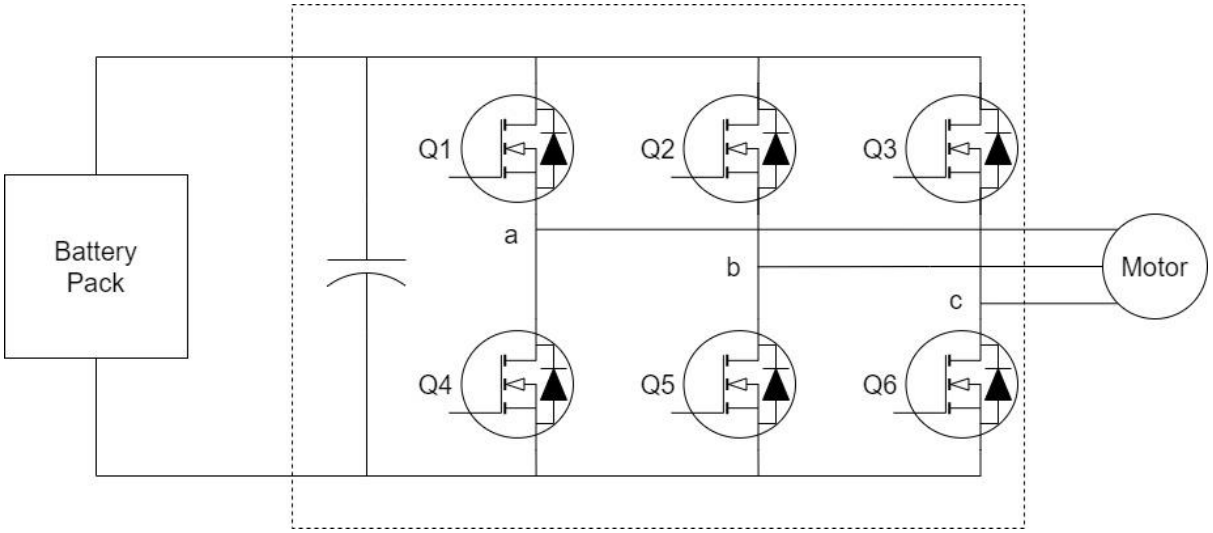


Figure 2.6. Full-bridge inverter powertrain for an EV

The main advantages of two-level inverters include:

- Basic control requirements
- Switching devices have identical ratings

The main disadvantages of two-level inverters include:

- High harmonic content in the current, resulting in the possible need for external filtering
- High switching losses
- Lack of inbuilt device fault protection

2.2.2. DC-DC CONVERTERS

A bidirectional DC-DC converter is implemented between the battery pack and inverter in some commercial hybrid EVs including the Prius, Camry, and Fusion [8]. This is done to boost the voltage input to the inverter without having to string together a large number of cells in series within the battery pack. In addition, the output voltage of the DC-DC converter can be regulated, whereas the batteries cannot. The efficiency of the boost converter style DC-DC converter is relatively low when compared to that of the inverter, due to the losses incurred by the in-line inductor. This problem cannot be simply solved by increasing the switching frequency, limiting the size, weight, and cost of the boost converter, due to the core and winding copper losses of the inductor increasing significantly [8]. To further complicate matters, the switching frequency is bound by the limitation of heat dissipation of the semiconductor switches. Resent developments in this space have yielded a solution in the form of the multi-phase DC-DC converters [12].

2.2.3. Precharge and Discharge Circuits

Many inverter/power converter topologies incorporate a capacitor on the DC bus input to filter high frequency switching noise generated by the inverter. This intermediate capacitor causes issues when connecting and disconnecting the inverter from a DC energy source. A basic interface between an EV battery pack with an inverter is provided in Figure 2.7.

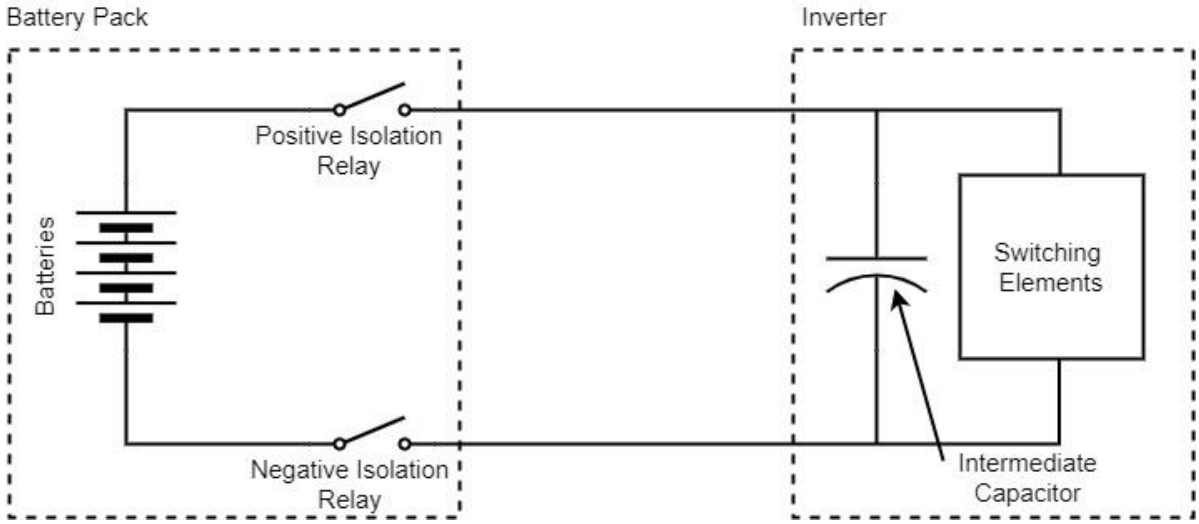


Figure 2.7. Basic powertrain DC bus

When the battery pack is connected to the DC bus by the isolation relays (controlled by the battery's energy management system) the capacitor will be charged with a current, calculated as follows

$$i_c = \frac{V_{DC}}{R}\left(1 - e^{\frac{-t}{RC}}\right) \tag{2.2}$$

Where, i_c is the capacitor charge current, V_{DC} is the output voltage of the battery pack, t is the time, R is the series resistance of the battery pack, wiring, and intermediate capacitor, and C is the capacitance of the intermediate capacitor. When the battery is connected to the bus (t = 0), a high current initially flows due to the low series resistance of the current path through the capacitor. To prevent this from damaging any componentry, all of the systems would need to be sufficiently rated for such a high current. This is unfavorable due to cost, packaging size, and availability of components rated for such high currents.

To prevent this high current on startup, the common solution is to precharge the intermediate capacitor through a current limiting resistance until the voltage gradient between the DC bus and the capacitor is too low for a high current to flow ($V_C \geq 0.9V_{DC}$) [13]. The basic DC drivetrain circuit with the addition of a precharge circuit is shown in Figure 2.8. As a result of the addition of this circuit, making the connection between the battery and the inverter becomes significantly more complicated. If the precharge resistor were to remain connected in series with the battery and inverter, the current delivered to the inverter would be severely limited during operation, and the resistor would overheat due to the large amount of continuous power flow through it. To avoid this, the resistor needs to be disconnected from the DC bus once the intermediate capacitor has been sufficiently charged. When the system is precharging, the precharge and negative isolation relays are closed. Once the precharging has been deemed successful (by either waiting a sufficiently long time or by measuring the voltage across the capacitor) the positive isolation relay will close and then the precharge relay will open.

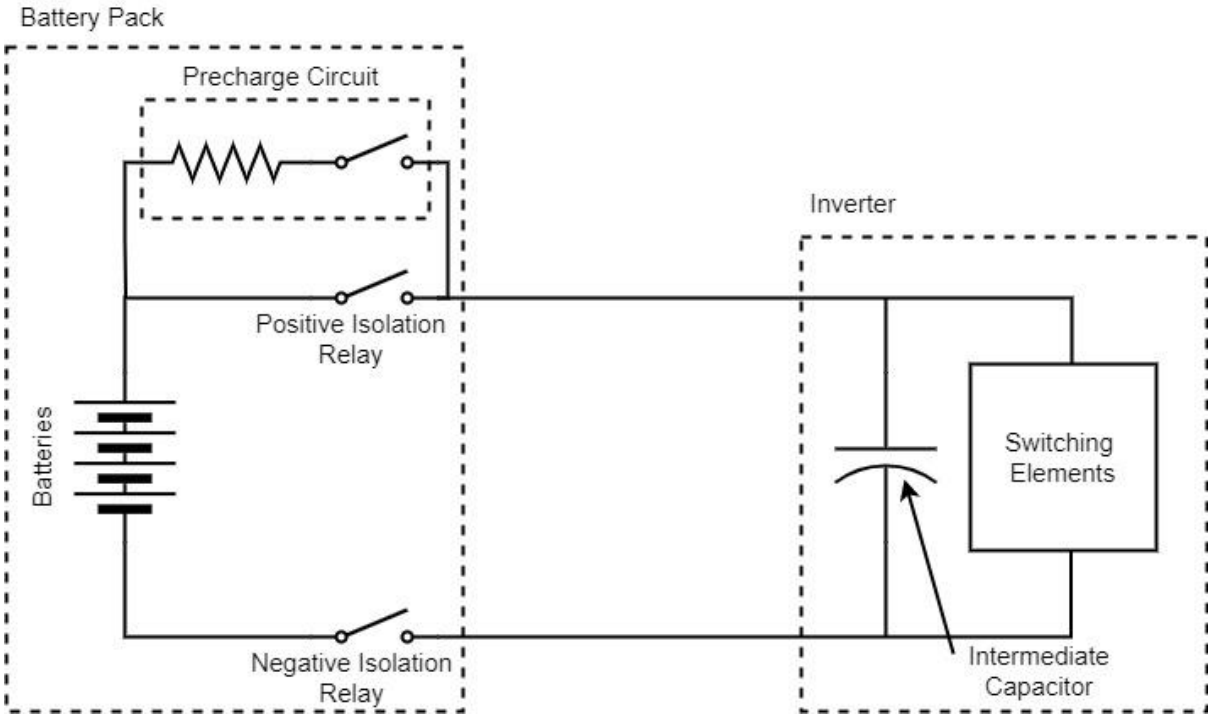


Figure 2.8. Basic DC powertrain bus with Precharge circuit

When the battery is disconnected from the DC drivetrain bus as a result of the vehicle shutting down, the intermediate capacitor will remain charged with a potentially high amount of stored energy. Although, due to high resistance paths the capacitor will eventually discharge, the time taken is unacceptable from a safety perspective [13]. A discharge circuit is used to dissipate the stored energy by switching in a discharge resistor across the intermediate capacitor. The complete basic DC drivetrain circuit with both precharge and discharge circuits is provided in Figure 2.9.

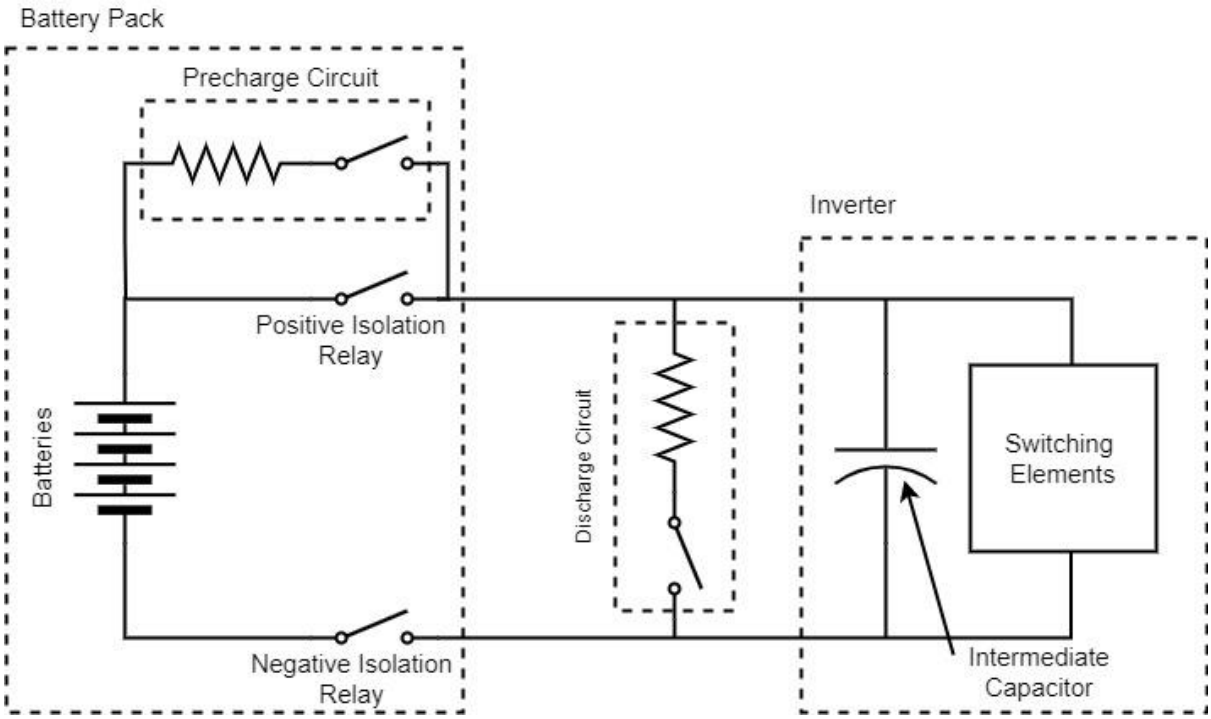


Figure 2.9. Basic powertrain DC bus with precharge and discharge circuit

2.3. MOTOR THEORY

The intended application is the primary design constraint for motor selection. While a large number of motor topologies exist, permanent magnet synchronous motors have been identified as the most promising technology for EV applications [14]. AC motors in general (PMSM, induction, BLDCM) are more ubiquitously used in comparison to DC motors due to higher efficiencies, higher power density, ability to utilize regenerative braking, robustness, higher reliability, and less need for maintenance [15].

PMSMs have low rotor inertia and high power density because of the usage of permanent magnets in place of field windings for the rotor [16]. Furthermore, with no secondary copper losses, PMSM have higher efficiencies compared with Induction Motors. This in conjunction with a wide constant power speed range (CPSR), PMSM are popular for usage in industrial drives, home appliances, and EVs [16, 17].

2.3.1. PMSM AND BLDCM

A simple three phase circuit comprised of inductors and EMF sources can be used as a simple model of a three phase AC motor, as shown in Figure 2.10. With the motor in a star/wye configuration, connected to a power source in the same configuration, and the neutral points of both virtually connected, the three phase circuit can be viewed as a series of three single phase systems.

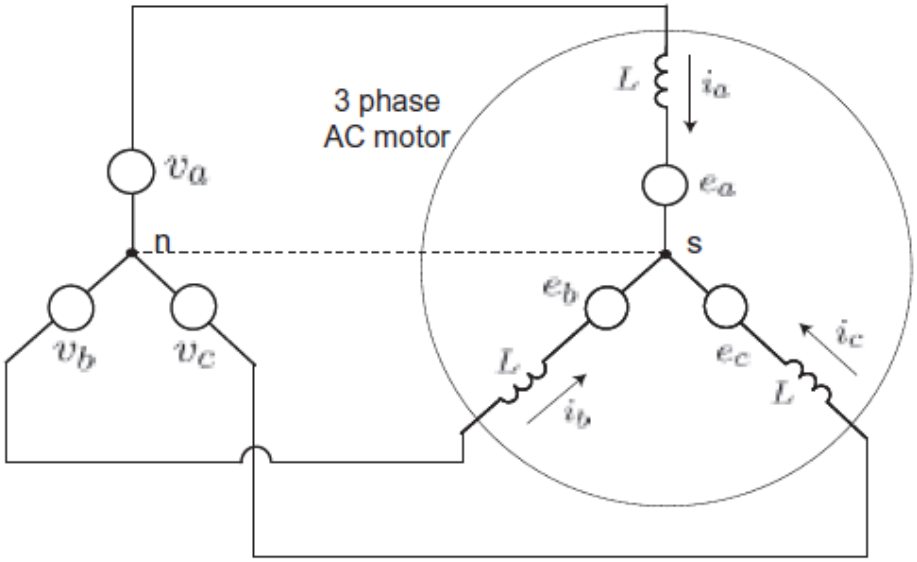
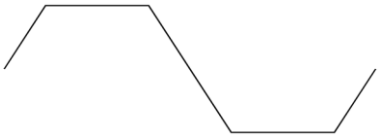
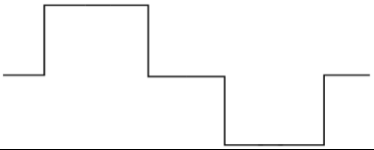


Figure 2.10. Simplified equivalent circuit of three phase motor [16]

PM motors can be separated into two distinct categories based off the back-EMF shape. One category is characterized by a sinusoidal back-EMF, known as permanent magnet synchronous motors (PMSMs). As opposed to the other characterized by a trapezoidal or linear back-EMF, known as brushless DC motors (BLDCMs). A comparison between the two options is shown in Table 2.1.

Table 2.1. Classification of PM motors based on back EMF and control method

Characteristic	PMSM or PMAC	BLDC
Control method	Vector control to the field weakening range	Current level with phase angle adjustment
Applications	High power/precise motion control	Small power/low cost drives
Back EMF		
Current		

2.3.2. PMSM TORQUE GENERATION

All PM motors have the same design goal, to establish a linear relation between the torque and phase current magnitude, independent of the rotor angle. Assuming a two-pole PMSM rotates at a constant speed ω, and the back EMF is sinusoidal:

$$[e_a, e_b, e_c] = \left[E\cos(\omega t), E\cos\left(\omega t - \frac{2\pi}{3}\right), E\cos\left(\omega t - \frac{4\pi}{3}\right)\right]$$

Furthermore, assuming the source provides balanced three phase sinusoidal currents in phase with the back EMF:

$$[i_a, i_b, i_c] = \left[I\cos(\omega t), I\cos\left(\omega t - \frac{2\pi}{3}\right), I\cos\left(\omega t - \frac{4\pi}{3}\right)\right]$$

Then the total electrical power consumption is equal to

$$P_e = e_a i_a + e_b i_b + e_c i_c \tag{2.3}$$

$$= EI\left[cos^2(\omega t) + cos^2\left(\omega t - \frac{2\pi}{3}\right) + cos^2\left(\omega t - \frac{4\pi}{3}\right)\right]$$

$$= \frac{EI}{2}\left[1 + \cos(2\omega t) + 1 + \cos\left(2\omega t - \frac{4\pi}{3}\right) + 1 + \cos\left(2\omega t - \frac{8\pi}{3}\right)\right] = \frac{3EI}{2}$$

The power per phase is not constant, but the total power is constant, as shown in Figure 2.11.

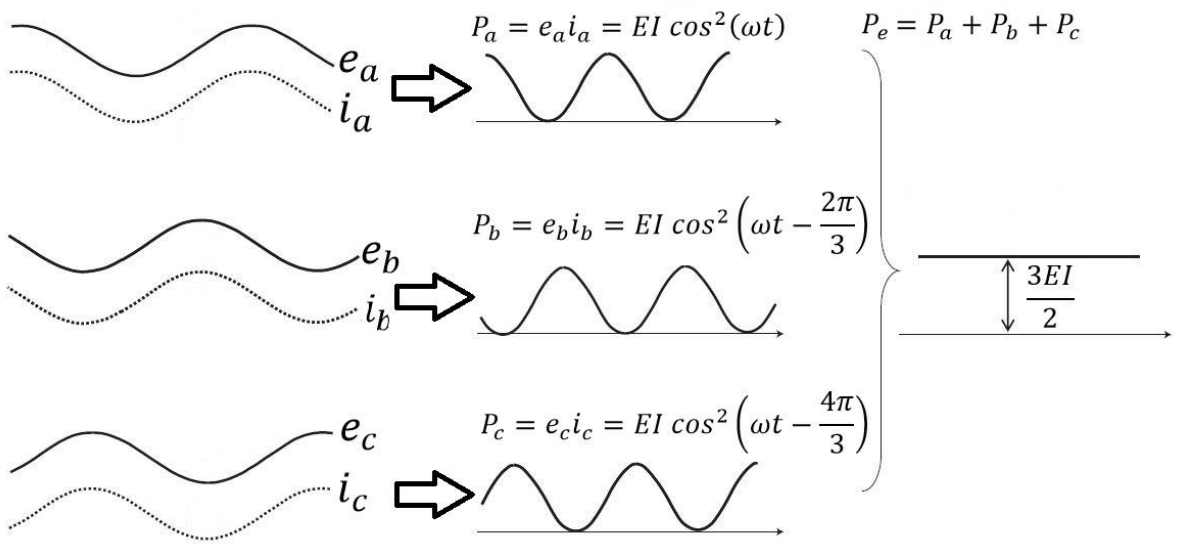


Figure 2.11. PMSM constant power production from balanced three-phase sinusoidal currents and sinusoidal back EMFs [16]

It is assumed the electrical power converted to mechanical power in the motor is conserved. From this, the shaft torque is synthetized by dividing the motor power by the mechanical speed.

$$T_m = \frac{P_e}{\omega_m} = \frac{3EI}{2\omega_m} \tag{2.4}$$

The back EMF is proportional to the rotor speed as follows

$$E = k_b \omega_m \tag{2.5}$$

Substituting Equation (2.5) into Equation (2.4) gives

$$T_m = \frac{3k_b}{2} I \tag{2.6}$$

Meaning, the motor torque is proportional only to the current magnitude independent of the phase angle, as is the case with DC motors.

2.3.3. TYPES OF PMSM

The location of the Permanent magnets in the rotor affects the voltage and torque generation, and so are classified into several different categories. If the PMs are mounted on the surface of the rotor, the motor is referred to as a surface mounted PMSM (SPMSM). Whereas, if the PMs are embedded within the rotor core, the motor is an interior PMSM (IPMSM). Other variations exist, including insetting the magnets into the surface of the rotor, and different orientations of the magnets embedded within the rotor.

For SPMSM the dq-axis inductance components are

$$L_d = \frac{\mu_0 N^2 A}{2(g + h_m)} \tag{2.7}$$

$$L_q = \frac{\mu_0 N^2 A}{2(g + h_m)}$$

Where

- μ_0 is the permeability of free space
- N is the number of stator winding turns
- A is the air gap area that the flux passes through
- g is the length of the air gap between the rotor and stator
- h_m is the height/thickness of the PM

Meaning, for SPMSM, the d-axis and q-axis inductances are the same. Whereas, for IPMSM the dq-frame inductances are

$$L_d = \frac{\mu_0 N^2 A}{2(g + h_m)} \tag{2.8}$$

$$L_q = \frac{\mu_0 N^2 A}{2g}$$

Therefore, the d-axis inductance is smaller than that of the q-axis. This is as a result of the PM being encountered along the d-axis flux, but no PM is found along the q-axis flux [16].

For all PMSM the voltage equation in the stationary dq-reference frame are

$$v_d = r_s i_d + L_d \frac{d}{dt} i_d - \omega_m L_q i_q \tag{2.9}$$

$$v_q = r_s i_q + L_q \frac{d}{dt} i_q + \omega_m L_d i_d + \omega_m \lambda$$

Where:

- r_s is the resistance of the stator windings
- ω_m is the mechanical speed of the motor rotor
- λ is the motor linkage flux

The motor flux linkage is related to the back-EMF constant as follows

$$\lambda = \frac{k_e}{\rho} \tag{2.10}$$

Where ρ is the number of pole pairs on the stator.

2.3.4. Comparison between PMSM and BLDCM

Generally, PMSMs have better speed and positional accuracy than BLDCMs, and do not produce as much torque ripple. In contrast, BLDCMs are simpler in construction and cost competitiveness. This leads to BLDCMs being more favorably used for low cost, low power (< 5 kW) applications such as household appliances. A comparison between the two is listed in Table 2.2 [16, 18].

Table 2.2. Comparison between BLDCM and PMSM

Motor Parameter	BLDCM	PMSM
Efficiency	85-90 %	> 90 %
Torque ripple	High	Low
Position feedback sensor	Hall-effect sensors (inexpensive)	Encoder or Resolver (expensive)
Stator winding orientation	Concentrated (less copper)	Distributed (more copper)
PM usage	Large	Relatively small
Eddy current losses in PMs	Large	Relatively small
EMI production	Medium	Low
Control complexity	Simple	Complex
Operating speed range	Narrow	Wide
Inverter cost	Low	High

2.4. MOTOR SELECTION

During initial consultation with the PhD student with regard to the design of the prototype MMC the decision was made to have the converter directly interface with the motor rather than through some interfacing hardware (step-up transformer). Because of this, a motor needed to be selected early in the design cycle so that the MMC could be designed to provide the necessary voltage range for the motor. Also within this consultation, the desired number of switching levels was set as five. This number was heavily influenced by the limited number of ADC channels available on the chosen controller (Table 7.1). Since every additional switching level requires an additional six ADC channels. The number of levels also adds to the control complexity for the PWM control scheme and the arm module balancing scheme, while in addition increasing the number of control signals required.

To prevent the voltage per module from being extremely high, a low voltage input range for the motor was deemed desirable. Since PMSM are the more commonly used synchronous AC motor option and the motor control simulations performed by the PHD student were with PMSM, these were deemed the preferable motor option. Based on the criteria defined above, for the application the Scorpion SII-6530-150KV PMSM was selected (Figure 2.12). Some of the performance characteristics are provided in Table 2.3.

Figure 2.12. Scorpion SII-6530-150KV motor [19]

Table 2.3. Scorpion SII-6530-150KV datasheet specifications [19]

Motor Parameter	Specified Value
No-Load Current (I_O/10V)	1.15 A
Maximum continuous current	95 A
Maximum continuous power	4.22 kW
Motor timing	5 degrees
Maximum peak current	140 A @ 2 s
Maximum peak power	5.8 kW @ 2 s

2.5. MOTOR POSITION FEEDBACK

The motor selected lacked any onboard means of measuring the rotor speed or position. Both of these parameters are important for the field-oriented control scheme detailed in Section 5.1.3. Several options exist for sensing rotor position, the most ubiquitous being resolvers, optical or capacitive encoders, and hall-effect sensors. These different options have different physical designs, implementation and electrical interfaces; so much consideration needs to be made when implementing an option.

Two different styles of position feedback sensor exist: incremental and absolute. Incremental sensors detect changes in position and output accordingly, so requires additional signal processing to generate a current position measurement. Absolute sensors output a unique positon value for each rotation step.

2.5.1. RESOLVERS

Resolvers are a highly accurate, robust, absolute transducer of position, using the basic properties of transformers to detect the rotor position (Figure 2.13). The design uses one primary winding in addition to two secondary windings, orientated in quadrature relative to each other. The turns ratio and the polarity between the primary and secondary are dependent on the angle of the rotor shaft.

The primary coil is excited by a reference AC waveform at a known constant frequency, with the secondary windings out of phase due to physical orientation. The peak voltage across the secondary coils varies as the rotor shaft moves, and is proportional to the shaft angle. Demodulating the secondary coil voltages by using the primary excitement signal as a reference, the resolver interfacing circuitry can provide a high-resolution measurement of the rotor shaft angle.

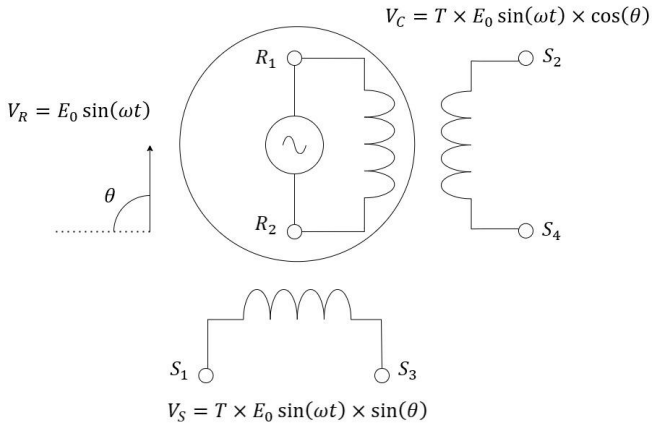


Figure 2.13. Basic resolver circuit

Since there is no physical contact between the primary and secondary coils, no additional brushes or bearings are required. Therefore, no points of friction exist to wear out through operating, and so the option is considered quite robust.

To the detriment of the technology, resolvers tend to be large and costly when compared with similar options. In addition, they require a large amount of power to excite the primary coil. Relatively complex interfacing circuitry is required for the generation and demodulation of the AC waveforms. Unlike other options, they offer an accurate positon on start-up and do not require any rotation to index or determine the initial angle.

2.5.2. Optical and Capacitive Encoders

Encoders give an incremental position output based on the effect a rotating disk has on an applied signal. For optical encoders, an LED directed towards a photosensor, with a disk with slots radiating from the center is used (Figure 2.14).

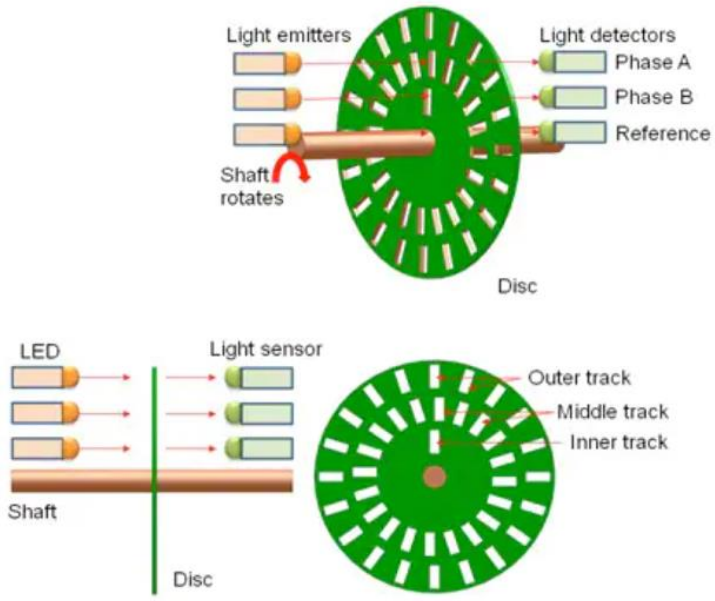


Figure 2.14. Optical encoder light source, encoder wheel, and light detector [20]

The physical positioning of the sensors and the etching on the disk allows the encoder to determine the direction of rotation. The encoder does have the drawback of being incremental rather than absolute. Determining the absolute position requires a third track and sensor to determine a zero reference point and requires the encoder to rotate enough to reach this reference point before the absolute position can be obtained. They offer good rotational resolution, lightweight, low power requirements, and are low cost. At the cost of being less robust when compared with resolvers, due to the possibility of foreign material blocking the encoder wheel.

Capacitive encoders operate in a similar manner to optical encoders, except the encoder wheel is replaced with a substrate with patterns of conductors etched into it and the photosensors are replaced with a capacitance measurement circuit.

2.5.3. Hall-effect Sensors

While traditionally used for current measurement, the hall-effect principle is used similarly to the encoder. Where a wheel magnetized with several magnetic poles is attached to the rotor shaft. Typically the wheel is magnetized with 32 poles, so the resolution is significantly less than that of an encoder or a resolver.

2.6. CHAPTER SUMMARY

This chapter important theory related to electric vehicles and the various electrical systems. The variety of powertrain structures available foe EVs are explored, with a particular interest paid to the energy sources, and the interfacing between the energy source and the drivetrain. Most notably the techniques for interfacing power sources and motors with differing operating voltage ranges, and the circuits required to safely interface the energy source with the inverter. Following on from this, the differences between permanent magnet synchronous motors and brushless DC motors were detailed. It was deemed that a PMSM was the best motor structure for this application, due to… PMSM being the more ubiquitous technology and the motor simulations used to design the application control system using PMSMs. The remaining section of the chapter was dedicated to the

methods of motor rotor position for feedback motor control. A summary of the available feedback sensor options was provided.

CHAPTER 3 BATTERY MANAGEMENT SYSTEMS

A single battery cell by itself is unable to provide the adequate voltage or current requirements for the vast majority of electrical systems they are used with. To overcome this multiple cells are strung together in series to increase the voltage, and cells are placed in parallel to increase the current capacity. For cells with the exact same properties no problems arise in this case, however due to imperfect manufacturing, all cells have marginally different characteristics (leakage currents, internal series resistance, and charge storage capacity). This results in each cell responding differently when being charged or discharged. Over time, these characteristic differences cause imbalances between the cells, creating potential differences between the cells. With cells in parallel, a potential difference between cells causes circulating currents to flow between the cells. With little to no resistance present to limit the current, a high potential difference can cause large current flow between the batteries, potentially damaging both batteries and the wiring. For cells in series, when charging or discharging, cells can become overcharged or overdischarged and thus begin operating outside of their recommended operating range. Such conditions ultimately leading to internal damage and reduction in their service life time [21].

To prevent battery imbalances from occurring a Battery Management System (BMS) is used to monitor the cells during discharging and control charging. One of the most important indicators required for monitoring batteries is the SOC, a good indicator of the current state of the battery. Equalizing, or “balancing” the SOC of all the batteries present to a common value is important for minimizing damage to individual batteries and improving the overall performance of a battery pack.

To achieve balancing, there are two distinct BMS designs: passive BMSs and active BMSs. Passive BMSs work simply by applying a resistive load to an individual battery with a higher SOC until the SOC matches that of cells at a lower SOC. The resistive load used can either be fixed [22, 23] or incorporate switching [22, 24-29].Active BMSs on the other hand, transfer energy from batteries with a higher SOC to those at a lower SOC. The variety in active BMS options is a result of various methods available to transfer, or “shunt” energy from cell to cell. For example, capacitors, inductors, transformers, and DC-DC converters, have all been used as energy transfer elements [22, 24-28]. Due to their basic control and hardware requirements, passive BMSs are significantly cheaper and easier to implement. Resulting in being the most widely used option. Albeit, at the cost of slower equalization rates and lower efficiencies, due to energy being dissipated as heat rather than redistributed to other cells.

3.1. BATTERY THEORY

A battery cell is comprised of an anode and a cathode electrode, insulated from each other by an ion-conductive separator and electrolyte [30]. Electrical potential energy is stored and released through a chemical reaction between the cathode (higher potential), anode (lower potential), and the electrolyte. Resulting in positively charged ions being transferred through the electrolyte, with electrons passing through an external electrical circuit. Different material choices to create the cathode, anode, and electrolyte, lead to the existence of various different cell chemistries with varying characteristics and different applications.

For EVs, the characteristics identified as most important include: specific energy, specific power, energy density, and power density [31]. Specific energy (gravimetric energy density) and specific power (gravimetric power density) relate to the cell’s energy storage capacity and the peak power

output compared with the unit mass. Similarly, the energy density and power density relate to the energy storage capacity and peak power compared with the unit volume. When viewed in terms of vehicle performance, acceleration is related to the specific power, while operating range is related to the specific energy.

For the perfect battery cell, the chemistry would maximize both power and energy capacity [13]. However, no chemistry available currently is able to maximize both of these traits. Because of this, different chemistries are used depending on the application. For commerciality available EVs, a chemistry with a higher specific energy is used to maximize the operating range of the vehicle. Whereas for vehicles used for shorter distances, chemistries with a greater specific power are implemented.

A summary of the battery cell chemistries used by EV and hybrid vehicle manufacturers is provided in Table 3.1. Nickel-metal hydride (NiMH) and lithium-ion (Li-ion) cell technologies are by far the preferred option for manufacturers. Historically NiMH was the preferred option when EVs were first commercially available, due to it being a more mature technology at the time. However, due to a lower specific energy and specific power rating compared with Li-ion technologies, contemporary EVs utilize Li-ion battery packs [32, 33].

Table 3.1. Summary of EV manufacturers and chosen battery cell chemistries [34].

Manufacturer	Country	Vehicle Model	Battery Technology
GM	USA	Chevy-Volt	Li-ion
		Saturn Vue Hybrid	NiMH
Ford	USA	Escape, Fusion, MKZ HEV	NiMH
		Escape PHEV	Li-ion
Toyota	Japan	Prius	NiMH
Honda	Japan	Civic	NiMH
Hyundai	South Korea	Sonata	Li-ion
Chrysler	USA	Chrysler 200C EV	Li-ion
BMW	Germany	X6	NiMH
		Mini E	Li-ion
		i3	Li-ion
		i8	Li-ion
BYD	China	E6	Li-ion
Mercedes-Benz	Germany	S400	NiMH
		Smart EV	Li-ion
Mitsubishi	Japan	iMiEV	Li-ion
Nissan	Japan	Altima	NiMH
		Leaf EV	Li-ion
Tesla	USA	Roadster	Li-ion
		Model S	Li-ion
		Model X	Li-ion

The Li-ion chemistry is a collection of different cell chemistries which all using lithium as the electrolyte. That is, they use the chemical reaction of lithium to store energy, as shown in the half-cell equation, Equation 3.1.

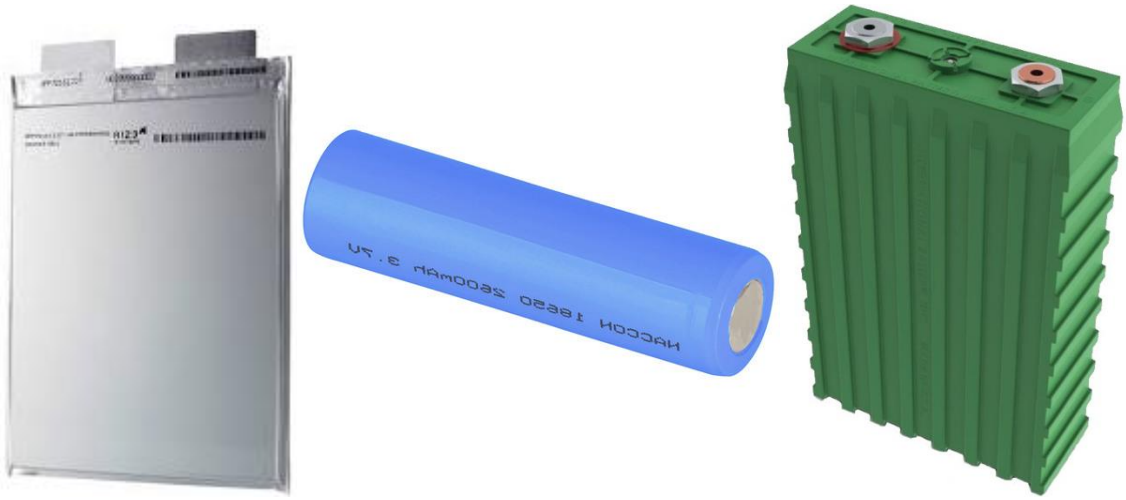
$$Li \rightarrow Li^{+} + e^{-} \tag{3.1}$$

Most Li-ion based chemistries incorporate graphite as the anode material, and varying the cathode material gives differing battery performance characteristics [30]. The performance characteristics for a variety of the most ubiquitous Li-ion based cell chemistries used for EV manufacturing are provided in Table 3.2 [30, 35-37].

Table 3.2. Comparison between Li-ion battery technologies

Cell Chemistry	Nominal Voltage (V)	Specific Energy (Wh/kg)	Specific Power (W/kg)	Cycle lifetime (No. of cycles)	Properties
$LiCoO_4$ (LCO)	3.7	400-500	300-400	500-1000	High safety risk, good lifetime
$LiMn_2O_4$ (LMO)	3.8	410-490	400-500	300-700	Cheaper, safer than LCO
$LiFePO_4$ (LiPO)	3.7	520-590	2000-3000	1000-2000	Long lifetime, high stability, basic low cost
$LiNiMnCoO_2$ (NMC)	3.6	610-650	1000-2000	1000-2000	High voltage, good specific capacity, high safety risk, good lifetime
$LiNiCoAlO_2$ (NCA)	3.6	680-760	1500-2500	500	High energy, high density, expensive

Li-Ion batteries also come in a variety of packaging options, the most common for EVs being: pouch, cylindrical, and prismatic (Figure 3.1) [13]. The cell chemistry of the cells is the same across each packaging solution, the benefits and shortcomings of each packaging option determine their application.



(a) Pouch cell (b) Cylindrical cell (c) Prismatic Cell

Figure 3.1. Examples of pouch (a), cylindrical (b), and prismatic (c) Li-ion battery cell enclosures

Cylindrical cells are the most ubiquitous packaging used in industry [38]. The chemical reaction surface area available is maximized by winding the electrodes and separator in a spiral pattern, within a steel cylinder. This construction method allows for cylindrical cells to be mass produced at a fraction of the cost of prismatic or pouch cells, while maintaining similar energy density properties [13]. The most common cylindrical cell package size is the 18650 (18 mm diameter, 65 mm length).

Because of a need to produce batteries with a thinner package, the prismatic cell was created. Layering the electrodes and separator in a ridged rectangular prism casing is used. Strong plastic is used for the casing to apply a consistent pressure on the cell internal layers. To reduce the complexity of packaging several batteries together, manufacturers generally incorporate mounting solutions into the plastic casing. However, this does increase the manufacturing costs for packaging and a lower energy density as a result of increased casing material.

Pouch cells are known for being the most energy dense packaging option. Similar to prismatic batteries, they use the electrode and separator stacking method. Except, instead of using a ridged plastic casing, they are sealed in a lightweight metallic bag. A gelatinous electrolyte is used, referred to as Lithium Polymer (LiPO). Pouch cells are generally considered to have the greatest energy density of the chemistries discussed [13]. However, requires greater care with mounting to prevent swelling while under load.

3.2. BATTERY SELECTION

For the module embedded batteries, the Li8P25RT battery module manufactured by Energus Power Solutions was selected. The module consists of eight parallel Samsung INR18650-25R battery cells within a plastic housing.

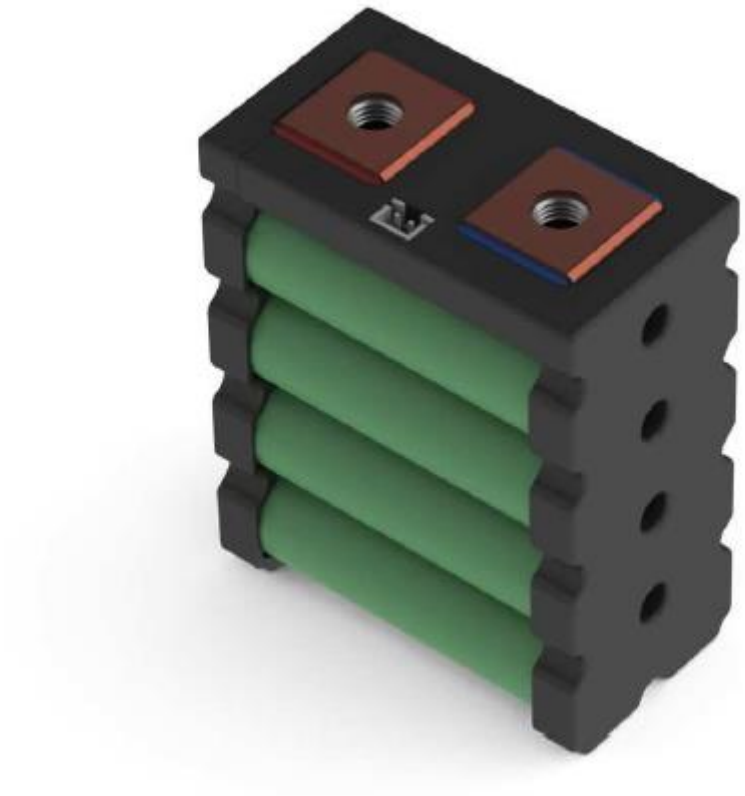


Figure 3.2. Energus Li8P25RT battery building block [39]

These batteries were selected because of their design being tailored for implementation in experimental EVs. The author also had prior experience working with these batteries on an experimental EV for FSAE competition [40]. The modules feature on-board parallel fusing on both cell terminals, and have design considerations for gas venting to avoid pressure build-up. The bolt connection allows for easy interfacing between bricks and for interfacing with a PCB. The brick also has a 4-point temperature sensor built-in, allowing for easy implementation of a thermal management component to the BMS.

The selected motor has a nominal voltage of approximately 50 V, which for a 5-level MMC requires the following number of cells per module

$$No.Series\ Cells\ per\ module = \frac{V_{motor,nom}}{2nV_{cell,nom}} = \frac{50}{2 \times 4 \times 3.6} = 1.7\ cells \tag{3.2}$$

Where n refers to the number of modules within the phase arm. For this application it was decided to use two cells in series per module, giving a nominal pack voltage of 57.6 V and a peak voltage of 67.2 V.

3.3. BATTERY SOC MONITORING

Batteries by themselves do not report the amount of energy stored within them, and the only information we can ascertain from them is their terminal voltage and the amount of current flowing in or out of the cells. The battery state-of-charge (SOC) is a percentage based representation of the energy stored in the battery versus the storage capacity of the battery. Such that a SOC of 100 % means energy stored in battery equals the battery energy capacity, and a SOC of 0 % represents no energy stored in the battery.

3.3.1. SOC ESTIMATION

To track the state and performance of a battery it is important that we measure the SOC to prevent irreversibly damaging the battery during operations. The SOC is simply a quantity used to represent the electrical charge available from the battery relative to the battery's capacity. The SOC can be simply expressed as

$$SOC = \frac{Q_{availble}}{Q_{rated}} \times 100\ \% \tag{3.3}$$

Where $Q_{availble}$ is the available capacity of the battery in Ah, and $Q_{capacity}$ is the maximum available capacity in Ah.

There are several different ways to estimate the SOC for Li-Ion batteries, these include:

- Impedance spectroscopy [41-44]
- Kalman filter/ extended Kalman filter [45-49]
- Lunenberger/Proportional integral/ Sliding mode observer [50-57]
- Neural network [58-61]
- Fuzzy logic [62-65]
- Support Vector Machine [66-69]
- Coulomb counting/ enhanced-coulomb counting [62, 70-73]
- Open-Circuit Voltage [74-76]

Impedance spectroscopy is highly accurate, although is difficult to implement and is extremely time consuming. Both the Kalman filter and observer model-based techniques have strong accuracy but are highly dependent on the accuracy of the battery model used and can be difficult to implement. Neural network, fuzzy logic, and Support Vector Machine are all data-oriented approaches. They are highly accurate, but rely on a large amount of training data to become accurate. Bookkeeping or Coulomb counter-based techniques have a reasonable degree of accuracy, are straightforward to implement, but rely on the accuracy of the sensor measurement and are prone to cumulative errors.

As shown in Figure 3.3, the battery terminal voltage is directly related to the SOC of the battery. Although this relation is linear over much of the operating region of the battery, near to the extremities of the operating region (SOC >95 %, SOC < 10 %) this relation becomes non-linear for Li-ion batteries. This problem does not exist for some battery chemistries, most notably Lead Acid batteries (Figure 3.4), and so is most prominently used for applications featuring such chemistries.

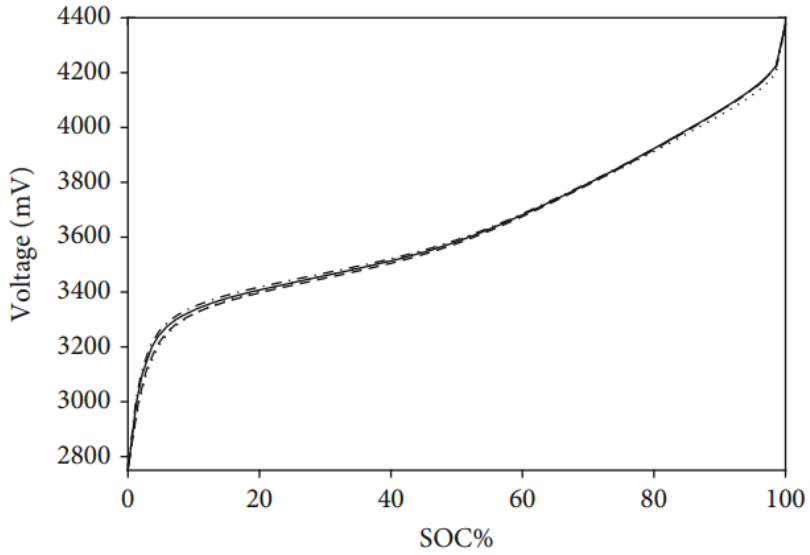


Figure 3.3. SOC-OCV curves for different lithium ion battery chemistries [77]

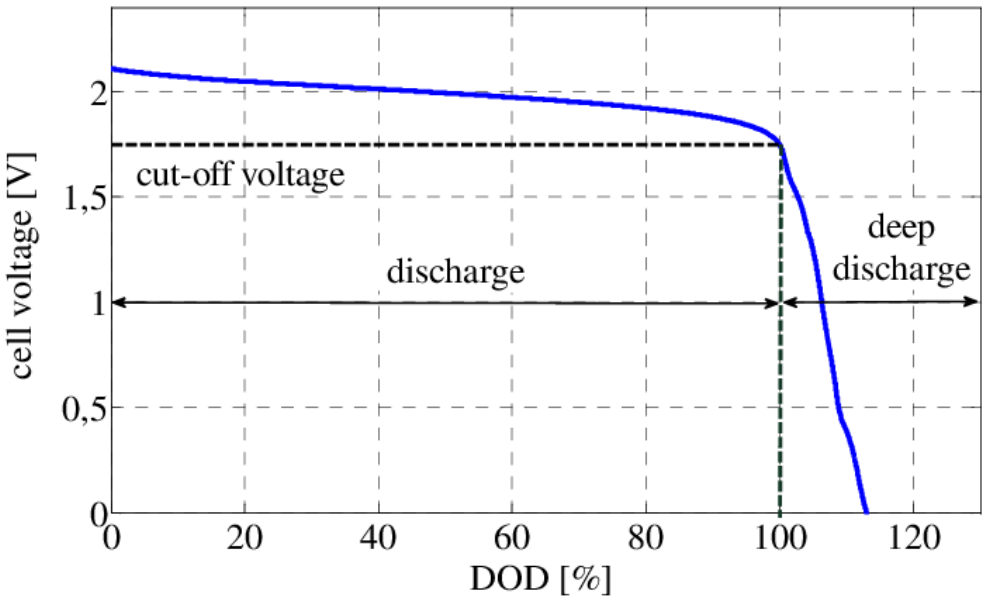


Figure 3.4. Voltage curve of lead-acid battery with deep discharge [78]

When measuring the open-circuit voltage, the battery needs to rest for a long time to allow for the terminal voltage to approach the OCV. This is to prevent discharging or charging effects on the battery to couple with the current SOC's effect on the terminal voltage. Another prevalent issue is the temperature dependence of the OCV-SOC relation is ignored [74].

The basic Coulomb Counter measures the energy input and output of the battery to calculate a change in SOC. However, this bookkeeping method is prone to cumulative errors due to its heavy reliance on the accuracy of the sensors used and the accuracy of the initial SOC used. To combat these deficiencies, the enhanced-Coulomb counter exists. In addition to monitoring current, the enhanced-Coulomb counter monitors battery voltage to limit the effect of cumulative errors. Assuming there is no current consumed by the loss reactions inside the battery, the current SOC of a battery calculated using coulomb counting is as follows

$$SOC(t) = SOC(t_0) + \frac{1}{Q_{rated}} \int_{t_0}^{t_0+t} I_b(\tau) d\tau \tag{3.4}$$

Where

- $SOC(t)$ is the SOC at time t
- $SOC(t_0)$ is the SOC at t $t = 0$
- Q_{rated} is the rated capacity of the battery in Ah
- I_b is the current flow through the battery

A fully charged battery cell has a maximal releasable capacitor (Q_{max}), which can be independent from the rated capacity. In practice Q_{max} does differ from Q_{rated} for a brand new battery, and will further decline with operating time. These can be used to evaluate the SOH of a battery

$$SOH = \frac{Q_{max}}{Q_{rated}} \times 100\ \% \tag{3.5}$$

When discharging the battery, the depth of discharge (DOD) can be expressed as the relation between the rated capacity and the quantity of charge released.

$$DOD = \frac{Q_{discharge}}{Q_{rated}} \times 100\ \% \tag{3.6}$$

Where $Q_{discharge}$ is the capacity discharged over an arbitrary period of time. The difference in DOD can be found by measuring the current flow through the battery over a period of time.

$$\Delta DOD = \frac{-\int_{t_0}^{t_0+t} I_b(\tau) d\tau}{Q_{rated}} \times 100\ \% \tag{3.7}$$

Where the battery current (I_b) is positive while charging and negative while discharging. Over time, the DOD is accumulated.

$$DOD(t) = DOD(t_0) + \Delta DOD \tag{3.8}$$

Assuming the operating efficiency is 100 % and battery aging has no effect, the SOC can be calculated as

$$SOC(t) = 100\ \% - DOD(t) \tag{3.9}$$

Considering the case where the SOC is not equal to 100 %, the SOC can be estimated as

$$SOC(t) = SOH(t) - DOD(t) \tag{3.10}$$

3.4. IMPLEMENTED SOC ESTIMATION ALGORITHM

For this application an enhanced-Coulomb counting method was selected because of its simplicity to implement and the minimal computational burden for the Simulink model. Both coulomb counter methods rely heavily on an initial SOC estimation to compare the calculated change in SOC to generate a current SOC value.

The algorithm is based off the enhanced-coulomb counter outlined in [71], which itself is a detailed version of the existing ubiquitous enhanced-coulomb counter method. That method uses historic SOC estimations to generate the initial SOC, in favor of a measurement based approach. The implemented algorithm uses an OCV method to generate the initial SOC value required for the coulomb counter. The scheme uses a characteristic curve in the form of a lookup table based of the characteristic curve outlined in [39].

The implemented algorithm in the form of a flow diagram is presented in Figure 3.5, and the developed embedded MATLAB function is included in Appendix A.

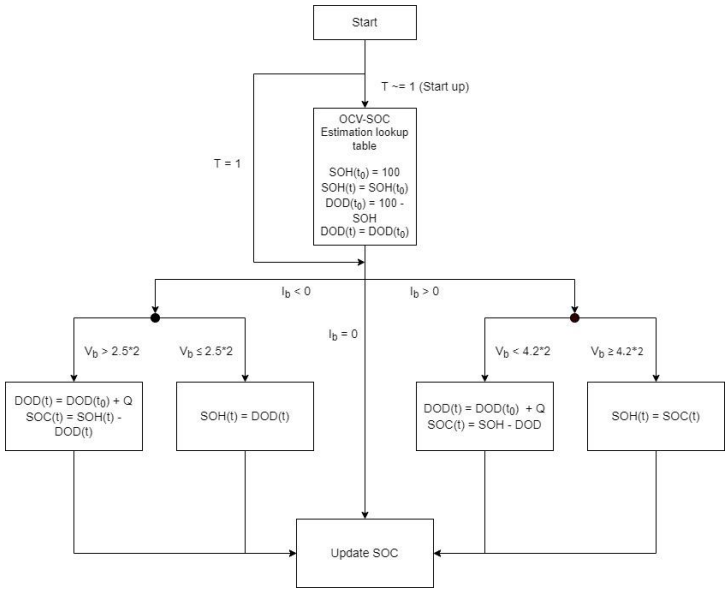


Figure 3.5. Flow-chart representation of the implemented hybrid enhanced-coulomb counter SOC estimation algorithm

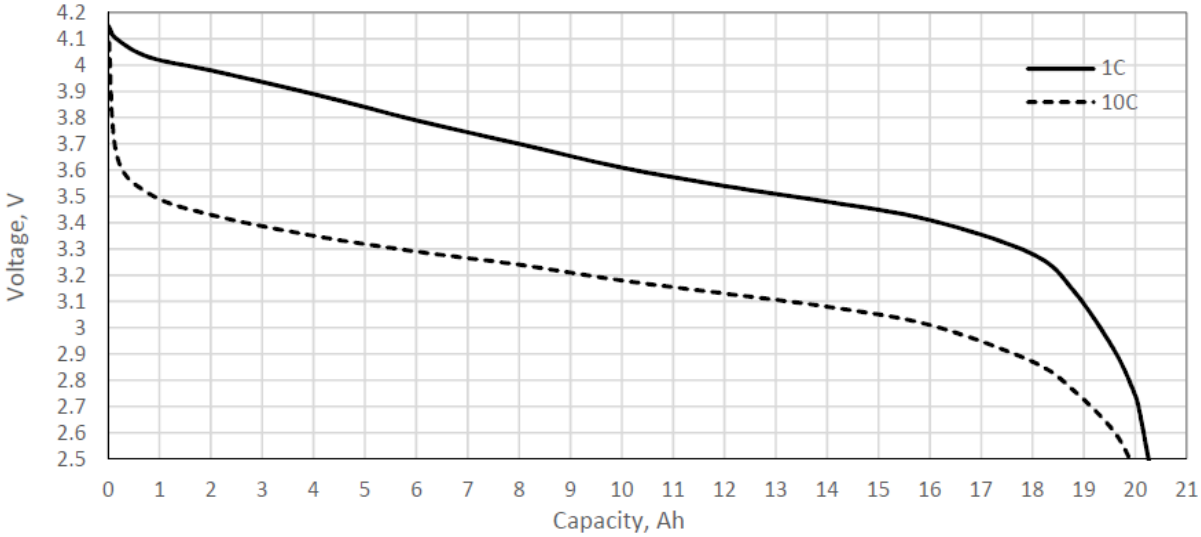


Figure 3.6. Characteristic discharge curve for Energus 1s8p 18650 cell brick [39]

After the MMC controller initialization period, the algorithm, now with an initial SOC for each module, switches to enhanced coulomb counter mode. If no arm current is detected then the algorithm simply retains the current SOC, SOH, and DOD measurements. If a negative arm current is detected, the algorithm will check if the module voltage is above the rated minimum voltage. If yes, the algorithm will update the DOD subtracting the measured change in charge out of the battery, and calculating the new SOC based off this. If not, the algorithm assumes an incorrect SOH estimation was made on startup (assuming it to be 100 %) and sets this the calculated DOD value, giving a SOC value of 0 %. If the arm current is positive, signifying a charging current, the scheme checks if the module voltage is greater than the maximum rated voltage. If not, the scheme just simply updates the DOD and SOC. If yes, the algorithm assumes the SOH estimation on startup was false and sets it to the current SOC, so the algorithm now assumes that the current SOC is the maximum SOC the embedded batteries can have.

Unlike with SOC-estimation algorithms for batteries within a singular battery pack, the implemented algorithm for integration within the proposed MMC needed to consider the switching state of the module while coulomb counting. While all modules within an arm have the same current through them, and thus only a single current sensor is required. The current measured is not necessarily the same as the current flow through a module battery at a given moment, since a module can have the battery connected to the bus, or being bypassed. This means the arm current while a specific battery is connected to the bus must be used by the coulomb counter. This was achieved by multiplying the arm current by the module high-side switch state (1 = on, 0 = off) on the input to the SOC-estimation algorithm.

3.4.1. SIMULATION

To test and develop the SOC estimation algorithm, a battery discharge/charge model was created in Simulink (Figure 3.7). Initially, the default battery model was used to test the algorithm to prevent any error introduced when creating a battery model of a specific battery.

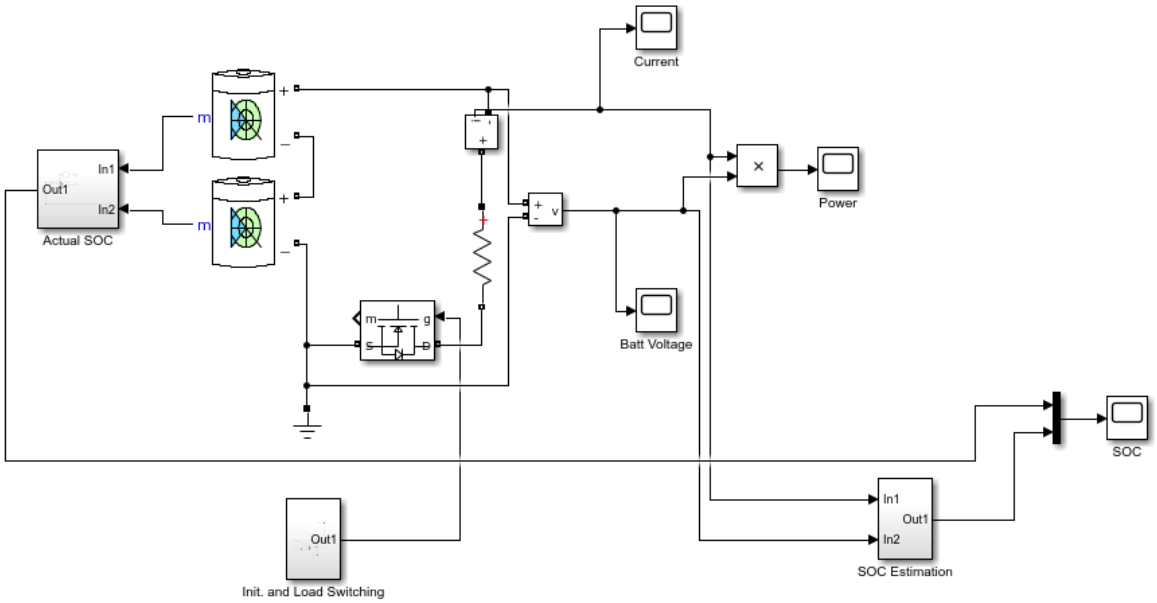
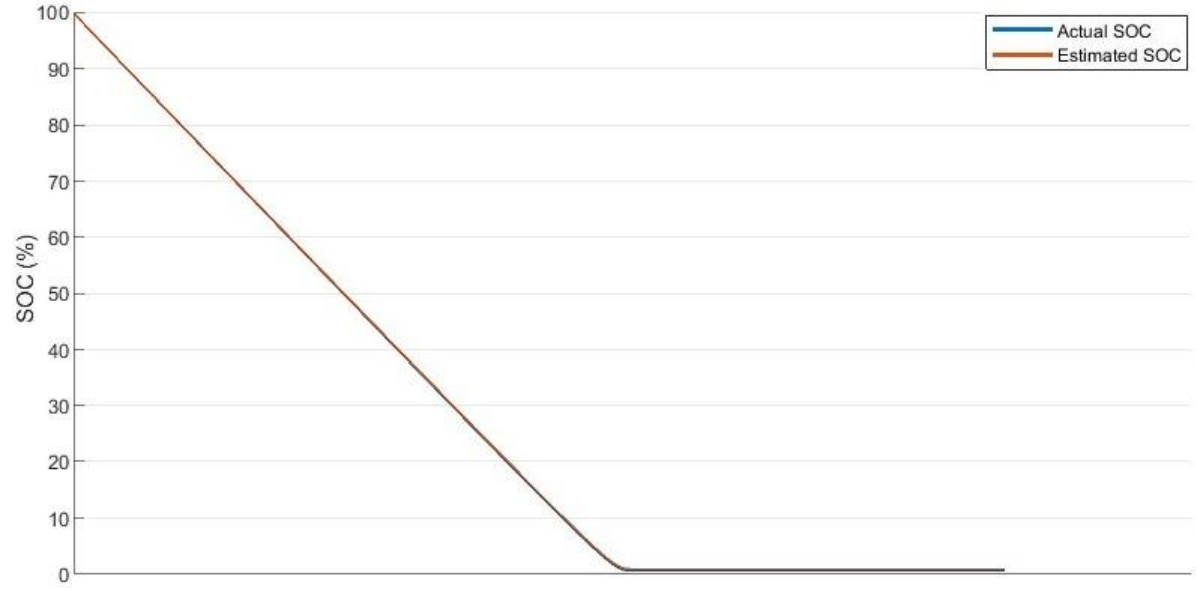
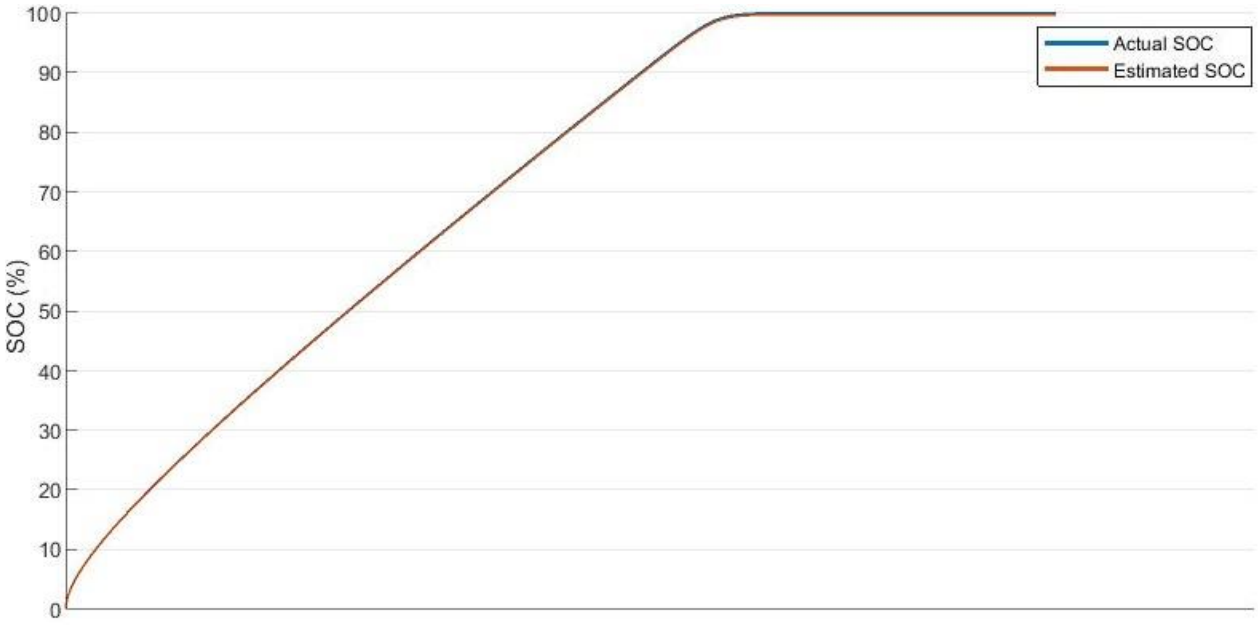


Figure 3.7. Simulink model for evaluating the performance of the developed SOC-estimation algorithm while discharging

The algorithm was deemed successful and fit for purpose when it was able to track the SOC of the two series-connected battery modules while discharging though a load and while being charged by a constant voltage Source (Figure 3.8).



(a)



(b)

Figure 3.8. Simulation SOC measurement curve for discharging and charging and the SOC-estimation curve for discharging (a) and charging (b)

For varying load levels, the estimation remained accurate to a high degree. However, when there was a difference between the two cell bricks in series, the algorithm would overestimate the average SOC of the two (Figure 3.9). For small differences in SOC (< 5%), this is tolerable; however, for larger discrepancies the algorithm is rendered ineffective. To prevent this measurement discrepancy, the battery cell bricks were manually managed by the author to ensure the bricks in each module are maintained at close to the same SOC.

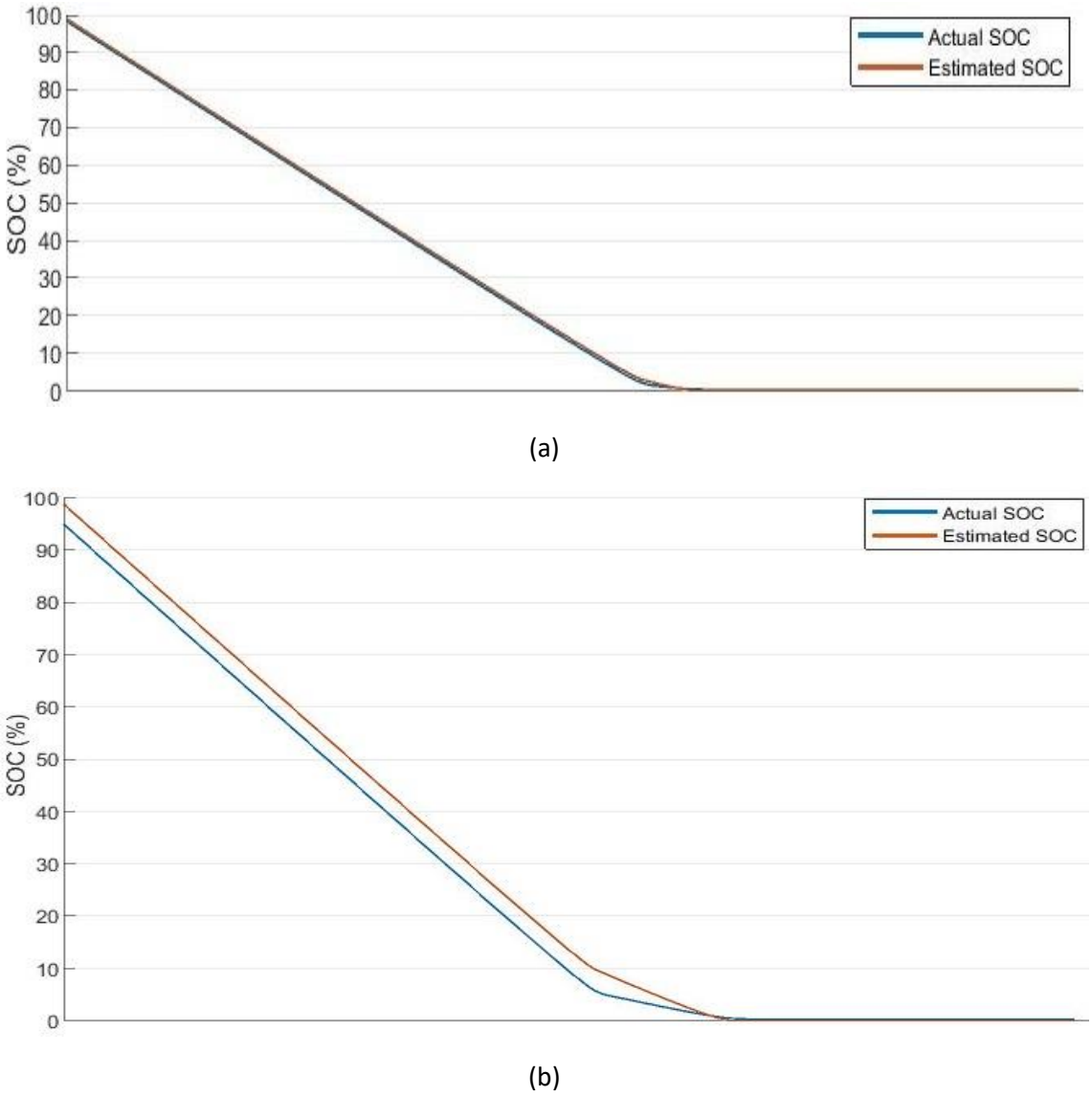


Figure 3.9. (a) SOC of 2s8p with 3 % difference in SOC between the two series batteries. (b) SOC of 2s8p with 10 % difference in SOC between the two series batteries.

After reproduction of the two-cell battery SOC was deemed to be sufficiently accurate, the estimation algorithm was adjusted to work with the cells selected for the hardware implementation of the proposed MMC. As part of this, the Energus 1s8p cell bricks were modeled using the Simulink Specialized Power Systems library Battery Model [79] based on the parameters provided by the cell brick and individual cell datasheets [39, 80]. Although other battery modeling options in Simulink exist, this block set model was chosen due to the fact that the rest of the MMC hardware model had been created using this library. Therefore, using this option allowed for the simplest implementation of a battery model into the proposed MMC and for the SOC estimation algorithm verification.

A discharge characteristic curve of the battery model was generated for creating a lookup table for the OCV SOC estimation stage of the algorithm. However, when comparing the generated model curve with the one provided in the datasheet, the two differ in the linear operating region (Nominal

area) (Figure 3.10). The model-based characteristic curve has a significantly flatter linear region compared with the manufacturer datasheet curve. Using this battery model for generating the OCV-SOC would result in a significantly overestimated SOC. Manipulation of the parameters used to form the battery model were performed in an attempt to correct for this, but no means of adjusting this linear region was found during development.

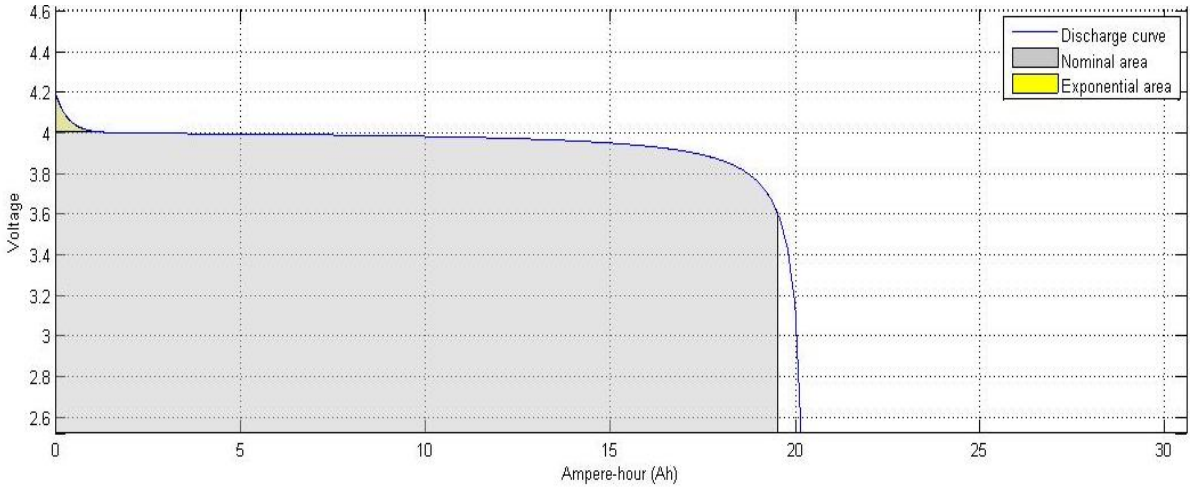


Figure 3.10. Characteristic discharge curve for Simulink model of the Energus 1s8p 18650 cell brick

Creation of a ground-up battery model would have required extensive research and validation, and so was deemed outside the scope of the project. Instead, the lookup table data points were generated by empirical derivation from the discharge curve from the datasheet and later verified with a measured discharge cycle of the batteries. This algorithm, featuring an imperially derived OSV-curve was then implemented within the MMC's control system for each individual module (Appendix A).

3.5. CHAPTER SUMMARY

This chapter detailed the necessity of battery management systems for large-scale battery packs, the required functionality for monitoring batteries, and the implementation of BMS functionality within the proposed MMC. The first section identified the issues encountered when connecting several electrochemical cells together to form a battery pack and the means of alleviating these issues in the form of a BMS. Following on from this, the techniques used by BMSs to balance battery cells are explored.

The basic theory behind electrochemical batteries with a focus on the li-ion technology is detailed. The battery technology choices made in the automotive industry are discussed, and based on these factors and the availability of batteries, the battery cells used for the prototype of the proposed MMC was decided upon.

The later section of Chapter 3 is focused on the techniques used to estimate the battery SOC and these are assessed based on their ease of implementation and their respective computational burden. From this, a hybrid enhanced-coulomb counter SOC estimation is proposed and implemented within Simulink. The performance of this scheme with respect to its viability for the proposed MMC is assessed. In particular, the discrepancies between the actual and measured SOCs and operation when the cells within the converter module have significantly different SOCs. As a part of this, the implementation of a Simulink model of the selected Li-ion battery cells is discussed.

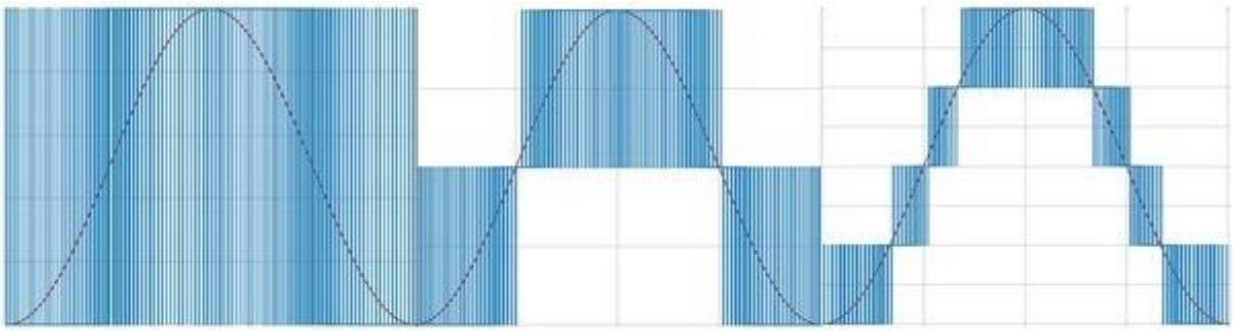
With attention paid to the discrepancies between the discharge curve of the simulation model and that of the manufacturer's datasheet.

CHAPTER 4 MODULAR MULTILEVEL CONVERTERS

This chapter details the structure and operating principle of standard multilevel inverters, including the basic modular multilevel converter. The proposed MMC structure is presented and the mathematical model used for the control system design outlined. The advantages of this proposed topology for EV applications in comparison with traditional two-level inverters is also discussed.

4.1. MULTILEVEL INVERTERS

All forms of voltage-sourced converter build up an AC voltage via a DC voltage through the usage of appropriately controlled semiconductor switches. The most common forms of inverter, the two-level and three-level, produce an AC waveform with two-levels and three-levels respectively [81]. The semiconductor switching scheme produces a sinusoidal average output. However, as shown be low in Figure 4.1 (a) and Figure 4.1 (b), the voltage switching levels are steep and high magnitude, thus creating the need for extensive filtering [82]. The multilevel converter output, shown in Figure 4.1 (c), while switching up to the same voltage magnitude, has lower voltage increments, substantially reducing the need for extensive output filtering.



(a) (b) (c)

Figure 4.1. VSC output voltages with SVM switching scheme. (a) 2-level switching level. (b) 3-level switching level. (c) Multilevel (5-level in this case) switching level

There are three common/primary types of multilevel inverter [83]:

- Neutral point clamped (NPC)
- Flying capacitors (FC)
- Cascaded H-bridge (CHB)

4.1.1. NPC INVERTERS

NPC multilevel inverters have been proposed as a suitable motor drive for EVs before [84-86]. For an n-level converter, each leg consists of $2n-2$ switches with $2n-2$ anti-parallel diodes, and $2n-4$ clamping diodes to produce an n-level phase-to-phase voltage. In addition, n-1 capacitors are connected in series across the DC-link, which are shared by each of the identical phase legs.

The basic structure of a four-level NPC inverter is shown in Figure 4.2. The switches Q_x and Q'_x, where $x = 1, 2, 3$, are controlled in a converse manner. Such that when Q_x is switched on, Q'_x is switched off and vice versa.

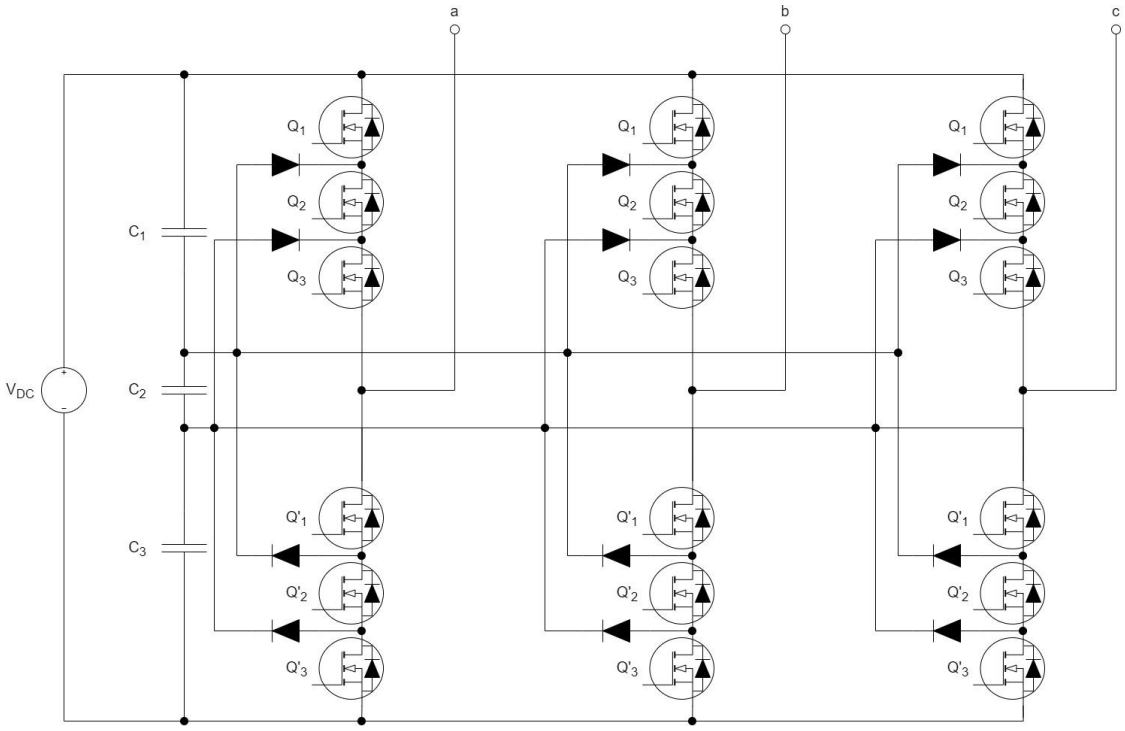


Figure 4.2. 4-level NPC multilevel inverter circuit diagram

The output voltage v_a has four voltage levels: V_{DC}, $\frac{2V_{DC}}{3}$, $\frac{V_{DC}}{3}$, and , 0. The clamping diodes are required to clamp the extremity switches to the terminals of the capacitors. This means that none of the switches can have a voltage greater than $\frac{V_{DC}}{n}$ applied across the switch.

Despite only needing to block a voltage of $\frac{V_{DC}}{n}$, some of the clamping diodes have a higher blocking voltage. This is due to the blocking voltage of each clamping diode being dependent on the relative position within the converter. However, by arranging the clamping diodes in a series configuration, this limitation is avoided. Although, this does increase the number of required components, this becomes significant for converters with a high number of switching levels. As $n(n-1)$ clamping diodes are required for the case where all the diodes have the same blocking voltage.

The current through each of the capacitors is different due to the voltage applied across the capacitors being different, leading to an imbalance in the capacitor charge levels. This can be solved by replacing the capacitors with controlled DC sources, or specific PWM strategies, or using balancing resistors [87].

Active NPC inverters are a variation of the basic NPC inverter, which incorporate switches in place of the clamping diodes to solve the unequal distribution of power issue solved by stringing diodes together in series. The switches provide a controllable path for the neutral-point current, allowing for equal loss distribution across the switches and helps to balance the neutral-point voltage.

The significant advantages of the NPC topology include [8]:

- THD of the output voltage and current are lower than comparable two-level inverters
- The switching frequency for a given THD of the output voltage is lower. Producing lower switching losses and improved efficiency.
- A lower blocking voltage is applied to each semiconductor switch. Allowing cheaper, low rated components to be used.

- Simple control methodology

Some of the disadvantages of the NPC topology include:

- The reverse voltage blocking ratings of the clamping diodes are non-identical, leading to a large number of clamping diodes being required as the number of switching levels increases.
- Each one of the semiconductor switches have unequal ratings.
- The capacitor voltages are unbalanced between the different switching levels.

4.1.2. FC INVERTERS

Similarly to NPC inverters, FC inverter have also been proposed for EV applications [88]. Structurally the FC inverter is similar to the NPC inverter; however, the clamping diodes are replaced with clamping capacitors. Each phase leg consists of $2n$ switches with $2n$ anti-parallel diodes, and $\sum_{i=1}^{n} n - i$ clamping capacitors to produce a phase-to-phase voltage with n levels.

The basic structure of a four-level FC multilevel inverter is shown in Figure 4.3. The capacitors spanning the DC link are shared by each of the identical phase legs. The capacitors clamp the switch voltage to $\frac{V_{DC}}{n}$. The switches, Q_x and Q'_x where $x = 1, 2, 3$, are controlled in a converse manner, the same as for an NPC inverter.

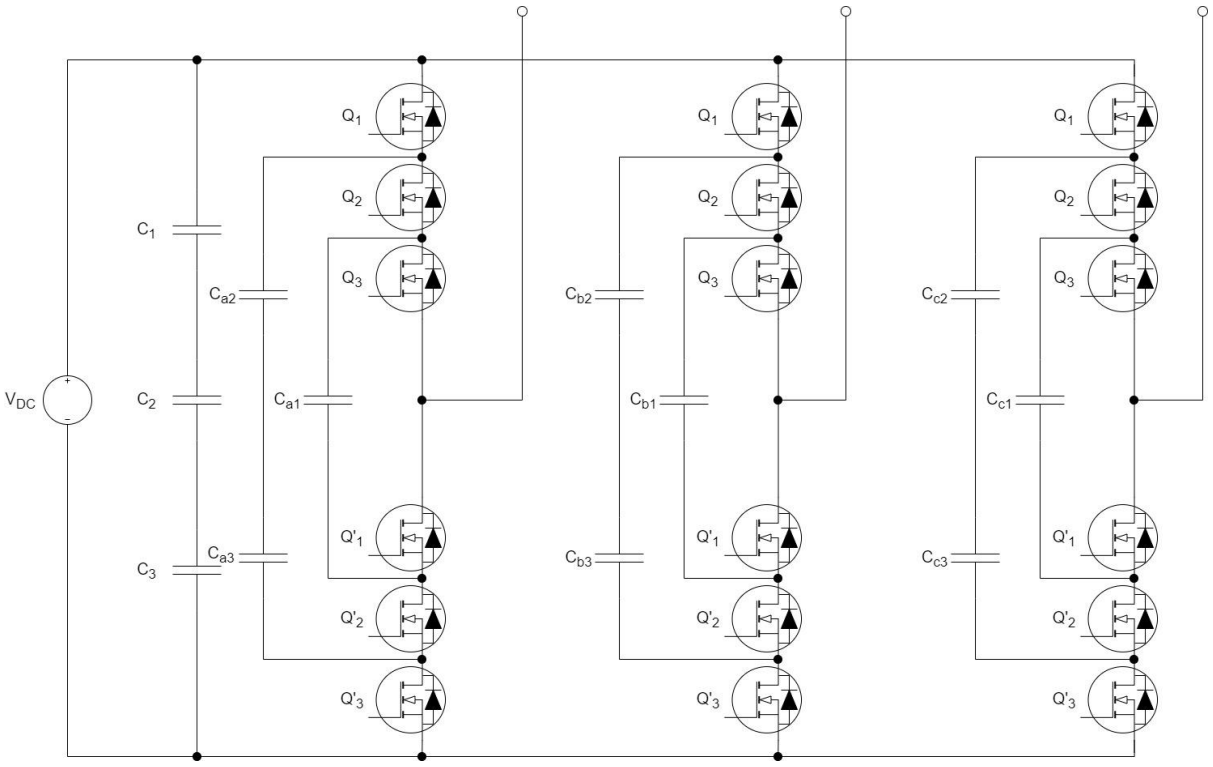


Figure 4.3. 4-level FC multilevel inverter circuit diagram

The output voltage of the inverter is the same as for NPC inverters. However, more useable switching states are available for this configuration, allowing for greater flexibility in the control of the capacitor voltages. The output voltage, v_{ao}, has four different voltage levels: V_{DC}, $\frac{2V_{DC}}{3}$, $\frac{V_{DC}}{3}$, and , 0. The inner voltage levels ($\frac{2V_{DC}}{3}$ and $\frac{V_{DC}}{3}$) have multiple redundant states, obtainable by three switch combinations, giving greater flexibility for the control of the flying capacitor voltages [87].

Some of the advantages of the FC topology include [8]:

- The THD of the output voltage and current is lower than for comparable two-level inverters.
- The high number of capacitors allow for a high fault-tolerance.
- Switching combination redundant states exist, allowing for individual balancing of the flying capacitors.
- A lower blocking voltage is applied to the semiconductor switches.

The disadvantages of the FC topology include:

- With increasing switching levels a large number of storage capacitors are required
- A large number of capacitors can cause packaging issues
- Complex control

4.1.3. CHB INVERTERS

CHB multilevel inverters with separate batteries acting as the individual DC sources have been proposed for motor speed drives for EVs [85]. The CHB consists of several H-bridge converters cascaded together, where each bridge is powered by a separate DC source. The basic structure of a three-phase 4-level CHB converter is shown in Figure 4.4. For an inverter with n H-bridges connected in series, the phase-to-phase line voltage has $n + 1$ switching levels. The phase output is simply the summation of the H-bridge output voltages. Each individual H-bridge produces three different output voltage levels, $\pm V_{DC}$ and 0, through different switching combinations of the four switches: Q_1, Q_2, Q_3, and Q_4 [87].

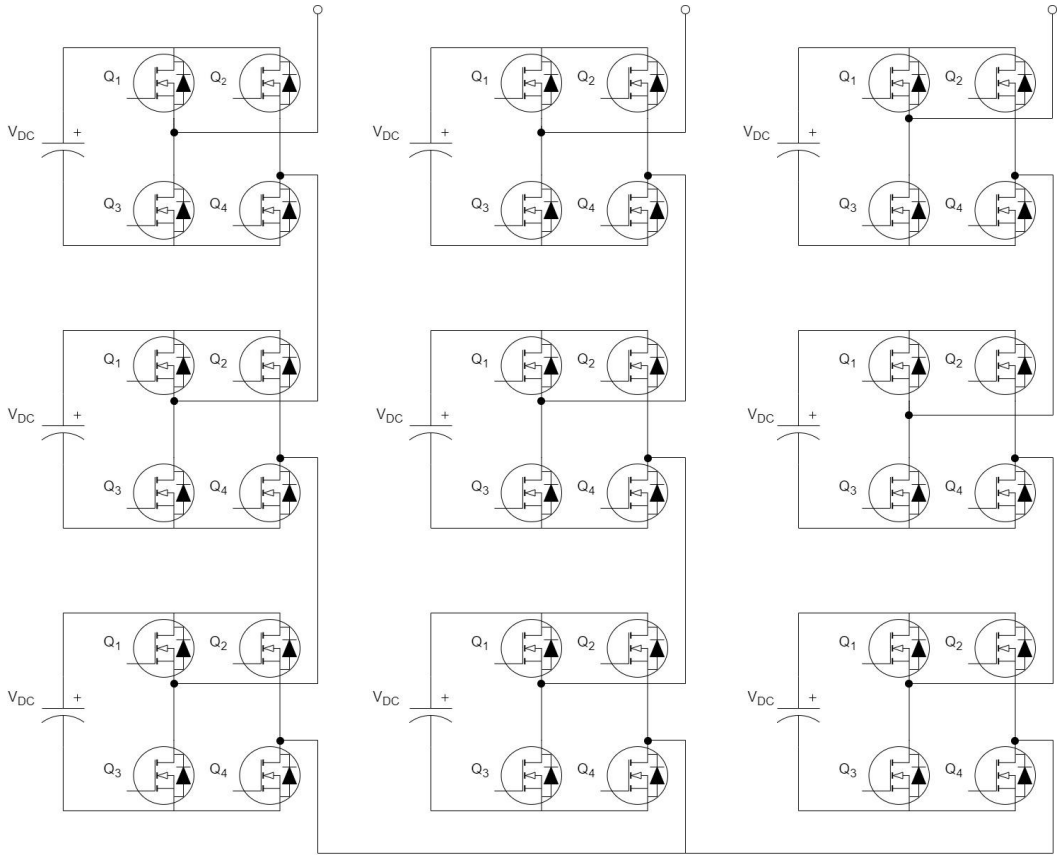


Figure 4.4. 4-level cascaded H-bridge multilevel inverter circuit diagram

The advantages of the CHB inverter include [8]:

- With increasing numbers of H-bridges, the harmonic content decreases, reducing the filtering requirements.
- CHB inverters require comparably lower components than NPC inverters.
- The circuit layout and packaging can be optimized, because of the identical structuring of each H-bridge.
- All of the switching devices have the same ratings.
- Switching losses and device stresses can be reduced by implementing soft switching.
- In the event of a fault occurring in an H-bridge, the inverter can operate with a reduced number of switching levels.
- By placing all four switches in the off-state, short-circuit states can be blocked by presenting a high impedance to the load

Some of the disadvantages of the CHB inverter include:

- Separate DC sources are required for each H-bridge.
- For the case where batteries are used as the DC source, the difference between the cells over successive recharge and discharge cycles leads to unbalanced SOCs of individual cells, necessitating the need for a BMS.
- For a star-configured CHB, the balance of the inverter legs through the use of circulating currents is difficult, due to this causing distorted motor currents. Using a delta-configured CHB partially mitigates this, as the zero-sequence current can be used. However, the zero-sequence current cannot individually balance each H-bridge's batteries, due to the zero-sequence current being the same for all three-phase legs.

4.2. STANDARD MODULAR MULTILEVEL CONVERTER TOPOLOGY

For all the advantages multilevel converter topologies have over their 2-level or 3-level counterparts, some detrimental traits persist. Both NPC and FC converters require a large number of components in series each rated for the entire DC bus voltage. The CHB lacks a DC bus for charging the individual H-bridge capacitors. Because of this, individual isolated DC-DC converters are required to charge the capacitors from a separate DC bus without bridging the H-bridges. Both of these cases mean multilevel inverters require large amounts of distributed hardware with ratings similar to those for a 2-level inverter. For increasing switching levels, these can make such a piece of hardware impractical. To overcome these limitations and provide a cost-efficient and versatile converter, the modular multilevel converter was proposed [89].

The overall structure for a standard three-phase MMC is shown in Figure 4.5. Modular Multilevel Converters expand upon the underlying principle of the multilevel converter concept by instead of a phase comprised of switches in a single series string being used, individual identical modules are switched in and out are used instead. This allows the module switches to be rated for only the individual module voltage, rather than the entire DC bus.

Each phase leg consists of an upper and lower arm, which in turn are comprised of an equal number of modules connected in series with an arm inductor connecting the phase arm to an AC load.

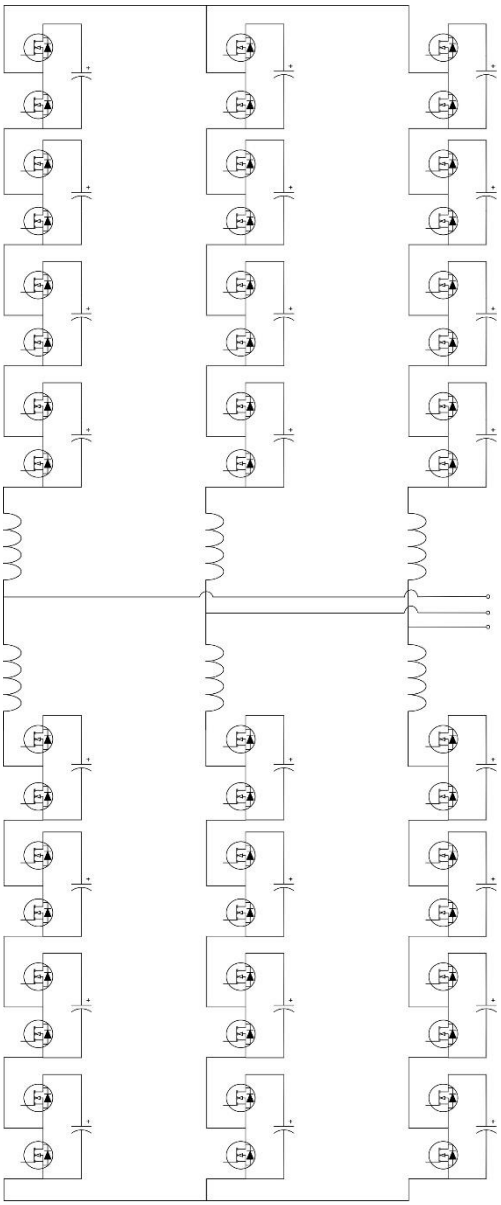


Figure 4.5. Standard three-phase five-level Modular Multilevel Converter with half-bridge modules

4.2.1. CONFIGURATION OF MODULES

The switching topology of the module can be any single-phase inverter arrangement, such as half-bridge or H-bridge. The multilevel topologies, the Neutral Point Clamped (NPC), Flying Capacitor Clamped (FCC), cascaded half-bridge, and double clamp options can offer additional switching levels within the module.

4.2.1.1. HALF-BRIDGE MODULES

The half-bridge module topology is sometimes referred to as a chopper cell [90]. The basic configuration is shown in Figure 4.6. It is comprised of two semiconductor switches with anti-parallel diodes (Q_1 and Q_2) arranged in a totem pole configuration with conventionally one capacitor (C).

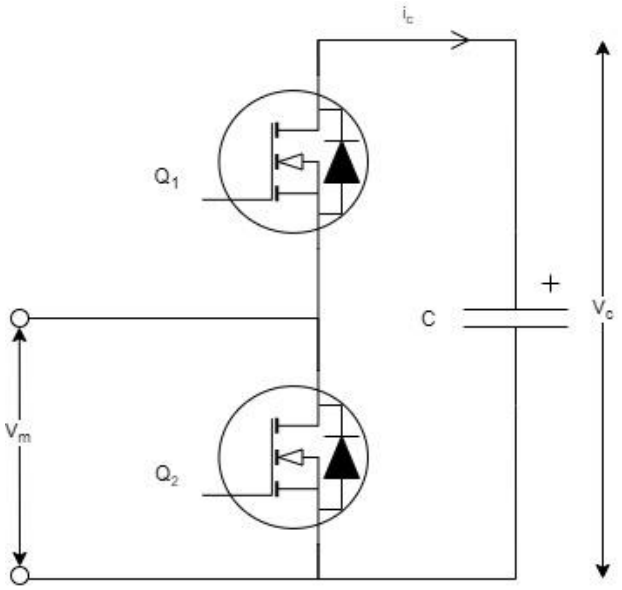


Figure 4.6. Half-bridge MMC Module

The two switches operate in a complementary manner to maintain the DC capacitor voltage at a desired voltage of V_c. The capacitor voltage is given by

$$V_C = \frac{1}{C}\int_{t_0}^{t_0+t} i_c(\tau)d\tau \tag{4.1}$$

The DC current flow through the capacitor relative to the AC arm current (i_{xy}) and the switching state of the capacitor connecting switch Q_1 is given by

$$i_c = Q_1 i_{xy} \tag{4.2}$$

Depending on the switching state of Q_1, the capacitor current is either equal to the magnitude of the arm current or zero. The possible states of Q_1 and Q_2, and their effect on the capacitor voltage for the different circuit states are shown in Table 4.1.

Table 4.1. Circuit states for half-bridge mmc module

Circuit State	Switch State		Output Voltage	Capacitor State	
	Q_1	Q_2	V_m	$i_{xy} > 0$	$i_{xy} \leq 0$
1	0	1	0	No change	No change
2	1	0	V_C	Charging	Discharging

The AC output voltage of the module has two voltage levels, 0 and V_C. When Q_1 is switched on, the module output voltage is equal to V_C. For this case, the capacitor is charged for the case where a positive current is flowing into the capacitor, and discharging when the current is following out of the module. When Q_2 is switched on, the output voltage of the module is zero. For this case, the capacitor is disconnected from the phase arm and left open-circuit, leaving the capacitor voltage constant, irrespective of the current direction. Since Q_2 is switched on, continuity of the phase arm is maintained, preserving current flow through the arm. The output voltage of the module can be described in terms of the voltage level of the capacitor and the switching state of Q_1 as follows

$$V_m = Q_1 V_C \tag{4.3}$$

4.2.1.2. H-BRIDGE MODULE

The h-bridge module topology is also known as a full-bridge converter. The basic configuration of the module is shown in Figure 4.7. The topology is made up of two half-bridge legs (Q_1, Q_2, Q_3, Q_4) with a single capacitor (C). Both of the legs consist of two switches with anti-parallel diodes operating in a complementary manner.

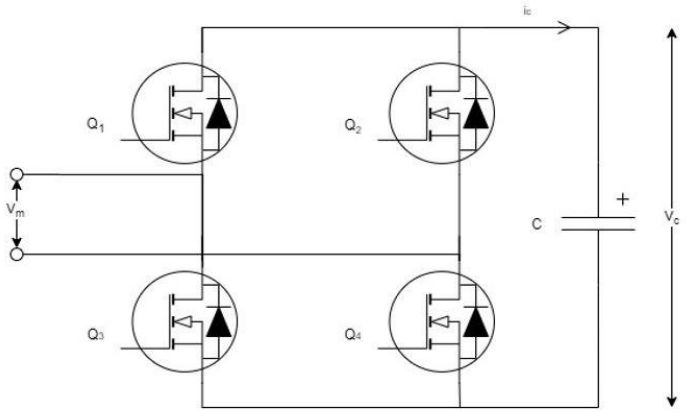


Figure 4.7. Full-bridge MMC Module

The capacitor voltage is regulated by the switching states of the four switches. The capacitor voltage for the H-bridge topology is the same as that of the half-bridge configuration (Equation 4.1). The current flow through the capacitor is dependent on the state of all four switches. The capacitor current is given as

$$i_c = (Q_1Q_4 - Q_3Q_2)i_{xy} \tag{4.4}$$

In Table 4.2, the effect of all of the switching states on the circuit state are outlined. The first four switching states generate three unique voltage levels: 0, V_C, and, $-V_C$.

Table 4.2. Circuit States for full-bridge mmc module

Switching State	Switch State				Output Voltage	Capacitor State	
	Q_1	Q_2	Q_3	Q_4	V_m	$i_{xy} > 0$	$i_{xy} \leq 0$
1	0	1	1	0	$-V_C$	Discharging	Charging
2	0	0	1	1	0	No change	No change
3	1	1	0	0	0	No change	No change
4	1	0	0	1	V_C	Charging	Discharging
5	0	0	0	0	Open-circuit	No change	No change

For the case of switching state 4, the AC output voltage is equal to the capacitor voltage. For this case, the capacitor begins charging when current is flowing into the module, and discharges when current is flowing out of the module. For switching states 2 and 3, the capacitor is disconnected from the phase arm and left open-circuit. While the arm continuity is maintained to allow current flow through the other phase arms. The multiple switching states for the same output voltage level are known as redundant switching states. The two redundant switching states are used to symmetrically distribute the power loses of the four switches. For switching state 1, the module generates an output voltage equal to the negative magnitude of the capacitor voltage. This state is used to limit the current for DC-side faults. Switching state 5 can be used to block short-circuit conditions by

presenting a high-impedance in both current directions. The output AC module voltage equation is given by

$$V_m = (Q_1 Q_4 - Q_2 Q_3) V_c \tag{4.5}$$

4.2.1.3. FLYING CAPACITOR MODULE

The configuration of a basic three-level flying capacitor module is shown in Figure 4.8. It is composed of four switches with anti-parallel diodes and two capacitors. Where switches Q_1 and Q_3 are controlled in a complementary manner, as is the case for switches Q_2 and Q_4. The voltage for the two capacitors are as follows

$$V_{c1} = \frac{1}{C_1} \int_{t_0}^{t_0+t} i_{c1}(\tau) d\tau \tag{4.6}$$

$$V_{c2} = \frac{1}{C_2} \int_{t_0}^{t_0+t} i_{c2}(\tau) d\tau$$

The capacitor current is dependent on the device switching states and the arm current as follows

$$i_{c1} = Q_1 i_{xy} \tag{4.7}$$

$$i_{c2} = (Q_2 - Q_1) i_{xy}$$

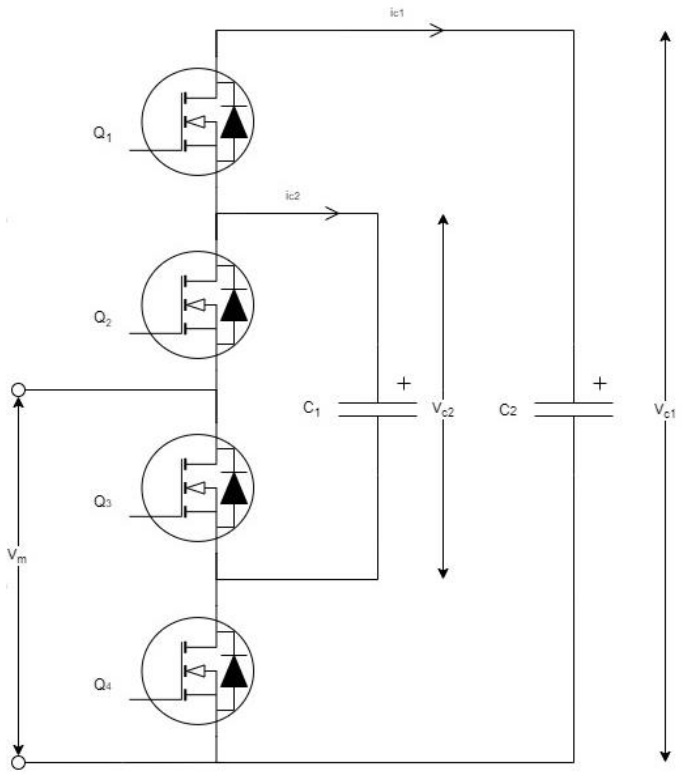


Figure 4.8. Three-level Flying Capacitor MMC Module

Table 4.3 denotes the different circuit states, the corresponding switching states, and the effect they have on the module capacitors.

Table 4.3. Circuit states for three-level flying capacitor mmc module

Switching State	Switch State				Output Voltage	Capacitor State			
						$i_{xy} > 0$		$i_{xy} \leq 0$	
	Q_1	Q_2	Q_3	Q_4	V_m	C_1 State	C_2 State	C_1 State	C_2 State
1	0	0	1	1	0	No change	No change	No change	No change
2	1	0	0	1	$V_{c1} - V_{c2}$	Charging	Discharging	Discharging	Charging
3	0	1	1	0	V_{c2}	No Change	Charging	No change	Discharging
4	1	1	0	0	V_{c1}	Charging	No change	Discharging	No change

There are four different switching combinations, generating three unique voltage levels of zero: $V_{c1} - V_{c2}$ or V_{c2}, and V_{c1}. The voltage of the capacitor C_1 is regulated as twice that of C_2, resulting in the output voltage steps being equal and voltage across the switches when the module output voltage is negative. For switching state 4, the module output voltage is equal to the voltage across C_1. For this case, the capacitor is charging while the current flow is positive, and discharging when the current is negative. While the capacitor C_2 remains constant and is unaffected by the current. For the case of switching state 2, the capacitor C_1 is being charged, while C_2 is discharged for a positive current flow, and vice versa. Similarly, for the case of switching state 3, the module output voltage is equal to V_{c2}. The capacitor C_2 will charge, while C_1 remains unaffected by the current. Since both switching states 2 and 3 have the same output voltage, they are used to balance the capacitor voltages. Finally, for switching state 1, the phase arm continuity is maintained while both the capacitors are disconnected from the module output.

The voltage output of the module is as follows

$$V_m = Q_1 V_{c1} + (Q_4 - Q_1) V_{c2} \tag{4.8}$$

The flying capacitor module can also function as a half-bridge module [91].

4.2.1.4. CASCADED HALF-BRIDGE MODULE

The cascaded half-bridge module is comprised of two half-bridges connected in series, as shown in Figure 4.9. The switches Q_1 and Q_2 are controlled in a complementary manner, the same applies for Q_3 and Q_4. The two capacitors C_1 and C_2 are charged to the same voltage. The DC current flow through the capacitors is as follows

$$i_{C1} = Q_1 i_{xy} \tag{4.9}$$

$$i_{C2} = Q_2 i_{xy}$$

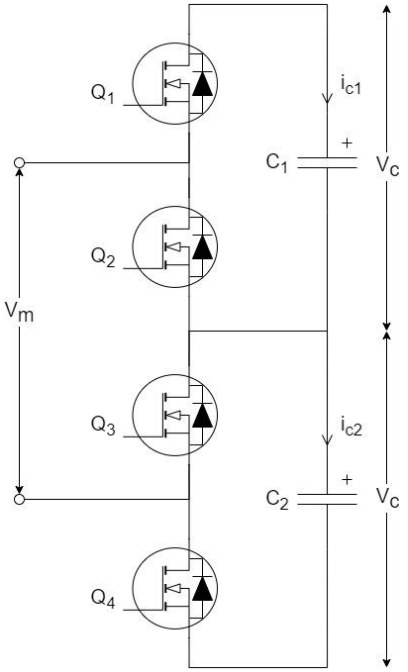


Figure 4.9. Cascaded half-bridge MMC module

Table 4.4 denotes the different circuit states, the corresponding switching states, and the effect they have on the module capacitors.

Table 4.4. Circuit states for cascaded half-bridge mmc module

Switching State	Switch State				Output Voltage	Capacitor State			
						$i_{xy} > 0$		$i_{xy} \leq 0$	
	Q_1	Q_2	Q_3	Q_4	V_m	C_1 State	C_2 State	C_1 State	C_2 State
1	0	1	1	0	0	No change	No change	No change	No change
2	0	1	0	1	V_{C2}	No change	Charging	No change	Discharging
3	1	0	1	0	V_{C1}	Charging	No change	Discharging	No change
4	1	0	0	1	$V_{C1} + V_{C2}$	Charging	Charging	Discharging	Discharging

For both switching states 2 and 3, one of the half-bridges is bypassed. For this case, the capacitor connected to the phase arm bus is charged when a positive current flow from the arm is present, and vice versa. The voltage of the bypassed capacitor remains constant, due to being left open-circuit. With switching state 1, both module capacitors are bypassed, while maintaining the continuity of the phase arm bus, giving a module output voltage of zero. The module AC voltage output can be expressed as

$$V_m = Q_1 V_{C1} + Q_4 V_{C2} \tag{4.10}$$

4.2.1.5. COMPARISON OF MODULE TOPOLOGIES

The module switching topologies outlined above are compared against one another in Table 4.5 [92, 93]. Of all the topologies presented, the half-bridge configuration is by far the most prevalent primarily due to the simple hardware requirements and basic control structure. During operation, only a single switch is turned on. Hence, the configuration boasts low losses and a high efficiency. However, the configuration only produces positive non-zero voltage levels, and cannot function with

bipolar operation and perform DC fault blocking. The H-bridge configuration offers the same voltage rating as the half-bridge module, but with twice the number of switches. Double the number of switches carry current during operation, resulting in higher power loses and lower efficiencies. The negative voltage levels produced by the configuration are used to limit currents during DC-side faults [94]. The flying capacitor configuration also features four switches (for a 3-level module), with a voltage rating of V_C. However, three module capacitors are required (each rated at V_C), three times that of the H-bridge configuration. The capacitors each have differing nominal voltages, necessitating higher design and control complexity to balance out the voltages. During operation, at most two switches are switched on and carry current. Therefore, the power losses and efficiencies are comparable to those of the H-bridge configuration. Although, like the half-bridge configuration, can only produce positive non-zero output voltages, and so cannot limit DC-side fault currents. The cascaded half-bridge topology places two half-bridges in series, resulting in a module with three level operation. However, can also produce higher voltage levels by placing additional half-bridges in series, at the cost of significantly greater control complexity. But for the three-level option, it has simple control, basic design complexity, low power loses, and high efficiencies comparable to a single half-bridge module.

Table 4.5. Comparison between MMC module topologies

Performance Criteria	Half-bridge	H-bridge	Flying Capacitor	Cascaded Half-bridge
No. of available output voltage levels	2	3	3	3
Max. blocking voltage of Module	V_C	V_C	$2V_C$	$2V_C$
Max. No. of capacitors normalized to V_C	1	1	3	2
Max. No. of switches in conduction path	1	2	2	2
Power losses	Low	Moderate	Moderate	Moderate
Bipolar operation	No	Yes	No	No
Design complexity	Low	Low	High	Low
Control complexity	Low	Low	High	Low
DC fault blocking capability	No	Yes	No	No

Other possible topologies that are implementable but not discussed here include the neutral-point clamped and double clamp module configurations.

For the purposes of this project a half-bridge topology was selected because of its reduced hardware and control requirements and its widespread use. Thus, when referring to module switching throughout the rest of this thesis, a half-bridge topology is assumed.

4.2.2. SWITCHING COMBINATIONS

The voltage levels achieved by a MMC are dependent on the number of modules incorporated in each phase arm. A summary of the relation between the output voltage, number of switching combinations available, and the selected switching level is provided in Table 4.6.

Table 4.6. The number of available switching levels with corresponding voltage levels

Output Voltage	Switching combinations	Level number, $\boldsymbol{l}$
$\frac{V_{DC}}{2}$	1	1
$V_{DC}\left(\frac{1}{2}-\frac{l-1}{n}\right)$	$\binom{n}{l-1}^2$	$1 < l \leq n$
$-\frac{V_{DC}}{2}$	1	$n+1$

The number of switching combinations available for the case where all or none of the modules are switched in is represented by a binomial coefficient, an expanded version of this is provided below

$$\binom{n}{l-1}^2 = \left(\frac{n!}{\big(n-(l-1)\big)! \times (l-1)!}\right)^2 \tag{4.11}$$

For a three-level MMC with modules charged to a constant voltage $\frac{V_{DC}}{2}$ the following switching combinations and corresponding output voltage levels are shown in Table 4.7. Where a module state of "0" denotes the module being bypassed, and a state of "1" denotes the module capacitor being connected to the phase arm bus.

Table 4.7. Output voltage levels and respective switching states for three-level mmc

Output Voltage	Module Switching State			
	M_{yu1}	M_{yu2}	M_{yl1}	M_{yl2}
$\frac{V_{DC}}{2}$	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
$-\frac{V_{DC}}{2}$	1	1	0	0

4.2.3. CONVERTER MATHEMATICAL MODEL AND CIRCULATING CURRENTS

To analyse the operation of the MMC, regard to a single phase-leg needs to be taken. This model is shown in Figure 4.10. The operation of the converter described uses a half-bridge module topology, where the module capacitors are charged to a voltage of $\frac{V_{DC}}{2}$. This three-level converter produces the output voltage levels: $\frac{V_{DC}}{2}$, 0, and $-\frac{V_{DC}}{2}$.

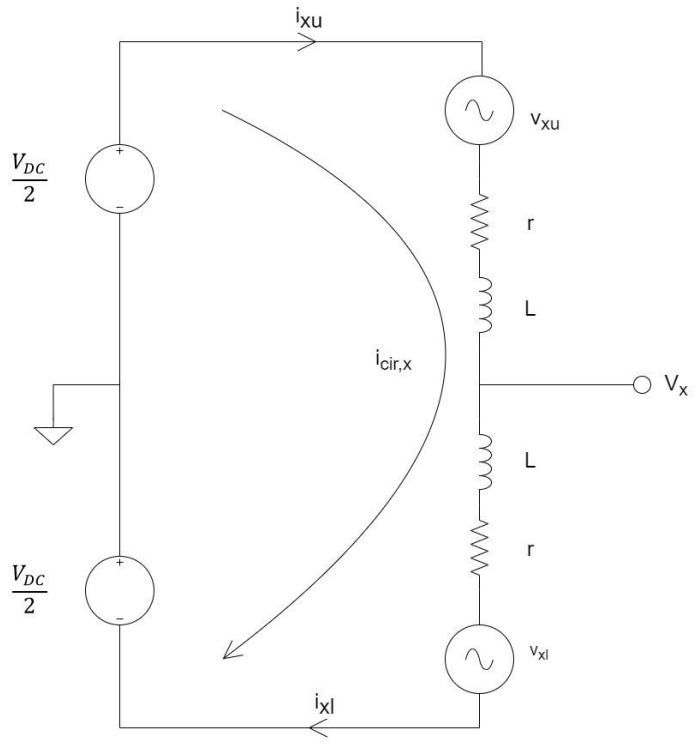


Figure 4.10. Single-phase leg model for a three-phase modular multilevel converter

The AC voltage source (v_{xu}, v_{xl}) represents the voltage output of the arm modules as follows

$$v_{xu} = v_{x1} + v_{x2} + \cdots + v_{xn} \tag{4.12}$$
$$= S_{x1}V_c + S_{x2}V_c + \ldots + S_{xn}V_c$$
$$v_{xl} = v_{xn+1} + v_{xn+1} + \ldots + v_{x2n}$$
$$= S_{xn+1}V_c + S_{xn+2}V_c + \ldots + S_{x2n}V_c$$

Where S_{xh} is the control scheme module control signal, $h \in (1,2,\ldots,2n)$ and is related to the module switch control signals as follows

$$S_h = Q_1 = -Q_2 \tag{4.13}$$

In terms of the overall converter leg, the relation between the arm voltage and the leg voltage can be expressed as

$$v_{xu} = \frac{V_{DC}}{2} - v_x - L\frac{di_{xu}}{dt} - ri_{xu} \tag{4.14}$$
$$v_{xl} = \frac{V_{DC}}{2} + v_x - L\frac{di_{xl}}{dt} - ri_{xl}$$

Where v_x represents the output phase to neutral voltage, L is the inductance of the arm inductor, and r is the resistance of the arm inductor. The arm inductor's impact on the circuit can also be represented by the voltage drop across the inductors, expressed as

$$V_{Lxy} = L\frac{di_{xy}}{dt} + ri_{xy} \tag{4.15}$$

Rearranging in terms of the leg voltage v_x and combining both parts of Equation 4.14 gives the complete leg mathematical model for the proposed MMC

$$L\left(\frac{di_{xu}}{dt}+\frac{di_{xl}}{dt}\right)+r(i_{xu}+i_{xl})=V_{DC}-v_{xu}-v_{xl} \tag{4.16}$$

Substituting for the inductor voltage using Equation 4.15 and rearranging with respect to the phase-to-neutral output voltage of the leg gives

$$v_x=\left(\frac{v_{xl}+v_{Lxl}-v_{xu}-v_{Lxu}}{2}\right) \tag{4.17}$$

Due to the structure of the MMC, circulating currents are inherent to the topology. They are a result of voltage imbalances between all of the module capacitors (voltage source). These currents do not contribute to the load current, and remain internalized within the MMC arms as common-mode currents. They do however contribute to the RMS current through the arm, meaning hardware has to be rated for currents greater than the expected load currents. The circulating current is comprised primarily of negative sequence components at double the fundamental frequency [95, 96]. The phase currents encompass the load and circulating currents. Assuming the system is balanced, the arm current (i_{xy}), circulating current ($i_{cir,x}$), and load current (i_x) are related for each phase leg as follows

$$i_{xu}=i_{cir,x}+\frac{i_x}{2} \tag{4.18}$$

$$i_{xl}=i_{cir,x}-\frac{i_x}{2}$$

The circulating current for the entire phase leg is the average of the upper and lower arm currents.

$$i_{cir,x}=\frac{i_{xu}+i_{xl}}{2}=\overline{i_{cir,x}}+\sum_{h=1}^{\infty}i_{h,x} \tag{4.19}$$

Meaning the circulating current of each phase leg is comprised of an average DC component $\overline{i_{cir,x}}$ and the summation of the harmonic components $i_{h,x}$.

With increasing switching levels, the THD decreases, improving the quality of the load-side voltage waveform. Unlike with more conventional two-level converters, MMCs can operate without output filters, improving efficiencies, reducing costs, and improving packaging.

The per-phase equivalent circuit model for a conventional MMC (Figure 4.10) with an external DC supply has the following upper and lower arm currents

$$i_{xu}=\frac{1}{3}i_{DC}+i_{cir,x}+\frac{1}{2}i_x \tag{4.20}$$

$$i_{xl}=\frac{1}{3}i_{DC}+i_{cir,x}-\frac{1}{2}i_x$$

So the arm current consists of a DC-bus current (i_{DC}), AC circulating currents (i_{xz}), and the AC output current (i_x). A common-mode current component flowing through each leg can be found using the average of the upper and lower arm currents.

$$i_{cm}=\frac{1}{2}(i_{xu}+i_{xl})=\frac{1}{3}i_{DC}+i_{cir,x} \tag{4.21}$$

4.2.4. APPLICATIONS

The MMC when it was first proposed by [89] was envisioned as a new solution for very high voltage applications, such as HVDC conversion or for back-to-back AC-AC converters. This was driven by the desire to work at higher voltages to minimize the cost and maximize efficiencies. Because of this it has found a place as a solution for HVDC applications [92-94, 96-98], grid facing motor drives [92, 96, 98-100], battery storage or renewable energy generation schemes [92, 94, 98, 101-103], and for STATCOM applications [94, 104-108]

4.3. EMBEDDED BATTERY TOPOLOGY

Replacing the module capacitors with embedded batteries eliminates the need for a separate DC source/ battery pack, giving the system arrangement shown in Figure 4.11.

Installing the energy source within the converter does reduce the amount of hardware required, but it also introduces some stringent design constraints. For the standard MMC, the voltage per module is simply the total DC bus voltage divided by the number of modules in a phase leg. Moreover, is extremely flexible, only being bounded by the rating of the capacitors. Whereas, for the embedded battery MMC, the total bus voltage is defined by the voltage per module multiplied by the number of modules in the phase leg. The voltage range available is also fixed to a discrete multiple of the voltage range for the selected battery chemistry. Therefore, when designing an embedded battery MMC for interfacing with a High Voltage motor, either a large number of modules are required or a large number of battery cells in series within the module are required. The high number of modules increases the control and hardware requirements significantly. With each additional switching level for a 3-phase inverter, an additional six modules, ADCs, and I/O pins are required. As discussed in Section 3.0, a large number of batteries in series requires monitoring and balancing to prevent significant voltage imbalances between those batteries. The simulation model used in [9] interfaces directly between the MMC three-phase AC output and an induction motor rated to 230 V_{AC}. This arrangement requires a total of 108 battery cells per arm.

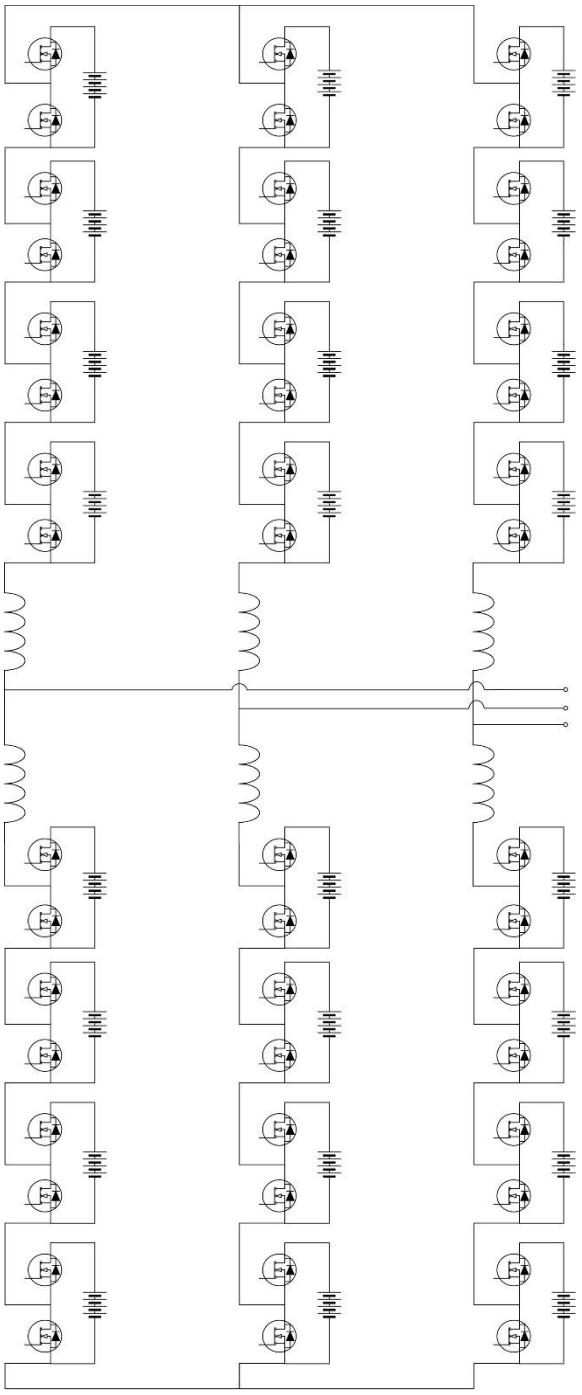


Figure 4.11. Basic three-phase five-level Modular Multilevel Converter with embedded batteries and half-bridge modules

This problem has been encountered by other attempts at developing a prototype of an embedded cell MMC interfacing with a motor. The two prevailing solutions involve either increasing the voltage per module, or increasing the AC bus voltage on the output of the inverter.

The embedded cell MMC proposed by [10] uses a basic bidirectional DC-DC converter to interface a battery with a half-bridge module (Figure 4.12). The methodology was designed on the pretense a battery could not directly replace the module capacitor, because batteries cannot be charged by oscillating currents. Although [8] proves it can with the use of controlled switching. The DC-DC

converter consists of a half bridge feeding the battery through a choke inductor with an inductance L and parasitic resistance R of the windings.

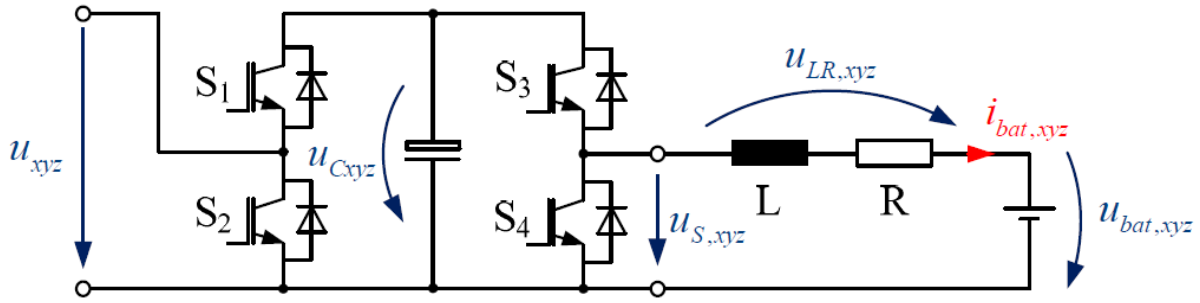


Figure 4.12. MMC module with an integrated battery and important values for control [10]

Based on the polarity of the battery current and the direction of the energy flow, the DC-DC converter operates in two modes:

- Buck converter mode
  Energy stored in the capacitor is transferred to the battery. The sign of the current $i_{bat,xyz}$ is positive, charging the battery. The switch S_3 is closed, while switch S_4 is left open.
- Boost converter mode
  Energy stored in the battery is transferred to the capacitor. The sign of the current $i_{bat,xyz}$ is negative, discharging the battery. The switch S_3 is left open, while switch S_4 is closed.

The operation modes of the proposed DC-DC converter are shown in Figure 4.13.

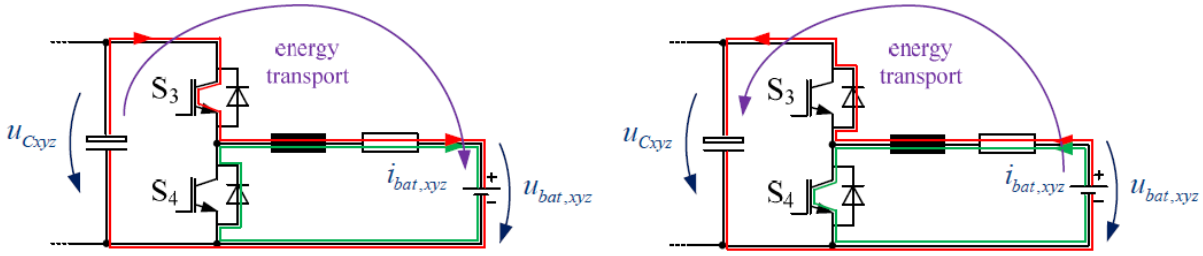


Figure 4.13. (Left) Current flow and energy transport through converter in buck converter mode. (Right) Current flow and energy transport through converter in boost converter mode [10].

Designing a DC-DC converter with buck/boost capability to increase the module voltage without stringing several batteries together in series allows for a relatively low number of arm modules required for interfacing with a high voltage motor.

In comparison, the Embedded Cell MMC proposed in [8] uses a three-phase step-up transformer to interface the AC output of the MMC with the stator of the motor. Similarly, to the usage of a bidirectional DC-DC converter to interface the battery pack with the inverter and motor by existing commercial EVs.

4.3.1. Embedded Cell Modular Multilevel Converter for Electric Vehicle

Applications

Given the lack of an intermediary capacitor on the input of the DC bus, and the lack of a DC bus in general, a precharge and a discharge circuit are no longer required for inverter operation in an EV.

This reduces the hardware complexity of the electrical powertrain and the control complexity for when the motor is powered. Through the usage of the module to control the flow of power in/out of the battery, the MMC can act in the same manner as an active BMS. This can be accomplished without the inclusion of additional power shunting hardware and with a small increase to the control system (discussed further in Section 5.4). Furthermore, this control can also be used for the control of charging the cells. Again, without the addition of large amounts of extra hardware and with some increase in control complexity (not discussed in this thesis). In the event of a hardware fault within a module, the converter can still operate either with unbalanced phases, or with a reduced switching level, improving the reliability of the powertrain.

4.4. CHAPTER SUMMARY

This chapter detailed the fundamental structure and operating principle of the modular multilevel converter. The first section identified and discussed the various non-modular multilevel inverter topologies with attention paid to their relative advantages/disadvantages. The following section details the standard MMC structure. The available module topologies are identified, their operation dissected, and their operation compared. Based on this, the half-bridge topology was selected for the prototype MMC because of the simple hardware and control structure and low power losses. Despite the lack of bi-polar operation and inability to use the control structure to limit fault currents. The available redundant switching states with respect to the output voltage level is discussed and the module switching state with regard to the module operation and energy flow is investigated. With the structure of the proposed MMC decided, the mathematical model representation of the converter from a per-phase perspective is derived. From this, the circulating currents inherent within the MMC topology are derived and the common-mode current flowing between phases determined. The final section related to the standard MMC topology discusses their usage for HV applications.

The following section introduces the embedded battery MMC by discussing the integration of batteries into the module structure in place of the external DC power source and module capacitors. This flows into a discussion on the design limitations imposed by interfacing with batteries on a cellular level and methods used to circumvent these inherent limitations. In particular, the need for either a high number of modules per arm or a large number of cells per module to produce a high voltage output. The chapter concludes with a discussion on the advantages this topology has for EV applications with regard to the ability to integrate the entire electrical powertrain into a singular system, thus reducing the overall complexity of the EV system and minimizing the amount of interfacing between different systems.

CHAPTER 5 MOTOR AND CONVERTER CONTROL

This chapter details the different components of the converter control systems. The primary functionality of the control scheme is to drive a traction motor while balancing the embedded battery cells. The balancing control is achieved by controlling the circulating currents flowing between the arms of the converter. The circulating current controller has the goal of balancing the energy between the upper and lower arms of each phase leg and to balance the energy between each leg. Finally, the Module SOC balance control balances the individual module battery cells within each arm. The motor is controlled using Field Oriented Control, and Space Vector Modulation is used for the PWM control.

A basic block model of the implemented MMC feedback control system is shown in Figure 5.1.

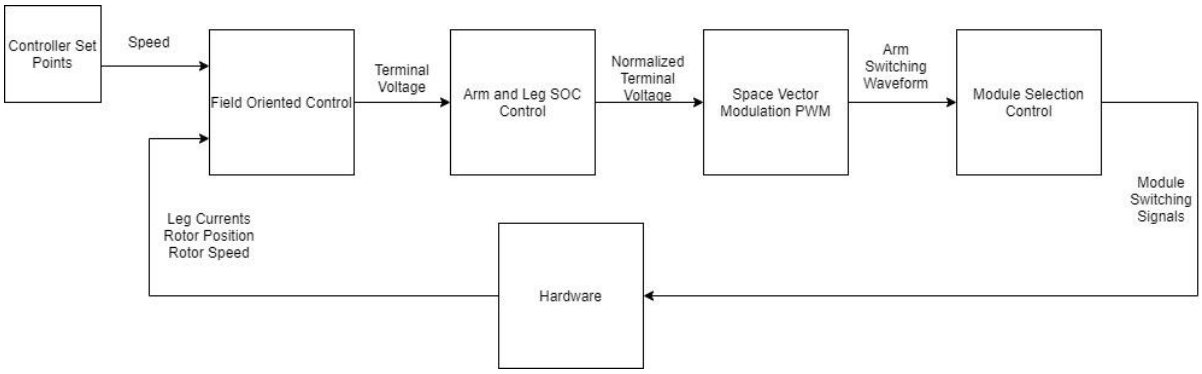


Figure 5.1. Basic MMC feedback control scheme

5.1. MOTOR CONTROL

To drive a synchronous motor at a range of speeds, a variable speed drive (VSD) control scheme is required. The control strategies for motors can be differentiated into two categories based on the variables being controlled. Scalar Control manages only variable magnitudes, whereas vector manages both magnitude and phase angle. These two categories are represented by a variety of methodologies, as shown in Figure 5.2.

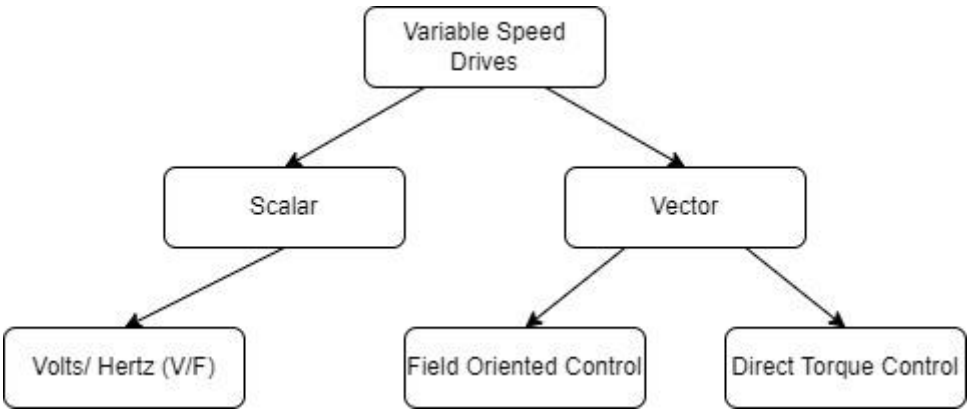


Figure 5.2. Motor control schemes available for PMSMs

5.1.1. Scalar Control

Scalar control is the simplest means of controlling a PMSM, due mainly to the schemes fundamental frequency being to maintain a constant relationship between the voltage and frequency across the motor speed range. The frequency is obtained from the desired synchronous speed and the magnitude of the terminal voltage is varied to maintain a constant ratio (V/f). The lack of feedback elements allows the system to operate as an open-loop control strategy, minimizing its complexity in implementation and operation. However, this lack of feedback can cause instability when operating outside the intended speed range. This can be compensated for by having damper windings in the rotor of the motor to maintain synchronization [109]. Although, this does limit the design choices for the rotor, and so, most PMSM are designed with these omitted. The lack of feedback also reduces the dynamic performance, which limits the number of applications it can be applied to. To improve this some schemes use variations in the inverters DC link voltage to determine the correct modulation [110, 111].

5.1.2. Vector Control

Controlling both the magnitude and phase of the motor flux allows for higher dynamic performance compared with Scalar control. Two distinct types of control strategy exist of executing vector control, field oriented control, and direct torque control. For this implementation, field oriented control was selected because the linked PhD students scheme used FOC. Also, in comparison with direct torque control, measurement of the phase voltages is not required, reducing the hardware requirements for the prototype.

5.1.3. Field Oriented Control

FOC is the vector control strategy that uses coordinate system transformation of the motor equations in the dq-reference frame which rotates synchronously with the motor flux [112]. Because of the fast dynamic response, basic control structure, and energy efficient operation, FOC is considered the best vector control scheme for PMSMs [113, 114].

The goal of FOC is to control the d-axis and q-axis current components to deliver a desired torque (Equation 5.1). Controlling i_d and i_q independently allows for a maximum torque per ampere ratio (MPTA) to be found for minimizing the current needed for a specific load torque, maximizing the motor efficiency [115].

$$T_e = \frac{3}{2}\rho\left[\lambda i_q + \left(L_d - L_q\right) i_d i_q\right] \tag{5.1}$$

The basic layout of a basic FOC scheme is shown in Figure 5.3. which includes conversion from the abc-reference frame to the dq-reference frame, generation of a target q-axis current component from the torque output of a speed controller, d-axis current controller to minimize motor flux, and dq-reference frame to abc-reference frame to create the output reference terminal voltage.

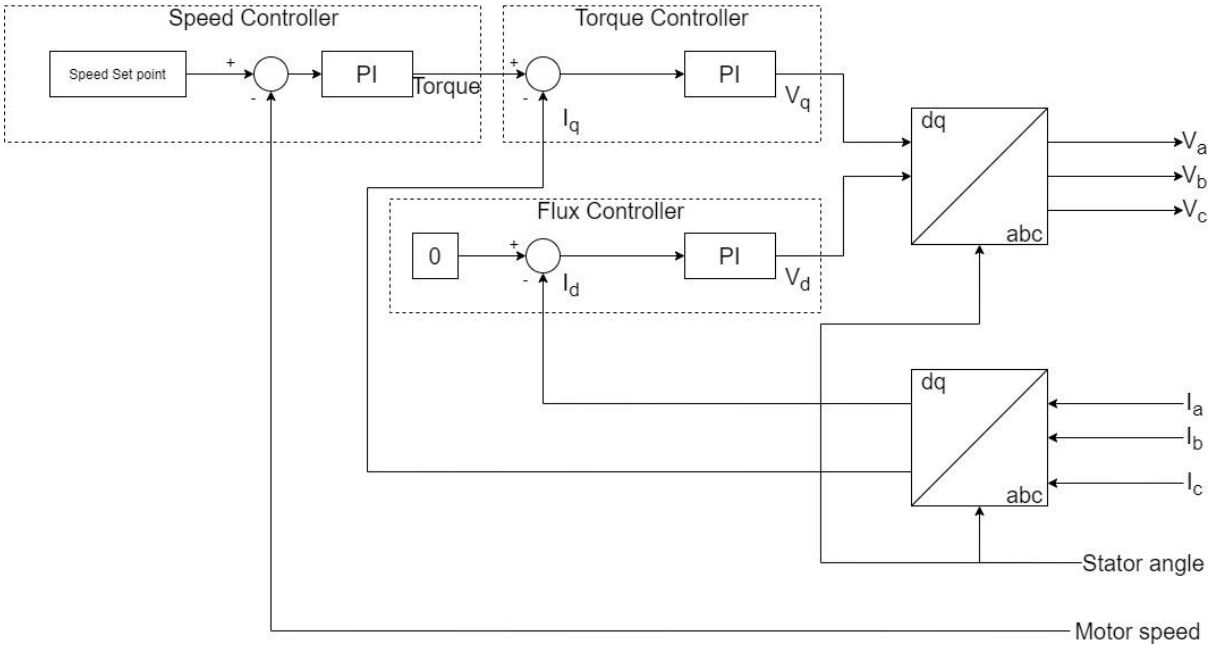


Figure 5.3. Basic field oriented control scheme

One of the critical feedback elements for the control scheme to work is the electrical position, which is required for the transformation between reference frames. The most common means of achieving this is the use of a mechanical sensor to detect the positon of the rotor shaft, known as Indirect FOC. Conversely, the position can be estimated through a sensorless approach using flux- or back-EMF vector detection, known as Direct FOC.

5.1.3.1. GENERATION OF FEEDBACK CURRENT COMPONENTS

The phase currents are synthesized from the measured upper and lower arm current sensors via the following expression

$$I_x = I_{xu} - I_{xl} \tag{5.2}$$

These phase currents are synthesized in the abc-reference frame but need to be transformed into the rotating reference frame. To do this, the time-varying abc-signal is converted to a rotating components on a two-axis space (Figure 5.4). This mathematical conversion, developed by Edith Clarke in 1937, is as follows

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{5.3}$$

Where i_α is the α-axis component, and i_β is the β-axis component. The transformation changes the rotating three-phase system into a rotating two-phase system with orthogonal components in a stationary reference frame.

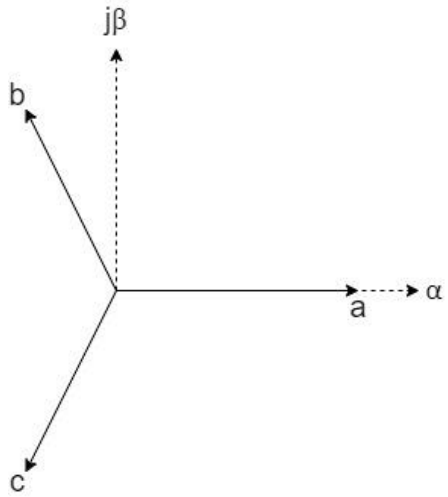


Figure 5.4. abc-reference frame to ab-reference frame conversion

The Park transform, similar to the Clarke transform, changes the rotating two-phase system with a stationary reference frame to a two-phase system in a rotating reference frame. The new two-phase system components are denoted d and q, and are referred to as the direct- and quadrature-axis components. The αβ parameters are transformed into dq-parameters by Equation 5.4, and is shown physically in Figure 5.5.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5.4}$$

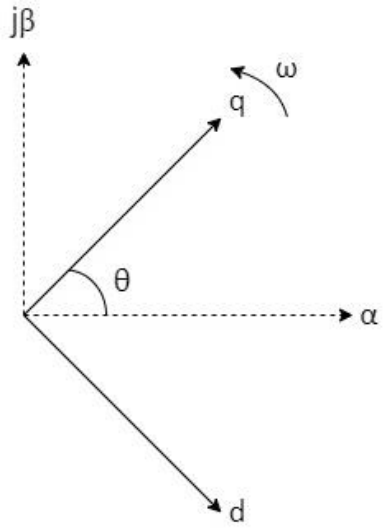


Figure 5.5. ab-reference frame to dq-reference frame conversion

5.1.3.2. CURRENT CONTROL SCHEME

The q-axis current component is used as the feedback error value for the torque controller section of Figure 5.3. Where the target torque value is generated by the speed controller section. The speed controller outputs a target torque required to reach the requested motor speed, at steady state this torque is equal to the torque load applied to the rotor of the motor. However, the speed controller is feeding into a current controller for the target q-axis current component. By rearranging Equation 2.6 with respect to I and using Equation 2.10 to substitute for the motor torque constant gives

$$I_q = \frac{2T_e}{3\rho\lambda} \tag{5.5}$$

For the direct current component, the target current is zero due to the d-axis component representing the current acting outward and orthogonal to the q-axis current, which represents the torque current component. Thus, for the desired motion of the motor, the d-axis component needs to be minimized.

5.1.3.3. TRANSFORM CONTROLLER OUTPUT INTO MOTOR STATOR VOLTAGE

The direct and quadrature current controllers output a terminal voltage for the MMC to output. These voltages are transformed into stator terminal voltages through the use of Equation 2.9, as shown in Figure 5.6.

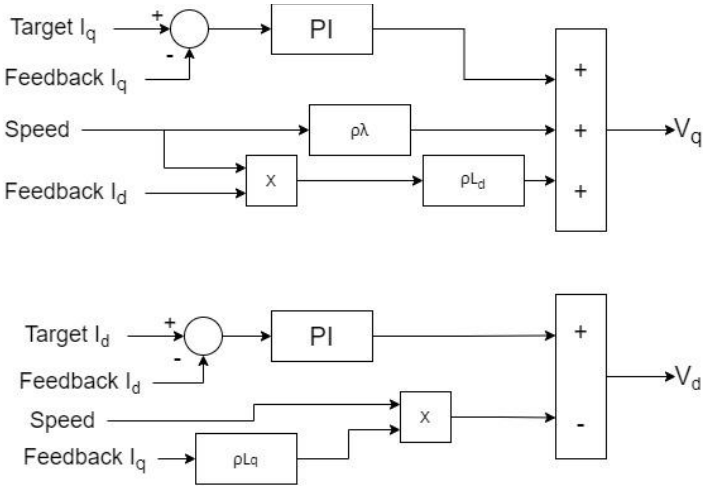


Figure 5.6. dq-reference frame voltage generation for PMSM within FOC

5.1.3.4. MOTOR STATOR VOLTAGE INTO THE STATOR COORDINATE FRAME

The target motor stator current produced by the control scheme are still in the rotating reference frame. The terminal voltage control signal can only be applied in stator coordinates (abc-reference frame); the inverse-Park (Equation 5.6) and inverse-Clarke (Equation 5.7) need to be applied.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{5.6}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} \\ -\frac{1}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5.7}$$

5.2. MOTOR MODELING

For the FOC scheme, the motor torque constant (K_t) is required to convert the torque request from the speed controller into a target quadrature current for the quadrature-current/ torque controller. The flux-linkage and the dq-inductive components of the stator are also required for the synthesis of the requested stator terminal voltage output of the control scheme.

CHAPTER 5 MOTOR AND CONVERTER CONTROL

To test and tune the performance of the designed control system, a model representation of the motor was also required. The manufacturer datasheet lacked some of the parameters required to model the motor. Correspondence with the manufacturer was unable to fill the information gaps required to accurately simulate the motor. Therefore, some empirical testing of the motor was required for determining some parameters.

The most used test for determining the dq-axis inductance components is the slip test. For this test, the field winding is left open-circuit (no DC excitation) and the rotor is derived using a prime mover. However, the slip test is non-applicable for PMSMs due to the inability to remove the excitation (the permanent magnets) [116].

The datasheet lacked any information on the inductance of the stator phase windings, in particular the L_q and L_d inductance components. Only revealing that the stator was wound in a delta configuration. While researching methods to determine these components, two measurement methods were found: direct measurement with an impedance analyzer, and applying a test voltage to measure a reactive time-constant.

5.2.1. DC Step Voltage Application Test

Locking the rotor shaft and applying a DC excitation to the stator aligned with either the d- or q-axis allows the stator to be reduced to a basic RL circuit (Figure 5.7). Where the crossed-out voltage sources are effective short-circuits when a DC excitation is applied.

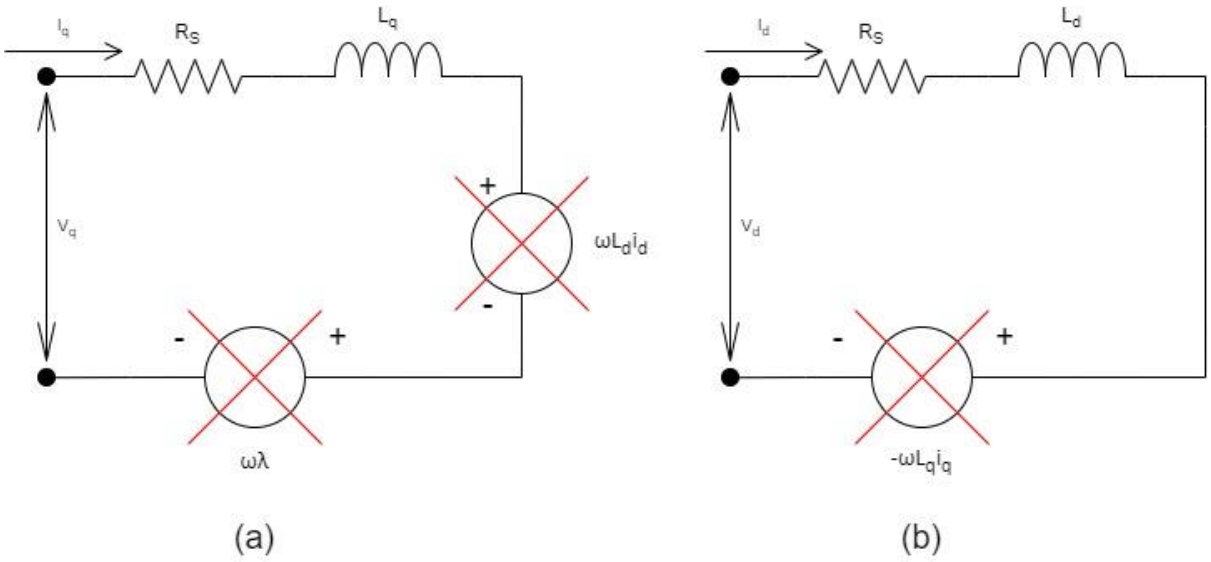


Figure 5.7. Equivalent circuit of PMSM stator with locked rotor and DC excitation: (a) q-axis; (b) d-axis

Because of this, the current through the winding is the same as that of a basic RL circuit

$$i_s(t) = \frac{V}{R_S}\left(1 - e^{\frac{-t}{\tau}}\right) \tag{5.8}$$

Where:

- i_s (t) is the current flow at moment t
- V is the voltage applied to the stator winding
- R_S is the resistance of the stator windings

- τ is the RL circuit characteristic time constant

$$\tau = \frac{L}{R} \tag{5.9}$$

Where

- L is the inductance of the stator for an arbitrary rotor position

Salient pole PMSM have differing q-axis and d-axis inductive components, whereas wound rotor PMSM have equal q-axis and d-axis components. For interior PMSM, the winding inductive components differ because of a lower reluctance in the q-axis ($L_d < L_q$). But the inductances for a surface mounted PMSM are closer in magnitude, due to positioning of the permanent magnets (Figure 5.8)

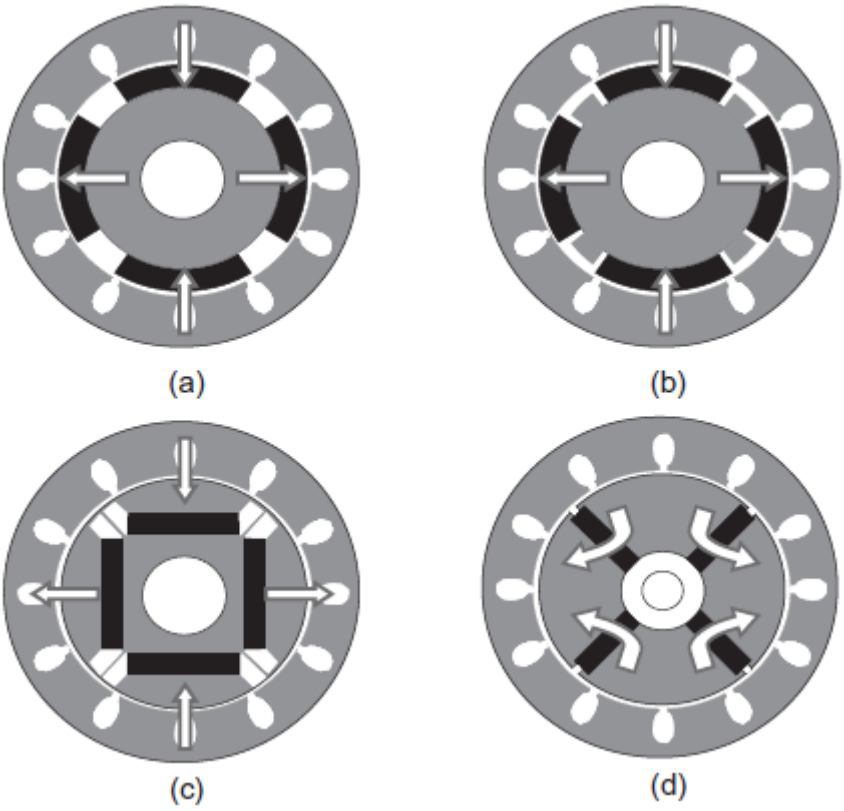


Figure 5.8. Various PMSM rotor magnet mounting structures. (a) surface mounted, (b) surface inset magnet, (c) interior magnet, (d) interior magnet (flux concentration) [16].

In real-world applications, magnetic circuits are affected by saturation as the current increases. This is particularly the case when the q-axis current component is increased, causing the q-axis inductance component to decrease. Since in most operating conditions the d-axis component is controlled at close to zero, saturation of the d-axis inductance occurs rarely [117].

Determination of the q-axis and d-axis inductive components, requires a balanced three-phase current condition. Aligning the rotor with the d-axis results in the inductive component of the stator winding being proportional to the d-axis inductance, using the following winding configuration (Figure 5.9).

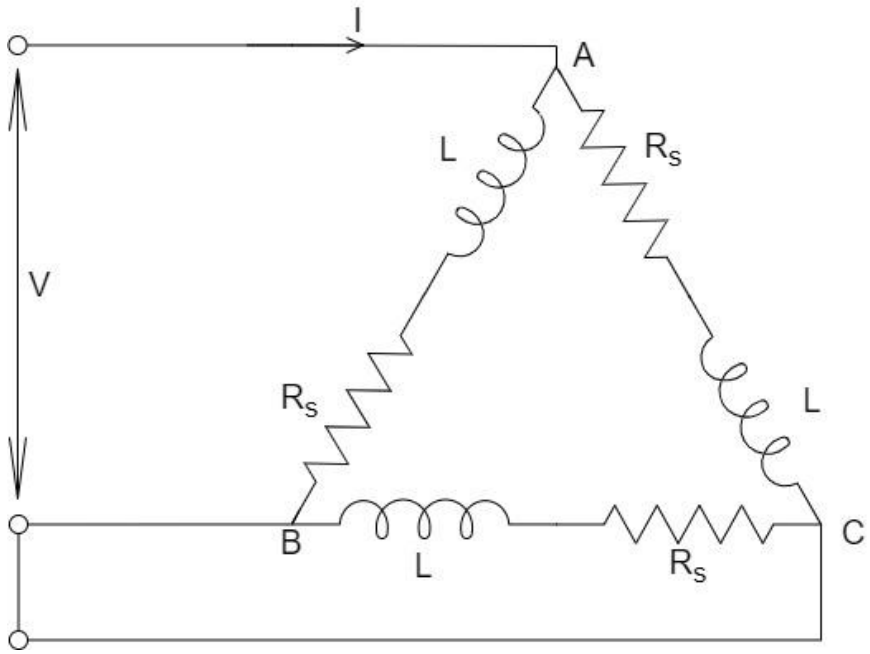


Figure 5.9. Motor stator inductance measurement circuit

For the rotor electrical angle, θ_{el}, the d-axis and q-axis inductive components can be determined for a delta-wound stator as follows

$$L_d = 2L\left(\theta_{el} = 0^{\circ}\right) \tag{5.10}$$

$$L_q = 2L\left(\theta_{el} = 90^{\circ}\right)$$

Where L refers to the inductance of the RL stator winding equivalent circuit, this difference is as a result of the equivalent circuit representation of the circuit outlined above being two phase windings in parallel.

When the rotor is aligned with phase A ($\theta_{el} = 0^{\circ}$) the current response is equal to that of a simple RL circuit (Equation 5.8).

After τ has been determined, the d-axis inductance can be calculated as follows

$$L_d = 2\tau R_S \tag{5.11}$$

A similar approach can be taken for measuring the q-axis component, this time by aligning the rotor with the q-axis of the stator. For aligning the d-axis, phase A is connected to DC positive, and phase B and phase C are connected to DC negative. A 90° electrical shifted position can be obtained when phase B terminal is connected to DC positive, phase C is connected to DC negative, and phase A is left floating [117].

5.2.1.1. STATOR EXCITATION TESTS

To align the rotor with the d-axis, a test voltage was applied to the stator using the circuit shown in Figure 5.9. The rotor was then fixed to prevent the alignment being interfered with. A negative test voltage (phase A connected to DC negative, phase B and phase C connected to DC positive) with the current limited to a fraction of the full load current (Figure 5.10).

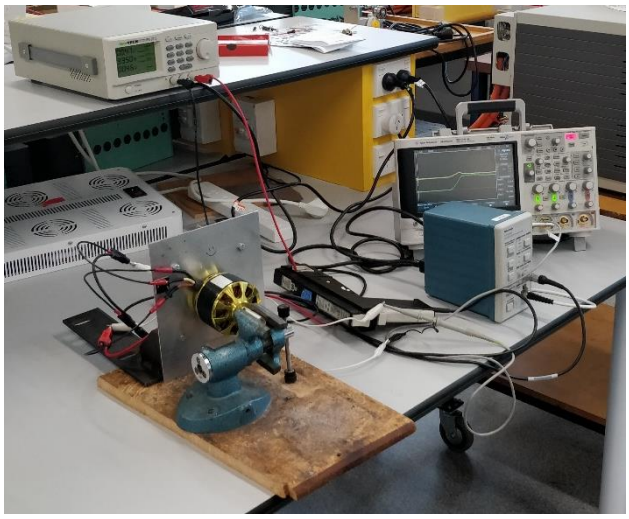


Figure 5.10. Inductance measurement test setup

The current response was measured with a current probe and graphed with the test voltage on an oscilloscope. The time constant was found by measuring the time difference between the rising edge of the voltage input and when the current reached 63.2 % of the steady-state current flow.

The waveforms obtained using this method are shown in Figure 5.11.

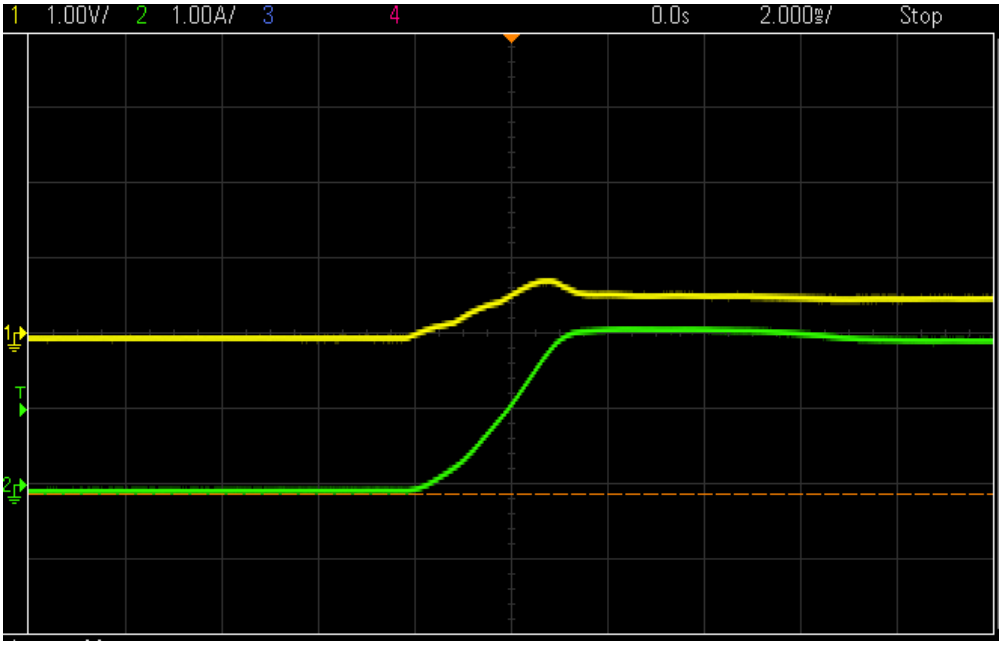


Figure 5.11. Stator DC excitation test to find d-axis inductance. (yellow trace) applied DC voltage, (green voltage) current response of stator.

For the d-axis component, the following calculations were made

$$\tau = 2.05 \times 10^{-3}\ s$$

$$L_d = 2\tau R_s = 2 \times 2.05 \times 10^{-3} \times 0.032 = 131\ \mu H$$

Similarly, for determining the q-axis component, the rotor was aligned with the q-axis by connecting the DC positive terminal to the phase B connection, the DC negative terminal to the phase C connection, and phase A left floating. The rotor was locked to prevent drift and movement due to

the q-axis component being the torque generating component. With phase A connected to the DC positive terminal, and phases B and C tied to the negative DC terminal, a test voltage is applied to give the required waveforms for calculating the time constant (Figure 5.12). The same equations used to find L_d are also applicable for finding L_q.

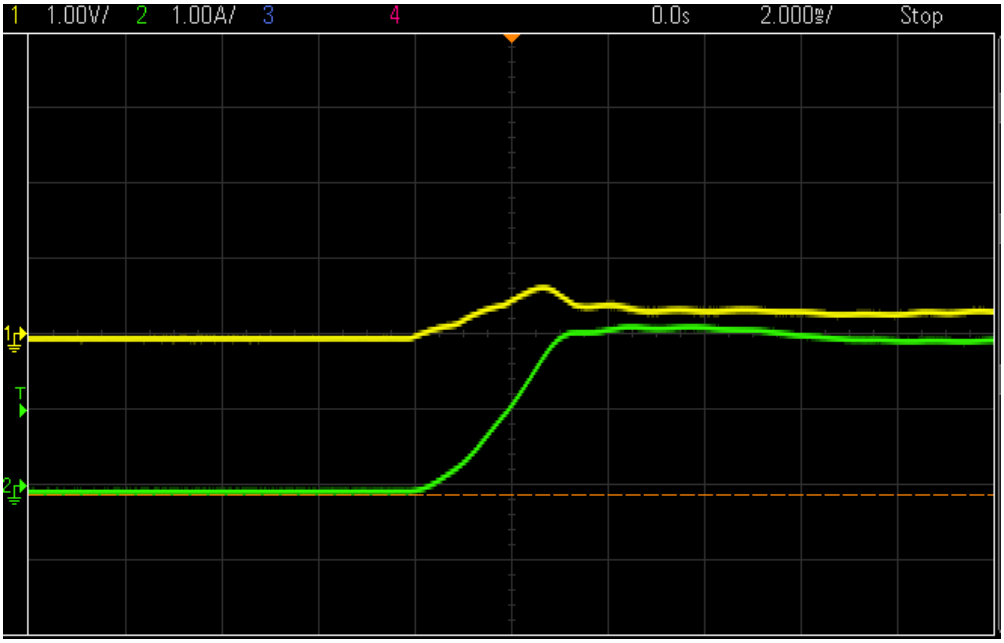


Figure 5.12. Stator DC excitation test to find q-axis inductance.

From this, the following waveforms and calculations were made.

$$\tau = 1.9 \times 10^{-3}\ s$$

$$L_q = 2\tau R_s = 2 \times 1.9 \times 10^{-3} \times 0.032 = 121\ \mu H$$

The circuit response given from this method differ significantly from the example in [117] shown in Figure 5.13.

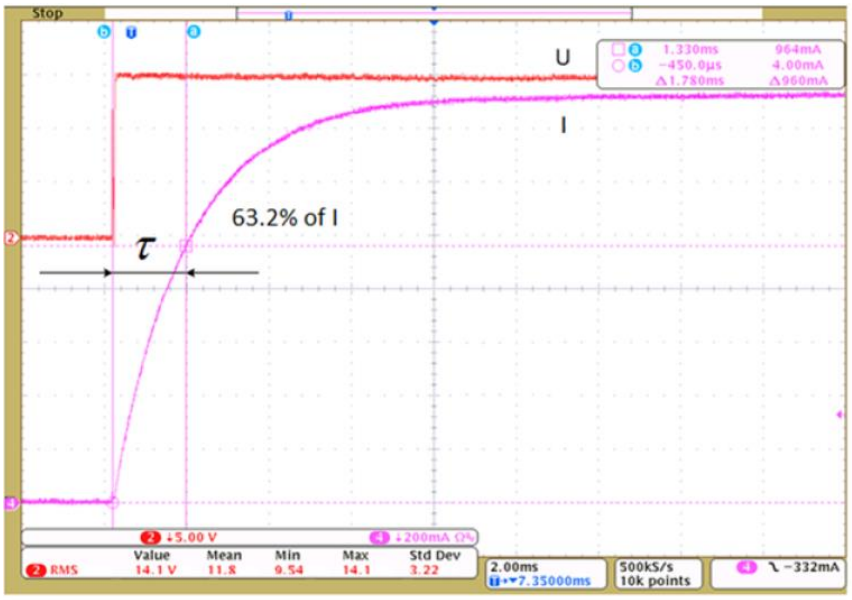
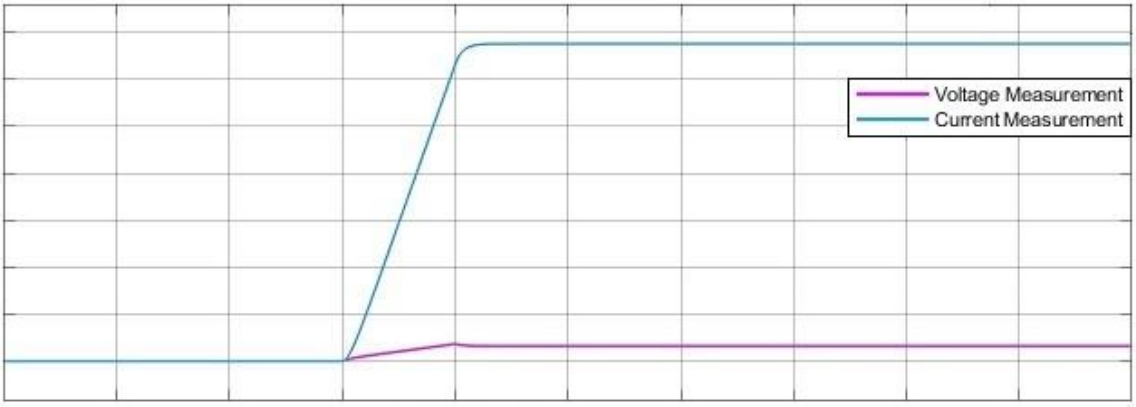
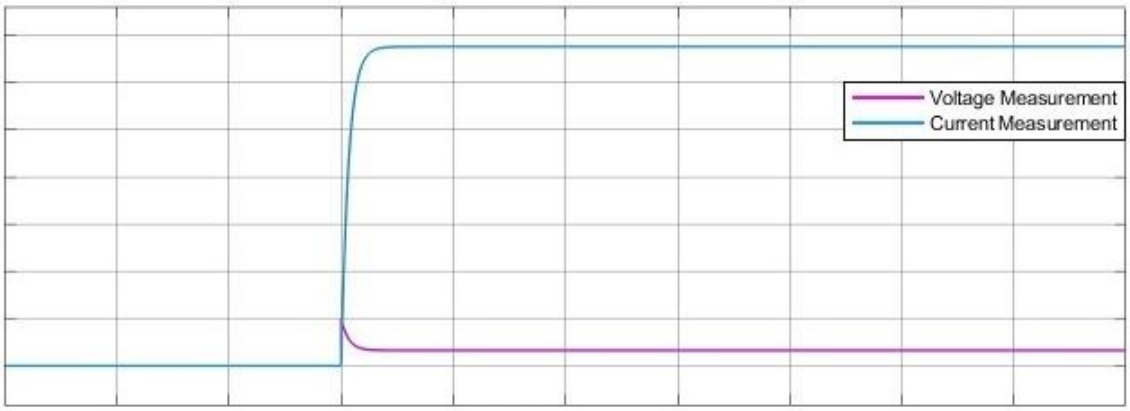


Figure 5.13. Current step response waveform [117]

In comparison with the example response, the power supply used in the measurement is unable to instantaneously apply the peak voltage in the form of a step function. This slow voltage rise affects the current response of the motor stator, as shown through the simulation shown in Figure 5.14.



(a)



(b)

Figure 5.14. Simulation of DC excitation test with: (a) real power supply, (b) ideal power supply

A number of power supplies set with varying voltage and current limits were used in an attempt to correct this error introduced by the slow power supply voltage rise. However, no supply was able to reduce this voltage rise time to such a degree that it became negligible.

5.2.2. Inductance Direct Measurement Test

Directly measuring the inductive reactance of the motor using an impedance analyzer/ LCR meter can be used to determine the inductance in place of measuring the time-response of the circuit. Similarly, to the initial measurement method, the rotor needs to be aligned with one of the dq-axis to measure the component for the respective axis. Since the response of the circuit is based on the frequency applied by the measuring equipment, a frequency sweep is required to determine the inductance. A sweep from 10 Hz up to 1 MHz was applied to the motor stator aligned with the d-axis (Figure 5.15) and aligned with the q-axis (Figure 5.16).

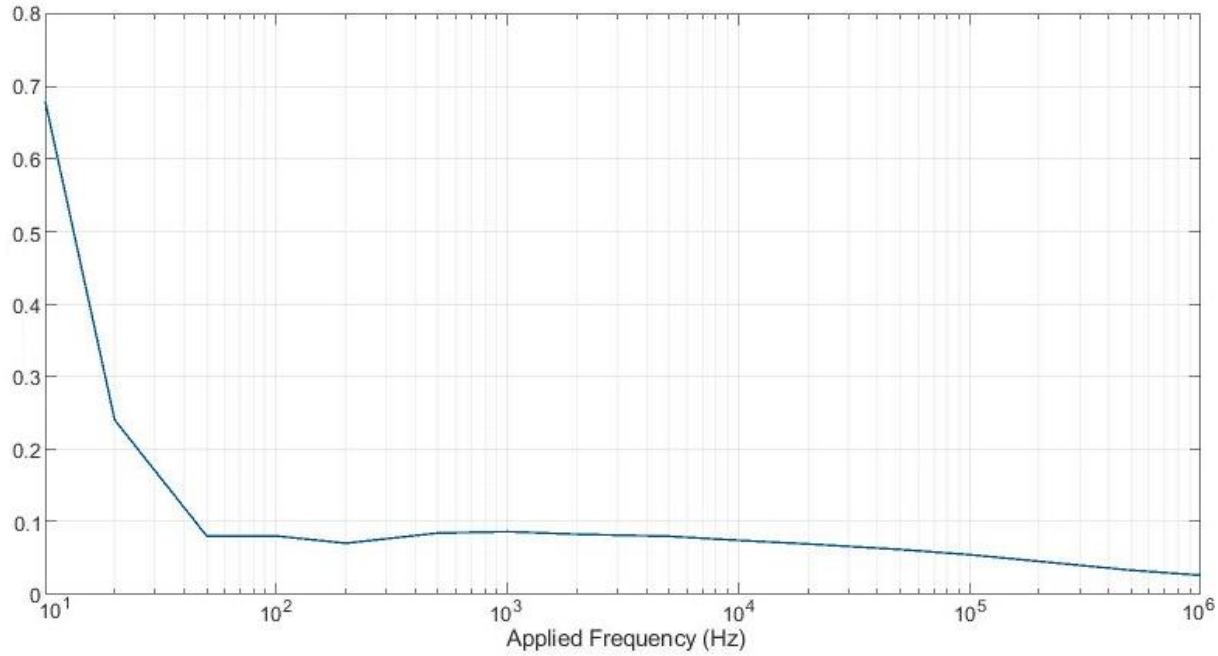


Figure 5.15. Impedance analyzer frequency sweep of d-axis stator inductance

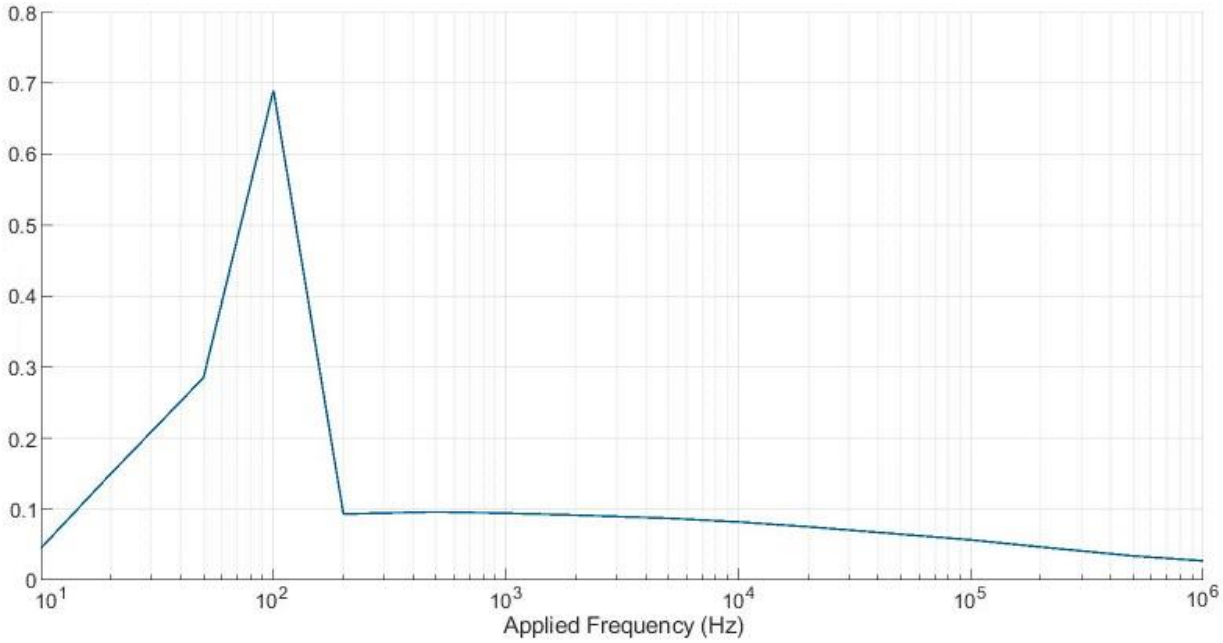


Figure 5.16. Impedance analyzer frequency sweep of q-axis stator inductance

The inductance values given by the DC-excitation test gave values in the range of those measured by the impedance analyzer with a low frequency input (< 100 Hz). At the planned switching carrier frequency for the PWM scheme of 5 kHz, the inductance is approximately two thirds of that calculated from the DC excitation test. Based off this discrepancy, it was decided to use the measured inductance at 5 kHz for the motor modelling and for the FOC.

5.2.3. PARAMETER DETERMINATION

More than just the dq-axis stator inductances were required to model the motor in MATLAB and use in the FOC. The stator resistance was provided by the datasheet, but a micro-ohmmeter placed

across two phases was used to directly measure the resistance of the stator windings. The only motor constant provided by the datasheet was the motor speed constant (K_v) in the form of 150 RPM/V. Since the motor speed constant is related to the motor speed (Equation 2.5) and the torque is inversely proportional to the motor speed for a constant power output, it follows that the torque constant is inversely proportional to motor speed constant, as shown here

$$K_t = \frac{\tau}{I} = \frac{1}{K_{v(SI)}} \tag{5.12}$$

Where $K_{v(SI)}$ referes to the motor speed constant in SI units (radians s^{-1}/ V). The motor constant given in the datasheet was 150 RPM/V, equivalent to 15.71 $rads^{-1}$/ V.

To find the motor linkage flux, λ, Equation 2.10 was used. The back-EMF constant K_e represents the peak voltage for a given no-load speed. In comparison, the motor speed constant represents the no-load speed for a given peak voltage. From this the following relation can be made

$$K_v = \frac{\omega_{no-load}}{V_{pk}}$$

$$K_e = \frac{V_{pk}}{\omega_{no-load}} = \frac{1}{K_v}$$

From this, the linkage flux was calculated as 0.0091 Wb.

Table 5.1. Summary of motor parameters, their quantities, and the source of the value

Motor Parameter	Determined Value	Determination Source
Stator Resistance, R_S	0.032 Ω	Measured with micro-ohmmeter, confirmed from datasheet
q-axis inductance, L_q	87 µH	Measured using impedance analyzer
d-axis inductance, L_d	80 µH	Measured using impedance analyzer
No. of pole pairs, ρ	7	Datasheet, clarified with visual inspection
Flux linkage, λ	0.0091	Calculated from motor back-emf constant
Torque constant, K_t	0.0637	Calculated from motor back-emf constant
Motor speed constant, K_v	150 RPM/ V	Motor datasheet

5.2.4. MODEL IMPLEMENTATION IN MATLAB

As stated in Section 3.4.1, the embedded battery MMC Simulink model was generated using the Simscape specialized power systems block set. As a part of this library a variety of synchronous motor modelling options were available. However, since this library was primarily designed for power system modelling, rather than EV powertrain modeling, all the synchronous motor stators use a wye/star winding configuration. However, the selected motor had a delta-wound rotor. This difference would result in the phase-to-phase voltage applied to the motor having a different effect, and the current through the stator also being different. To verify the operation with a delta-wound PMSM model, an alternative within the other Simulink blockset libraries was needed.

The SimScape electrical library offered a generic PMSM model capable of being configured with a delta-wound stator (Figure 5.17); however, there were several issues with interfacing the SimScape electrical library components with the specialized power systems library components.

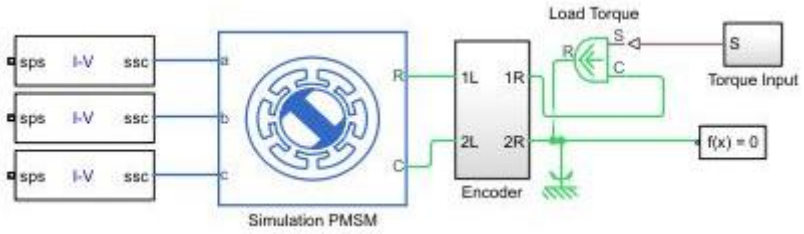


Figure 5.17. SimScape electrical model section of the hardware simulation model

For the SimScape electrical library components to work, the overall model solver method needed to use a variable step time solver, rather than a fixed time step solver. For this to work with the model elements designed for fixed step times, the variable step time limit needed to be set to an extremely low time threshold (magnitude of ns). This resulted in the model execution time increasing excessively to the point a minute of simulation time corresponded to multiple hours in real-time. The SimScape electrical elements also required a sophisticated mechanical model to simulate the load applied to the rotor of the motor. While configuring this, the author was unable to configure the motor to operate with a positive torque and a positive rotational velocity when trying to interface the sensing of these elements with the motor control scheme. The model for developing the control system with simulated hardware still had the startup initialization period used for calculating the battery SOCs, fill the ADC buffers, and calibrate the current sensors. During this initialization process, the output of the control system is disabled. However, during simulation voltages and current flows were observed, despite the lack of energy sources connected. This unexpected power flow was fed back into the control system, causing the control scheme to attempt to respond to and control power flow it was not responsible for, leading to the system becoming unstable. These factors ultimately lead to the Simscape electrical motor solution being abandoned in favour of another solution. A solution was found through the usage of the MATLAB file exchange server in the form of a user-made PMSM model [118] (Figure 5.18).

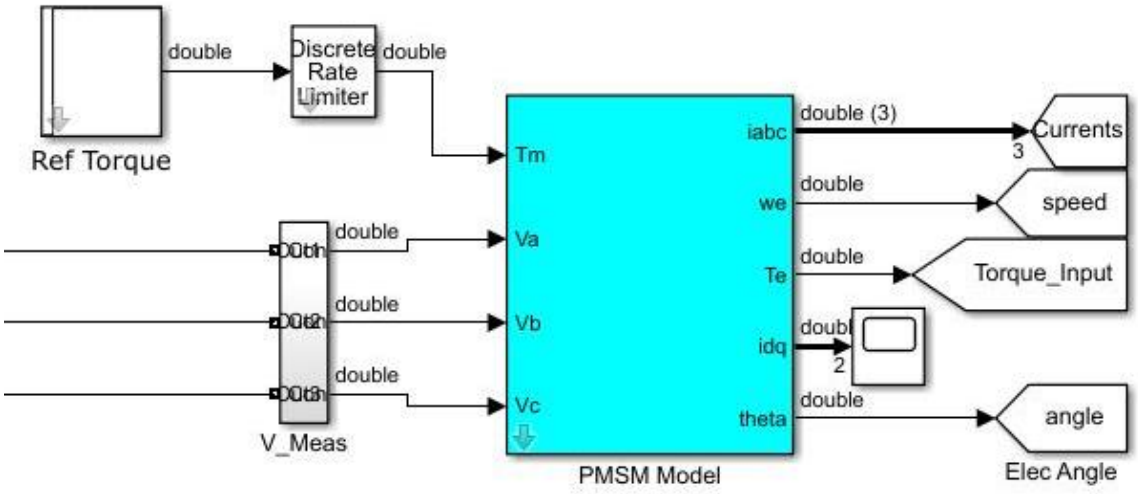


Figure 5.18. Math-based model representation of delta-wound PMSM

This model could only be used for testing the motor control portion of the control scheme, since no actual current was drawn from the embedded batteries in the simulation. This was due to the model

taking a phase-to-phase voltage measurement of the MMC phase legs and using this to mathematically simulate the operation of the motor, generating stator phase currents, the rotor position, rotor speed, and motor torque as outputs. This simulated stator current was able to be fed-back to the FOC scheme. However, since the motor has no real power flow, the cells never discharge, leading to the SOC-balance control failing to function. The FOC scheme setup for the star-wound motor model was tested using the math-based delta-wound motor model and was able to operate the same as the star-wound motor, albeit with different current and voltage magnitudes and differing levels of torque ripple.

5.3. CONVENTIONAL CIRCULATING CURRENT CONTROL

For conventional MMCs, high magnitude circulating currents are deemed detrimental to the operation of the converter. Therefore, the objective of circulating current control was to minimize this current by balancing the module capacitor voltages. Although hardware considerations such as specifying the arm inductors to suppress circulating currents can be made, closed-loop control is required to minimise the circulating currents.

Typically, a synchronous reference frame based control scheme is used for this elimination strategy [90]. With this strategy, the circulating currents in the abc-reference frame are transformed into a dq-reference frame rotating at double the fundamental frequency. This reference frame conversion turns the circulating currents into DC signals. In turn these signals can now be easily controlled using simple PI-controllers [119, 120]. An alternative method, which does not utilize a reference frame conversion, uses resonant regulators designed to eliminate the specific dominant harmonic frequency components. In particular, the second- and fourth-order harmonic components from the circulating currents [121].

These harmonic components are time-varying in nature, inherently difficult to control using a simple PI-controller strategy without steady-state errors. Converting these from the abc-reference frame to the dq-reference frame transforms these into DC components. From Equation 4.15, the three-phase circulating current model in the abc-reference frame can be expressed as

$$\begin{bmatrix} v_{az} \\ v_{bz} \\ v_{cz} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{az} \\ i_{bz} \\ i_{cz} \end{bmatrix} + r\begin{bmatrix} i_{az} \\ i_{bz} \\ i_{cz} \end{bmatrix} \tag{5.13}$$

The scheme proposed in [90] utilizes a synchronous dq-frame controller designed to eliminate the second-order harmonic component from the circulating current. Based off of this, the circulating current model in the dq-frame, rotating at -2ω is given by

$$\begin{bmatrix} v_{dz} \\ v_{qz} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{dz} \\ i_{qz} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega L \\ 2\omega L & 0 \end{bmatrix}\begin{bmatrix} i_{dz} \\ i_{qz} \end{bmatrix} + r\begin{bmatrix} i_{dz} \\ i_{qz} \end{bmatrix} \tag{5.14}$$

Based off this mathematical model, the circulating current control structure shown in Figure 5.19 is derived. The feedback circulating currents are obtained from the measured arm currents using Equation 4.19. This current is then transformed from the abc-reference frame to the dq-reference frame to generate the i_{dz} and i_{qz} current components. For the goal of circulating current elimination, the target control values i_{dz}^* and i_{qz}^* are set to zero. The difference between the measured current and the target values gives the current errors Δi_{dz} and Δi_{qz}. These current errors are then minimized using PI-controllers. The d-axis and q-axis current control components are decoupled by adding the induced speed voltages from the inductor to the current control loops. The PI-controllers generate the reference voltage commands v_{dz}^* and v_{qz}^*. These two dq-reference frame

components are then transformed back to abc-reference frame components. The resultant reference voltages ($v^*_{z,abc}$) are then combined with the module capacitor voltage control and the terminal voltage control to improve the efficiency and reliability of the MMC.

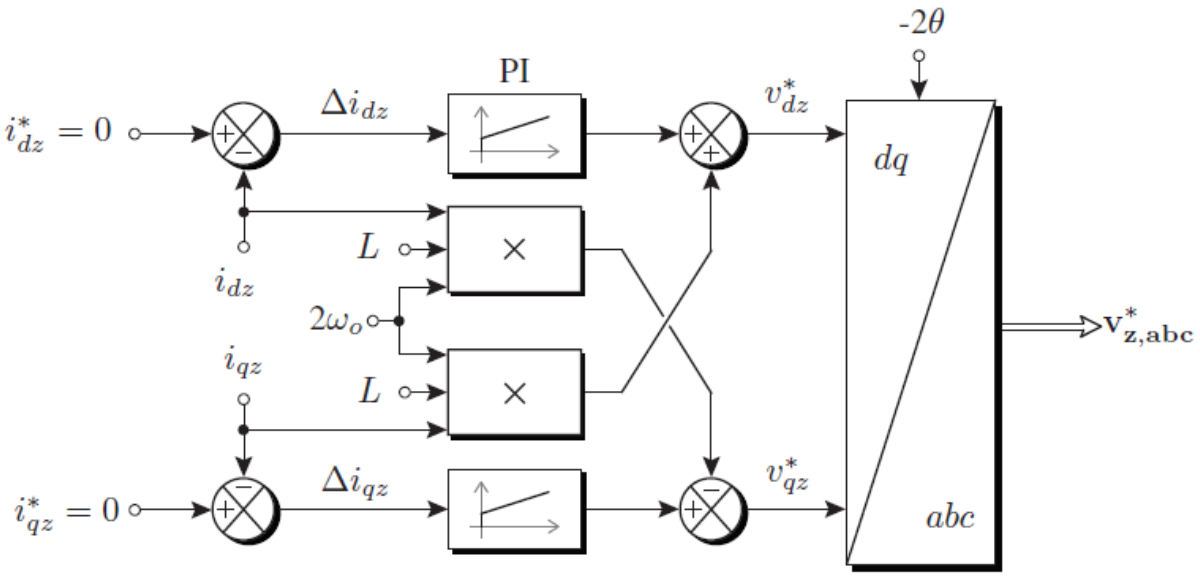


Figure 5.19. dq-reference frame circulating control through the elimination of the second harmonic current component [90].

5.4. EMBEDDED BATTERY MMC CIRCULATING CURRENT CONTROL

Much like with conventional circulating current control, the objective of the control scheme is to balance the arm-energy between the upper and lower arms, and to balance the overall leg energy. Figure 5.20 shows the block diagram of the SOC balancing using circulating current control proposed by [8]. The primary goal of this scheme is to balance the battery SOCs during converter operation

without affecting the output current of the converter.

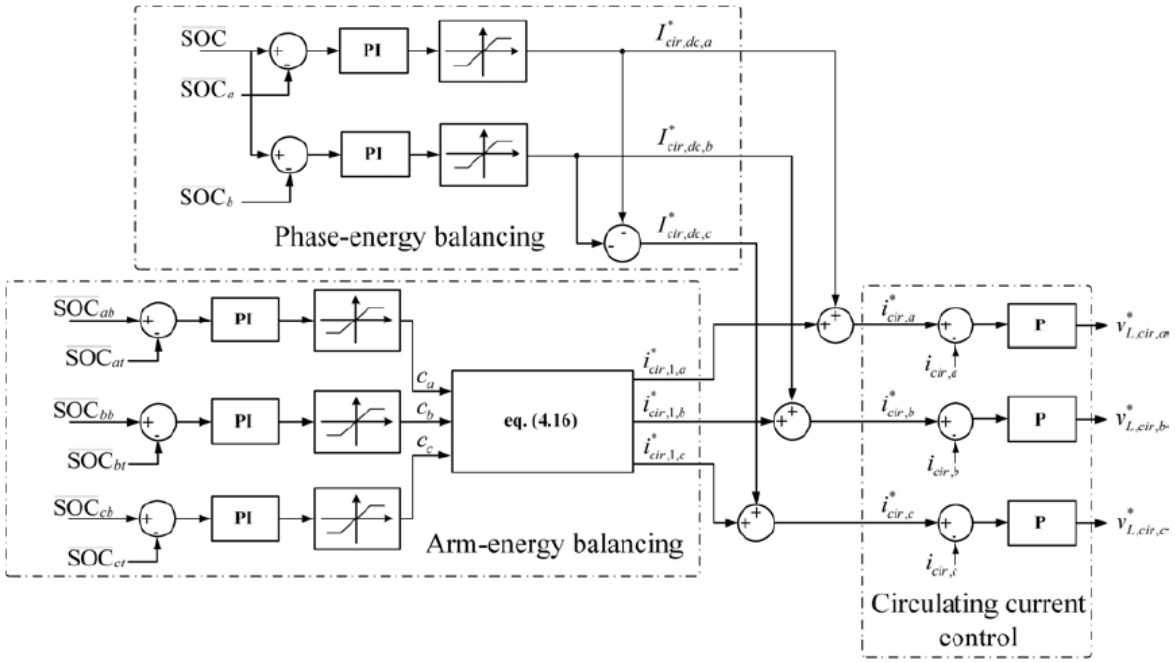


Figure 5.20. Embedded battery SOC balancing scheme using circulating control [8]

5.5. ARM SOC BALANCING CONTROL

The module balancing control will passively balance the modules in a given arm to the same SOC, but a difference in average SOC between the upper and lower arms can still persist. This will result in imbalanced current flow from each of the arms, and contribute to the circulating current throughout the converter.

However, when trying to implement the form of arm balancing control proposed by [8], the scheme had a detrimental effect on the terminal voltage control. The PhD student created their own module battery SOC balancing scheme based off the method described above, a modified version of this was implemented in the control scheme for this research. This version is shown in Figure 5.21.

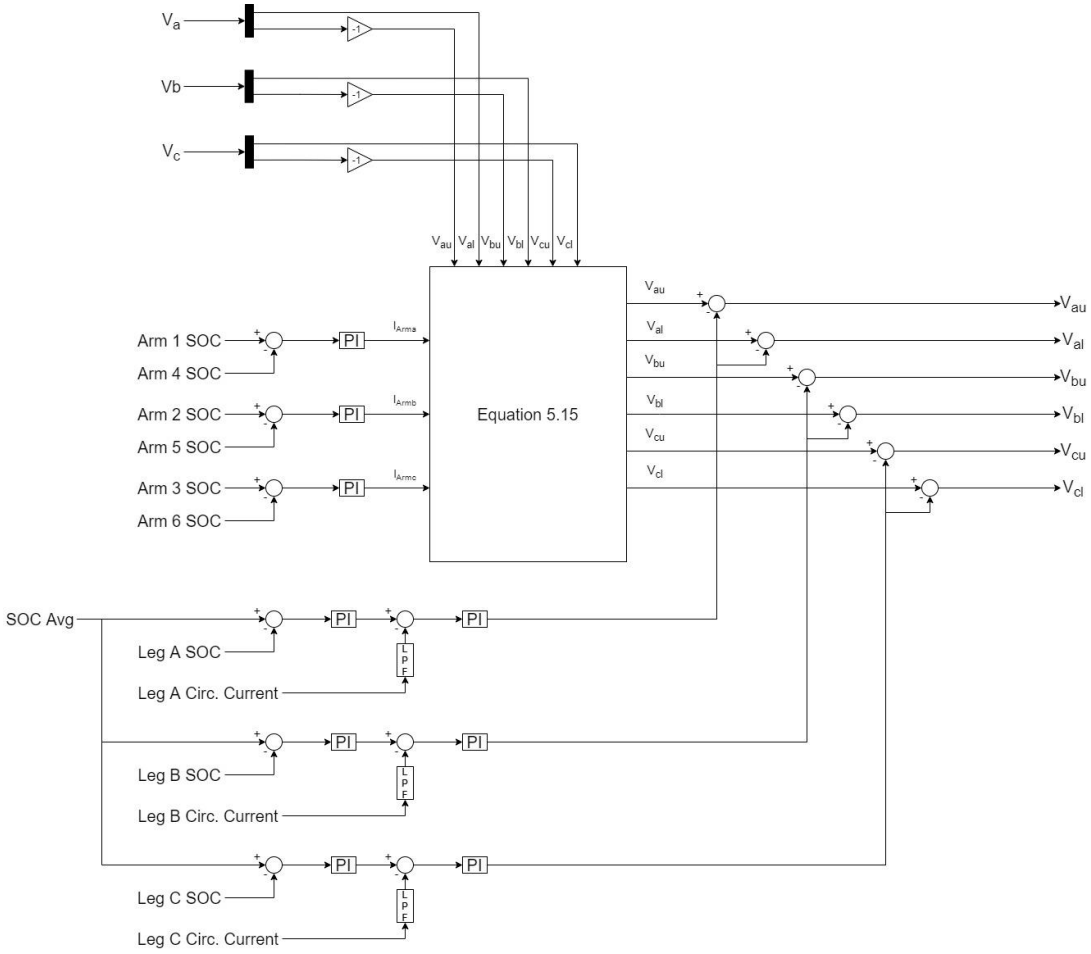


Figure 5.21. Implemented module battery SOC balancing scheme

Instead of generating a target circulating current, which combined with the target circulating current produced by the phase leg balancing control is fed into a separate circulating current control (the output of which is added to the terminal voltage signal), a separate voltage control signal is generated by using the target circulating current as a scaling factor for the terminal voltage control output signal of the FOC.

This scaling factor is configured such that the arm with the higher SOC will have the arm reference signal fed into the SVM generator scaled up by the same factor that the complementary arm is lowered. While the individual arm voltages are changed, the subsequent phase-leg voltage feeding the load remains unaffected. Mathematically this is represented as

$$\overrightarrow{V_{xu}} = \overrightarrow{V_{xu}} + \overrightarrow{I_{Arm}} = \begin{bmatrix} V_{au} \\ V_{bu} \\ V_{cu} \end{bmatrix} + \begin{bmatrix} I_{Arma} \\ I_{Armb} \\ I_{Armc} \end{bmatrix} \tag{5.15}$$

$$\overrightarrow{V_{xl}} = \overrightarrow{V_{xl}} - \overrightarrow{I_{Arm}} = \begin{bmatrix} V_{al} \\ V_{bl} \\ V_{cl} \end{bmatrix} - \begin{bmatrix} I_{Arma} \\ I_{Armb} \\ I_{Armc} \end{bmatrix}$$

Where:

- V_{xy} is the respective terminal voltage signal for the arm location y (upper or lower)
- I_{Arm} is the target circulating current used to scale the reference signals

5.6. LEG SOC BALANCING CONTROL

To balance the overall phase leg SOC (the average of the two corresponding arm SOCs) the DC component of the circulating current is used. A PI controller using the difference between the current overall pack average SOC and the phase leg average SOC generates a target DC circulating current needed to balance the leg with the pack. The circulating current is passed through a low pass filter (LPF) block to remove the oscillating harmonic current component and leave the DC offset. The difference between the circulating current DC component and the target circulating current are passed through a PI controller to generate a DC offset value for the terminal voltage control signal, where this value is applied equally to both the arm control signals.

5.7. PWM SCHEMES

For controlling the AC voltage output of power converters, Pulse Width Modulation (PWM) is the most widely used method of choice. A target AC output voltage based off a reference input is achieved by varying the duty cycle (width of input pulse) of the control signal to switching devices. Various PWM schemes have been devised to achieve specific control objectives such as: reducing harmonic distortion of output voltage, maximize output voltage at a given switching frequency, voltage balancing, common-mode voltage reduction, minimizing switching frequency of devices, reducing power losses, and minimizing ripple of output current [90].

These schemes can be characterized by the switching frequency into high switching frequency, low switching frequency, and fundamental switching frequency. A selection of PWM schemes employed for MMC's are shown in Figure 5.22 [90].

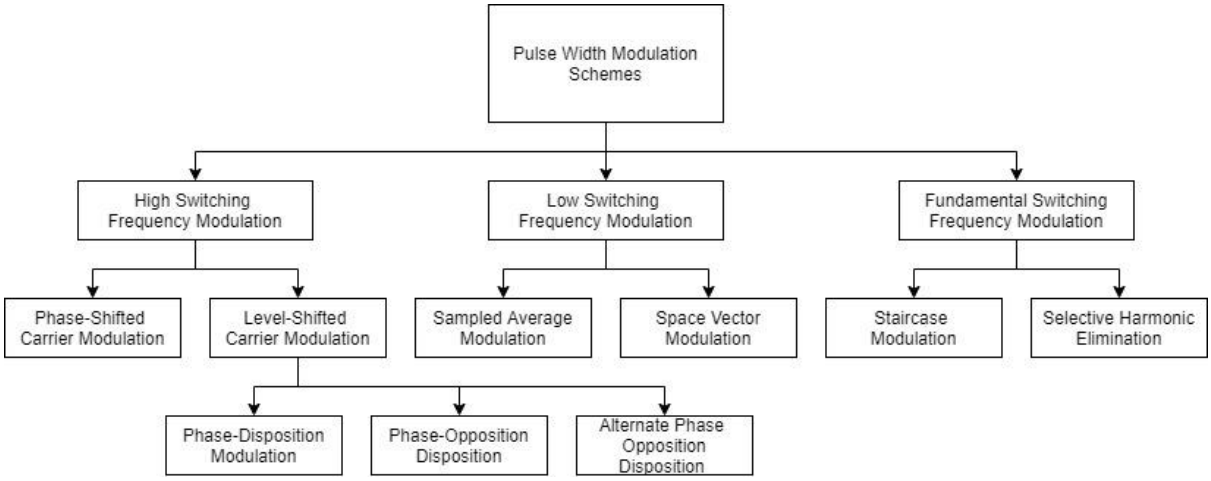


Figure 5.22. Multilevel PWM schemes implementable in MMCs

5.8. SPACE VECTOR MODULATION

Space Vector Modulation (SVM) utilizes a low switching frequency modulation for usage in high-power multilevel converters [90]. The SVM methodology offers flexibility of selecting the best switching vector amongst the redundant switching vectors to maximize the DC-bus utilization. In comparison with other schemes, the determination of the redundant vectors and the switching vectors is significantly more computationally intensive [90]. This is largely due to the large number of switching vectors being generated. As well as conversions between the abc- and $\alpha\beta$-reference frame, trigonometric functions, and usage of lookup tables.

5.8.1. SCHEME DEVELOPMENT

For the purposes of this project, a SVM based PWM scheme was selected for implementation on the hardware. This was due to the superior DC-bus utilization, and the redundant switching vectors. The algorithm outlined in [90] was selected as a basis for the scheme implemented in Simulink due to its unique usage of the a-b-c reference frame to generate the switching vectors. In comparison, many other methods exclusively use the α-β reference frame, which necessitates the need for lookup tables, and thus have high computational requirements. The ability for the scheme to be extended to higher switching levels with no modification allowed for greater flexibility of design for the system. The scheme also offers a dual SVM approach, which allows the upper and lower arms to be controlled independently. This allows the scheme to function with the battery balancing control.

5.9. SYNTHESIS OF REFERENCE ARM VOLTAGE VECTORS

The normalized reference output of the terminal voltage control (V_{term}) is defined as

$$\vec{V}_{term} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} V_{norm,a} \sin(\omega t) \\ V_{norm,b} \sin\left(\omega t - \frac{2\pi}{3}\right) \\ V_{norm,c} \sin\left(\omega t - \frac{4\pi}{3}\right) \end{bmatrix} \tag{5.16}$$

Where V_a, V_b, and V_c represent the three-phase reference modulation signals, m is the number of switching levels, and ω is the fundamental reference angular frequency. The term V_{norm} refers to the normalized terminal voltage output of the SOC balancing control, and can be found using

$$\vec{V}_{norm} = \begin{bmatrix} V_{norm,a} \\ V_{norm,b} \\ V_{norm,c} \end{bmatrix} = \begin{bmatrix} \frac{V_a}{\left(\frac{V_{DC}}{2}\right)} \\ \frac{V_b}{\left(\frac{V_{DC}}{2}\right)} \\ \frac{V_c}{\left(\frac{V_{DC}}{2}\right)} \end{bmatrix} \tag{5.17}$$

The dual reference signals are obtained through a 180° phase shift and then passed through the battery balancing control. The upper and lower arm voltages, synthesized from $\vec{V}_{term}$ are

$$\vec{V}_{xu} = \begin{bmatrix} V_{au} \\ V_{bu} \\ V_{cu} \end{bmatrix} = \begin{bmatrix} V_{norm,a} \sin(\omega t - \pi) \\ V_{norm,b} \sin\left(\omega t - \frac{2\pi}{3} - \pi\right) \\ V_{norm,c} \sin\left(\omega t - \frac{4\pi}{3} - \pi\right) \end{bmatrix} \tag{5.18}$$

$$\vec{V}_{xl} = \begin{bmatrix} V_{al} \\ V_{bl} \\ V_{cl} \end{bmatrix} = \begin{bmatrix} V_{norm} \sin(\omega t) \\ V_{norm} \sin\left(\omega t - \frac{2\pi}{3}\right) \\ V_{norm} \sin\left(\omega t - \frac{4\pi}{3}\right) \end{bmatrix}$$

For the purposes of this explanation it is assumed the battery SOC's are perfectly balanced and thus the reference input to the SVM scheme is equal to $\vec{V}_{ru}$ and $\vec{V}_{rl}$ for the upper and lower phase arms

respectively. To synthesize the upper and lower arm reference modulation signals, nearest-level modulation is applied to generate a $m-1$ level reference.

$$\vec{V}_{xuSVM} = \begin{bmatrix} V_{auSVM} \\ V_{buSVM} \\ V_{cuSVM} \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} 1 + V_{norm}\sin(\omega t - \pi) \\ 1 + V_{norm}\sin\left(\omega t - \frac{2\pi}{3} - \pi\right) \\ 1 + V_{norm}\sin\left(\omega t - \frac{4\pi}{3} - \pi\right) \end{bmatrix} \tag{5.19}$$

$$\vec{V}_{xlSVM} = \begin{bmatrix} V_{alSVM} \\ V_{blSVM} \\ V_{clSVM} \end{bmatrix} = \frac{m-1}{2} \begin{bmatrix} 1 + V_{norm}\sin(\omega t) \\ 1 + V_{norm}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ 1 + V_{norm}\sin\left(\omega t - \frac{4\pi}{3}\right) \end{bmatrix}$$

5.10. FINDING THE OFFSET VOLTAGE VECTOR AND DEFINITION OF SWITCHING VECTORS

For a five-level SVM scheme, the space vector diagram in the α-β reference frame is shown in Figure 5.23. Finding the applicable switching vectors from all the possible available switching vectors is extremely computationally excessive, due to the sheer number of available vectors. Generally for an m-level converter, there are m^3 switching vectors and $3m(m-1)+1$ unique switching vectors.

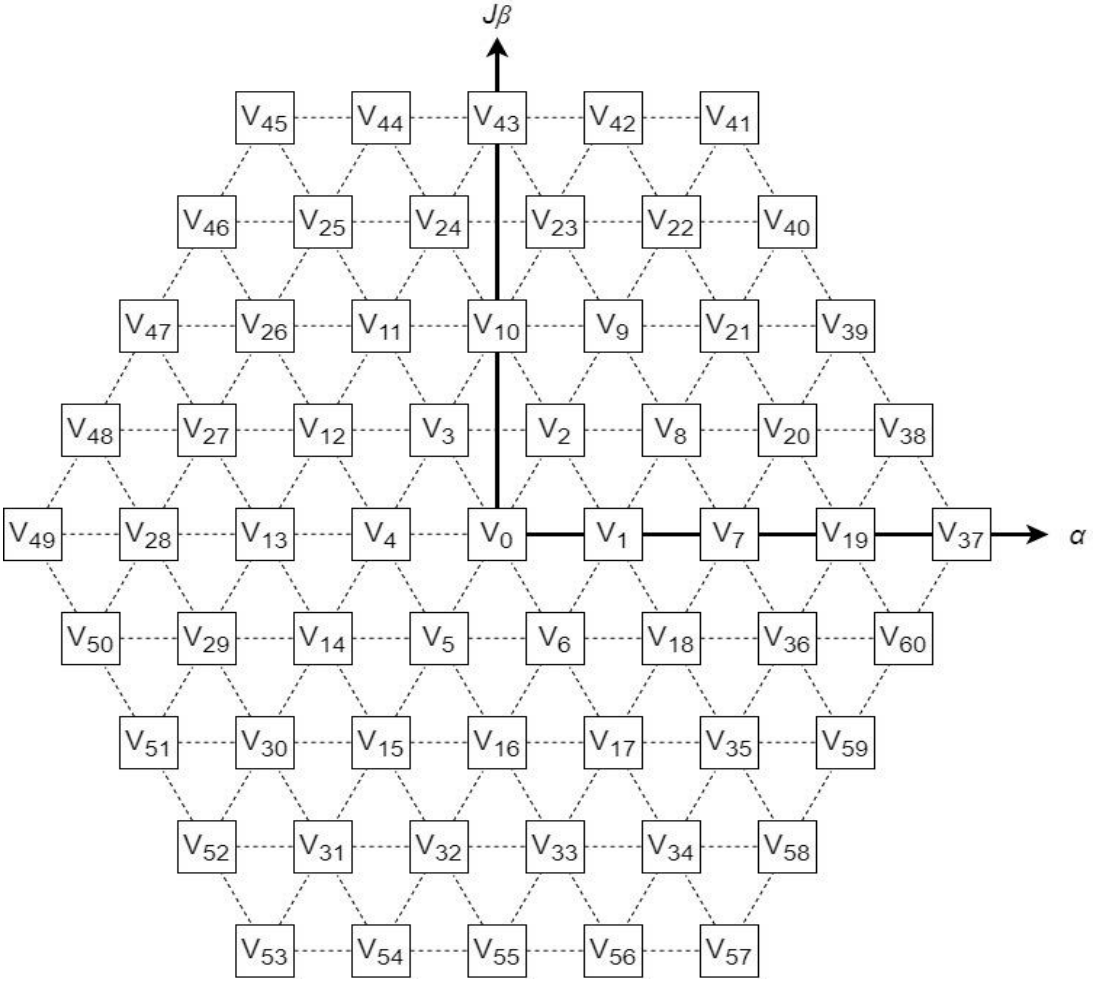


Figure 5.23. Unique space vectors available for 5-level MMC in the αβ-reference frame

To simplify this process, the reference (V_{xy}) can be decomposed to being an offset voltage vector (V_{xyo}) and a two-level voltage vector (V_{xyt}) as

$$\overrightarrow{V_{xy}} = \overrightarrow{V_{xyo}} + \overrightarrow{V_{xyt}} \tag{5.20}$$

By doing this, the m-level space vector diagram is reduced to being a 2-level space vector diagram (Figure 5.24).

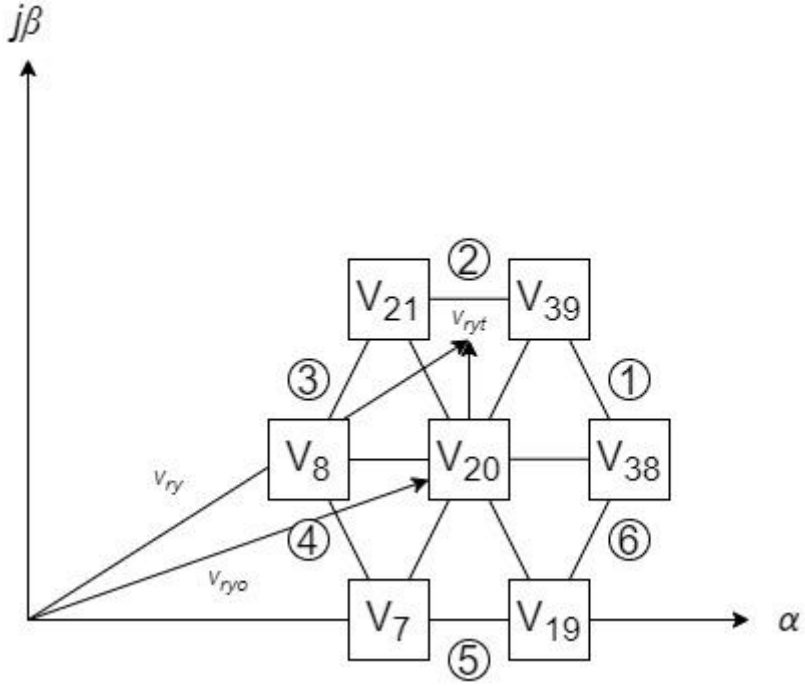


Figure 5.24. Two-level space vector embedded within multi-level vector space with voltage components and space vector sectors

The offset voltage vector represents the origin of the two-level space vector diagram, and the coordinates for it in the m-level space vector diagram ($a_{y0},\ b_{y0},\ c_{y0}$) are given by

$$\begin{bmatrix} a_{y0} \\ b_{y0} \\ c_{y0} \end{bmatrix} = floor\begin{pmatrix} a_y^* \\ b_y^* \\ b_y^* \end{pmatrix} \tag{5.21}$$

The two-level voltage vector is located within one of the six triangles in the two-level space vector diagram as shown in Figure 5.24. The switching vectors who form the two-level space vector diagram are combinations of the coordinates (a_{y0}, b_{y0}, c_{y0}) and (a_{y1}, b_{y1}, c_{y1}) . Where the coordinates (a_{y1}, b_{y1}, c_{y1}) are given by

$$\begin{aligned} a_{y1} &= 1 + a_{y0} \\ b_{y1} &= 1 + b_{y0} \\ c_{y1} &= 1 + c_{y0} \end{aligned} \tag{5.22}$$

The switching vectors who form the two-level space vector diagram are (a_{y0}, b_{y0}, c_{y0}), (a_{y1}, b_{y0}, c_{y0}), (a_{y1}, b_{y1}, c_{y0}), (a_{y0}, b_{y1}, c_{y0}), (a_{y0}, b_{y1}, c_{y1}), (a_{y0}, b_{y0}, c_{y1}), (a_{y1}, b_{y0}, c_{y1}), and (a_{y1}, b_{y1}, c_{y1}).

The required switching sequence for each sector defined in Figure 5.24 are outlined in Table 5.2.

Table 5.2. Space vector switching sequences for respective switching region

Sector	$\overrightarrow{V_{y1}}$	$\overrightarrow{V_{y2}}$	$\overrightarrow{V_{y3}}$	$\overrightarrow{V_{y4}}$
1	(a_{y0}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y0})	(a_{y1}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y1})
2	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y0})	(a_{y1}, b_{y1}, c_{y1})
3	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y1}, c_{y0})	(a_{y0}, b_{y1}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
4	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y0}, c_{y1})	(a_{y0}, b_{y1}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
5	(a_{y0}, b_{y0}, c_{y0})	(a_{y0}, b_{y0}, c_{y1})	(a_{y1}, b_{y0}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})
6	(a_{y0}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y0})	(a_{y1}, b_{y0}, c_{y1})	(a_{y1}, b_{y1}, c_{y1})

5.11. DETERMINATION OF SWITCHING VECTORS

In the abc-coordinate system, the nearest four switching vectors are used to generate the normalized reference vector. The reference vector volt-sec balance is defined as

$$\overrightarrow{V_{xy}}T_s = \overrightarrow{V_{y1}}T_{y1} + \overrightarrow{V_{y2}}T_{y2} + \overrightarrow{V_{y3}}T_{y3} + \overrightarrow{V_{y4}}T_{y4} \tag{5.23}$$

$$T_s = T_{y1} + T_{y2} + T_{y3} + T_{y4}$$

The required switching vectors ($\overrightarrow{V_{xy}}$) are identified based on the sector of the two-level space vector diagram the two-level voltage vector (V_{ryt}) occupies. This is found by measuring the angle of the two-level voltage vector in the αβ-coordinate system relative to the origin of the two-level space vector diagram (Figure 5.24).

The nearest four switching vectors for each of the six sectors are shown in Table 5.2. Switching vectors $\overrightarrow{V_{y1}}$ and $\overrightarrow{V_{y4}}$ are both located on the origin of the two-level space vector diagram. The distribution of the duty-cycles between these two only affects the zero-sequence voltage component. The method outlined in [90] uses a fixed distribution between the duty-cycles of the two vectors. The dwell timing sequence and the output switching sequences are shown in Figure 5.25.

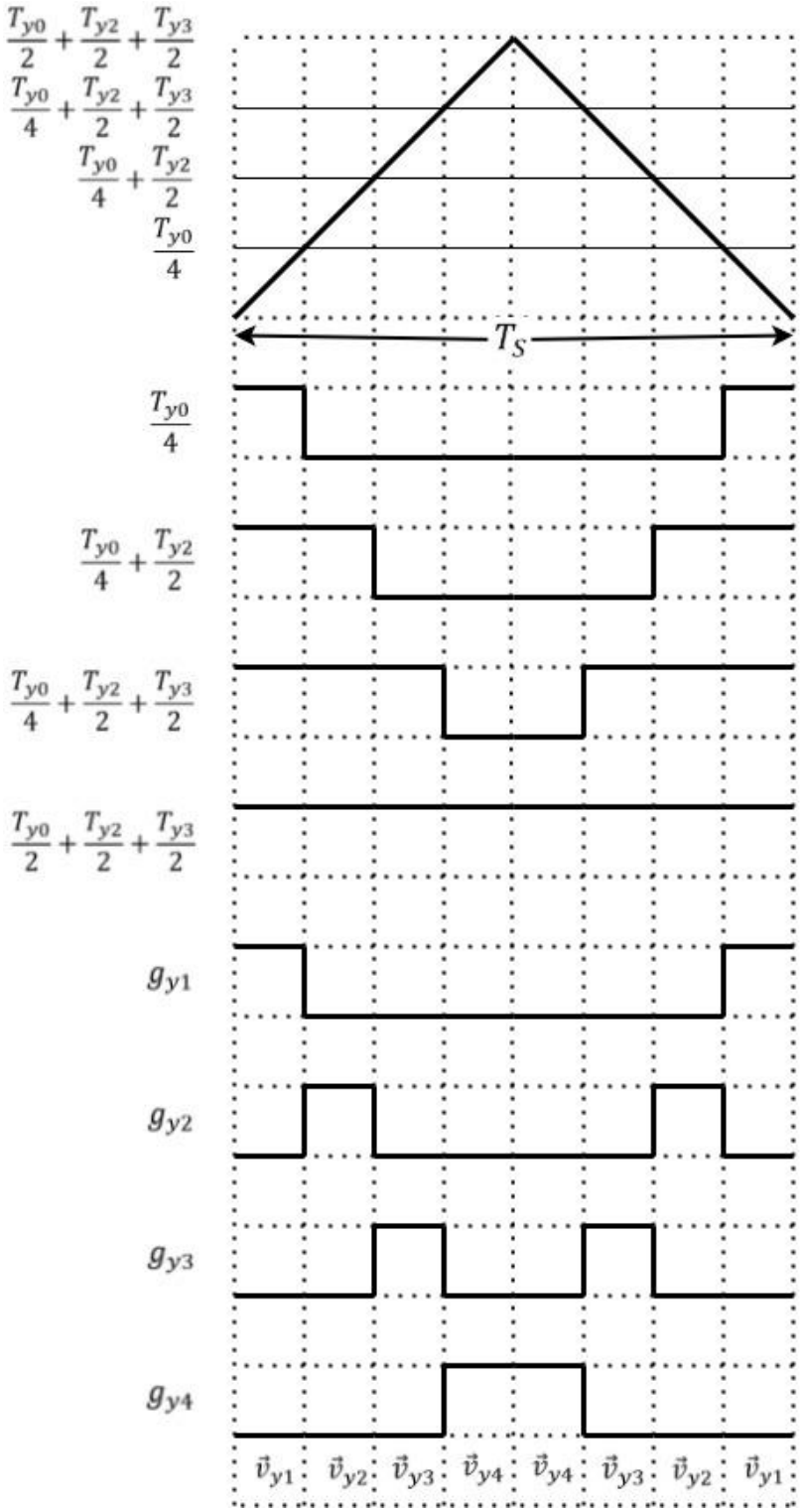


Figure 5.25. Dwell times and vector selection for SVM generation

5.12. CALCULATION OF DWELL TIMES

After the switching vectors have been identified, the dwell times for each switching vector needs to be synthesized. The dwell times are based off the two-level voltage vectors for each reference arm voltage. The dwell times for each arm are defined as

$$T_{ay} = a_{yt} \times T_s$$

$$T_{by} = b_{yt} \times T_s \tag{5.24}$$
$$T_{cy} = c_{yt} \times T_s$$

The dwell times for each switching vector are given by

$$\begin{aligned} T_{y1} &= T_s - max(T_{ay}, T_{by}, T_{cy}) \\ T_{y2} &= max(T_{ay}, T_{by}, T_{cy}) - med(T_{ay}, T_{by}, T_{cy}) \\ T_{y3} &= med(T_{ay}, T_{by}, T_{cy}) - \min(T_{ay}, T_{by}, T_{cy}) \\ T_{y4} &= min(T_{ay}, T_{by}, T_{cy}) \\ T_{y0} &= T_{y1} + T_{y4} \end{aligned} \tag{5.25}$$

As shown in Figure 5.25, the duty cycles are compared with the symmetrical triangle wave with period T_s to obtain the switching pulses g_{y1}, g_{y2}, g_{y3}, and g_{y4}, which correspond to the switching vectors $\overrightarrow{V_{y1}}$, $\overrightarrow{V_{y2}}$, $\overrightarrow{V_{y3}}$, and $\overrightarrow{V_{y4}}$, respectively. Once the switching vectors and duty-cycles have been calculated, the final output of the SMV scheme can be determined by applying a selected switching vector for a given duty-cycle. A symmetrical switching sequence is used to minimize the voltage harmonic distortion and current rippling. The sequence used, as shown in Figure 5.25, $\overrightarrow{V_{y1}} \rightarrow \overrightarrow{V_{y2}} \rightarrow \overrightarrow{V_{y3}} \rightarrow \overrightarrow{V_{y4}} \rightarrow \overrightarrow{V_{y4}} \rightarrow \overrightarrow{V_{y3}} \rightarrow \overrightarrow{V_{y2}} \rightarrow \overrightarrow{V_{y1}}$ is applied over a sampling period of T_s.

5.12.1. IMPLEMENTATION

The SVM scheme was then implemented as an embedded MATLAB function in Simulink. To generate the triangular reference for the switching pulse generation and defining the sampling period, initially an external continuous time repeating sequence block was used. However, to improve the performance of the model computation speed on the DS1103 this was replaced with a discrete time repeating sequence. So that the block could operate at a lower sampling frequency. As such, a solver method was not required for the model. This change resulted in synchronization issues within the model, as the discrete triangle wave was moving one time step out of phase with the SVM sampling period each period. To fix this issue, the external triangle reference generation was replaced with an internal reference generator within the SVM MATLAB function.

For the angle measurement of the two-level switching vector, the MATLAB 'atand' function was used. This function returns the vector angle in degrees over the interval of -90 to 90 degrees. The 'atan2d' function, which returns the angle over the interval of -180 to 180 degrees was not used. This was due to the SVM scheme being implemented on the DS1103 while the initial programming setup was still being used (Discussed further in Section 7.2.1.), and in the 2010 version of MATLAB the atan2d function was not available. Because of this, additional manipulation of the calculated angle was required to determine which sector the two-level switching vector was in. The polarity of the α and β components was used to determine which quadrant of the $\alpha\beta$-coordinate space the vector was in. Then the calculated angle was added to the angle of the closest positive major axis to generate the actual two-level switching vector (Shown in Appendix C).

The scheme the implemented SVM generator was designed off [90] uses a modulation index m_a for a fixed magnitude reference input, which allows the scheme to assume the normalized reference magnitude was less than one. However, within the MMC control-loop this assumption could not be made for certain. The issue with this arises when the offset voltage vector has a switching level equal to the maximum switching level. This will result in the scheme attempting to switch using a switching

level outside the switching capability of the MMC. This generates a switching sequence the hardware cannot complete. To prevent this, the scheme prevents a vector on the outer edge of the space vector diagram from being selected as the offset vector.

Since Embedded MATLAB functions do not inherently store variable values after the block has finished executing, the variables required to continue to generate the vector output over the sampling period is required. Experimenting with just feeding back the reference vector inputs to the block and with feeding back the calculated switching vectors and dwell times were performed. The former only requires the upper and lower arm reference signals to be feedback, but requires the dwell times and switching vectors to be recalculated each time the block is executed. Whereas the latter requires eight values to be feedback, but only requires the basic conditional logic to decide which vectors and which dwell times need to be used in a given moment. Through empirical testing it was found the former was significantly faster to execute within Simulink and so this method of memory was implemented in the version used with the DS1103 and the MicroLabBox.

5.13. SVM GENERATOR TESTING SCRIPT

To develop the SVM generator embedded function, a testing Simulink model which interfaces with a MATLAB script was made (Appendix C). The script takes in user specified switching parameters including:

- The maximum switching level (m),
- The switching frequency ($1/T_s$),
- The fundamental reference frequency ($\omega/2\pi$),
- And the Simulink model operating sample time.

The script then generates all the unique space vectors up to the level specified by the user in the abc-coordinate space and converts these to points in the αβ-coordinate space. The script then enters the user generated parameters into the Simulink model and simulates the SVM block's performance. The reference input, unique switching vectors, and the switching output are then plotted as a space vector diagram. For the desired carrier frequency of 5 kHz, with a reference frequency of 50 Hz, the SVM generator response is shown in Figure 5.26 and Figure 5.27.

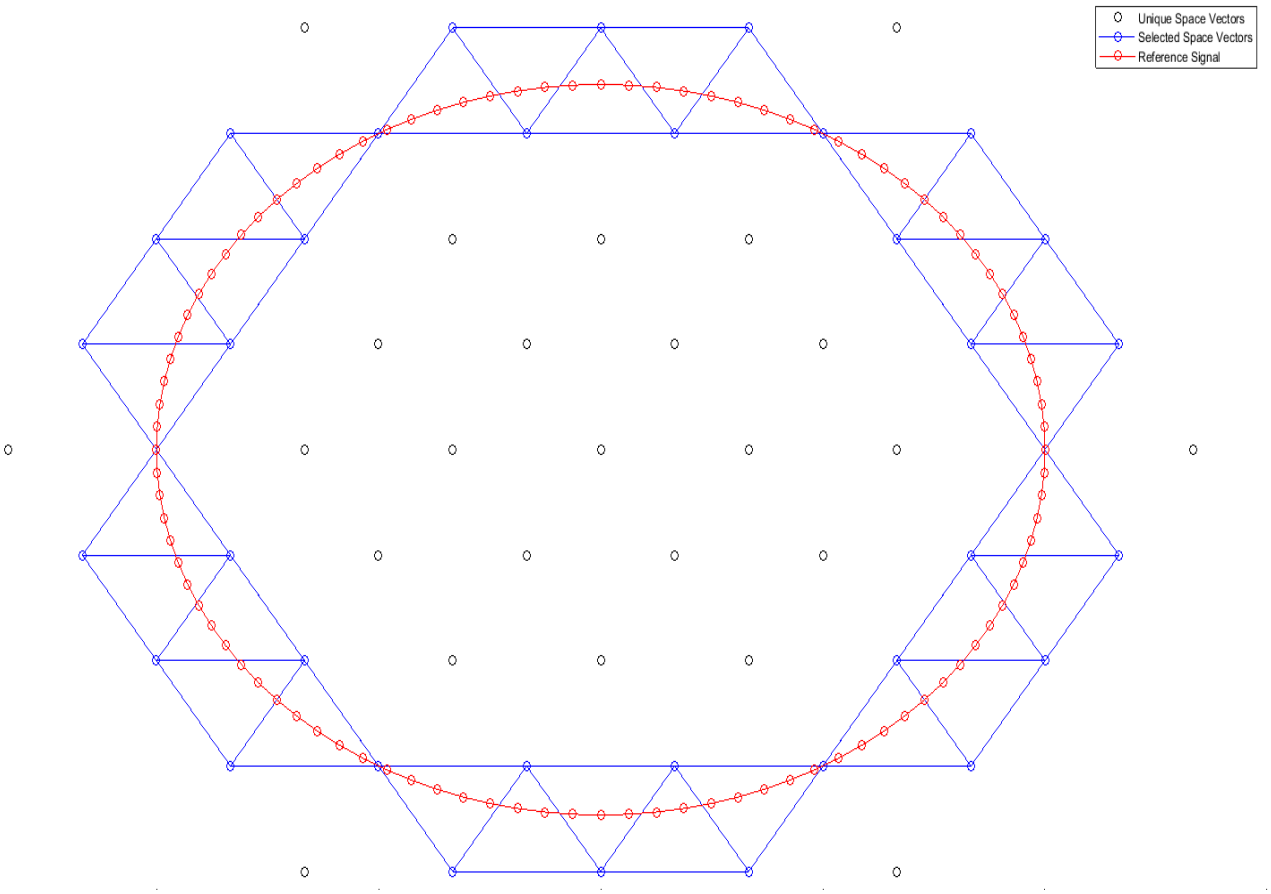


Figure 5.26. αβ-reference frame output of the implemented SVM scheme set for 5-level MMC

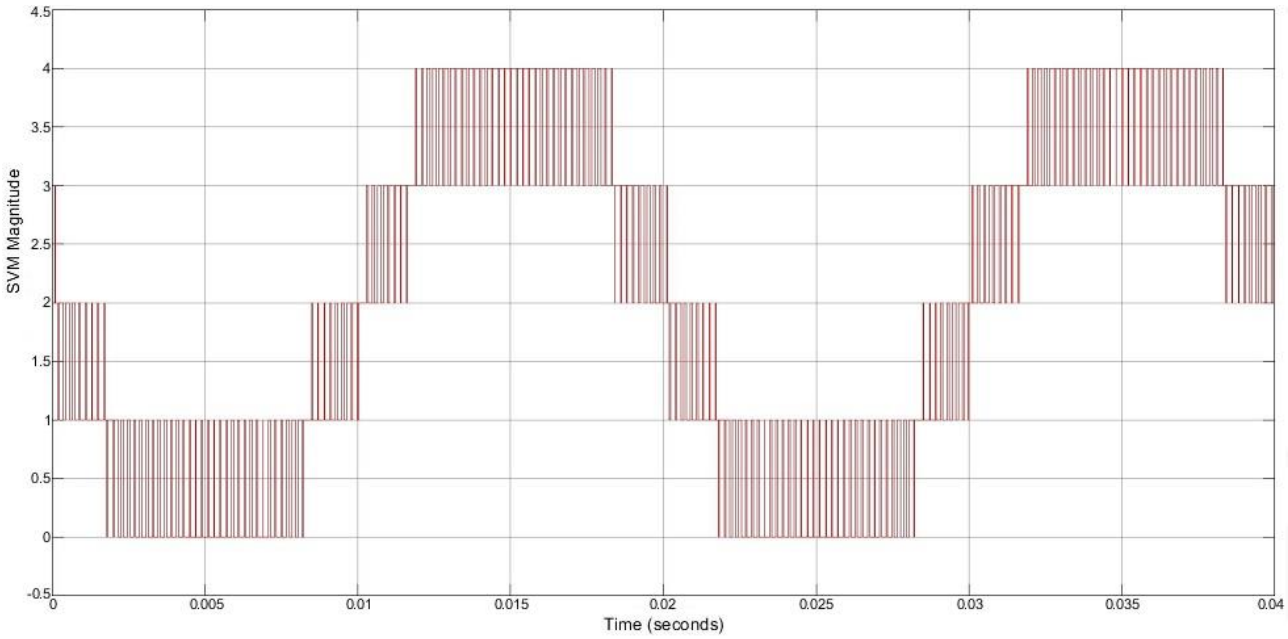


Figure 5.27. A single arm reference output of the developed SVM scheme in the abc-reference frame

Through the usage of the script, the relation between the SVM carrier frequency and the fundamental step time of the Simulink model was defined. Based off this relation, optimization of the SVM scheme could be evaluated based on the reduction of this. For the initial implemented

scheme, the fundamental operating frequency of the model needed to be at least 18 times the carrier frequency for the scheme to operate correctly by selecting all the switching vectors the corresponding triangle is made up of. This timing limitation was determined through observation of the sequence of switching vectors selected shown on the generated αβ-reference frame diagram. After a variety of techniques to improve the operation of the embedded MATLAB function (Section 7.2), this was reduced down to a factor of 10. The minimum factor for this is bound to eight. Due to the voltage vector application sequence applying the four unique switching vectors twice over the course of a sampling period, thus requiring at least eight fundamental time steps per sampling period to execute the switching sequence.

5.14. MODULE SOC BALANCING CONTROL

The SOCs of the modules within an arm with no selection scheme do not naturally converge, as shown in Figure 5.28. The arm and leg SOC control schemes are unable to dictate the balancing of the modules within an arm due to their ability to only select the number of modules connected to the bus, and not the specific modules.

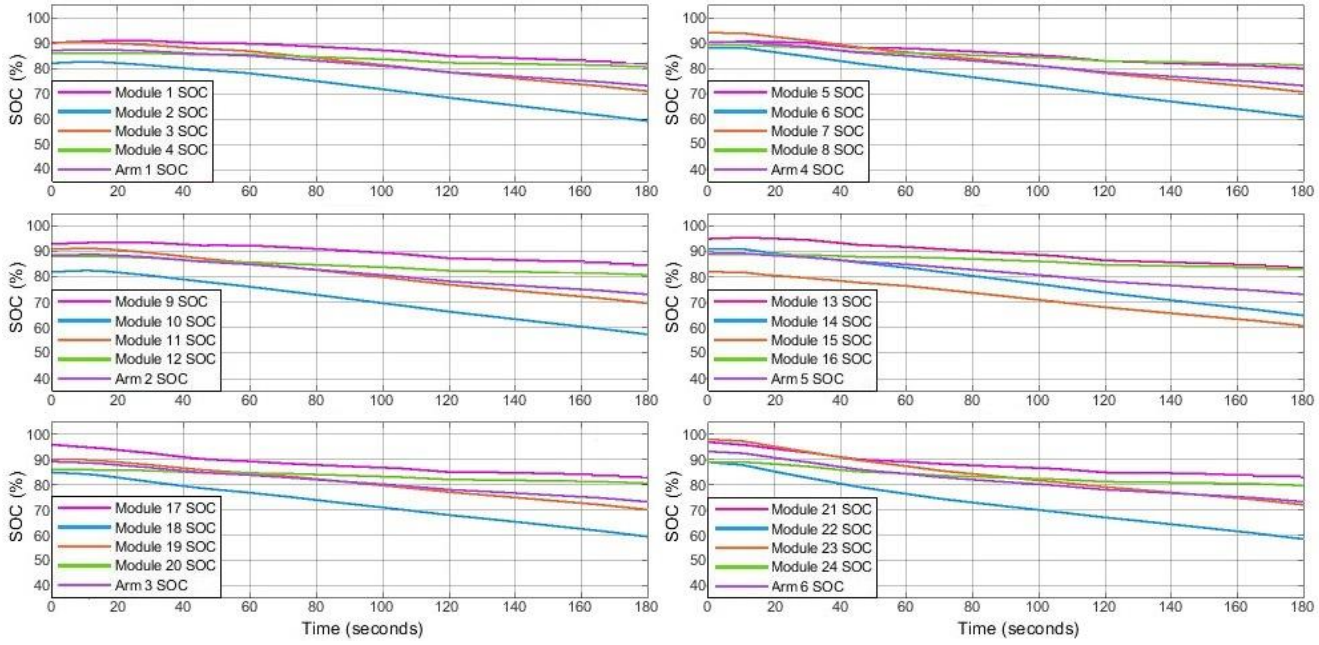


Figure 5.28. Arm module SOCs without module balancing control

As outlined in Section 4.3.1, one of the many advantages of the MMC topology is the ability to actively balance the embedded batteries without any additional circuitry while the converter is operating. This ability is a result of the fact that as a modular system, any of the modules in an arm can be switched in as required. Meaning, modules can be assigned a priority and the frequency/duration they are switched in for can vary based on the applied control. This allows for the case where modules at a higher SOC can be switched in more than those with a lower SOC when they are discharging, and the converse as well when charging. To implement a priority switching algorithm, one based off the one proposed in [90] was implemented. A state-flow diagram of the priority assignment scheme is shown in Figure 5.29.

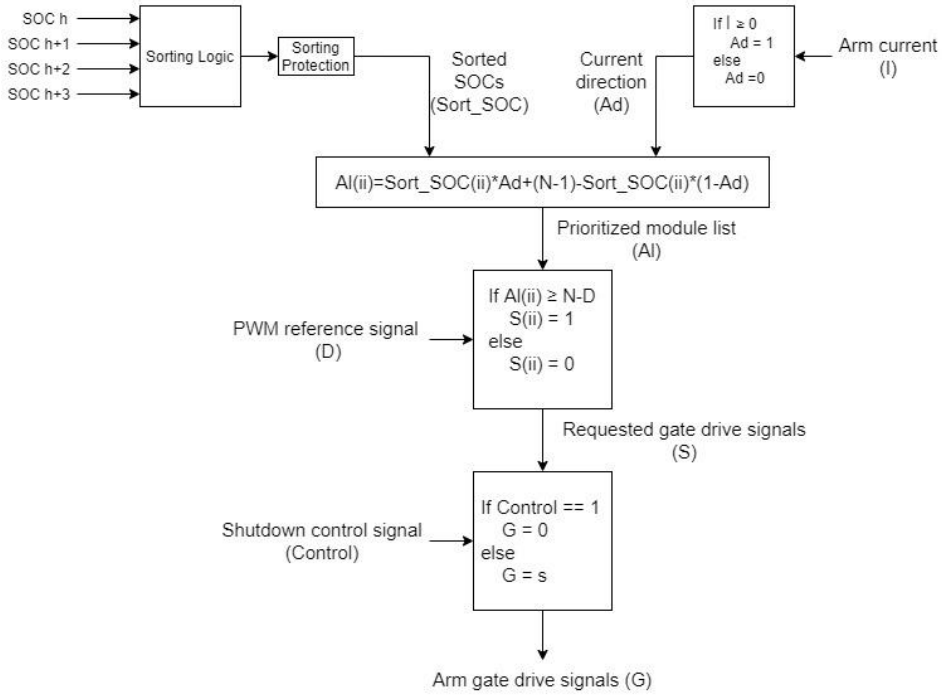
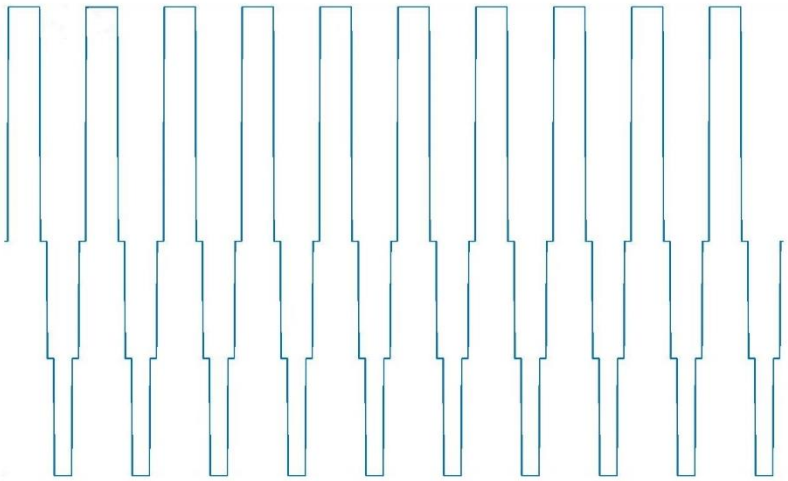


Figure 5.29. Flow chart representation of the Arm module SOC balancing control scheme

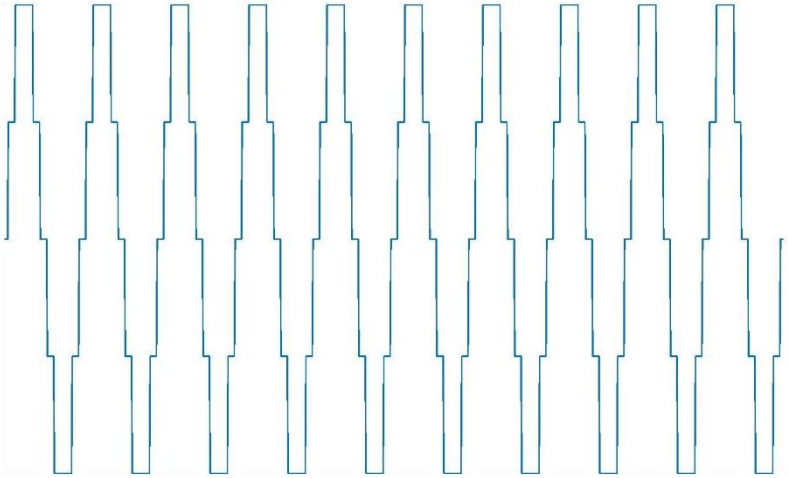
The scheme operates by sorting the modules into order based on increasing SOC, then reordering them based on if they are being charged (reverse order) or being discharged (no change in order). The scheme then determines how many modules to switch in based off the SVM PWM input before finally outputting the switching vector based off how many modules are required to achieve the desire PWM output, and the priority of the modules.

5.14.1. SIMULATION TESTING

During test simulations of the scheme, it was discovered that the algorithm proposed in [90] lacked any protection for the case where multiple modules are assigned the same priority. This will occur when two or more of the modules in the arm have the same SOC. Since the goal of the module balancing algorithms are to balance the modules to the point they are at the same SOC, protection against this was required to allow the motor control to still function. This resulted in multiple level changes occurring each switching cycle. To prevent this, additional priority assignment steps were added (Appendix D). A comparison between switching waveforms for the case where the two modules with the lowest SOC are given the same priority during discharge is shown in Figure 5.30.



(a)



(b)

Figure 5.30. (a) Output of the Module SOC balancing control scheme without priority assignment protection. (b) Output of the Module SOC balancing control scheme with priority assignment protection

A visual summary of the SOC-balancing operation of the implemented switching scheme is provided in Figure 5.31.

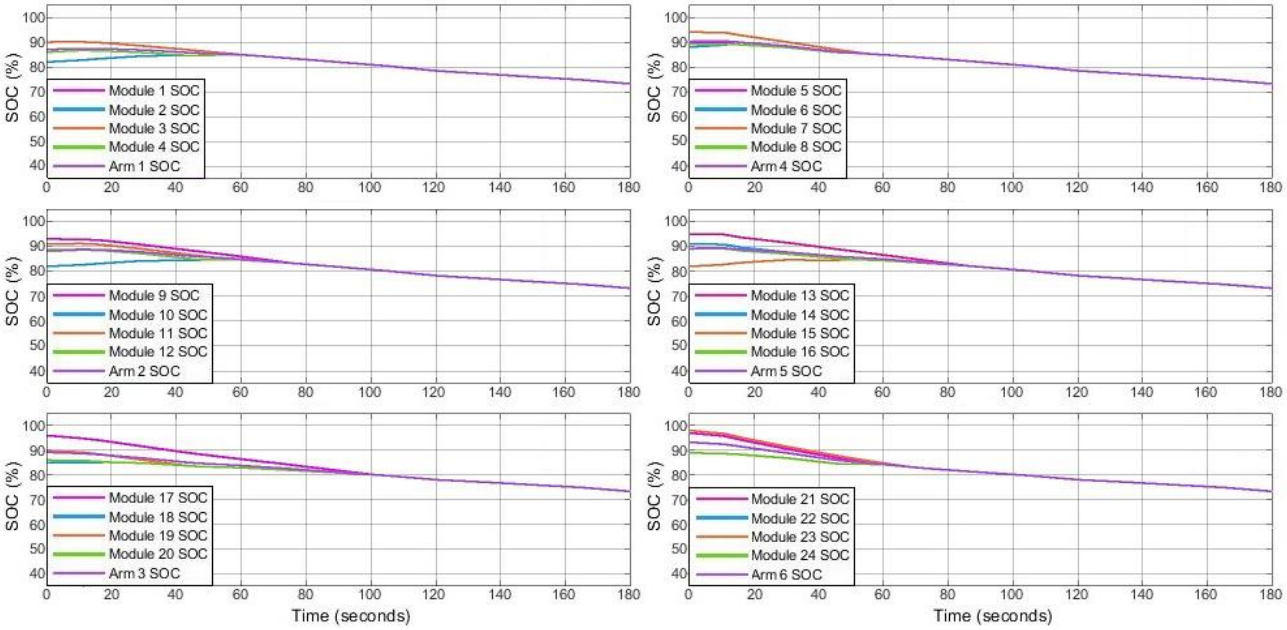


Figure 5.31. Arm module SOCs with module balancing control

While the SOC balancing control does balance the individual module SOCs to a common value. This only minimizes the RMS component of the circulating current without affecting the harmonic component. This is due to the implemented scheme only being designed to control the circulating current for the purposes of balancing the SOC differences between each leg. An additional control scheme designed to assume control once pack balancing has been obtained would need to be developed to minimize the circulating currents.

5.15. CHAPTER SUMMARY

This chapter detailed the various components of the MMC control system. The first section explains the FOC motor control scheme developed and implemented. As part of this, several of the selected motor's parameters needed to determined through testing of the motor. The process of determining these parameters, in particular the stator dq-axis inductances through the usage excitation tests, and impedance measurement. Following on from this, the technique used to balance the arms and legs of the converter is discussed. While discussing this, attention is paid to circulating current control for conventional MMCs and how this differs from the circulating control used for embedded battery MMCs.

The following section introduces the implemented SVM scheme used to generate a multilevel reference signal for the upper and lower arms of each phase. Since this PWM method is difficult to fully evaluate in the abc-reference frame, a testing script for interpreting the operation in the $\alpha\beta$-reference frame was used. This script was also used for evaluating the computational performance of the PWM generation scheme, since the initial version was inefficient in its construction.

The chapter concludes with the design of the control scheme for balancing the SOCs of the individual modules within an arm. This is achieved by ranking the priority for connecting the modules to the arm based on the SOC of the batteries and the direction of current flow through the arm. Such that modules at a lower SOC while discharging are less likely to be switched in, and more likely to be connected while charging.

CHAPTER 6 HARDWARE DESIGN

This chapter describes the design, manufacturing, and refinement of all the hardware components of the proposed MMC and the physical implementation of a laboratory prototype of a 5-level MMC. The majority of the chapter is focused on the design of the module PCB, comprised of an isolated half-bridge driver and isolated voltage measurement circuit. The tuning of this circuit through the usage of a simulation script is detailed, and the interfacing of the circuit with the main hardware controller is also discussed. The arm current sensors and arm inductor chokes are also specified in this chapter.

6.1. MODULE DESIGN

The module drive PCB was designed to be the interface between the main controller, embedded cells, and the rest of the converter. As such, this PCB needed to be designed to incorporate multiple systems and interface with several systems. Since the ground reference of one set of embedded cells can be connected directly to the positive battery terminal of the module beneath it, the modules needed to have separate ground references due to the case where a module is connected to the bus will cause a short between the positive terminal of the lower module and the ground reference of the module above it. To prevent this, either the modules had to operate on entirely separate ground references, or the cells and gate drive needed to be galvanically isolated from the rest of the module PCB. Since all the modules needed to interface with a single controller, the former option would be logistically difficult and hardware intensive, so the latter option was selected.

6.1.1. SEMICONDUCTOR SWITCH SELECTION

The vast variety of power semiconductor switches covers all applications in the power range, from applications using only a couple of watts, up to GW level applications [122]. However, as shown in Figure 6.1, these differing technologies are designed to operate at different power levels and at different switching frequencies. MOSFETs are the best option for low voltage applications because of the low on-state losses, high switching speeds, and high gate impedance. For MMC applications, a high V_{DS} is not required, due to the voltage applied across the drain and source while blocking is only the terminal voltage of the module batteries. In fact, a low break-down V_{DS} is desirable, due to the drain-to-source on resistance ($R_{DS(ON)}$) being inversely proportional to the drain-source breakdown voltage [123]. For this application the NTB6412ANG N-Channel Power MOSFET was selected, the characteristics of which are provided in Table 6.1.

Table 6.1. NTB6412ANG operating limits and switching characteristics [124]

Parameter	Symbol	Value
Drain-to-Source Voltage	V_{DS}	100 V
Gate-to-Source Voltage	V_{GS}	± 20 V
Continuous Drain Current	I_D	58 A
Power Dissipation	P_D	167 W
Drain-to-Source On Resistance	$R_{DS(ON)}$	18.2 mΩ
Turn-On Delay Time	$t_{d(ON)}$	16 ns
Rise Time	t_r	140 ns
Turn-Off Delay Time	$t_{d(OFF)}$	70 ns
Fall Time	t_f	126 ns

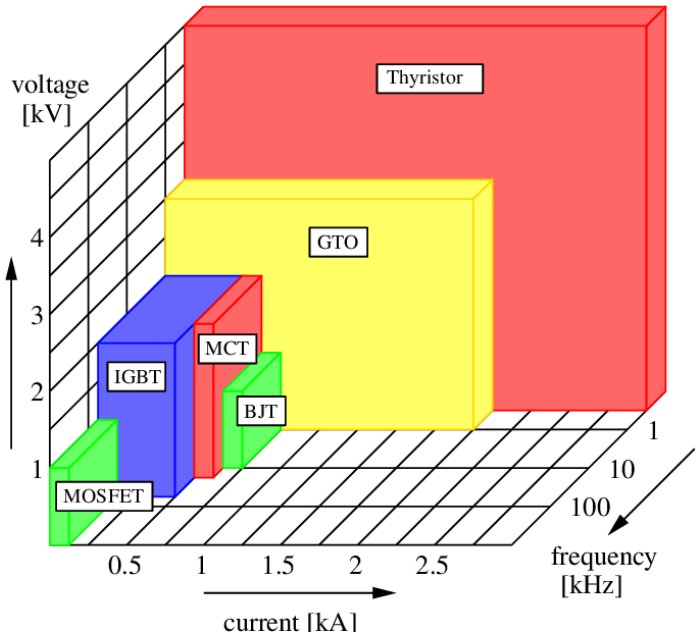


Figure 6.1. Summary of power semiconductor device capabilities [125]

6.1.2. Gate Drive Design

As detailed in Section 4.2.1.5, a half-bridge module topology was selected, and as discussed before, an isolated gate-driving solution was required to prevent battery shorts from occurring. Based off these two design criteria, a gate-driver circuit using the UCC21521 Isolated Dual-Channel Gate Driver was selected [126].

This package featured two independent isolated gate drives, which necessitated two separate control signals to control the half-bridge. Either two separate control signals from the controller were required, or a way of splitting the control signal into the two required signals was required. Since the former required an additional 24 PWM control signals, it was discarded in favor of an on-board signal splitting method. An on-board signal splitting option was helped by the inherently simple logic required to control the two gate drives. In that, the two drives must have opposing logic states at all times or else the embedded battery will be shorted (both drives HIGH) or the bus will be disconnected (both drives LOW). To implement this complimentary logic control a CMOS inverter was added to generate the second gate drive signal. To prevent propagation delay issues between the first and second gate control signals, a CMOS AND gate was added for the first gate control signal (Figure 6.2). By selecting two devices in the same series, it was expected that no significant propagation delays between the two control signals would occur and so no undesirable gate drive situations would occur. The two logic gates also act as an impedance buffer between the I/O pin on the main controller and the input pin on the UCC21521.

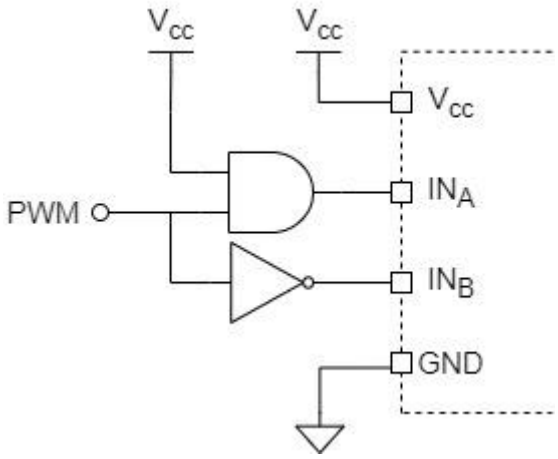


Figure 6.2. Logic gate arrangement for generation of half-bridge control signals

For a 2 kHz PWM input signal the switching propagation for the output of the logic gates is shown in Figure 6.3.

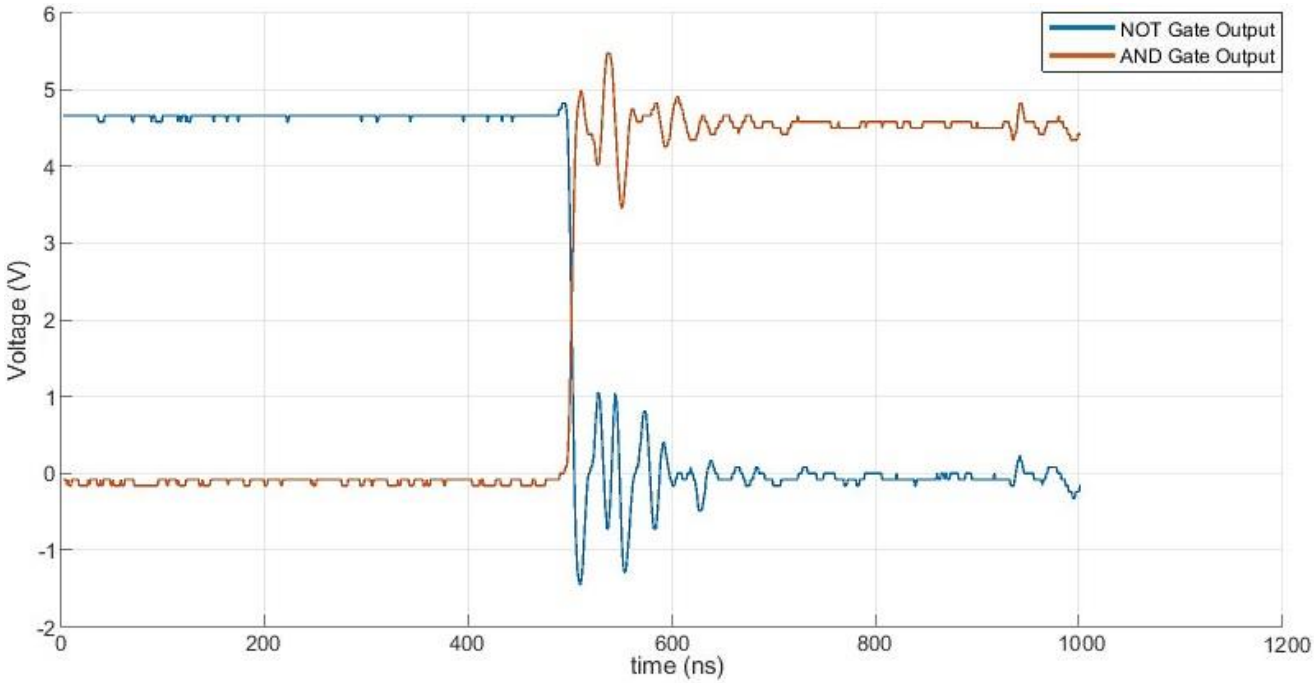


Figure 6.3. Output of logic gates used to generate half-bridge gate drive signals

The gate driver datasheet recommends a low pass filter on the PWM input to filter out ringing associated with imperfect PCB layout or long PCB traces. A high order LPF was discouraged due to the inherent trade-off between noise immunity and propagation delay. For the implemented circuit the first-order filter recommended by the datasheet with a cut-off frequency at 100 MHz was used.

6.1.2.1. DEAD TIME

To further prevent the unstable condition where both gate drives have the same state, the programmable dead time (DT) control pin was biased by connecting the pin to GND through a specified R_{DT}. Doing this causes the diver to drive the two output stages low in the event both drive inputs are high, preventing the embedded batteries from being shorted. The DT needed to be set to

a significantly smaller fixed delay time than the control switching period to prevent significant propagation delays through the gate driver. The DT resistor, R_{DT} in kΩ for a t_{DT} in ns is found with:

$$t_{DT} \approx 10 \times R_{DT} \tag{6.1}$$

A R_{DT} of 20 kΩ was selected, which corresponds to a DT of 200 ns. For a switching carrier frequency of 2 kHz corresponds to a switching period of 0.5 ms, 2500 times greater than the DT. Thus, any propagation delay introduced will have no effect on the carrier frequency switching. A 2.7 nF capacitor was placed in parallel with R_{DT} to improve the noise immunity on the pin.

6.1.2.2. ENABLE PIN

The UCC21521 also features an enable pin to enable or disable the output stage of the driver. This pin was driven high to disable it because the disable state will disconnect the module entirely from converter arm, rather than just going into a bypass state. Since the control within the main controller can individually control the modules and set them to a permanent bypass state if required, this form of drive disabling was deemed to be better for module disabling during operation of the converter. In addition, this reduced the need to have an additional 24 I/O connections between the controller and the modules.

6.1.2.3. BOOTSTRAP CIRCUIT

Since the MOSFET used for connecting the embedded cells to the MMC arm is connecting a power source to a load, it is acting as a high-side switch. NMOS require additional hardware for this situation, due to the source being in a floating position and not tied directly to the ground reference, as is the case with low-side switching. The case where the floating voltage is high enough that the V_{GS} required to drive the NMOS high is unattainable [127]. To prevent this, the gate of the high-side switch needs to be boosted when trying to drive the MOSFET on.

The basic half-bridge drive with a bootstrap is shown in Figure 6.4.

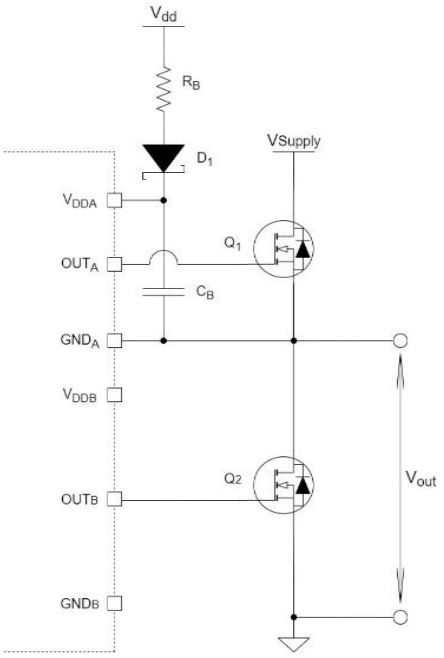


Figure 6.4. Simple half-bridge gate drive circuit with bootstrap circuit for high-side switch

When the high-side switch is turned off or when the GND_A rail voltage/output voltage dips below V_{DD}, the bootstrap capacitor, C_{BOOT}, charges through the bootstrap current limiting resistor, R_{BOOT},

and bootstrap blocking diode D_{BOOT} from the V_{DD} power supply. When the GND_A rail voltage is pulled to a higher voltage by the high-side switch, V_{BS} (the potential across the bootstrap capacitor C_B) acts as the power supply, since the V_{BS} supply floats and the bootstrap diode reverse bias and blocks the rail voltage (the high-side switch is turned on and the low-side switch is turned off) from the supply voltage, V_{DD}.

The estimated worst case peak current through D_{BOOT} is

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} \tag{6.2}$$

Where

- V_{BDF} is the forward voltage drop of the bootstrap diode
- R_{Boot} is the selected current limiting resistor resistance
- $I_{DBoot(pk)}$ is the largest current through the bootstrap diode

The datasheet recommends a high voltage, fast recovery or SiC Schottky diode, for this application the SD101AWS Schottky diode was selected.

$$I_{DBOOT(pk)} = \frac{15 - 0.4}{20} \approx 0.73\ A$$

The absolute minimum C_{BOOT} required is

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{VDDA}} \tag{6.3}$$

Where

- Q_{Total} is the total charge needed per switching cycle
- ΔV_{VDDA} is the voltage ripple at V_{DDA}.

The total charge needed per switching cycle can be estimated by

$$Q_{Total} = Q_G + \frac{I_{VDD}@f_{sw}(No\ Load)}{f_{sw}} \tag{6.4}$$

Where

- Q_G is the gate charge of the NMOS
- I_{VDD} is the channel self-current consumption with no load at the switching frequency

$$Q_{Total} = 100\ nC + \frac{1.5\ mA}{2\ kHz} = 850\ nC$$

Therefore, the absolute minimum capacitor value required is

$$C_{BOOT} = \frac{850\ nC}{0.5\ V} = 1.7\ \mu F$$

The datasheet notes that this value is the absolute minimum capacitance required and strongly recommends using a safety margin and so using a larger capacitor value was recommended. The datasheet also notes that an extremely large capacitor value would result in a failure to fully charge the capacitor within the first few switching cycles and cause V_{BOOT} to stay below the UVLO or fails to correctly bias the high-side switch gate. For this application a 2.2 µF capacitor was selected.

Since the bootstrap capacitor cannot be charged within an infinitely small period of time, having both the MOSFET drive circuits powered by the same isolated DC-DC converter has the potential to impose limitations on the achievable duty cycles for the bootstrap charged switch. Since, the bootstrap capacitor is only charged while the low-side switch is conducting, the duty cycle must be long enough for the bootstrap capacitor to sufficiently charge. To decouple the two circuits and prevent the bootstrap from introducing duty cycle limitations an additional isolated DC-DC converter was added to power the non-bootstrap circuit switch. With a power supply connected between the bootstrap diode and GND_A, the low-side switch does not need to be conducting for a current loop to form for charging the capacitor. Thus allowing the bootstrap capacitor to be charge irrespective of the state of the low-side switch.

6.1.2.4. GATE RESISTANCE

The external gate driver resistors, R_{ON}/R_{OFF} are designed to [126]:

- Limit ringing as a result of parasitic inductance/capacitances
- Limit ringing caused by high dv/dt, di/dt, and body-diode reverse recovery
- Tune the peak sink and source currents to minimize the switching losses
- Reduce EMI

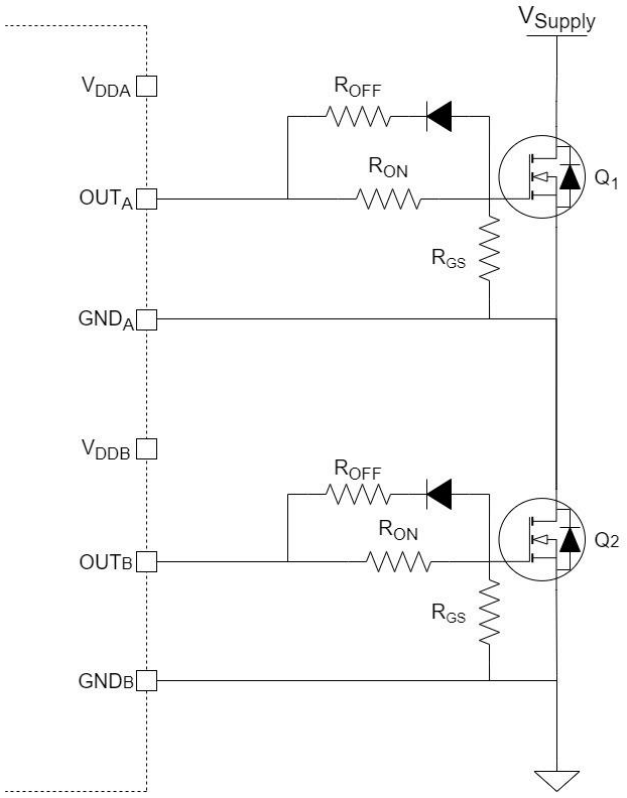


Figure 6.5. Typical half-bridge MOSFET gate drive circuit

Internally the UCC21521 has a pull-up structure with a PMOS and an additional NMOS in parallel. Given that the combined peak source current is 4A, the peak source current can be predicted as

$$I_{OA+} = min\left(4A, \frac{V_{DD} - V_{BDF}}{(R_{NMOS}||R_{OH}) + R_{ON} + R_G}\right)$$

$$I_{OB+} = min\left(4A, \frac{V_{DD}}{(R_{NMOS}||R_{OH}) + R_{ON} + R_G}\right) \quad (6.5)$$

Where:

- The equation for I_{OA+} assumes a bootstrap circuit with a forward voltage drop of V_{BDF} is used
- R_{NMOS} is the R_{DS} of the internal NMOS, found in the driver datasheet
- R_{OH} is the R_{DS} of the internal PMOS, found in the driver datasheet
- R_{ON} is the resistance of the external resistor in series with the gate (Figure 6.5)
- R_G is the characteristic gate resistance of the selected MOSFET
- I_{O+} is the peak source current

For the designed circuit:

$$I_{OA+} = \frac{15 - 0.4}{(1.47||5) + 15 + 2.2} \approx 0.81\ A$$

$$I_{OB+} = \frac{15}{(1.47||5) + 15 + 2.2} \approx 0.83\ A$$

Similarly, the peak sink current can be found by

$$I_{OA-} = min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + (R_{OFF}||R_{ON}) + R_G}\right)$$

$$I_{OB-} = min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + (R_{OFF}||R_{ON}) + R_G}\right) \quad (6.6)$$

Where:

- R_{OL} is the R_{DS} of the internal pull-down NMOS
- R_{OFF} is the external turn-off resistance (Figure 6.5)
- V_{GDF} is the forward voltage drop of the anti-parallel diode in series with R_{OFF}
- I_{O-} is the peak sink current

For the designed circuit

$$I_{OA-} = \frac{15 - 0.4 - 0.41}{0.55 + (10||15) + 2.2} \approx 1.63\ A$$

$$I_{OB-} = \frac{15 - 0.41}{0.55 + (10||15) + 2.2} \approx 1.67\ A$$

Bypass capacitors connected between the V_{DD} and V_{SS} pins of both gate drivers supports the transient current needed for the switching logic, and the total current consumption of the gate drive. For this 100 nF capacitors was selected.

A pulldown resistor (R_{GS}) between the gate and source acts as a short-circuit protection and to limit the power consumption of the circuit. When initially testing the circuit after manufacturing a prototype of the circuit, a resistor value of 800 Ω had been used. Which offered strong noise immunity during switching, but the power flow through the R_{ON} resistor was sufficiently high enough to damage the 1206 package surface mount resistor. These were subsequently replaced with 10 kΩ resistors, at the cost of an increase in voltage transients after each switching event.

The overall gate driver circuit implemented is shown in Figure 6.6.

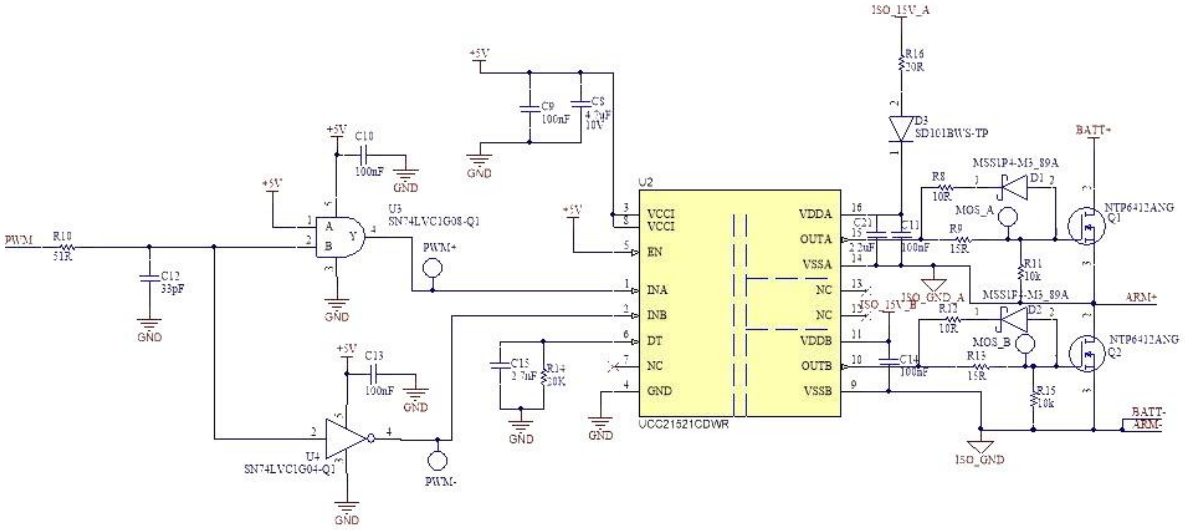


Figure 6.6. MMC Module full half-bridge drive

6.1.2.5. POWER SUPPLY

During the initial design of the module PCB, the energy source for the gate drive circuit needed to be considered. Whether it be from the embedded batteries supplying the individual module circuits or from an external supply, feeding all the circuits from a single source. The former option reduces the overall system complexity by removing a large amount of wiring between a large number of PCBs. whereas the latter offers easier interfaceability with the controller.

With the case of sourcing power from the batteries, a high level of voltage regulation is required to ensure the rail voltage of the electronics interfacing with the controller is the same across all the modules. This ensures the output operating range is consistent for all the modules, so no error is introduced when comparing the circuit outputs against one another. Even with the energy being sourced from the module batteries, an external power supply was still required for powering the current sensors and the rotor position sensor. When designing the module circuit for this case, the number of cells in series per module is needed to be known before the power distribution circuit can be designed. Which in of itself is dependent on the motor the prototype will interface with. At this stage of the design process, the 2020 COVID-19 outbreak in New Zealand had resulted in research being conducted remotely. With no motor selected for the application yet, the decision was made to use an external power supply, to simplify the module circuit design and the interfacing between the controller and the modules.

For the actual gate-drive circuit, an isolated power supply was required. This was due to the battery cells needing to be galvanically isolated from controller interfacing circuitry. Without isolation the negative terminal of the battery will need to be connected to the ground rail of the module circuit. All of these module circuits will need to share a common ground with the controller, to prevent floating voltage states creating measurement or interfacing errors. When more than one module connects their respective batteries to the arm bus, the negative terminal of a battery will be connected directly to the positive terminal of a downstream battery. With no galvanic isolation present a short-circuit between the positive terminal and the negative terminal of the downstream battery will occur, damaging both the circuit and the batteries. To prevent this case, the battery interfacing circuits need to be galvanically isolated from the controller interfacing circuits. To achieve this in regard to powering the circuits, isolated DC-DC converters would be used to power the MOSFET gate-driver circuit.

The UCC21521 features an under-voltage lockout (UVLO). For the UCC21521CDW the UVLO is set to 12V and recommends a V_{DD} of at least 14 V.

To determine the correct power supply, the power consumption of the gate drive circuit needs to be considered. The total power loss (P_G) in the gate drive includes the power losses of the UCC21521 (P_{GD}) and the power losses in the interfacing circuitry. P_{GD} is the primary source of power losses and can be estimated by calculating the losses from several components.

The static power loss, P_{GDQ}, includes quiescent power losses in the driver in addition to the driver self-power consumption for operation at a given switching frequency. P_{GDQ} can be determined from the per output current consumption vs. operating frequency with no load graph provided in the datasheet. For a 5 kHz switching frequency, a self-current consumption of ~1 mA is reported, and $I_{VDDA} = I_{VDDB} = 1.5$ mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} \tag{6.7}$$
$$= 5 \times 0.0010 + 15 \times 0.0015 + 15 \times 0.0015 = 50\ mW$$

The second component is the operational losses during switching, P_{GDO}, for a given capacitive load which the driver charges and discharges during each switching cycle. The total dynamic loss due to this load during switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \tag{6.8}$$

Where

- Q_G is the gate charge of the MOSFET

For the designed circuit

$$P_{GSW} = 2 \times 15 \times 73\ nC \times 5\ kHz = 11\ mW$$

The UCC21521 gate drive loss on the output stage, P_{GDO}, is a part of P_{GSW}. P_{GDO} is equal to P_{GSW} for the case where the external gate drive resistances are zero, so all the gate drive losses are dissipated within the UCC21521. For external turn-on and turn-off resistances, the total losses will be distributed between the gate drive pull-up/down resistances and the external gate resistances. For a pull-up/down resistor structure, the switching operating losses are

$$P_{GDO} = P_{GSW} \times \left(\frac{R_{OH}||R_{NMOS}}{R_{OH}||R_{NMOS} + R_{ON} + R_G} + \frac{R_{OL}}{R_{OL} + R_{OFF}||R_{ON} + R_G}\right) \tag{6.9}$$
$$= 11\ mW \times \left(\frac{5\Omega||2.2\Omega}{5\Omega||1.47\Omega + 15\Omega + 2.2\Omega} + \frac{0.55\Omega}{0.55\Omega + 10\Omega||15\Omega + 2.2\Omega}\right) = 1.37\ mW$$

The total power losses dissipated within the gate drive, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{6.10}$$
$$= 50\ mW + 1.37\ mW \approx 51\ mW$$

To provide this the SPU01L-15 5-15 V 1W Isolated DC-DC converter was used to bridge the isolation gap and increase the voltage applied to the gate drive.

6.1.3. Isolated Voltage Measurement Circuit

While galvanically isolating the embedded cells and the gate drive from the controller interfacing circuitry prevents grounding issues, it creates problems with measuring the embedded battery voltages. The battery voltage is needed to generate the initial SOC for the enhanced-Coulomb counter SOC estimation algorithm and for monitoring to prevent cells being overcharged or overdischarged. To measure this and relay it to the controller requires a means of bridging across the isolation gap without violating it.

For this, an isolation amplifier was used; the ACPL-C870 precision optically isolated voltage sensor was implemented, as shown in Figure 6.7. A voltage divider is used to down scale the measured voltage into the 2V input range of the isolation amplifier. The capacitor is used for filtering high frequency noise from coupling through, and with the values used, a cut-off frequency of 100 Hz has been applied.

The output of the isolation amplifier is a differential signal and so needs to be run through a differential amplifier to reconstruct the voltage measurement signal as a single ended signal. The differential amplifier also has another LPF built in to it, this time with a cut-off frequency of 10 Hz.

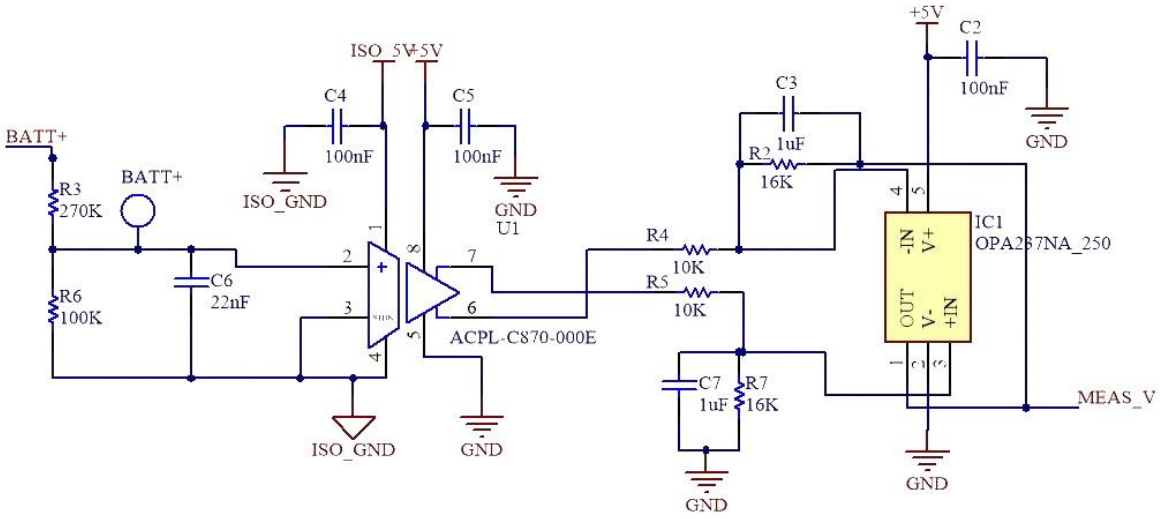


Figure 6.7. Isolated voltage measurement circuit used on module PCB

A separate isolated DC-DC converter was required for powering the isolated battery interfacing section, due to the ACPL-C870 having a maximum supply voltage of 5 V.

6.1.4. Isolated Voltage Measurement Circuit Tuning Script

To test and tune the circuit, a script in MATLAB (Appendix F) was created to model the circuit response at each stage of the circuit. This was done to help with the laborious task of empirically measuring the voltage on the manufactured PCB for a series of test input voltages.

Initial testing with the circuit involved applying a test voltage from a power supply to simulate a battery and then measuring the circuit response at each point in the circuit. Through this testing the physical maximum input voltages to both the isolation amplifier and the differential amplifier op-amp could be applied. To speed up circuit response tuning, a script was developed based off the physical limits found during the empirical testing. The script takes in a desired nominal DC voltage

for the battery pack of a MMC and generates statistics for the specified battery pack and gives the required component values for the circuit. The script assumes the desired MMC uses 5 levels and is using the Energus 1s8p 18650 cell bricks, however could easily be expanded for any desired level or battery chemistry.

Based off the desired nominal voltage, the script calculates how many bricks per module are required to achieve a nominal voltage equal or greater than the target nominal voltage. The script then generates a voltage divider with an input range greater than the possible battery terminal voltage range as a safety factor. Since the most optimal voltage divider transfer function will most likely use a non-standard resistor value. To compensate for this, the script determines if the resistor size selected is valid, or will calculate the closest possible valid resistor size that maintains a working transfer function. The script then checks if the designed voltage divider for the calculated voltage range will saturate the input of the isolation amplifier to validate it.

While performing empirical testing, the internal transfer function for the isolation amplifier turning the single ended input into a differential output was defined. This was used to model the response of the isolation amplifier to give the expected input range for the differential amplifier. Since the script was designed to always utilize the maximum input range of the isolation amplifier, irrespective of the number of batteries in series it is measuring, the voltage range applied to the differential amplifier would always be over the same range. However, to ensure the circuit output to the main controller is over the entire operational range possible, the script still simulates the response of the differential amplifier. The simulated circuit response for the designed circuit is shown in Figure 6.8. Finally, the script calculates a scalar compensation factor the controller needs to multiply the ADC input value by to calculate the measured battery voltage. For the designed circuit, the calculated interfacing component values are shown in Figure 6.9.

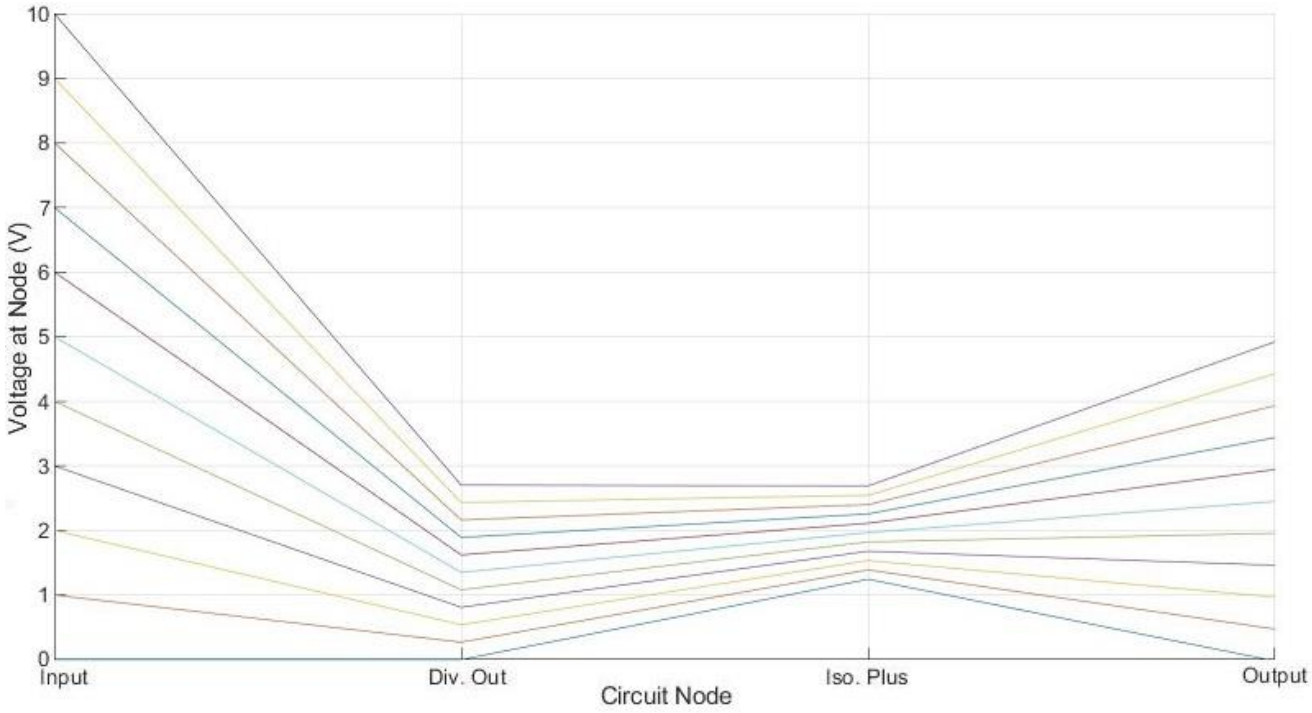


Figure 6.8. Isolated voltage measurement circuit response for the implemented circuit

Summary of Battery Pack Parameters		
Battery Pack Peak Voltage:	67.2	V
Battery Pack Nominal Voltage:	57.6	V
Number of Batteries per Module:	2	
Total Number of Batteries Required:	48	
Battery Pack Capacity:	3.46	kWh
Maximum Module Voltage:	8.4	V
Nominal Module Voltage:	7.2	V
Voltage Divider R1:	270	kOhm
Voltage Divider R2:	100	kOhm
Diff. Amp. R1 and R2:	10	kOhm
Diff. Amp. R3 and R4:	16	kOhm
Iso Amp. Filter Capacitor	22	nF
Diff Amp. Filter Capacitor	1	uF
Iso Amp. Cut-off Freq.	99	Hz
Diff Amp. Cut-off Freq.	10	Hz
Required software compensation coefficient	2.160	

Figure 6.9. Calculated parameters for isolated battery voltage measurement circuit

6.2. CURRENT SENSOR DESIGN

For the FOC motor control scheme to work, the converter phase leg current is required for feedback control of the direct and quadrature current components.

For the extended-Coulomb counter SOC estimation algorithm the current in/out of the module embedded batteries is required for calculating the change in battery charge storage. For a converter arm, the current through each set of embedded cells is the same, since they are in series. Meaning only a single current measurement is required to measure the current flow through each module in an arm.

For this application, a Hall-effect based sensor method was selected as opposed to a current shunt based method due to the inherent galvanic isolation of hall-effect sensors. However, it should be noted that some modern shunt sensors feature isolation amplifiers or isolation modulators [128]. For a Hall-effect sensor, the measured-current to output voltage transfer function is as follows

$$V_{Meas} = V_{ref} \pm \left(0.625 \times \frac{I_{Meas}}{I_{Nom}}\right) \tag{6.11}$$

Where

- V_{Meas} is the voltage output of the hall-effect sensor
- V_{ref} is the reference voltage generated by the sensor (generally 2.5 V)
- I_{Meas} is the current through the sensor
- I_{Nom} is the nominal current rating of the sensor

To reconstruct the current measured by the sensor from the output voltage of the sensor, the following transfer function can be used

$$I_{Meas} = 1.6 \times I_{Nom}\left(V_{Meas} - V_{ref}\right) \tag{6.12}$$

The sensor selected for this application is the LEM HLSR 32-P [129] because of its ± 128 A measurement range, nominal current value of 32 A, and easy PCB mounting.

The initial PCB design featured the hall-effect sensor feeding into a differential amplifier to convert the differential output of the sensor into a single-ended signal for interfacing with the controller ADCs (Figure 6.10).

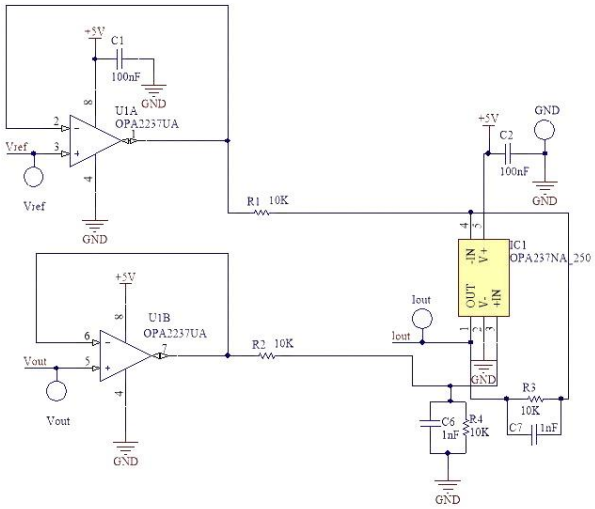


Figure 6.10. Current sensor interface with differential amplifier

However, during initial testing of this circuit, despite being the same construction as the one featured in the isolated voltage measurement circuit, it failed to give a correct system response. In the interest of speeding up the development of the circuit, instead of thoroughly analyzing the circuit response and redesigning, the circuit was instead restructured. On the PCB the differential amplifier components were removed and the V_{Meas} signal was routed directly to the output connector.

During the controller start-up phase where the initial embedded battery SOC is calculated and the moving-average filter buffers are settling, the controller measures the voltage output of the current sensor and stores this as the V_{ref} value. This can be done since on start-up no current is flowing through the system, meaning $V_{Meas} = V_{ref}$. An assumed V_{ref} value of 2.5 V could be used, but from empirical measurement of the output voltage, $V_{ref} = 2.50 \pm 0.02\,V$. Where a difference of 0.02 V corresponds to a difference of ~ 1 A.

When noise coupling was determined to be the issue with the current measurement waveform (as discussed in Section 6.5) a range of low-pass filtering techniques were implemented. To implement a physical hardware-based LPF some of the componentry for the differential amplifier was reinstated to reconfigure the circuit as a first-order LPF with an impedance buffering op-amp, as shown in Figure 6.11.

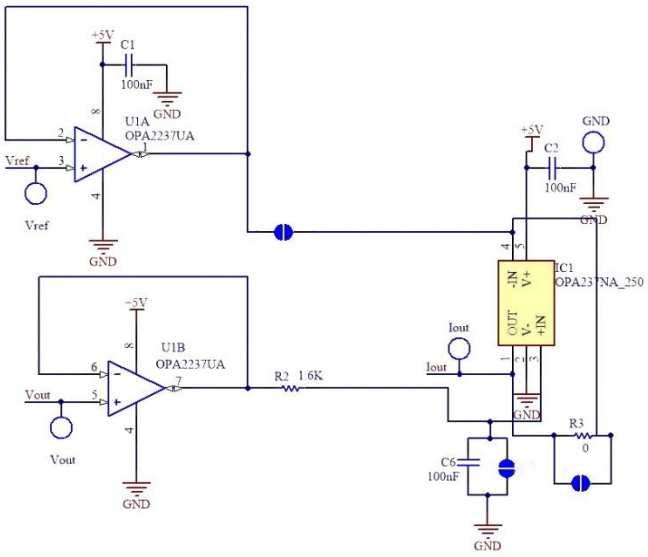


Figure 6.11. Current sensor interface circuit reconfigured as 1st order low-pass filter

6.3. ARM INDUCTOR DESIGN

The main design function of the arm inductor is to limit the magnitude of circulating currents and fault currents flowing through the arms. In particular, they are used to compensate for the voltage difference between the voltage of the phase-leg and the DC-side voltage [130]. As mentioned in Section 5.3, the second-order harmonic current component dominates the circulating currents. For the standard MMC topology the arm inductance value required for suppressing the second harmonic component of the circulating current can be found from [131] as

$$L \geq \frac{1}{8\omega_0 C V_C}\left(\frac{P_s}{3I_{2f}} + V_{DC}\right) \tag{6.13}$$

Where

- C is the module capacitance value
- V_C is the module voltage
- P_s is the apparent power
- I_{2f} is the second-harmonic component of the circulating current

This value is only designed for suppressing the circulating current, but ignores the role of limiting fault currents. As found in [132], selecting an arm inductance based on the fault limiting capability is done as follows

$$L = \frac{V_{DC}}{2\alpha} \tag{6.14}$$

Where α is the fault current rise rate, found using

$$\alpha = \frac{di_{xu}}{dt} = \frac{di_{ul}}{dt} \tag{6.15}$$

However, Equation 6.10 cannot be used for designing the inductors for an embedded battery MMC, due to the inductor rating being dependent on the module capacitance.

This problem was encountered by others who have developed a prototype embedded battery MMC, [8] derived an alternative means of determining the appropriate size for the arm inductor to sufficiently suppress circulating currents and limit fault currents. The current flow through the inductor is equal to the arm current. Thus, the magnitude of the steady-state voltage across the arm inductor is as follows

$$|\Delta v_L| = \omega L |I_{arm}| \tag{6.16}$$

Where, $|\Delta v_L|$ is the voltage across the inductor and $|I_{arm}|$ is the steady-state arm current. This current is dependent on the peak of the load current and the circulating current. The maximum value of the steady-state arm current is calculated as

$$|I_{arm}|_{max} = \frac{1}{2} I_{nom} + I_{cir,max} \tag{6.17}$$

Where I_{nom} is the nominal peak value of the load current ($I_{nom} = \sqrt{2} \times 95$ A) and $I_{cir,max}$ is the maximum peak value of the circulating current, which has been set to saturate at 5 % within the control. Substituting this for the arm current in Equation 6.13 is the maximum steady-state voltage drop across the arm inductor.

$$|\Delta v_L|_{max} = \omega L |I_{arm}|_{max} \tag{6.18}$$

Rearranging this for finding the minimum required value for the arm inductor gives

$$L \leq \frac{|\Delta v_L|_{max}}{\omega |I_{arm}|_{max}} \tag{6.19}$$

Assuming the voltage drop across the arm inductor is approximately 12 % of the nominal peak value of the load voltage V_{nom} and the operating frequency of the converter is double the nominal motor frequency (2x50 Hz), the buffer inductor is specified as

$$L \leq \frac{12\% \times V_{nom}}{(0.5 + 0.05) \times I_{nom} \times \omega_{max}} = \frac{0.12 \times (nV_{mod}/2)}{0.55 \times I_{nom} \times \omega_{max}} = \frac{0.12 \times (4 \times 3.6 \times 2/2)}{0.55 \times 95\sqrt{2} \times 2\pi \times 100}$$
$$= 37.2\ \mu H \Rightarrow 33\ \mu H$$

6.4. CONVERTER SETUP DESIGN

A full small-scale prototype of the proposed 5-level MMC with four modules per arm was built in the laboratory, shown in Figure 6.12. MATLAB/Simulink, dSPACE controller, the designed module PCBs, Li-ion bricks, current sensors, arm inductors, scorpion motor, motor feedback sensor, and LV power supply are employed to build the hardware-in-the-loop test rig.

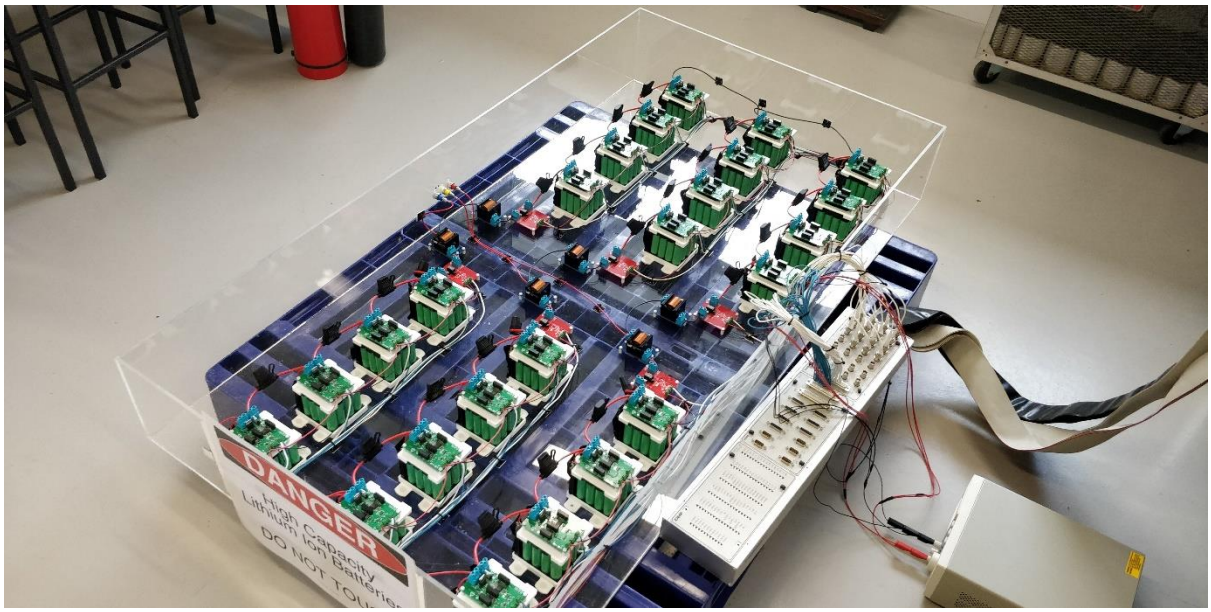


Figure 6.12. First iteration of the 5-level MMC with embedded li-ion batteries prototype

6.4.1. Module Mechanical Design

A protective non-conductive enclosure was required to house the prototype to prevent any physical damage to the Li-ion cells. As part of this, a means of securing the cells needed to be devised. A 3D printed baseplate and PCB holder were designed to package the Energus cell bricks and module PCB together. The design focused on design flexibility by being easy to scale the number of cell bricks in series. A proof-of-concept model was printed to ensure the design interfaced correctly with the bricks and module PCBs before being mass produced. To minimise material usage and printing time, the design was optimised to use as little material as possible while maintaining the required structural integrity. The final mass-produced module is shown in Figure 6.13.

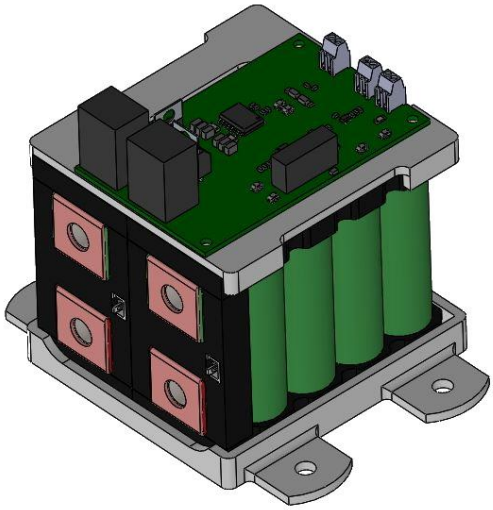


Figure 6.13. MMC Module PCB and embedded battery packaging

6.4.2. LV Bus Wiring

While testing the individual module PCBs to validate their functionality, the current drawn from the powers supply was observed as approximately 0.13 A. This meant an expected total current of at least 3 A for the entire converter setup. Since the DS1103 5 V bus had a current limit of only 1.5 A, a separate power supply was required to power the MMC.

Initially, the wiring of the 5 V and GND connections for the arms (four modules and a current sensor in series) was a single series string. The voltage of the 5 V rail at the PCB closest to the LV power supply and the PCB at the end of the bus in addition to the ground rail at those PCBs was measured. All voltage measurements were measured with respect to the ground point at the LV supply, so that any potential rises along the bus could be measured. A large discrepancy between the voltage at the top and bottom of the chain was observed. The LV bus wiring was then reconfigured as two parallel strings of devices in series, and then six parallel strings and the results compared as shown in Table 6.2.

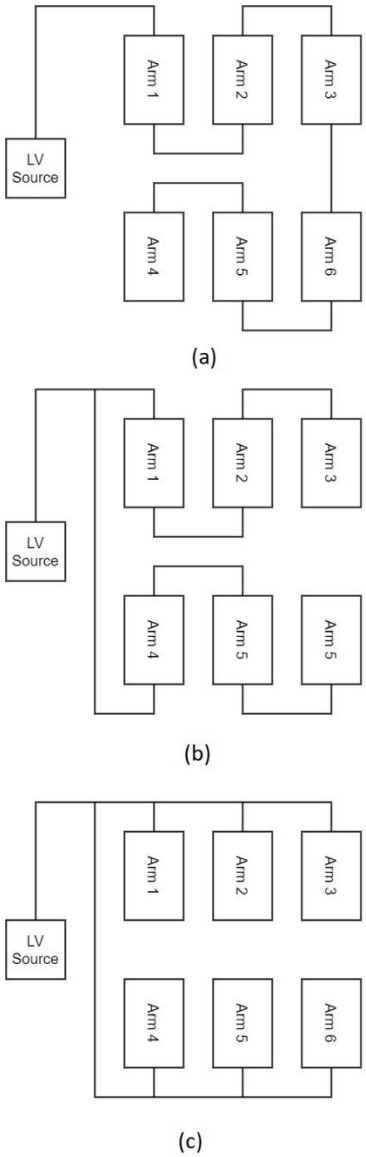


Figure 6.14. MMC 5V bus wiring configurations (a) a single series string, (b) upper and lower arms in separate series strings, (c) upper and lower arms in separate parallel strings

Table 6.2. Voltage measurements from LV bus configuration test

Configuration Number	Measurement Location	PCB 5V rail Voltage (V)	PCB GND rail Voltage (V)
(a)	Start	3.66	1.23
	End	3.44	1.44
(b)	Start	3.71	1.17
	End	3.21	1.53
(c)	Start	3.69	1.22
	End	3.68	1.22

It was important that both the 5V rail and GND rail voltages are equal across all the modules and current sensors as they all feed back to the DS1103. Therefore, the controller is receiving signals being generated across the same voltage operating range. Configuration (a) was first implemented due to the reduced amount of wire and required no wires to be spliced together. However, due to the large voltage discrepancy between modules using this configuration, the other options were explored. Based on the measured voltage distribution, configuration (c) was selected as the most suitable option. This was in spite of the significantly higher amount of wiring required.

In the event thermal runaway occurred within one of the module batteries, resulting in cells catching fire, the potential for this to damage neighbouring module batteries needs to be mitigated. To do this, the modules were separated from one another in an arm by 200 mm, so it was less likely a fire could spread from module to module. This large amount of spacing resulted in the prototype MMC being quite large and bulky in size, which had a follow on effect on the wiring. This large size necessitated long stretches of wiring, creating large inductive loops in the circuit. The effect of this was observed as the voltage losses measured while configuring the LV bus.

6.5. SIGNAL WIRING

Even though MMCs have a much lower THD than traditional 2-level converters and produce lower levels of electrical noise, they still nonetheless produce some electrical noise. Thus, consideration must still be made in regard to the prevention of noise coupling and proliferation within the circuit. The bespoke hardware designed for the project had on-board hardware based low-pass filtering for filtering out noise coupling through the connection to the arm bus. However, with the long sections of signal wiring between the prototype MMC and the controller, there is the prospect of noise coupling at this point in the circuit.

When the prototype was initially setup with just the filtering on the measurement circuits, a large amount of noise was observed while the converter was operating. An observed effect was that, the enhanced-Coulomb counter was being affected by large spikes in battery voltage causing the voltage tracking component of SOC-estimation scheme to override the Coulomb-counter component. The scheme believes the battery is either fully-charged or fully-discharged, seeing that the SOH or DOD are such that this is a discrepancy, the scheme assumes the estimated SOD and DOD on start-up are incorrect. So these values are updated based on the noise-affected battery voltage signals.

While considering methods for counteracting the noise coupling between the hardware and the controller, ferrite beads were considered as an easy to implement solution. However, due to ferrite beads being designed to filter out noise at extremely high frequencies (>1 MHz), it was unlikely to help with filtering out the 5 kHz switching noise.

Simple, ordinary copper core multistrand wire was used for wiring the module battery voltage connections to the controller to minimize the wire usage and cable management. Removal of noise

from these signals was achieved using low-pass filtering within the controller, since the battery voltage is a DC quantity, and will only vary over a long period of time as the batteries charge or discharge.

Since the current sensors need to transmit at significantly higher frequencies (closer to the switching frequency of the converter) than the battery voltage measurement circuit, filtering could be relied on less to prevent noise affecting the signal measurement by the system control. To make up for this, the choice of wire was used to improve noise immunity. For interfacing with the DS1103 slave-DSP, twisted-pair cable with a ground shield was used, since the slave-DSP interface was using a 30-pin d-sub connector. Whereas for interfacing with the PPC board, coaxial cables were used as the PPC board used BNC connectors for interfacing. While attempting to tune the software low-pass filtering to remove noise coupled through the wiring connection between the hardware and the controller, attention was paid to waveform shape for an applied known AC current waveform. During this testing, it became clear there was a distinct difference between the waveforms for the upper and lower arms. Namely, the upper arms had substantially more noise distortion in comparison with the lower arms. The only difference between the two was the wiring choice and the board the ADC connection was to. To isolate the cause of this noise, the current sensors connected to the slave-DSP were rewired to the PPC board ADCs using the twisted-pair cable. No observable difference was seen between connecting to the slave-DSP and the PPC board, meaning the choice of twisted pair cable was causing this unusual increase in noise coupling. This was surprising given the fact shielded twisted pair is well regarded for its noise shielding properties. Because of this, the rest of the current sensors were rewired using coaxial cable to the BNC connectors on the PPC board.

6.6. ENCODER SELECTION

As discussed in Section 2.5 position feedback of the stator electrical angle and the motor speed are required for the feedback component of the FOC scheme.

The dSPACE DS1103 connector panel featured dedicated encoder ports and offered dedicated incremental encoder blocks within Simulink, allowing for easy implementation of an encoder on both a hardware level, and on a software level. Since, no pin configuration was required and a state machine for tracking the output of the encoder to synthesize the encoder position was required. Because of these factors, an incremental encoder was chosen as the preferred feedback sensor.

Many encoder options require external interfacing componentry to electrically interface with the encoder or the mechanical mounting of the encoder or the encoder wheel. For ease of installation, options requiring little to no external interfacing design were deemed more favourable when searching for suitable encoders.

The motor selected proved difficult to mount an encoder using traditional mounting methods (encoder mounted to the casing with the encoder coupled with the rotor output shaft), due to the rotor permanent magnets being attached to the inner section of the front motor casing section and this being connected to the rotor shaft. The motor featured a threaded nut mechanically attached to the rotor, allowing for the rotor position to be measured from the back of the motor. However, the motor mounting points are closely situated radially around this port, and would interfere with the mounting of any encoder mounted directly to the rear casing. To overcome this, a 3D printed stage was designed to offset the encoder mounting from the motor chassis (Figure 6.15).

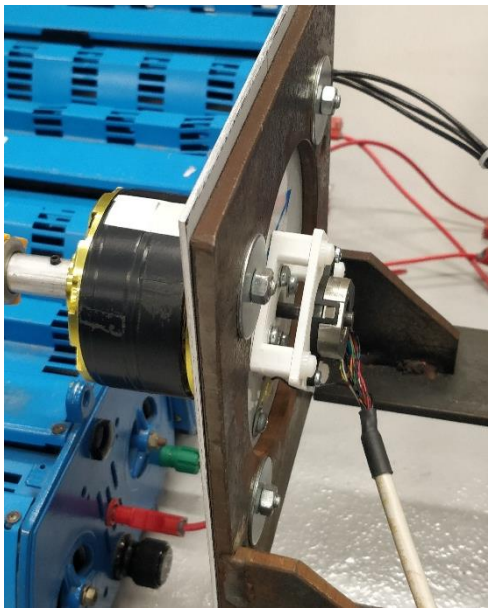


Figure 6.15. Motor with encoder mounting

For this application the AMT11 series capacitive incremental encoder was chosen [133]. The differential signal model chosen to prevent noise produced by the converter from affecting the output of the encoder.

While testing the converter, the original encoder had a hardware failure, resulting in the differential outputs being driven high irrespective of the position of the rotor. In the interest of completing the project in a timely manner, the decision was made to outright purchase a new encoder, rather than investigate the source of error within the encoder.

Due to the inability to source an identical encoder without long lead times (a now common issue owning to COVID-19), a new encoder needed to be sourced. The AMT10 series was chosen to as a replacement [134]. This encoder was selected as it had the same mounting footprint as the pervious encoder and was configurable to operate with the same resolution. Meaning, no changes to the interface in Simulink needed to be made. Although, this did come at the cost of noise immunity, since the new encoder only offered single-ended signals. Rather than a differential output, which offers improved immunity to noise on the signal lines.

6.7. CHAPTER SUMMARY

This chapter detailed the design, manufacturing, and refinement of the hardware components of the prototype MMC. The first section details the design of the isolated half-bridge driver circuit for the modules. While designing the circuit, considerations needed to be made as to the source of power for the circuit, whether it be from the module embedded batteries, or from an external bulk power supply. The design of the gate drive for both switches and the bootstrap circuit for the high-side switch is also detailed.

In addition to the isolated half-bridge driver, an isolated voltage measurement circuit for measuring the module embedded battery terminal voltage was also present on the same PCB. During the design and manufacturing of the circuit, tuning the circuit to interface with the batteries while maintaining the maximum possible resolution, and preventing any signal saturation, was required. To assist with this, a script in MATLAB was created to simulate the circuit at each stage and generate the appropriate biasing component values for the circuit.

CHAPTER 6 HARDWARE DESIGN

The following section discusses the design of the arm current sensors and the arm inductors. In particular, the interfacing circuitry for the current sensor and how this was reconfigured as a first-order LPF. While specifying the arm inductor choke, consideration needed to be made with regard to the way of determining the required inductance. Since, the conventional equation used for calculating the required inductance being proportional to the capacitance of the module capacitors for a standard MMC. For the embedded battery MMC, the arm inductor choke is designed with a focus on limiting the peak current flow through the arm.

The following section details the design of the prototype 5-level converter, with attention paid to the mounting of the embedded batteries and the module PCBs. While designing the converter setup, the wiring configuration of the LV bus supplying power to the individual PCBs needed to be considered to ensure the rail voltage was consistent across all the PCBs. As a part of this, various wiring configurations were considered and compared through empirical testing. Considerations also needed to be made with regard to the signal wiring between the PCBs and the main controller, in particular the threat of noise coupling along these wires, giving distorted measurement values to the controller. To avoid this a variety of methods were used, in this chapter close attention was paid to the choice of wire and the expected frequency range of the signals being carried.

The final section details the specification of the incremental encoder used for motor position feedback and the difficulties encountered mounting the device. The selection process was driven by the convenience of interfacing with the controller, the need for external interfacing components, and the ability to mount on the selected motor. Based on these, the AMT11 series capacitive incremental encoder was selected. While using this encoder an error prevented the selected encoder from functioning. After acquisition of a new unit was deemed impossible due to long lead times, the encoder was replaced with one from the AMT10 series.

CHAPTER 7 SIMULINK, DSPACE, AND HARDWARE IN THE LOOP SIMULATION

This chapter describes the process of implementing the designed control scheme in Simulink and the application of the Simulink model onto the dSPACE controller hardware. The hardware in the loop (HiL) development methodology is explained, and its implementation for electric vehicle applications is explored. The DS1103, the initial dSPACE hardware controller used with the prototype MMC is described and the challenges faced working with the controller are discussed.

7.1. HARDWARE IN THE LOOP SIMULATION

The basic philosophy of hardware-in-the-loop simulation is to include a section of the real hardware in the simulation loop during development of a system. Rather than developing and testing a control algorithm using a purely mathematical model of the system, real hardware can be implemented within the simulation loop. This can be used to remove the need to model complex physical systems, such as actuators, by implementing the physical components in the simulation system. This method is performed in real-time, ensuring the embedded control system can operate and deliver the control input within the required sample period. This is important for system validation, since the failure to deliver a control signal within a given sample period can affect the stability of the system. Historically, this method has been used for over 50 years, but has been carried out in an ad hoc fashion arbitrary to the given application [135]. Of the wide variety of applications, some include:

- Flight simulation [136]
- Missile guidance systems [137]
- Highly maneuverable aircraft [138]
- Anti-lock braking systems [139]
- Traction control systems [140]

Within the context of automotive powertrain control development, this method of control system development is widely used for testing engine control units (for ICE vehicles) and vehicle control units (for EVs). Due to the time-consuming nature of testing in real vehicles and coming very late in the automotive development process [141]. Instead of being implemented within a physical vehicle, the VCU/ECU to be tested is connected to a HiL simulation system. Software and hardware models implemented within the HiL simulation system are used to simulate the vehicle and related sensors and actuators. Note, in this situation the HiL hardware is used to simulate the hardware the controller (the VCU/ECU) is used to control. Conversely, HiL can be used as the controller and interface with designed hardware, as is the case for the subject of this thesis. Typically, the models are developed with an applicable modelling tool, the most ubiquitous being MATLAB/Simulink. The program automatically generates C code, which is downloaded to the real-time processor for execution. I/O boards provide the interface to the VCU/ECU pins. A typical HiL architecture for VCU/ECU development is shown in Figure 7.1.

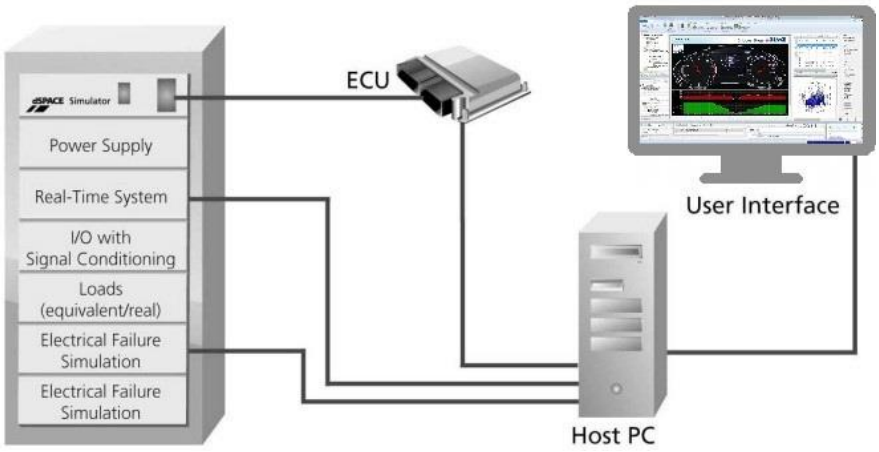


Figure 7.1. Typical HiL system architecture for VCU/ECU development [141]

From the initial stages of this research, it was determined a HiL approach to the design and validation of the control system would be used. This was to allow for the development of both the hardware and control systems in conjunction, removing the requirement of fully developing one to validate the other.

7.2. DSPACE CONTROLLER

7.2.1. DS1103

For the implementation of the HIL development strategy, a controller interface capable of using MATLAB/Simulink models to control the developed hardware was required. The department of Electrical Engineering already had on-hand a dSPACE DS1103 PPC Controller which had been previously used for research [142]. This unit was specifically designed for development of high-speed multi-variable digital controllers and real-time simulations in various fields. It was a complete real-time control system, based on the Power-PC (PPC) processor. In addition to the PPC processor, the unit also features an on-board slave-DSP subsystem based on the TMS320F240 micro-controller.

The CLP1103 connector panel provides an interface between the DS1103 controller board and the developed hardware. The CLP1103 connector panel uses 28 BNC connectors, 20 for ADC inputs and 8 for DAC outputs, and several other d-sub connectors used for digital I/O, slave-DSP I/O, incremental encoder interfacing, Controller Area Network (CAN) interfacing, and serial interfacing. Only the ADCs, slave-DSP I/O, and the encoder interfaces were used for interfacing with the hardware.

A summary of the technical properties of the DS1103 is given in Table 7.1.

Table 7.1. Technical parameters of the DS1103 [143]

Hardware parameter		Specifications
Processor	PowerPC Type	PPC 750GX
	CPU Clock	1 GHz
	Bus Frequency	133 MHz
Memory	Local Memory	32 MB application SDRAM
	Global memory	96 MB communication SDRAM for data storage and exchange with host
Timer	2 General purpose timers	One 32-bit down and one 32-bit up counter
	1 Sampling rate timer	32-bit down counter
	1 time base counter	64-bit up counter
Interrupt controller		20 interrupts
ADC	Channels	16 multiplexed channels and 4 parallel channels
	Resolution	16-bit
	Input Voltage range	± 10 V
	Overvoltage protection	± 15 V
	Conversion time	Multiplexed channels: 1 µs Parallel channels: 800 ns
	SNR	≥ 83 dB
	Offset error	± 5 mV
DAC	Channels	8 channels
	Resolution	16-bit
	Output range	± 10 V
	SNR	≥ 83 dB
	Offset error	± 1 mV
Digital I/O	Channels	32-bit parallel I/O organized in four 8-bit groups
	Voltage range	TTL input/output levels
Incremental Encoder	Channels	6 digital channels and 1 analogue channel
Slave DSP	Type	Texas Instruments TMS320F240 DSP
	Clock rate	20 MHz
	Memory	64Kx16 external code memory 28Kx16 external data memory 4Kx16 dual-port memory for communication 32 KB flash memory
	I/O channels	16 ADC inputs 10 PWM outputs 4 capture inputs 2 serial ports
	Input voltage range	TTL input/output level ADC inputs: 0-5 V

For interfacing the dSPACE hardware with MATLAB, the ControlDesk experiment software is used. This software serves a variety of purposes. Firstly, it provides an interface for downloading controller models implemented in Simulink onto the controller board. The “instrument panel” function of ControlDesk is used to display input/output values to the dSPACE and the internal variables within the uploaded Simulink model.

The inherited PC setup used for interfacing with the DS1103 was tied to an archaic version of MATLAB (2010), which created an increased degree of difficulty when converting the simulation model into a control scheme model for the DS1103. This was due to many of the blocksets or functions added in subsequent iterations of Simulink and MATLAB being unimplementable within the control scheme, requiring additional steps being taken to maintain the designed control functionality.

7.2.1.1. HARDWARE INTERFACING

Despite being packaged together and externally appearing the same, interfacing with the PPC board and the slave-DSP was significantly different. For the interfacing between the external analogue signals and the internal digital signals, an internal scaling factor was applied both on the input and on the output of signals. As such, converting a signal generated within the Simulink model to an external analogue signal is a factor of 10 times the magnitude specified within the model, and the inverse holds true for the analogue input to the model. However, this scaling only applies for the analogue/digital interfaces for the PPC board, whereas for the slave-DSP this is only a factor of five. Other differences between the interfaces of the two processors is the initial pin state of the I/O, where the slave-DSP pins are pulled high by default, whereas the PPC board pins are pulled low.

Initially, it was envisioned the controller would supply power to the hardware, via a combination of the dedicated 5 V supply rails. This is, why the module PCBs and current sensor PCBs were designed with a 5 V input. Subsequently, it was discovered all the supply rails had a combined supply current limit of 1.5 A. All the module PCBs and current sensors had a combined current demand of >3 A, making this configuration impossible, and necessitating the external LV power supply.

7.2.2. MICROLABBOX / DS1202

7.2.2.2. CONTROLLER SELECTION

Soon after the hardware interface between the DS1103 and the prototype MMC was functioning, the department made the decision to pursue purchasing a more contemporary dSPACE controller. This decision was partially motivated by the challenges faced by the author working with the existing DS1103 setup.

The selection of a new controller in terms of this project was governed by the quantity of interfaces required by the hardware. From a control setup perspective, one of the major limitations for MMCs that becomes increasingly prevalent as the number of switching levels increases is the quantity of I/O and ADC inputs required to interface with all of the modules and current sensors. For this application, 30 ADCs were required for battery voltage and current sensor measurement, 24 I/O pins were required for the PWM control of the modules, and an incremental encoder interface for the motor position sensor.

Initially, a focus was placed on using a scalable modular option that could be easily reconfigured. This is offered by dSPACE in the form of the SCALEXIO modular real-time system. Due to financial limitations imposed by the department, this option was abandoned due to the high base cost of the

card interface and processing unit. In addition to the low amount of analogue interfacing offered across the various available cards. Based on the hardware interfacing requirements and the financial limitations imposed, the MicroLabBox was deemed the most appropriate option. Given the high number of available ADCs (Table 7.2) and digital I/O. The only trade-off between the outdated DS1103 unit and the more contemporary MicroLabBox unit is the lack of a dedicated encoder interface. While the DS1103 connector board features several separate d-sub connector interfaces, the MicroLabBox only offers this for resolver interfaces. With the encoder interface part of a generic digital interface connector, lacking any dedicated sensor power supply pins, and requiring the generic interface pins to be configured within the Simulink model.

Table 7.2. Technical parameters of the MicroLabBox/ DS1202 [144]

Hardware Parameter		Specification
Processor	Real-time processor	NXP (Freescale) QorIQ P5020, dual-core 2 GHz
	Host communication co-processor	NXP (Freescale) QorIQ P1011 800 MHz for communication with host PC
Memory	I GB DRAM 128 MB flash memory	
Programmable FPGA	Xilinx Kintex-7 XC7K325T FPGA	
Analogue input	Resolution and type	8 14-bit channels, 10 Msps, differential; functionality: free running mode 24 16-bit channels. 1 Msps, differential; functionality: single conversion and burst conversion with different trigger and interrupt options
	Input voltage range	± 10 V
Analogue output	Resolution and type	16 16-bit channels, 1 Msps, settling time: 1 µs
	Output voltage range	± 10 V
Digital I/O	Number of channels	48 single-ended 12 bidirectional
	Output voltage levels	2.5/3.3/5
	I/O usage	Single-ended: bit I/O, PWM generation and measurement (10 ns resolution), pulse generation and measurement (10 ns resolution) Bidirectional: sensors with differential interfaces
Electric motor control I/O functionality	Separate interfaces	2 x Resolver interface 6 x Encoder sensor input 2 x Hall sensor input 2 x EnDat interface 2 x SSI interface
	Functionality on digital I/O channels	Synchronous multi-channel PWM Block computational PWM

Sensor supply	1 x 12 V, max. 3 W/250 mA (fixed) 1 x 2-20 V, max. 1 W/200 mA (variable)

7.2.2.3. HARDWARE INTERFACING

Rather than rewiring all of the connections between the MMC PCBs and the new dSPACE controller, the decision was made to instead make interfacing connectors between the existing connectors and the MicroLabBox connectors. This was to reduce the time dedicated to reconfiguring the converter and allow the converter to be easily reverted back to interfacing with the DS1103 if required.

The key difference between interfacing with the ADCs on the DS1103 and the MicroLabBox was the fact all the DS1103 interfaces share a common ground reference. Whereas, the MicroLabBox uses isolated ground references for each individual ADC. Because of this, an external grounding scheme for the 30 ADC connections was made to tie these connections to a common reference. This was to prevent the ADC measurement signals with a floating reference causing an incorrect measurement by the ADC.

The prototype MMC interfacing with the MicrolabBox is shown in Figure 7.2.

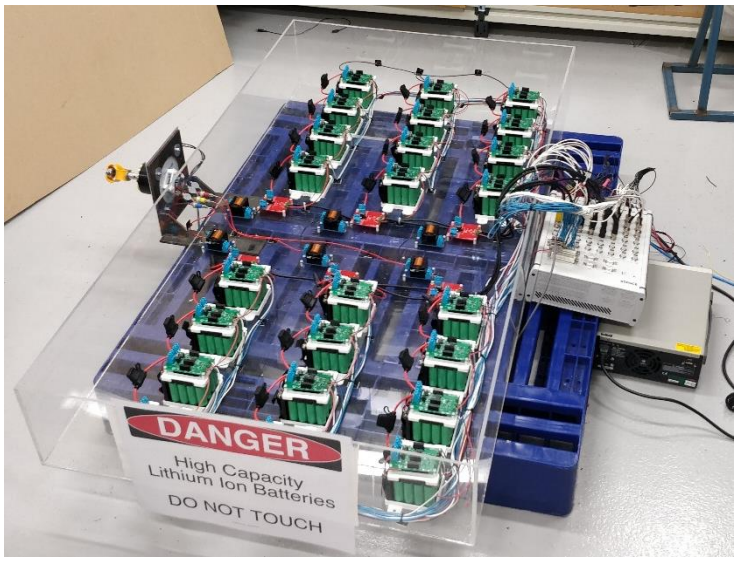


Figure 7.2. Final iteration of the MMC prototype and controller

7.3. SIMULINK MODEL OPTIMIZATION

As mentioned previously, the most widely used development platform for control algorithms for HiL controller hardware is the Simulink modeling software tool housed within the MATLAB computing environment. Simulink differs from many other electrical system simulation programs such as SPICE-based systems, who use circuit simulation processes, as it instead uses an equation solver process. This approach allows MATLAB to be used for wider simulation cases outside of purely electrical circuits, such as interfacing with digital or mechanical systems.

The limited processing power of the DS1103 proved a challenge while developing the model on the hardware, due to the model relying on a large amount of parallel processing. If the model was too computationally intensive for the hardware processor, the processor failed to meet the timing requirements of the hardware interrupts used to trigger the execution of the individual system blocks, leading to the model being inexecutable in real-time. To compensate for this, a high degree

of attention was paid to the execution timing/ operating frequency and the sequencing of calculations of the system blocks within the model.

During initial testing of the incremental encoder interface with the controller it was discovered the encoder was inaccurate at low speeds. Through research it was discovered this is characteristic of incremental encoders when sampled at high frequencies [145]. Being sampled at the operating frequency of the model (50 kHz) was excessive for something measuring in the order of hundreds of hertz. A triggered subsystem controlled by a continuous repeating sequence generator block configured with a sawtooth wave output was used to limit the sampling of the encoder input. This was later reconfigured as a discrete time signal, combined with the triggered subsystem control signals used for controlling the sampling of the ADCs.

Within the RTI1103 blockset (the interface between the DS1103 hardware and the Simulink model), there exists no option for selecting the sampling frequency of the ADCs. Because of this, they all sample at each time step within the simulation, meaning they would be sampling at 50 kHz, far above the frequency of the signals they are measuring. While acting as a considerable burden on the processor while operating, it also presents an issue for high frequency noise coupling with the signal lines on the input to the ADC pins. Initially, to counteract this a gain block with a limited sampling frequency was used to limit the operating frequency of the components servicing the ADC input. This configuration did little to reduce the computational loading of the controller, due to the model still sampling the ADC at 50 kHz. The same solution applied to the encoder interface was used to control the ADC sample rate, significantly reducing the computational loading of the model.

To minimize operation complexity from a base model level, the choice of model solver method was considered. The solver method is the mathematical technique used to solve ordinary differential equations for simulating continuous system states. Of the available fixed step-time solvers, the discrete method was found to execute the fastest. This was found by executing a Simulink model comprised of a sawtooth generator, and measuring the real-time taken to execute a single second of simulation time. An extremely fast fundamental step time of 10 ns was used to detect any slight variations in execution time. However, as shown in Table 7.3, the discrete solver method was significantly faster, while the other methods had near identical execution times. Implementation of the discrete solver method within the model could only be achieved by eliminating any model blocks relying on the solver method to interpolate a continuous state value. Within the existing model, the only blocks requiring this were the repeating sequence generators used to control the sampling of the encoder and the ADCs, and generation of the triangle wave shown in Figure 5.25 for determining the SVM output vectors.

Table 7.3. Execution times of sawtooth generator Simulink model with a step time of 10 ns and simulation time of 1 s for different solver methods

Solver Method	Execution time (s)
discrete	113
ode1 (Euler)	166
ode2 (Heun)	170
ode3 (Bogacki-Shampine)	170
ode4 (Runge-Kutta)	167
ode5 (Dormand-Prince)	168
ode8 (Dormand-Prince)	169
ode14x (extrapolation)	169
ode1be (Backward Euler)	168

The SOC estimation algorithm initially used an external lookup table block to generate the initial SOC on startup. In this configuration, despite only being used during the initialization process, the block was executing every execution cycle of the SOC-estimation subsystem. To prevent the SOC estimation for the 24 modules overtaxing the dSPACE processor and preventing the motor control scheme from executing, the lookup table was integrated directly into the SOC estimation algorithm (Appendix A). A linear-interpolation function was used to generate a continuous spectrum of values based on the discrete lookup table data points obtained from the datasheet. The execution time of the SOC-estimation algorithm was also varied to minimize the computational intensity of the system. While the voltage measurement was only being measured in the 10s of Hertz and the SOC itself viewed as non-oscillating components, the current limited the lowest allowable SOC-estimation execution time. Since the enhanced-Coulomb counter needed to track the current flow through the batteries, a sampling frequency in the order of hundreds of hertz was required.

While using the SVM generation script to validate the operation of the implemented SVM scheme, methods to optimize the operation of the embedded MATLAB function to maximize the required model fundamental step time were explored. As part of this, investigation into optimizing the operation through the selection of elements to feedback into the function over the course of a sampling period was considered. Initially, the value held by the control algorithm over the course of a sampling period was just the normalized terminal voltage reference value. This resulted in generating the upper and lower arm reference vectors, the required space vectors, and the switching dwell times, every operating cycle of the model. For comparison the control algorithm was reconfigured to feedback the switching vectors and the dwell times. This eliminated the need to generate the arm references and calculate the switching vectors and dwell times. However, this had no discernable effect on the operation of the algorithm and as such was reverted to the original configuration with only the sinusoidal reference value being fed back.

The Module switching selection algorithm discussed in Section 5.14, was initially setup such that in the latter stage of the original algorithm, the requested number of modules based on the PWM reference for the present iteration is compared with that of the previous iteration. If the PWM reference is still at the same level, the module selection will override itself and instead of using the selected modulus, will use the ones from the previous iteration. This is to prevent the modules from being switched in and out rapidly each model step (at most 50,000 times a second) when the module SOCs are extremely close to each other. This was restructured such that the selection scheme shown in Figure 5.29 is only executed once the SVM output level changes, and latches this value until the level shifts again.

7.4. SOFTWARE FILTERS

7.4.1. FILTER SIMULATION

While hardware filtering and hardware noise limiting techniques in the form of RC filters and shielded cables were used, noise on the input to the ADC pins of the controller persisted. A number of software based filtering options were explored: z-transform, discrete Laplace-transform filter based off IEEE Standard 421.5, DSP FIR Simulink LPF block, and a custom made moving average filter. The filter response of some of these is shown in Figure 7.3.

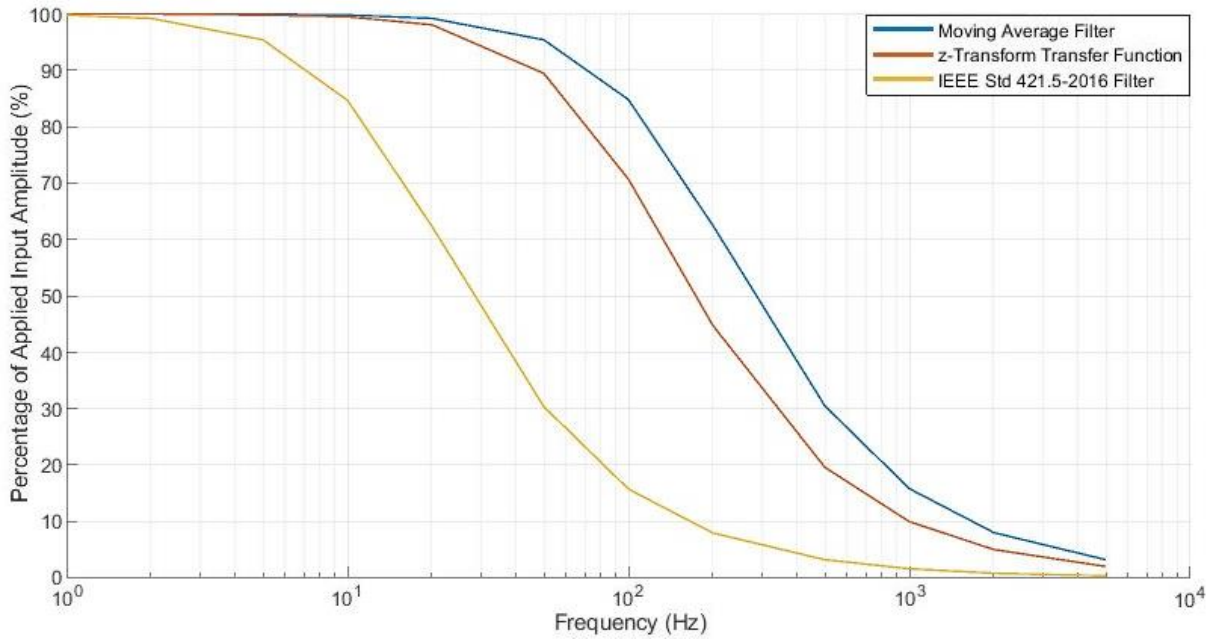


Figure 7.3. Response of discrete filters with designed cut-off frequency of 100 Hz

Based off the fact the discrete filter (IEEE Standard 421.5) gave a significantly different response than was intended, it was discarded from consideration within the mode. The z-transform based filter was selected for the filtering within the control system because of the faster roll-off response by the filter.

Further evaluation of the software filters was carried out, where the filtered response for a 50 Hz AC signal with coupled noise was considered (Figure 7.4).

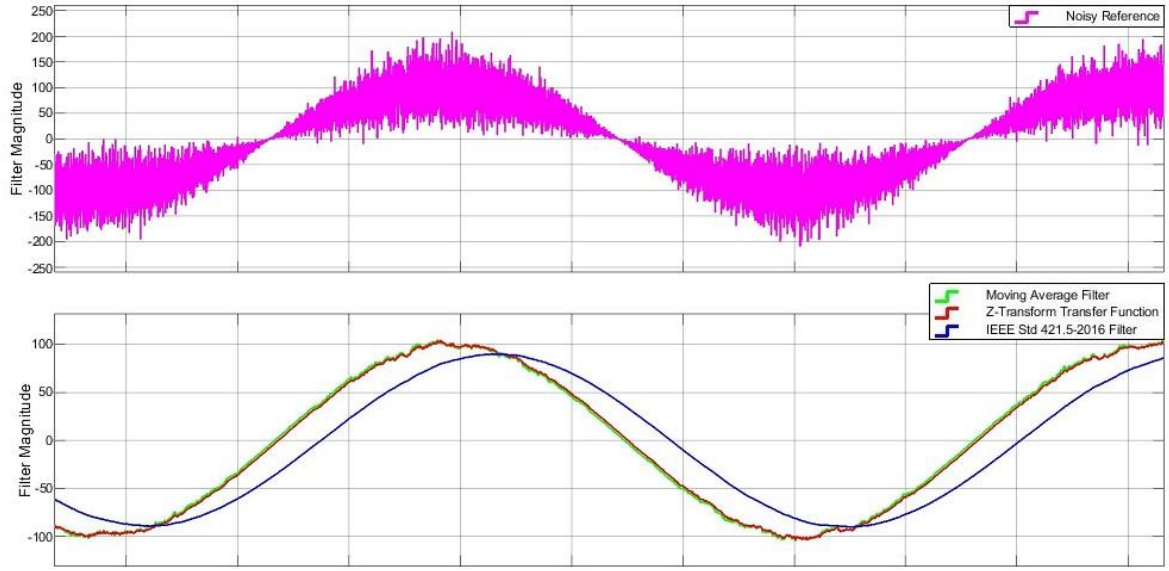


Figure 7.4. Response of discrete filters for 50 Hz sinusoid with noise coupling

While the IEEE Standard filter offered greater noise immunity, this was at the expense of a significant phase delay. This phase delay becomes significant when applied to the measured arm currents, used for the FOC, which can significantly reduce the performance of the feedback control

system. In comparison, both the moving average and z-transform based filters have a near identical response, although noise-coupling causes a noticeable ripple in the signal, the filtered signal is still in phase with the reference. To differentiate between the two, the computational intensity was compared by simulating the two filters with an extremely small fundamental step time (1e-7 s) and determining how long in real-time a second of simulation time took. Based off this, the z-Transform was found to be nearly three times faster in execution.

For further investigation of the suitability of the identified filtering options, a simulation model of the current sensor filtering hardware and transmission between the sensor and controller was created (Figure 7.5). Noise coupling with the sensor input to the circuit and noise coupling on the transmission line between the sensor circuit output and the controller filter was modelled.

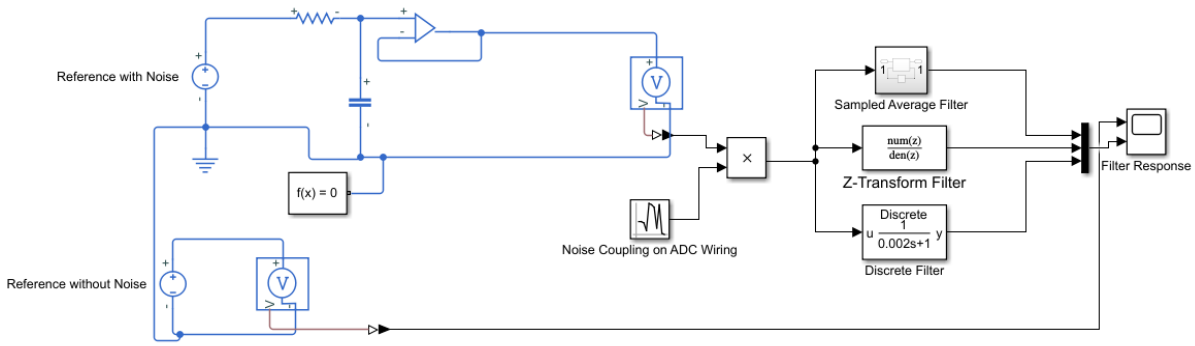


Figure 7.5. Simulation model of current sensor first-order RC filter interfacing with controller software filter with noise coupling on the reference input and transmission between sensor and controller

The response of the three filter options compared with the reference input to the sensor is shown in Figure 7.6. While the moving average filter and z-transform filters gave the same response when interfacing directly with a noisy reference input, their responses differ significantly when interfacing with the RC filter. The moving average filter in comparison with the z-transform introduces a significant phase lag, similar to the Laplace-transform filter.

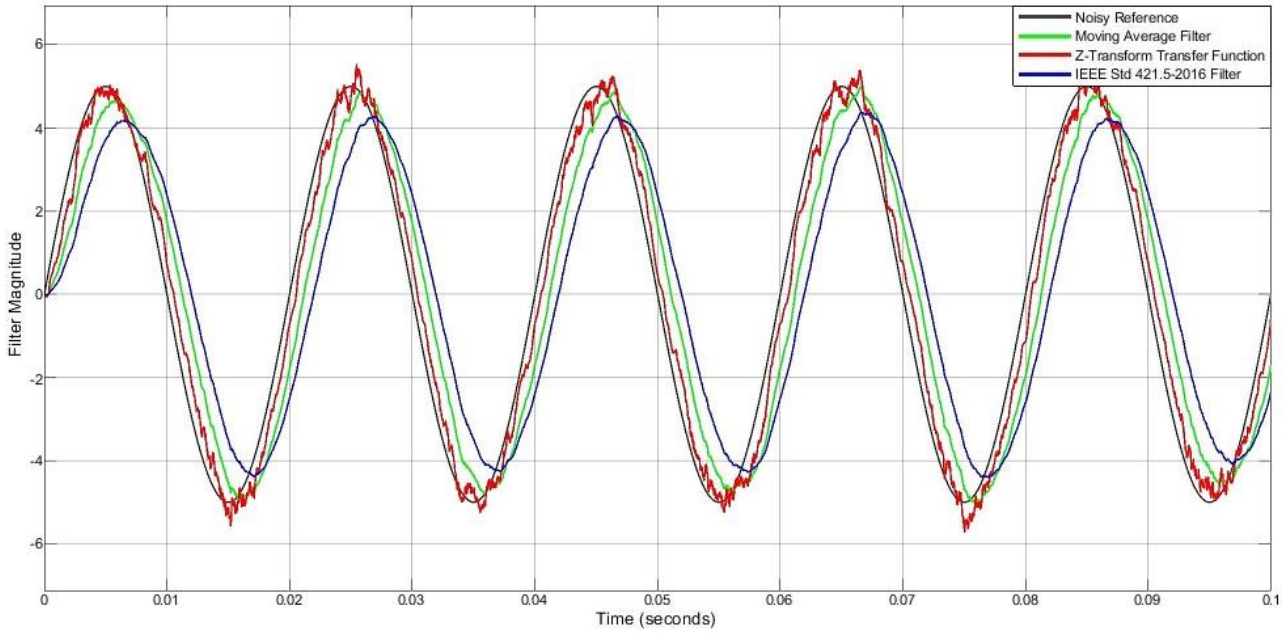


Figure 7.6. Response of software filters and the reference input with no noise

Based off all these factors, the z-transform based filter was deemed the most suitable for option for this application.

7.4.2. Filter Implementation

To test the current measurement process, the prototype was configured as a single arm module, arm current sensor, upper and lower arm inductors, and a fixed resistive load in a single loop. From this circuit arrangement, the current waveform shown in Figure 7.7 was obtained.

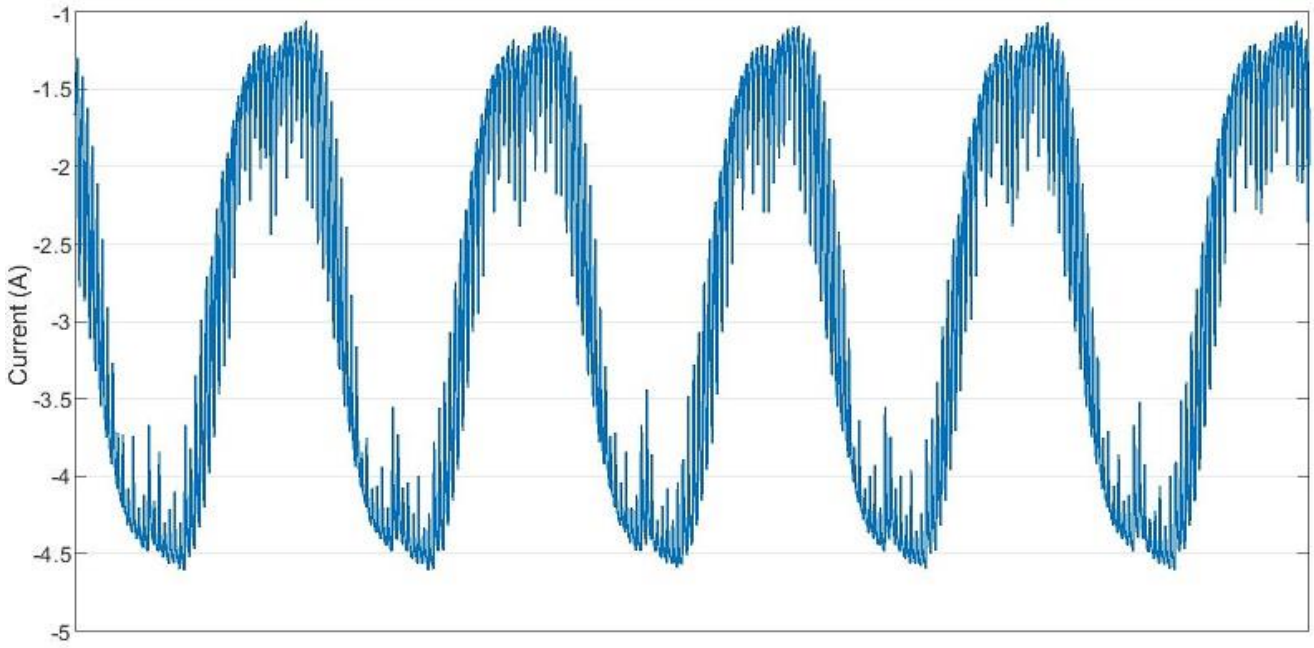


Figure 7.7. Test current waveform for analysing the current measurement process

The voltage output from the arm current sensor measured from the direct output of the sensor interfacing PCB is shown in Figure 7.8.

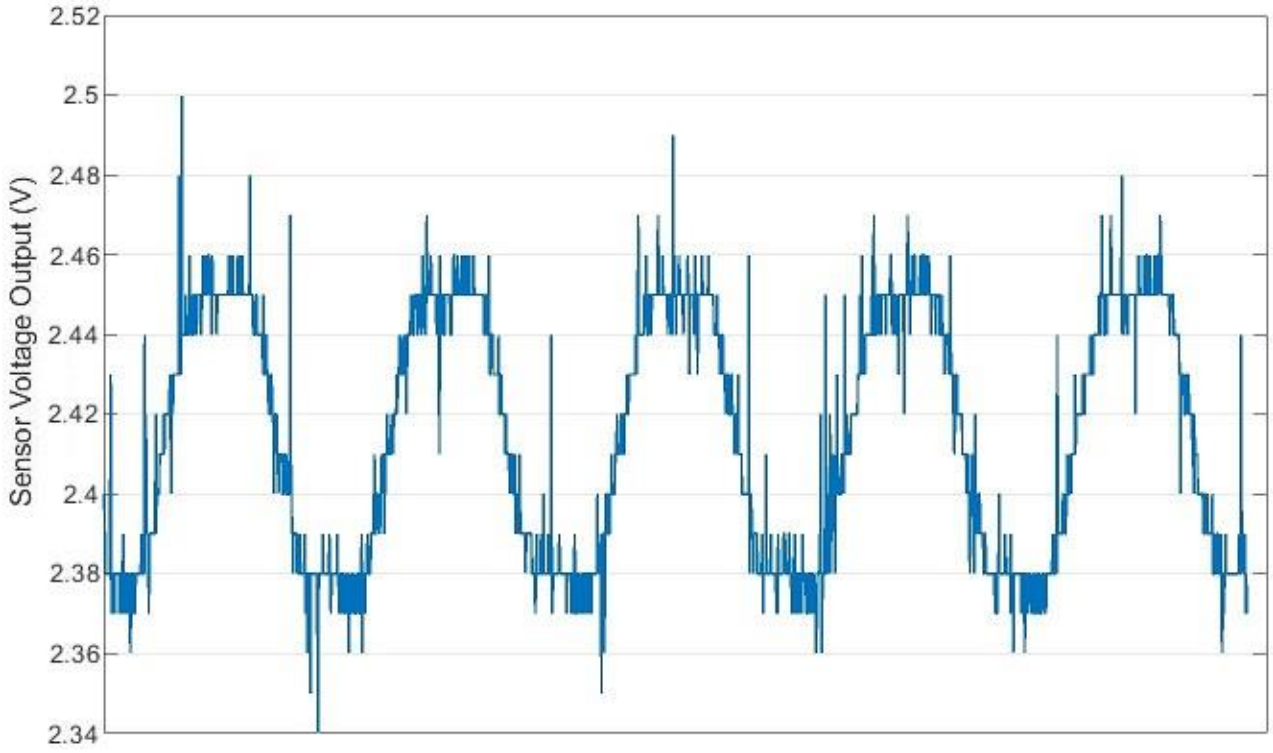


Figure 7.8. Voltage output of arm current sensor PCB

In terms of the current measured, the synthesised current measurement waveform is shown in Figure 7.9.

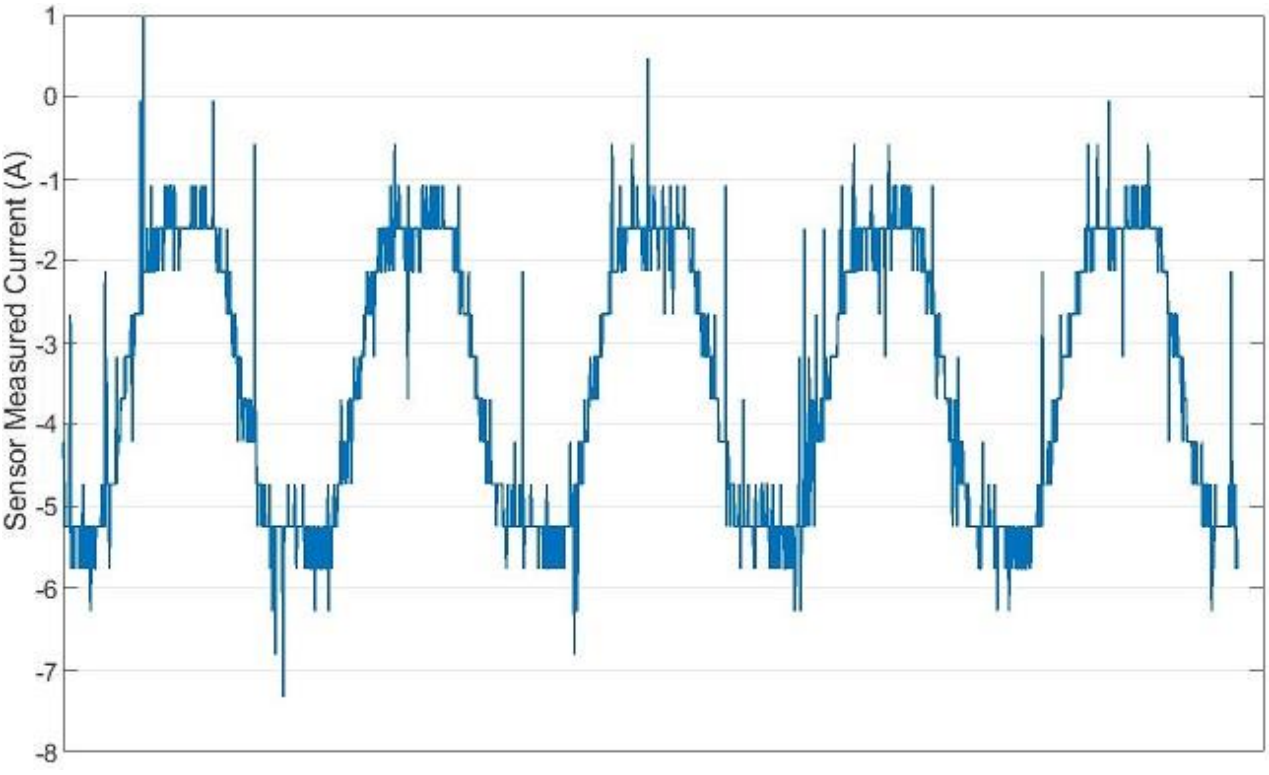


Figure 7.9. Current waveform measured using arm current sensor

The synthesised current without any form of software filtering is shown in Figure 7.10. For comparison, the same waveform with software based filtering is shown in Figure 7.11.

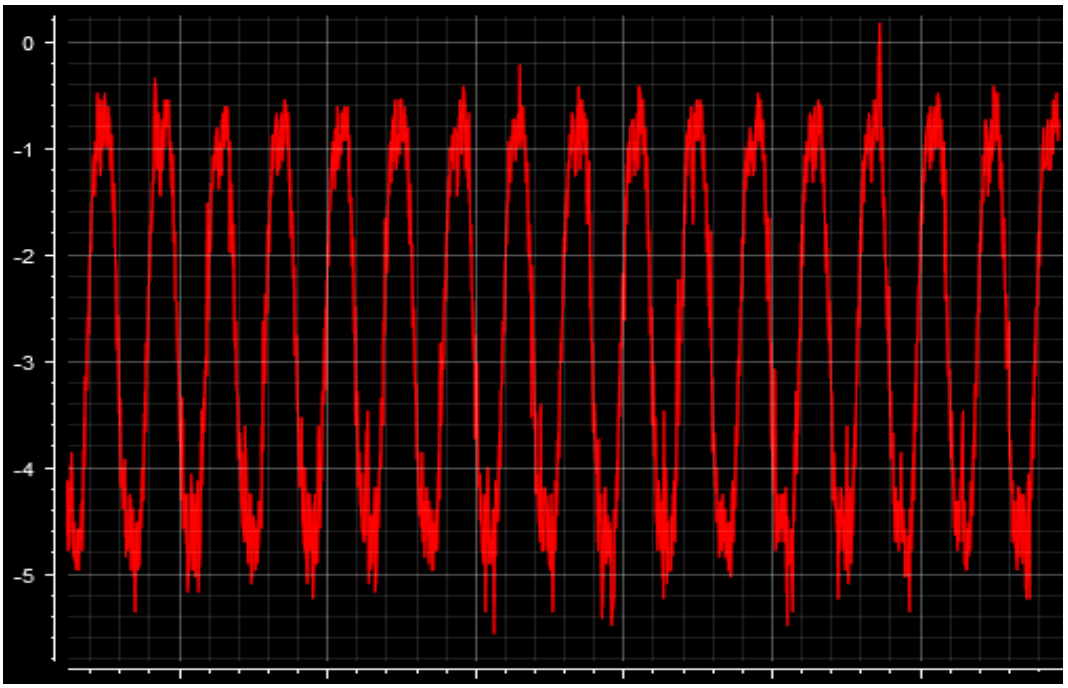


Figure 7.10. Synthesised current without software filtering

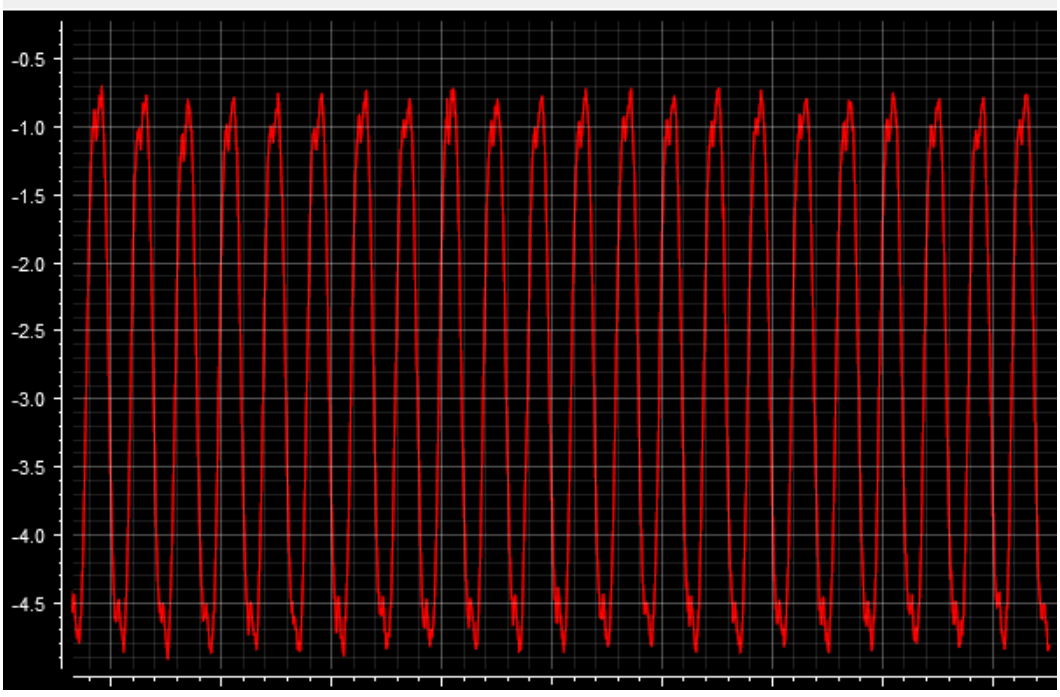


Figure 7.11. Synthesised current with z-transform based low pass filter

The filtered signal is less susceptible to the noise spikes introduced by the transmission line between the sensor and the ADC, while providing a smoother waveform transitioning between the waveform maxima and minima and reducing noise around these signal extremes.

7.5. CHAPTER SUMMARY

In this chapter the implementation of the control system within the Simulink modeling software and then the interfacing with the dSPACE controller.

Firstly, the Hardware in the Loop development technique and the role it plays in electric vehicle development is explored. The initial controller setup using the DS1103 and the difficulties encountered using this arrangement

During the course of the research, the decision was made by the department to purchase a contemporary controller. Based on the hardware requirements for the project, the MicroLabBox was purchased and the hardware interface between the developed hardware and the controller changed to suit this.

Developing the control scheme on the DS1103 proved challenging due to the limited processing power and the large quantity of parallel processing required by the control system. To compensate for this, steps were taken to optimize the execution times of system blocks, such as the space vector modulation generator, ADC sampling, encoder interfacing, and SOC-estimation.

Finally, the development of software based filtering to accompany the already implanted hardware filter is explored. This involved simulation of the filter response for varying input frequencies and analyzing the response to a noise-coupled 50 Hz sinusoid. Based off this a z-transform based filter was selected as the most appropriate filtering option for this application. The effect of this filter was then verified using an isolated section of the prototype using the interface between the developed hardware and the controller.

CHAPTER 8 SIMULATION AND EXPERIMENTAL RESULTS

This chapter describes the operating characteristics of the proposed MMC with embedded batteries through the use of simulation and on the developed physical prototype. The simulation includes results obtained using both static and dynamic loads of an inductive nature. This chapter also includes a study of the effectiveness of the developed SOC-balancing scheme and FOC scheme.

Since the project from its inception was focused on the design of an embedded battery MMC prototype, all simulation was focused on design and validation of the designed hardware. This approach was taken rather than evaluating the validity of the proposed operating principle for specific EV applications. The approach taken means the simulated hardware was not changed to be analogous with contemporary EV powertrains or changed to suit required operation profiles, but was fixed to model the designed hardware.

The battery model used in simulation was the model based off the Energus 1s8p brick discussed in Section 3.4.1. For the purposes of simulation, the battery capacity of each module battery was reduced from 20 Ah to 0.6 Ah to speed up simulation times and prevent the simulation running out of memory. A summary of the simulation parameters for the batteries is provided below in Table 8.1. For verifying the capability of the SOC balancing, the simulation begins with the cells at differing SOCs ranging between 80 % and 100 %, with the exact SOC for each module being randomly selected. The exact SOCs used for modeling and corresponding statistics are provided in Appendix G.

Table 8.1. Battery parameters used for Li-ion battery model

E_0 (V)	R (mΩ)	K (V/Ah)	A (A)	B (Ah^{-1})	Q (Ah)
4.0458	2.7	0.000097	0.20822	3	0.6

8.1. MODULE BATTERY SOC BALANCING SIMULATION

The module SOC balancing scheme was evaluated through simulation for three separate loading cases: no-load, a static RL-load, and a PMSM (dynamic load). This was to test the versatility of the developed control algorithm for a variety of load conditions. The proportional and integral control gains used for the arm and leg SOC controllers remained constant across all three loading conditions, and are shown in Table 8.2. Saturation on the output of the controller is used to limit the effect the control output has on the terminal voltage output of the FOC/ reference sinusoid, to prevent the balancing control from dominating the voltage control.

Table 8.2. SOC balancing controller gains with respective output saturation

Controller Gain	Gain Value	Saturation
Arm Proportional, K_P	10	± 0.15
Arm Integral, K_I	0	± 0.15
Leg SOC Proportional, K_P	1.4	None
Leg SOC Integral, K_I	0.056	None
Leg Circulating Current Proportional, K_P	1.44	1.68
Leg Circulating Current Integral, K_I	1.8	1.68

8.1.1. NO-LOAD SOC BALANCING

With no load applied between the three-phase output, no overall leg current is observed. However, an identical current flow (as opposed to being symmetric under load conditions) through the upper and lower arms of the respective legs exists (Figure 8.1).

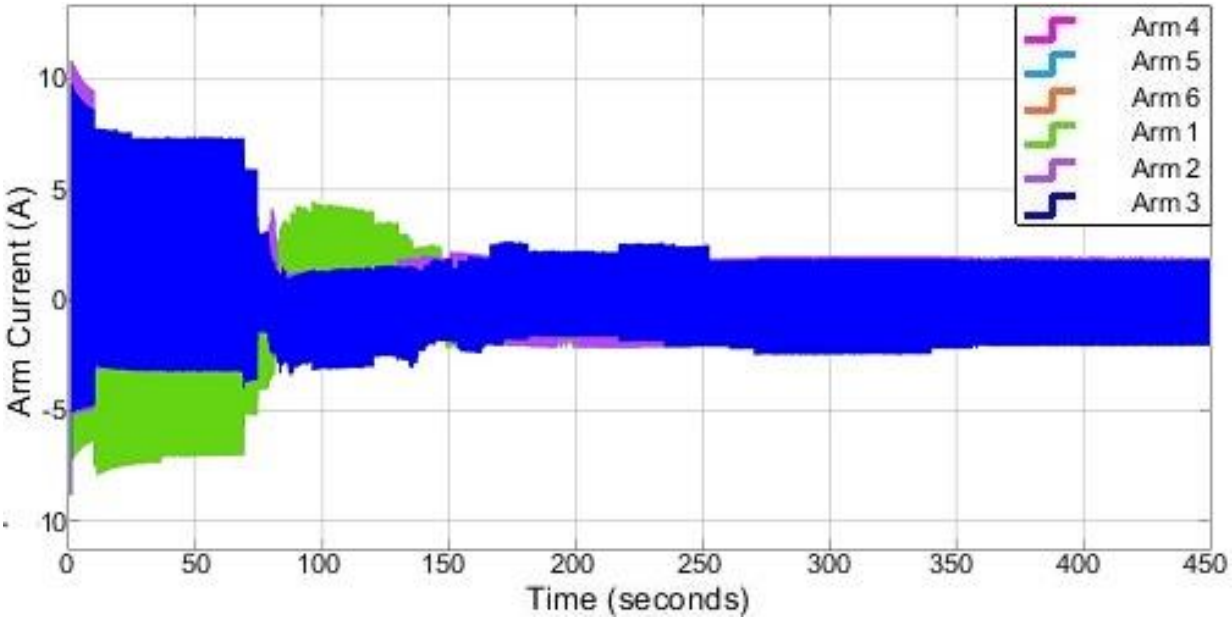


Figure 8.1. Arm currents under no-load conditions

This current is solely the circulating current flowing between each leg. Applying SOC-balancing control while operating the MMC under no-load conditions balances the upper and lower arm SOCs quickly, while the modules within the arms and the leg SOCs take significantly longer to balance. With no load discharging the cells, the arms at a lower average SOC will begin to charge (Figure 8.2). The lack of load current component flow causes the module selection scheme to struggle to balance the individual modules once the circulating current RMS component has been minimized (Figure 8.3).

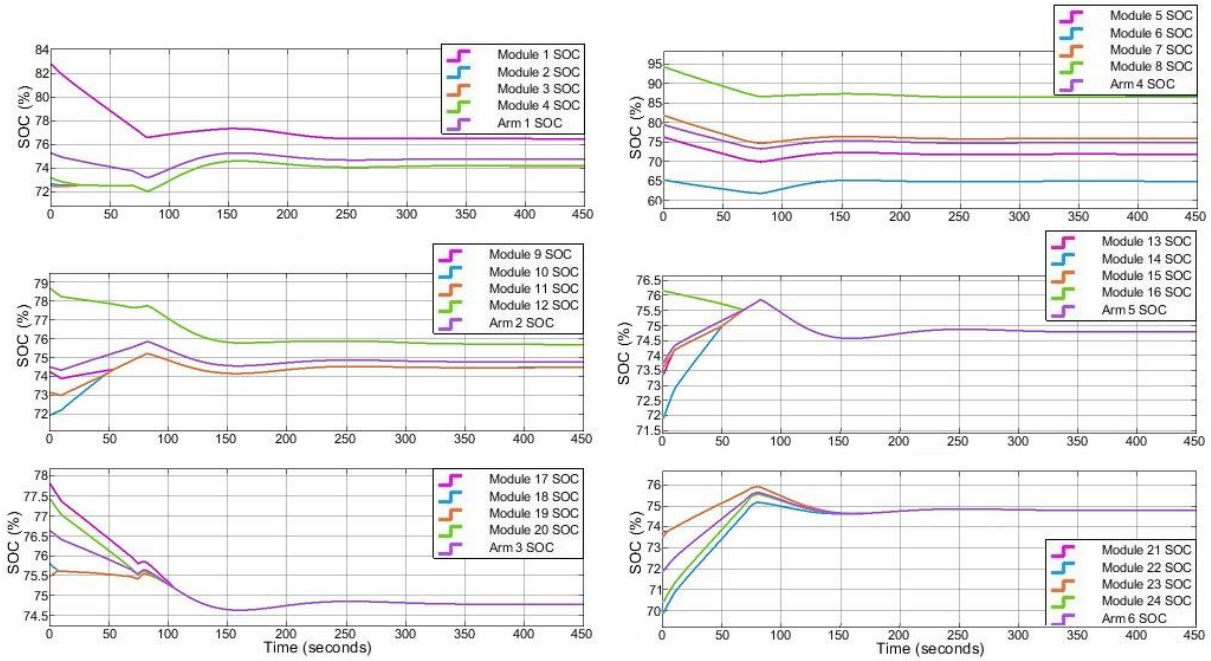


Figure 8.2. SOC of modules within respective arms under no-load conditions

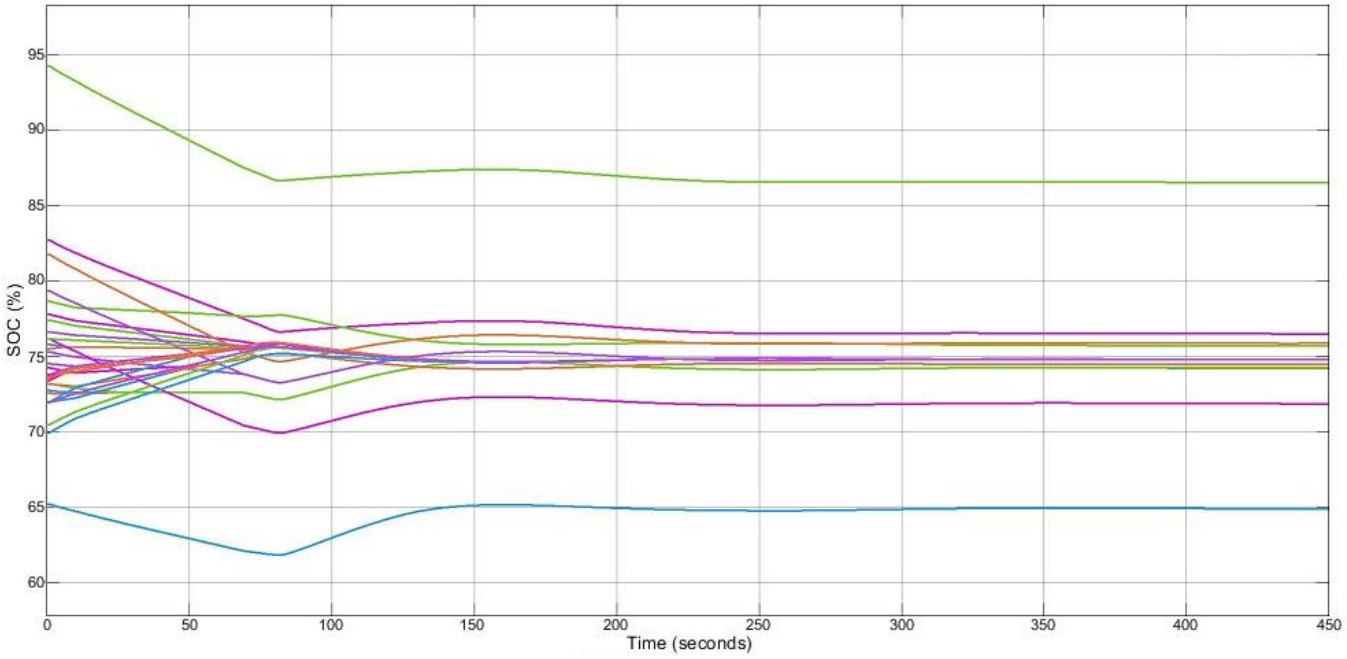


Figure 8.3. SOC of module batteries under no-load conditions

8.1.2. Static RL-load SOC Balancing

The static RL-load was configured in a delta configuration for the simulation, since the stator of the motor selected shared the same winding sequence.

To remove the influence of the FOC on the control sinusoids used for MMC switching, the SOC-balancing was simulated using an RL-load with a fixed amplitude and frequency sinusoid as the reference. With the only manipulation of the reference sinusoid being the arm controller scaling and the leg control shift.

As shown in Figure 8.4, the individual module batteries are all successfully balanced to the same SOC after approximately 130 seconds. With the addition of a load current, the control algorithm is able to successfully balance the module batteries. Whereas under no-load conditions the controller was unsuccessful.

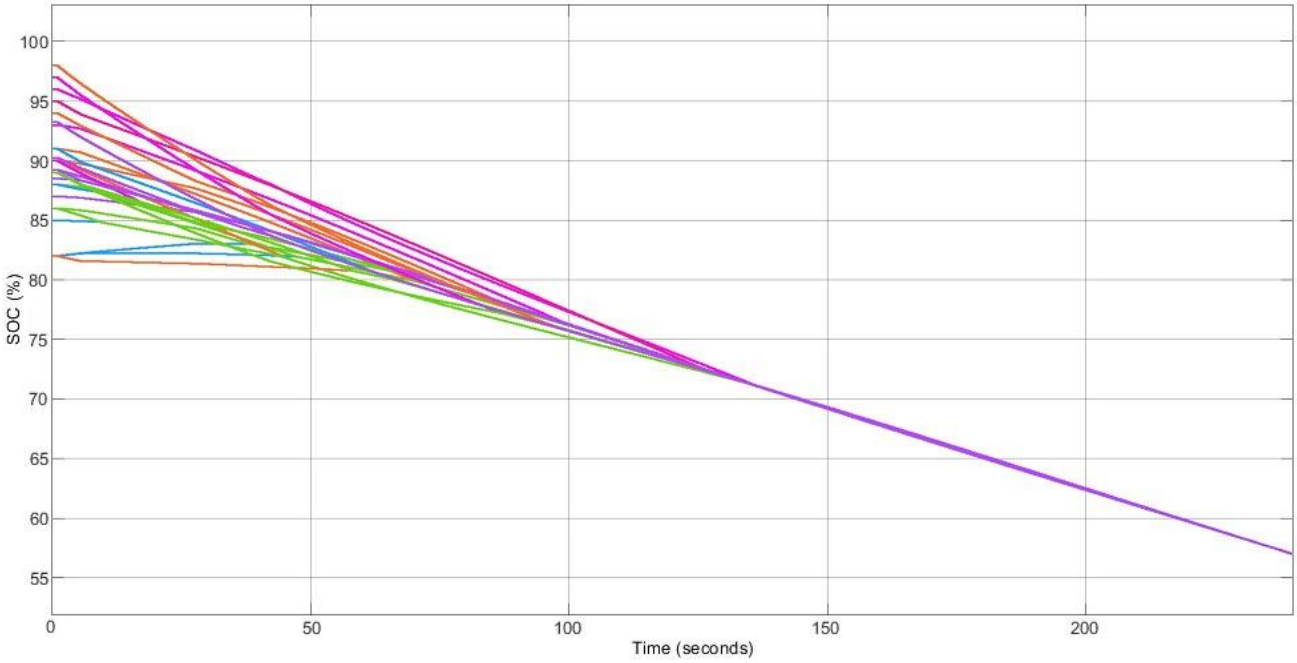
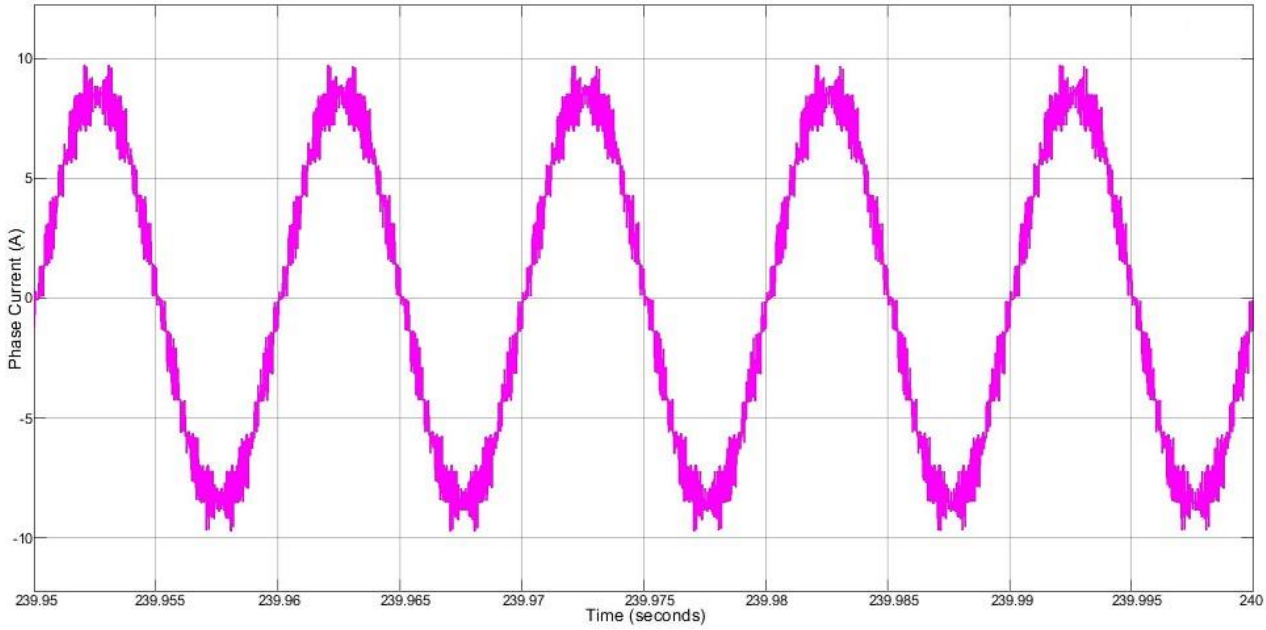


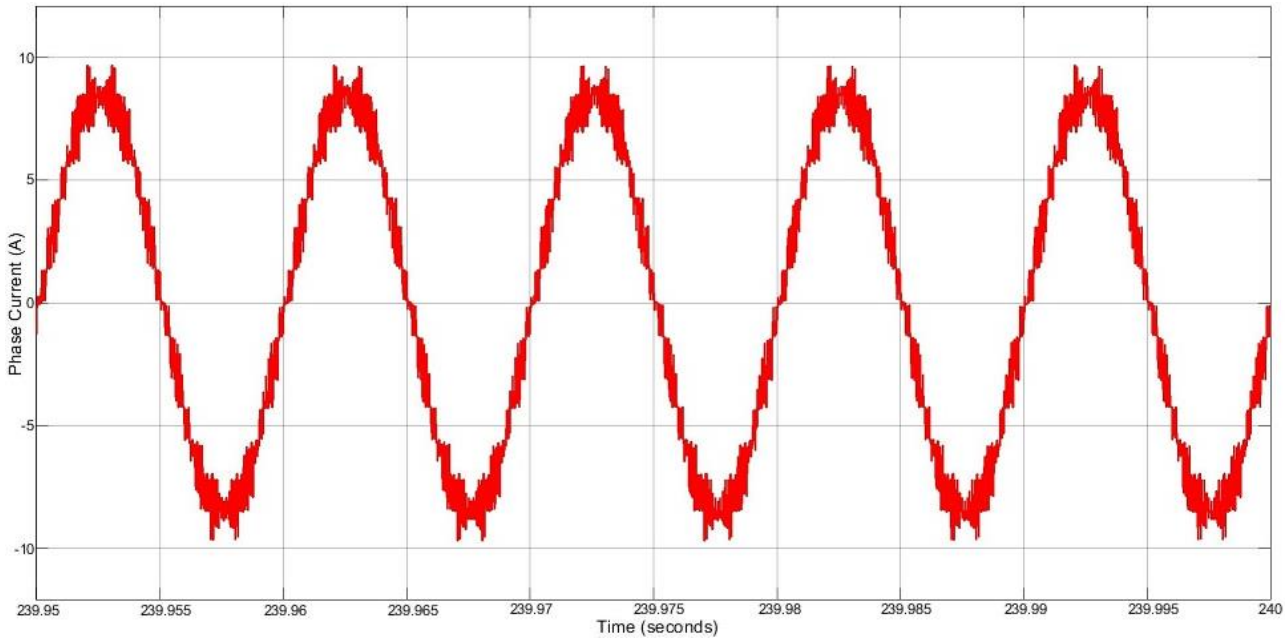
Figure 8.4. SOC of each module battery over the course of discharge through a static RL-load

During the initial stages of the discharge cycle, the modules at a higher SOC are switched in more often, and thus are discharged at a higher rate. Meanwhile, the modules at lower SOCs are switched in less often and are discharged at a lower rate than other modules, or are charged until they are balanced with the rest of the arm modules. Under no-load conditions, the modules at lower SOCs are charged more significantly than under load conditions, due to the lower SOC modules acting as an internal load within the converter, as opposed to acting as a mixture of an internal load and energy source to the external load.

The arm currents are comprised of a load current and a circulating current component. The SOC balancing control leaves the load current component unaffected, and controls the circulating current to balance the upper and lower arm SOCs and the leg SOCs. The independence of the load/phase current and the circulating current is demonstrated in Figure 8.5.



(a)



(b)

Figure 8.5. (a) The actual phase current synthesised from arm current signals (b) Phase current constructed from arm current signals with the calculated circulating current component removed

The arm currents are unbalanced on startup of the converter, because of the circulating currents coupling with the load current (and this owning to the imposed initial SOC imbalance). The DC component of the circulating current causes a DC offset within the arm current, and the harmonic component is observed as distortion in the load current.

8.1.3. PMSM SOC BALANCING SIMULATION

The proposed converter has been simulated as the motor controller for a PMSM. Both the star- and delta-wound PMSM models were used for evaluation of the FOC and SOC balancing scheme working

in conjunction. For the simulation of the SOC-balancing algorithm, the star-wound PMSM model was used, for reasons discussed in Section 5.2.4.

The SOCs of the module batteries during operation of the PMSM are shown in Figure 8.6.

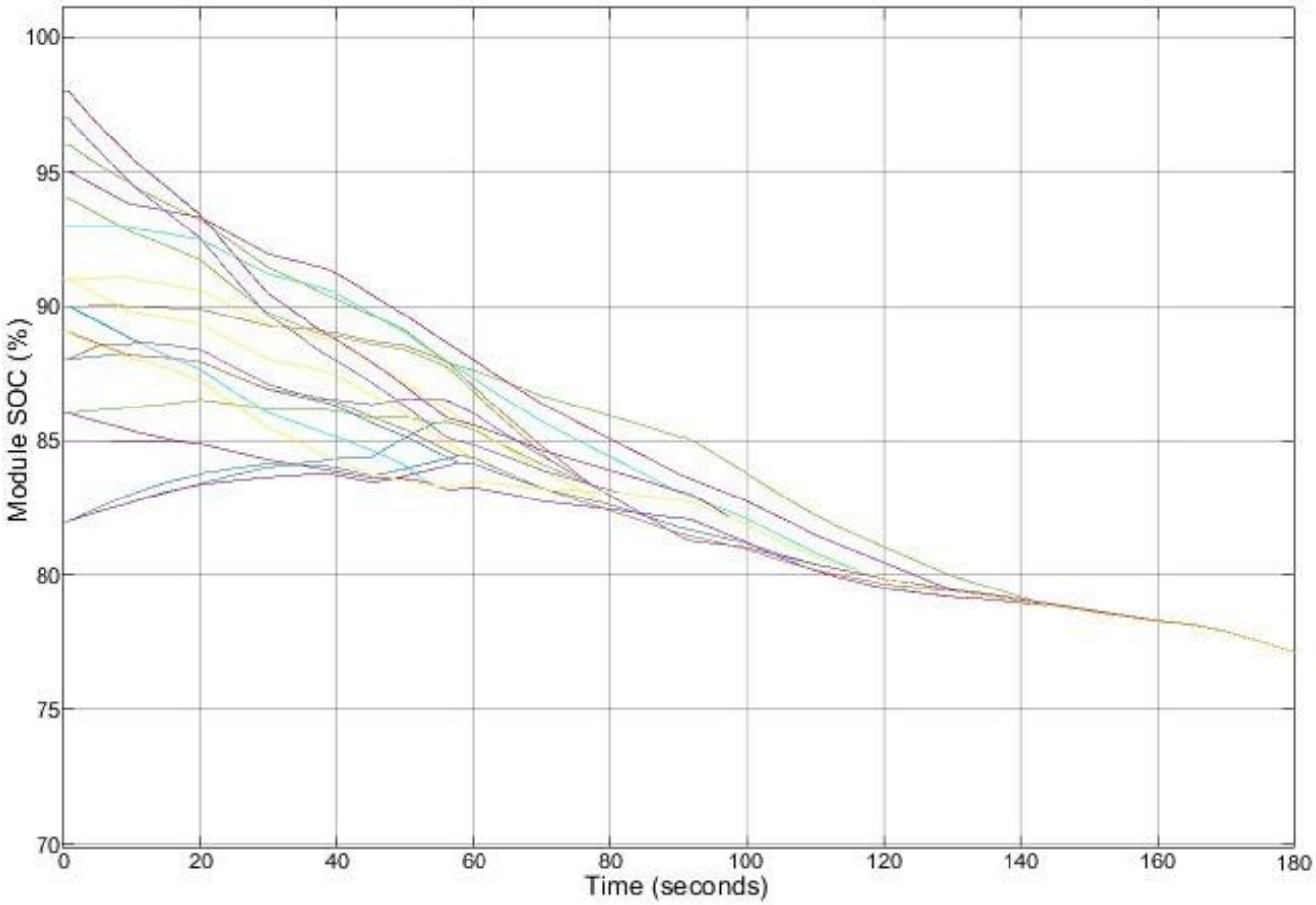


Figure 8.6. Module Battery SOCs during discharge with PMSM load with varying speed and torque operation

Balancing using a PMSM load is slower in comparison with the static RL-load and less smooth, because of the influence of the FOC terminal voltage control. The static RL-load used a fixed amplitude/frequency reference input to the balancing algorithm for the controller response shown in Figure 8.4. Whereas the response in Figure 8.6 has a varying reference signal amplitude as a result of the influence of the FOC, and a varying frequency as a result of the speed controller.

8.2. MOTOR SPEED CONTROL

Through simulation in Simulink, performance of both a star-wound and delta-wound stator PMSM was considered for evaluation of the FOC control scheme. The same controller gains and setup was used for both motor stator-winding configurations, these gains are provided in Table 8.3.

Table 8.3. Motor control gains with respective controller output saturation

Controller Gain	Gain Value	Saturation
Speed Control Proportional, K_P	0.6	± 20
Speed Control Integral, K_I	1.75	± 20
FOC Direct Proportional, K_P	0.1	± 33.6

FOC Direct Integral, K_I	0.32	± 33.6
FOC Quadrature Proportional, K_P	0.1	± 33.6
FOC Quadrature Integral, K_I	0.32	± 33.6

The response of the speed control for a varying target speed input with a changing torque load for both stator configurations is shown in Figure 8.7.

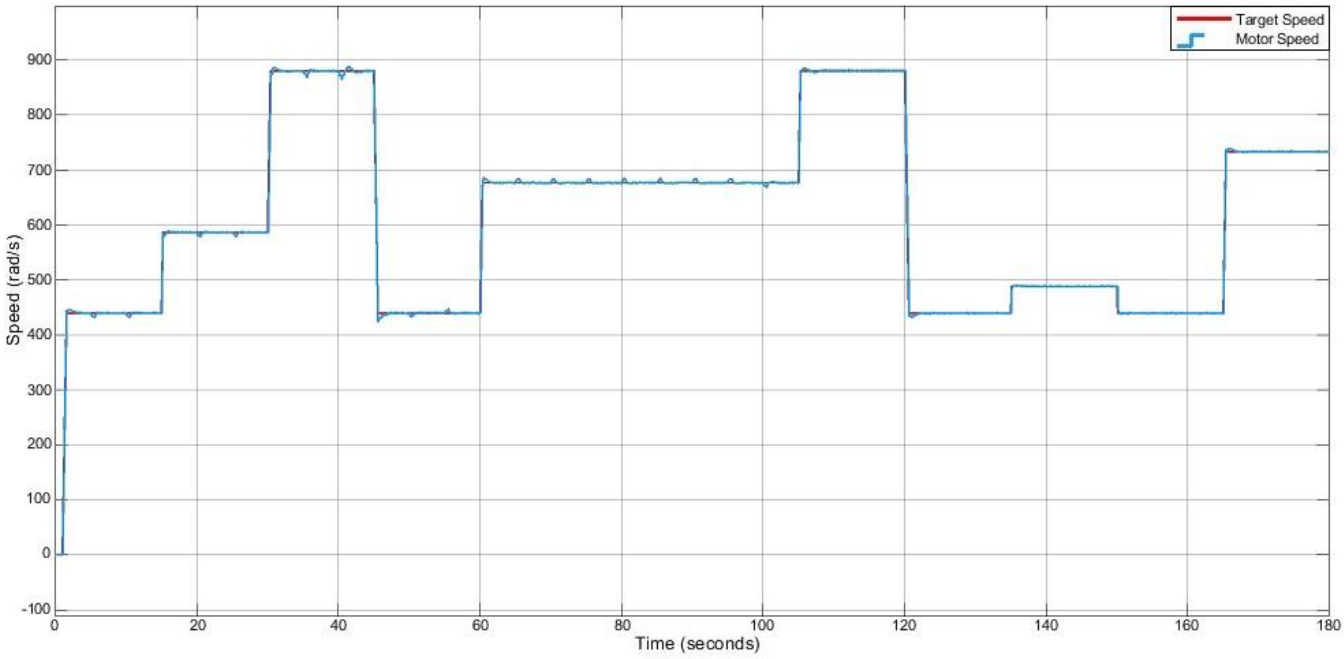


Figure 8.7. Speed Control of PMSM speed for arbitrary speed set points

The speed controller output and the applied motor torque load for the delta-winding configuration PMSM are shown in Figure 8.8.

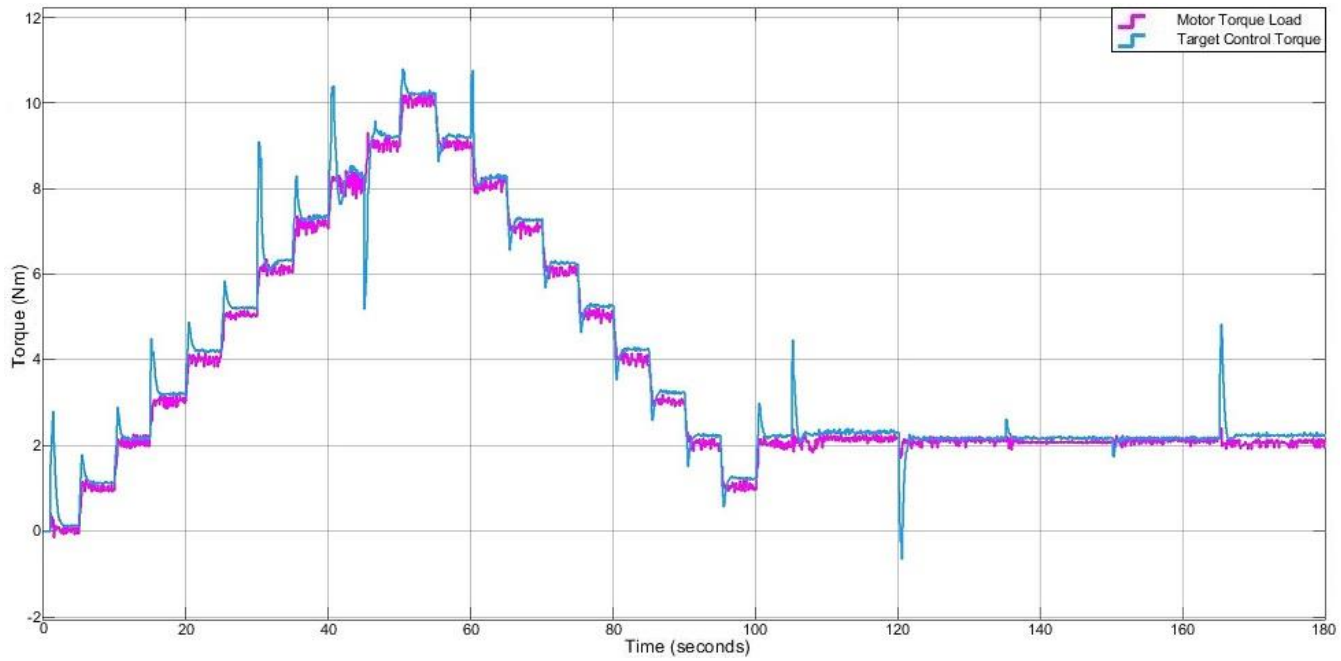


Figure 8.8. Speed controller torque output and torque load on PMSM

The scheme was simulated using Gaussian white noise with a signal to noise ratio of 10 dB injected into the current measurement signals with no filtering to test the robustness of the scheme, in particular the schemes ability to maintain control of the motor despite poor feedback quality. Noise coupling affects the calculation of the circulating current, which presents an issue for the leg SOC-balancing scheme by creating a non-DC feedback current for the circulating current control. This leads to the controller taking longer to balance the leg SOCs.

In the presence of significant noise, the motor speed struggles to converge with the target speed. The torque ripple on the motor and the target torque of the speed controller output both increase significantly.

This increase in target torque output can couple into the FOC terminal voltage output, which can further affect the SOC-balancing algorithm by introducing significant voltage spikes, overpowering the SOC-controller signals.

8.3. TOTAL HARMONIC DISTORTION OF PHASE CURRENT SIMULATION

One of the many advantages of multilevel converter topologies over 2-level converters over a range of applications is the reduced levels of THD without the use of additional LC filters for high power applications. The THD of the phase current over a wide speed range (wide reference frequency input range for the static load) and over a wide torque/ phase current range was investigated for both static and dynamic loads. As mentioned before, the circulating current is not present within the phase current, so the effect of battery balancing on the THD was not explored. However, the imbalance in module SOCs will have an impact on the phase voltage output, and thus the THD of the phase voltage.

8.3.1. STATIC RL-LOAD THD SIMULATION

With a static RL-load, the THD of the leg current over a wide reference frequency input range and wide load current range are shown in Figure 8.9 and Figure 8.10 respectively.

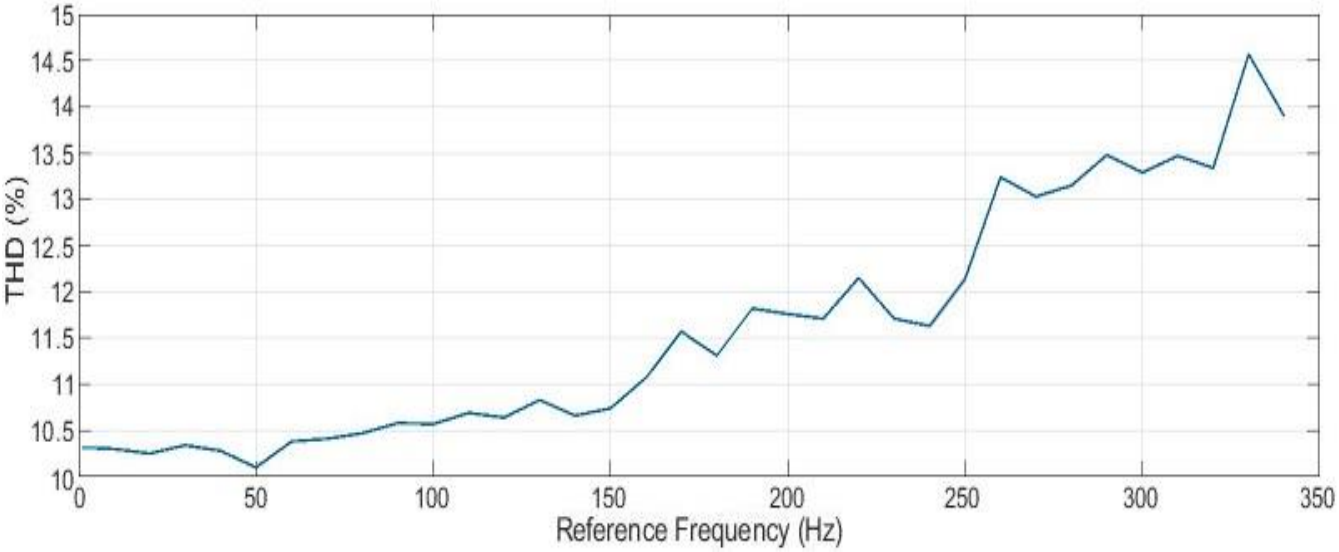


Figure 8.9. THD of phase current with varying frequency of reference SPWM sinusoid

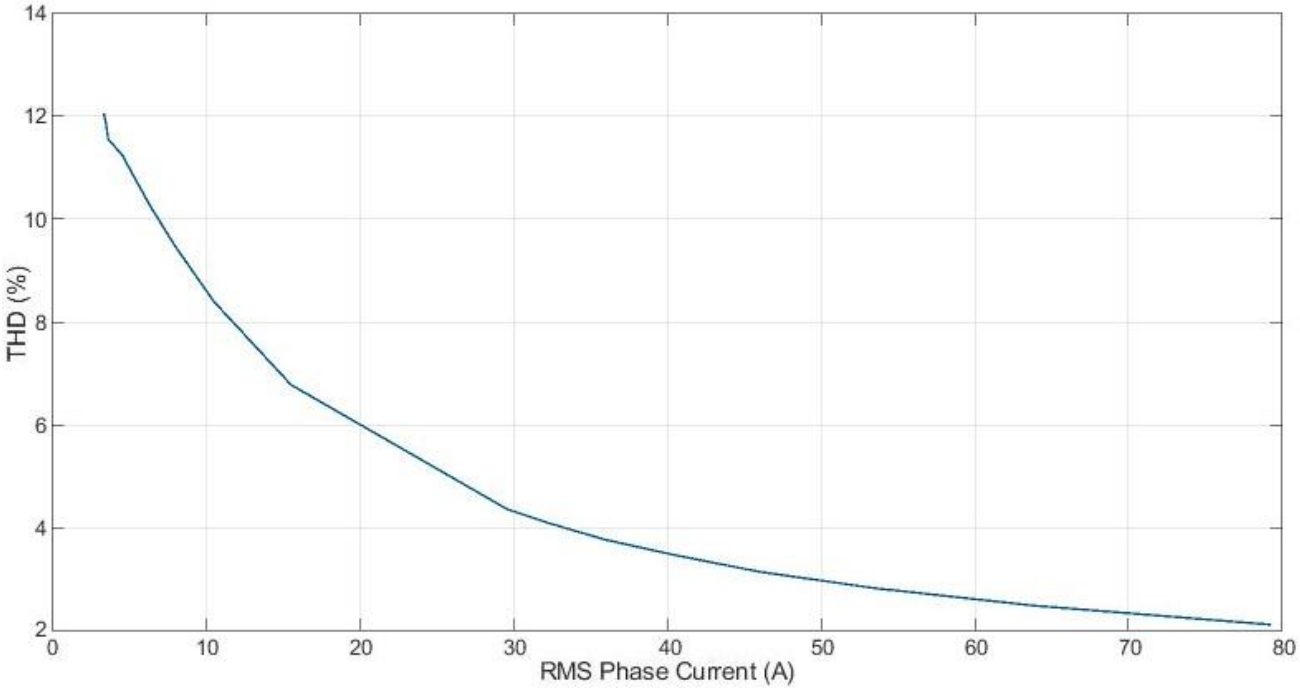


Figure 8.10. THD of phase current with varying phase current (varying load)

The THD of the load current decreases significantly with increasing load current, whereas with increasing the reference frequency does increase the THD, however, this increase is minimal over a wide frequency range.

8.3.2. PMSM THD SIMULATION

The PMSM was modeled with a ramping target speed and with a ramping torque load to evaluate the THD over the operating range of the motor.

As shown in Figure 8.11, the THD remains fairly constant at low reference frequencies/ operating speeds but does increase significantly while operating at the high end of the operating speed range (> 20,000 RPM). In terms of the torque input/ phase current, the THD decreases significantly as the load increases (as shown in Figure 8.12).

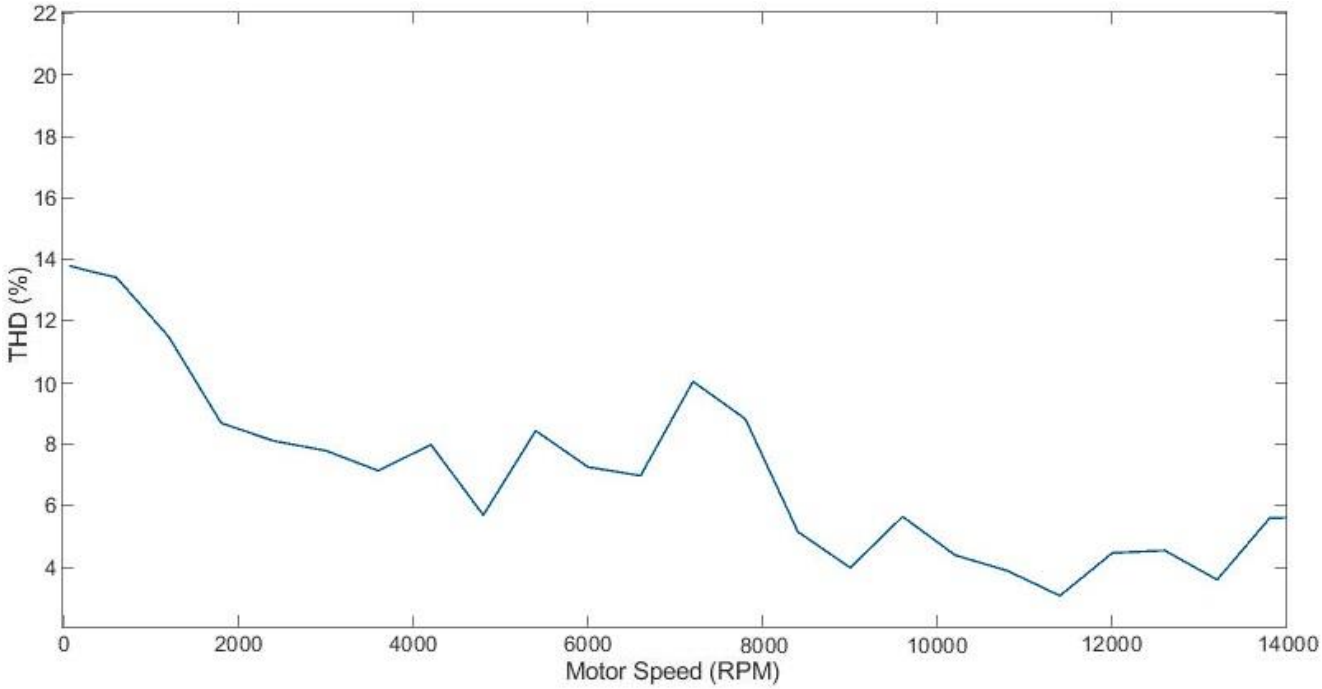


Figure 8.11. THD of phase current over wide motor operating speed range

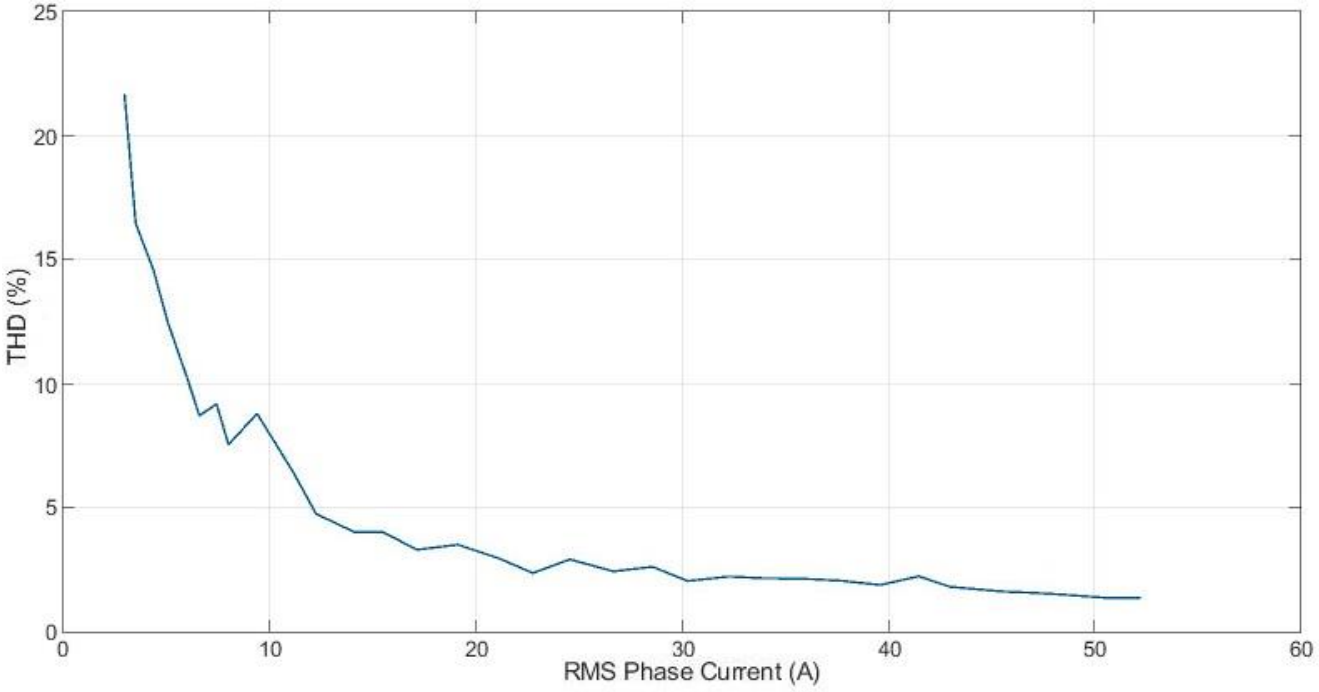


Figure 8.12. THD of phase current with increasing torque loading on PMSM

The response for the increase in load current/ applied torque load between the static and dynamic loads both follow an inverse square relation. Whereas in comparison the THD response with variation in the frequency of the control sinusoid have opposing trends. Where the THD increased as the reference frequency increased for the static load, and decreased for the PMSM load. In addition, the variation in THD for the static load was minimal in comparison with the change as a result of phase current variation. With the dynamic load, the change in THD was in the same level of magnitude as the response from changing torque load.

8.3.3. EFFICIENCY

Traditionally, the operating efficiency of an inverter is simply evaluated by measuring the power input from an external power supply into the inverter and measuring the power output from the inverter, and determining the power losses through the DC to AC conversion. In comparison, the embedded battery MMC lacks a single power input, with each individual module acting as a power source at any given moment. This means, the individual losses for the individual loss generating components need to be summated to determine the operating efficiency for a point in time, as opposed to using a black-box modelling approach.

Due to the large number of switching devices in series and parallel, the overwhelming majority of losses within a MMC are as a result of switch conduction and switching losses [8]. However, the ability to use low voltage, low resistance MOSFETs with low switching losses, and general operation at low frequency switching, offsets this increase in sources of losses. The other sources of losses within the MMC include the arm buffer inductors, module batteries, and wiring.

For determining converter losses, [8] has developed a method of determining the MOSFET conduction and switching losses, while ignoring the other sources of losses. However, this method is highly dependent on the PWM scheme used. To use this evaluation method for this research, a modified method using the developed SVM scheme would need to be created. Due to time constraints on the completion of this research, a new model was not synthesized nor validated.

8.4. EXPERIMENTAL RESULTS WITH STATIC RL-LOAD

The developed MMC prototype was operated with a static resistive and inductive load to verify the effectiveness of the SOC balancing and the operation of the prototype with varying reference frequency and load current.

8.4.1. DISCHARGING USING STATIC RL-LOAD

For this experiment, the converter was controlled using SPWM with a 5 kHz switching frequency. Table 8.4 summarizes the circuit and control parameters used for the static RL-load discharge experiment.

Table 8.4. Circuit and control parameters for static RL-load experiment

Load phase-phase Resistance	2.9 Ω
Load phase-phase Inductance	11.5 µH
Nominal phase-phase RMS voltage	20 V
Reference Frequency	50 Hz
Arm Inductor	33 µH
Nominal module battery capacity	20 Ah
Nominal module battery voltage	7.2 V
Switching frequency	5 kHz
Number of modules per arm	4

Demonstration of the successful operation of the SOC balancing algorithm was achieved by charging the 24 module batteries to different SOC values with a SOC range of 20%, the same range used for the simulation. With the designed controller, the SOCs of the module batteries converge toward a common charge level and are successfully balanced after approximately 1500 seconds (25 minutes).

The experiment ran for several minutes after the modules were successfully balanced to ensure the balanced SOC was maintained and did not subsequently destabilize, shown in Figure 8.13.

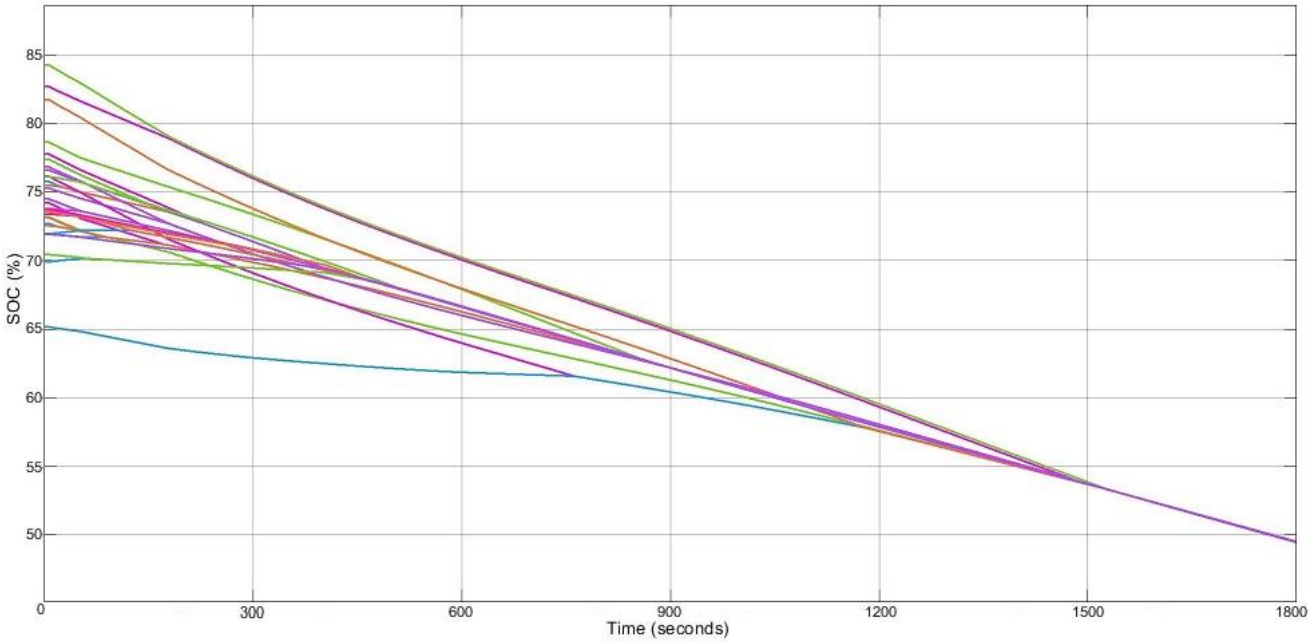


Figure 8.13. Module SOCs over course of discharge test using the prototype MMC with a Static RL-Load

8.4.2. Prototype operating range with Static RL-Load

The THD of the prototype while operating with a static RL-Load was investigated to validate the operation shown through the simulation model. The MMC phase current THD for varying frequency and load current are shown in Figure 8.14 and Figure 8.15 respectively.

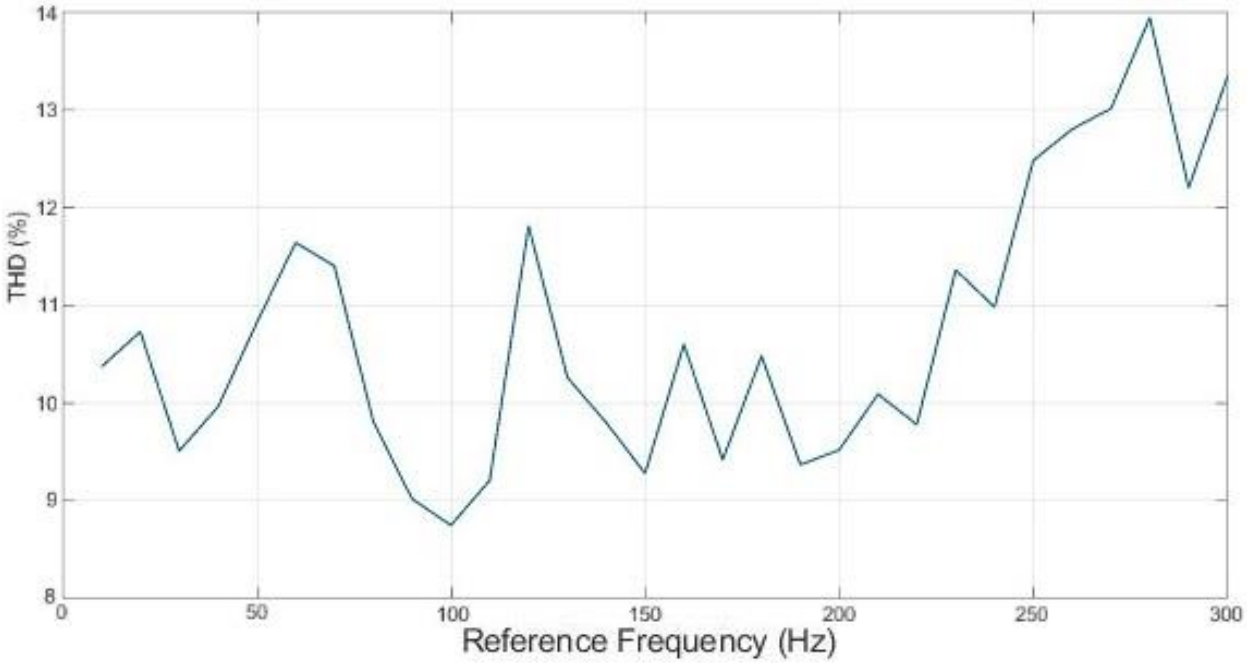


Figure 8.14. THD of prototype MMC with varying frequency of reference input

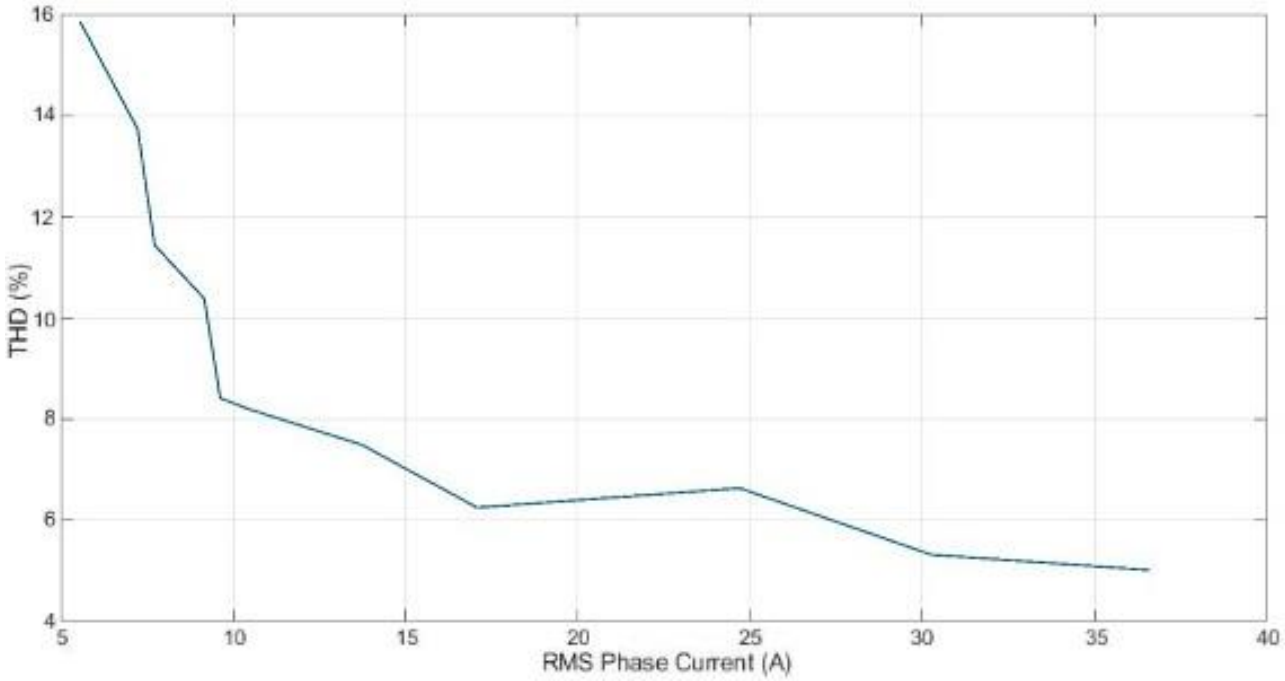


Figure 8.15. THD of prototype MMC with varying phase current

In comparison with the simulation using a static RL-load, they both trend upwards as the reference sinusoid frequency increases. With the variance in THD over the evaluation range of 300 Hz only causing an approximately 5 % change in THD.

The load was simulated with a higher load current range than the experimental test operated with, due to the limited I_{DS} of the real semiconductor switches. However, as shown by Figure 8.10 and Figure 8.15, the same inverse square relation between the THD and the load current was still observed.

8.5. EXPERIMENTAL RESULTS WITH PMSM

For this experiment, the converter was controlled using the developed FOC scheme. The MMC related parameters shown in Table 8.4 were used for testing with the PMSM, and the motor parameters are those outlined in Table 5.1.

8.5.1. DISCHARGING USING PMSM

The SOC balancing scheme implemented on the prototype MMC has been validated for use with a dynamic load, using a SOC imbalance of approximately 20 %. The motor rotated at the nominal speed (3000 RPM) throughout the course of the SOC balancing cycle. Figure 8.16 shows the SOC of all of the module batteries across the experiment.

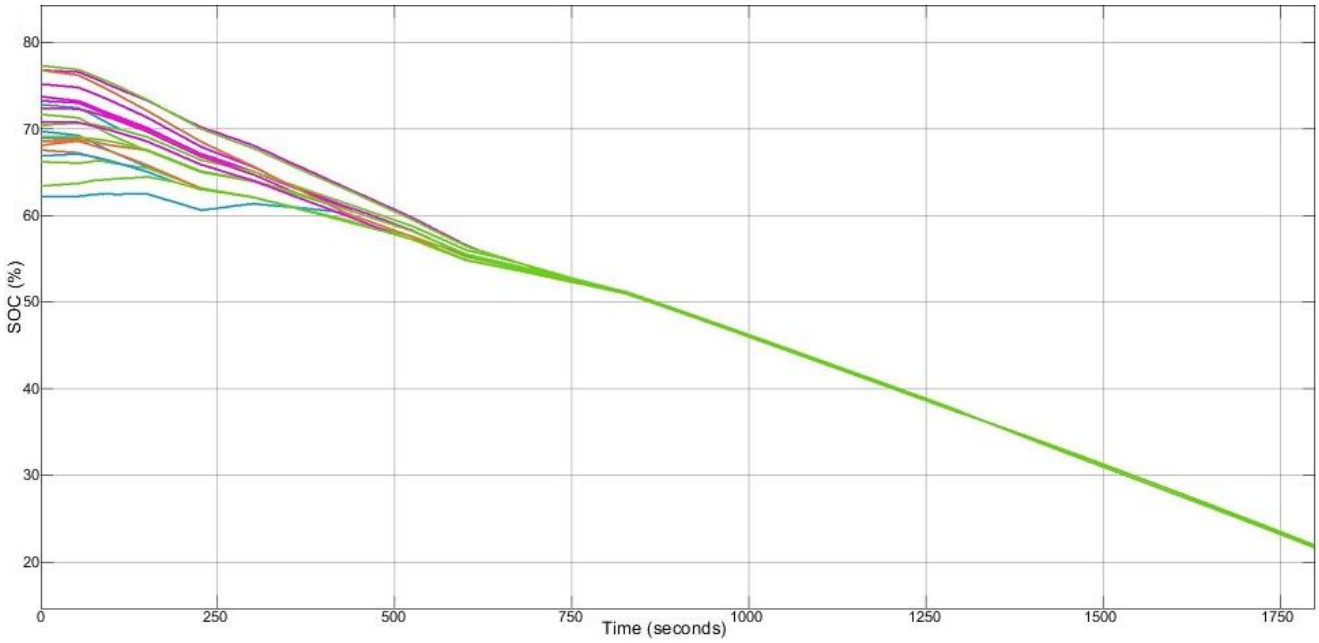


Figure 8.16. Module SOCs over course of discharge test using the prototype MMC with PMSM

In comparison with the response of the SOC-balancing using the static RL-load (Figure 8.13), the SOCs reach a similar value within 13 minutes for the PMSM. Whereas, for the static load approximately 25 minutes was required. This was a result of the load current for the static load being half that of the PMSM. However, due to noise on the current measurement signals, convergence to a single SOC took significantly longer. This was caused by the noise effects on the measured circulating current discussed at the end of Section 8.2.

8.5.2. PMSM Motor Control

As with the simulation, the FOC schemes ability to control the motor speed at arbitrary speed points was assessed. The speed control response using the prototype MMC is shown in Figure 8.17.

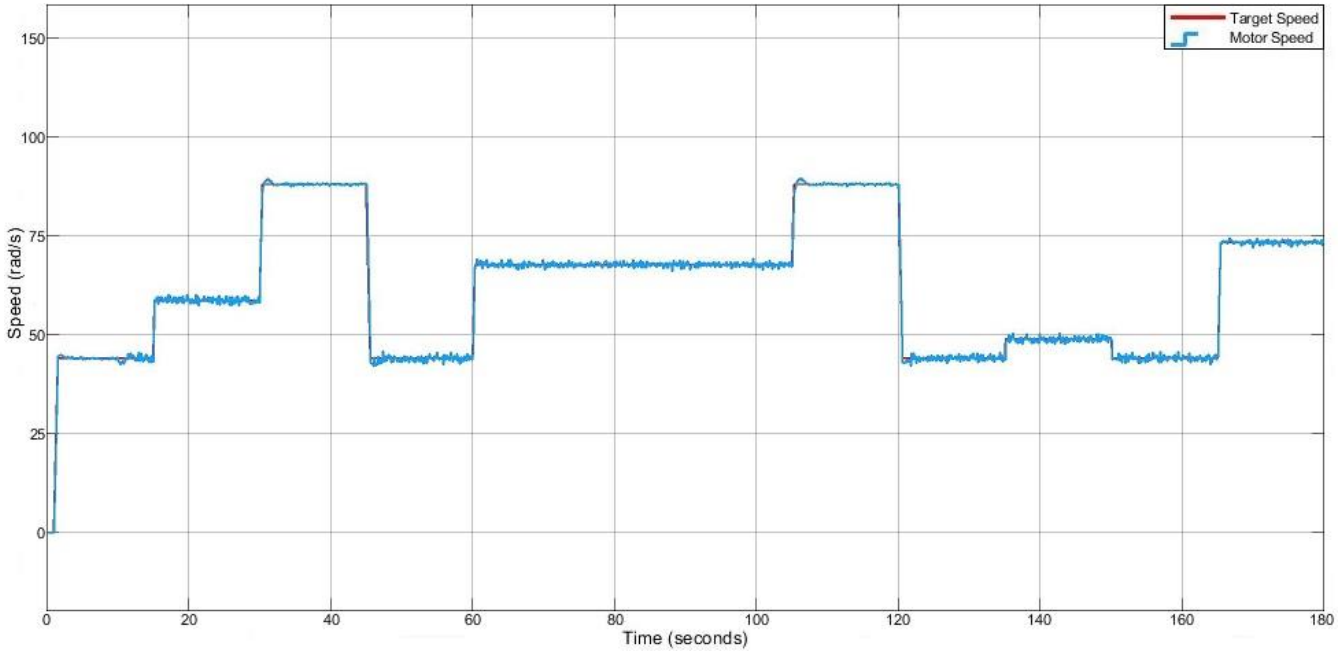


Figure 8.17. Speed Control of prototype MMC with PMSM for arbitrary speed set points

The performance of the speed control was impeded by the quality of the current measurement signals, as these were the primary feedback element for the FOC. This caused a significant amount of speed variation when trying to stabilize at the target speed, as reflected by Figure 8.17.

8.5.3. PROTOTYPE OPERATING RANGE WITH PMSM

The performance of the prototype was evaluated over a wide operating speed range for comparison with the simulation model. The THD with a variety of target motor speeds is shown in Figure 8.18.

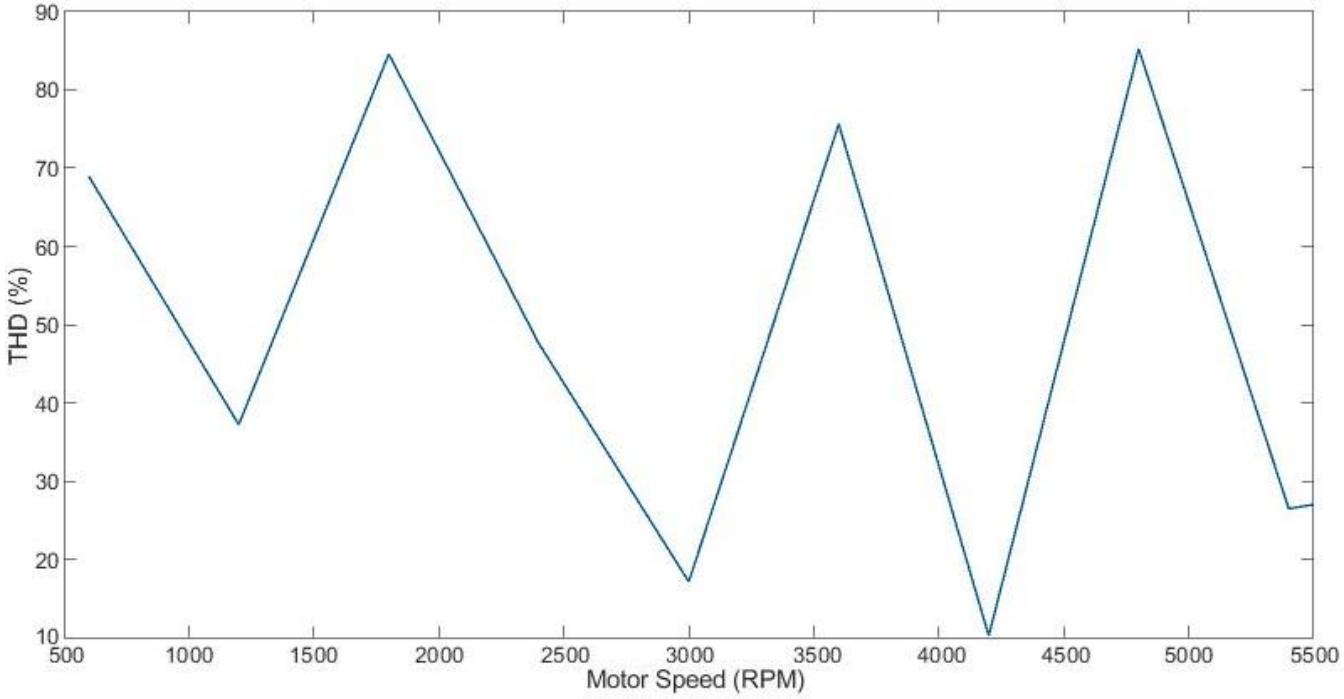


Figure 8.18. THD of prototype MMC with varying frequency of reference input for PMSM

The motor used had a rated operating speed of 5,500 RPM, significantly less than the operating speed range used for evaluation by the simulation model. The THD of the phase current measured over the rated operating range of the motor varied significantly from those predicted through simulation. The measured THD varied considerably with increasing frequency, showing no overall trend, and nearly jump by an order of magnitude with some transitions.

Due to timing constraints, the design of the FOC algorithm devised using simulation was implemented as is on the hardware; with little to no variation in controller gains explored using the experimental setup. This timing constraint also prevented the measurement of the variation in torque load on the motor from being investigated and compared with the response shown through simulation.

8.1. CHAPTER SUMMARY

In this chapter, the results of the hardware and control simulations and the validation of the prototype 5-level embedded battery MMC are detailed. Simulations of the designed embedded battery MMC were used to develop the control scheme for the laboratory-scale prototype.

The battery model used for simulation had to be modified from the physical batteries to speed up simulation time due to their high 20Ah capacity per module.

CHAPTER 8 SIMULATION AND EXPERIMENTAL RESULTS

The developed SOC-balancing scheme was simulated under no-load, static, and dynamic load conditions. With no load present, the individual module batteries were unable to be successfully balanced once the arms and legs were balanced, due to the absence of the DC current component of the circulating current and a load current component. Whereas, with the static and dynamic load connected to the MMC, all of the module batteries were successfully balanced to a common SOC and remained balanced with continued discharge. This was confirmed by replicating these simulation conditions on the hardware prototype, which provided similar results to those produced through simulation.

The FOC motor control scheme was evaluated through simulation of the selected PMSM. A wide torque and speed range was used for the simulation. However, due to timing limitations, only the rated operating speed range was investigated using the physical prototype MMC. Although the designed FOC scheme was designed and tuned using the simulation model, the transition between simulation and physical hardware did not yield identical results, signified by the differing THD responses with increasing frequency.

CHAPTER 9 CONCLUSION

9.1. CONCLUSIONS

This thesis presented the design, manufacture, development, and testing of a Modular Multilevel Converter with embedded batteries acting as the motor controller and battery pack as a concept for electric vehicle applications.

This topology distinguishes itself by integrating the functionality of an active battery management system within the motor controller, removing the need for external balancing circuits and a separate battery pack. While other topologies are limited by the selection of power devices, the proposed topology can use low-voltage MOSFETs. Due to the module batteries being directly connected to the arm bus, the required switch blocking voltage being equal to the module battery voltage. This feature allows the topology to take advantage of the comparatively low on-state resistance of MOSFETS. The state of charge of the batteries is estimated by the controller and balanced using a dedicated controller that balances the energy of the leg, arm, and modules of the converter while the systems operates independently as a motor controller. The developed converter provides low distortion to the output phase current, directly benefiting the motor control operation. This increases the motor efficiency, improving the overall operation of the electric vehicle.

The proposed converter has been tested by simulation and validated by experiments on a developed physical converter prototype with four modules per arm. The tests have demonstrated the operation of the converter driving both a static RL load and a PMSM. The SOC balancing control has been verified to operate irrespective of the nature of the load.

The proposed converter enables a new concept for BEV powertrain topologies by directly embedding the battery cells within the power converter and allowing for active BMS functionality without the addition of energy shunting hardware.

9.2. FUTURE WORK

The work detailed in this thesis on modular multilevel converters with embedded batteries for electric vehicle applications presents multiple opportunities for further hardware research and development, both in terms of the system control, and the hardware structure of the system. The main areas of future investigation identified by the author are the following:

- In addition to using circulating current control to balance the module battery SOC by eliminating the RMS circulating current component, development of a control scheme for elimination of the harmonic current, in particular the second harmonic component is required to minimize the circulating current.
- Integrating all the separate module PCBs, current sensor, and inductor for a single arm into a single PCB with a built-in busbar between the half-bridges will improve the system packaging, and thus make the topology more manufacturable.
- Create an arm control board that interfaces with the arm modules and reports values back to the central controller. This would allow for a reduction in the quantity of wiring and to reduce the computational load of the controller. Creating an embedded system interface between the main controller and the modules will minimize the analogue sensor lines and reduce the computational needs of the main controller by distributing it amongst the arm control interfaces. The SOC estimation algorithm, module selection scheme, battery voltage

measurement, and current sensor interface tasks could all be shifted to the embedded systems. Furthermore, a dedicated embedded system controller to replace the dSPACE could be created once the control has been sufficiently developed to improve the practicality of the prototype and bring it closer to an application implementable system.

- Scale system up to interface with a higher voltage motor. Expand the prototype to interface with a higher power motor more analogous with those integrated into an electric vehicle. This could be achieved by either increasing the number of modules per arm, increasing the number of batteries per module (however, this would require the addition of an inner module battery management system to balance the batteries), or integrating a buck/boost converter interface between the batteries and the half-bridge chopper to increase the voltage output of the module.
- Expand the functionality of the battery management system to monitor the temperature of the battery cells and implement a fault detection system to disconnect excessively hot modules.
- Analyze the proposed MMC under fault conditions. This includes cases where one or more modules is operating open or short-circuited; evaluation of the performance with a reduced number of functioning modules; incorporation of a scheme for generating a pool of available modules; and the impact operating at a reduced state has on the THD of the phase currents.
- Developing a charging interface between the prototype and a single-phase supply for charging the module batteries through the converter.
- Replace the external LV power supply with power sourced from the module batteries. However, attention would need to be paid for redesigning the gate drive circuit isolation between the high-side and low-side switch drive circuits, to ensure the bootstrap circuit will always be able to recharge the bootstrap capacitor.

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APPENDIX A SOC ESTIMATION ALGORITHM FOR ENERGUS 1S8P CELL BRICK

```
function [SOC, SOH_t0, DOD_t0, SOH, DOD] = fcn(Vb, Ib, Q_in, t, SOH_t,
DOD_t, SOH1, DOD1, SOC1)
%#SOC estimation algorithm using enhanced-coulomb counter. With OCV
measurement for calculating the initial SOC

%Initialise variables and read memory values
SOH_t0 = SOH_t;
DOD_t0 = DOD_t;
SOH = SOH1;
DOD = DOD1;
SOC = SOC1;
xdata =
[5.0,6.2,6.6,6.7,6.8,6.9,6.94,7.0,7.1,7.14,7.2,7.3,7.4,7.5,7.6,7.7,7.8,7.9,
8.00,8.04,8.3];
ydata = [0,5,10,15,20,25,30,35,40,45,50,55,60,65,70,75,80,85,90,95,100];
index = 20;
data_len = 21;
data_diff = 5;
Q = -1/(2.5*8*100)*Q_in;

%OCV to SOC calculation, uses linear interpolation to generate SOC based on
a discrete OCV to SOC dataset
if t ~= 1
    for ii = 1:1:data_len
        if Vb - xdata(ii) < 0
        index = ii-1;
        if index < 1
            index = 1;
        end
        break
        end
    end
    var1 = Vb - xdata(index);
    var2 = xdata(index+1) - xdata(index);
    var3 = var1/var2;
    var4 = var3*data_diff;
    OCV = ydata(index) + var4;

    SOC = OCV;
    SOH_t0 = 100;
    SOH = SOH_t0;
    DOD_t0 = 100 - SOC;
    DOD = DOD_t0;
End

%Enhanced-Coulomb Counter
if Ib < -1
    if Vb > 2.5 * 2
        DOD = DOD_t0 + Q;
        SOC = SOH - DOD;
    else
    SOH = DOD;
    end
end
if Ib > 1
    if Vb >= 4.2 * 2
```

```
        SOH = SOC;
    else
    DOD = DOD_t0 + Q;
    SOC = SOH - DOD;
    end
end
if SOC < 0
    SOC = 0;
end
```

APPENDIX B SPACE VECTOR MODULATION SCHEME

```
function [Va, Vb, Vc, ref_out_up, ref_out_down, timer]   = fcn(ref_up,
ref_down, time_in, m, ref_mem_up, ref_mem_down)
%#
%Initialise variables\
Fs = 5000;
Ts = 1/Fs;
Ttri = Ts/2;
Tsc = 1e-5;
%m = 5; Enable if not using error detection
N = m-1;

%Prevent number of used modules exceeding the actual number of modules
if N < 0
    N = 0;
end
if N > 4
    N = 4;
end

scale = N/2;

%Initialise vectors
Vu1 = [0;0;0];
Vu2 = [0;0;0];
Vu3 = [0;0;0];
Vu4 = [0;0;0];
Vl1 = [0;0;0];
Vl2 = [0;0;0];
Vl3 = [0;0;0];
Vl4 = [0;0;0];
Vu = [0;0;0];
Vl = [0;0;0];
Va = [0;0];
Vb = [0;0];
Vc = [0;0];

%Internal switching timer
timer = time_in;

if timer <= Ttri
    tri = timer;
else
    tri = Ts - timer;
end

timer = timer + Tsc;

if tri < 0
    tri = 0;
end
if tri > Ttri
    tri = Ttri;
end
if timer > Ts
    timer = 0;
```

```
end

%Split reference Sine wave into upper and lower 5-level signals and sample
check
if tri == 0
    Yl = scale+scale*ref_down;
    Yu = scale+scale*ref_up;
    ref_out_up = ref_up;
    ref_out_down = ref_down;
else
    Yl = scale+scale*ref_mem_down;
    Yu = scale+scale*ref_mem_up;
    ref_out_up = ref_mem_up;
    ref_out_down = ref_mem_down;
end


% Find the centre of two-level Space Vector hexagon
Vru = floor(Yu);

if Vru(1) > N-1
    Vru(1) = N-1;
end
if Vru(1) < 0
    Vru(1) = 0;
end
if Vru(2) > N-1
    Vru(2) = N-1;
end
if Vru(2) < 0
    Vru(2) = 0;
end
if Vru(3) > N-1
    Vru(3) = N-1;
end
if Vru(3) < 0
    Vru(3) = 0;
end

Vrl = floor(Yl);

if Vrl(1) > N-1
    Vrl(1) = N-1;
end
if Vrl(1) < 0
    Vrl(1) = 0;
end
if Vrl(2) > N-1
    Vrl(2) = N-1;
end
if Vrl(2) < 0
    Vrl(2) = 0;
end
if Vrl(3) > N-1
    Vrl(3) = N-1;
end
if Vrl(3) < 0
    Vrl(3) = 0;
end
```

```
% Calculate two-level vector from the reference sine and offset vector
Vut = Yu - Vru;
Vlt = Yl - Vrl;

% Convert to ab reference frame
Vuab = (2/3)*[1, -0.5, -0.5; 0, sqrt(3)/2, -sqrt(3)/2] * Vut;
Vlab = (2/3)*[1, -0.5, -0.5; 0, sqrt(3)/2, -sqrt(3)/2] * Vlt;

% Calculate angle of two-level vector within the two-level hexagon
thetau = atand(Vuab(2)/Vuab(1));
thetal = atand(Vlab(2)/Vlab(1));
if isnan(thetau)
    thetau = 0;
end
if isnan(thetal)
    thetal = 0;
end
if Vuab(1) <= 0 && Vuab(2) > 0
    thetau = 180 + thetau;
end
if Vuab(1) < 0 && Vuab(2) <= 0
    thetau = 180 + thetau;
end
if Vuab(1) > 0 && Vuab(2) < 0
    thetau = 360 + thetau;
end

if Vlab(1) <= 0 && Vlab(2) > 0
    thetal = 180 + thetal;
end
if Vlab(1) < 0 && Vlab(2) <= 0
    thetal = 180 + thetal;
end
if Vlab(1) > 0 && Vlab(2) < 0
    thetal = 360 + thetal;
end
if thetau == 360
    thetau = 0;
end
if thetal == 360
    thetal = 0;
end
if thetau < 0
    thetau = 0;
end
if thetal < 0
    thetal = 0;
end
% Find required switching vectors based on where in hexagon two-level
vector is
if 0 <= thetau && thetau < 60
    Vu1 = [Vru(1); Vru(2); Vru(3)];
    Vu2 = [(Vru(1) + 1); Vru(2); Vru(3)];
    Vu3 = [(Vru(1) + 1); (Vru(2) + 1); Vru(3)];
    Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
else
    if 60 <= thetau && thetau < 120
        Vu1 = [Vru(1); Vru(2); Vru(3)];
        Vu2 = [Vru(1); (Vru(2) + 1); Vru(3)];
        Vu3 = [(Vru(1) + 1); (Vru(2) + 1); Vru(3)];
        Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
```

```
    else
        if 120 <= thetau && thetau < 180
            Vu1 = [Vru(1); Vru(2); Vru(3)];
            Vu2 = [Vru(1); (Vru(2) + 1); Vru(3)];
            Vu3 = [Vru(1); (Vru(2) + 1); (Vru(3) + 1)];
            Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
        else
            if 180 <= thetau && thetau < 240
                Vu1 = [Vru(1); Vru(2); Vru(3)];
                Vu2 = [Vru(1); Vru(2); (Vru(3) + 1)];
                Vu3 = [Vru(1); (Vru(2) + 1); (Vru(3) + 1)];
                Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
            else
                if 240 <= thetau && thetau < 300
                    Vu1 = [Vru(1); Vru(2); Vru(3)];
                    Vu2 = [Vru(1); Vru(2); (Vru(3) + 1)];
                    Vu3 = [(Vru(1) + 1); Vru(2); (Vru(3) + 1)];
                    Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
                else
                    if 300 <= thetau && thetau < 360
                        Vu1 = [Vru(1); Vru(2); Vru(3)];
                        Vu2 = [(Vru(1) + 1); Vru(2); Vru(3)];
                        Vu3 = [(Vru(1) + 1); Vru(2); (Vru(3) + 1)];
                        Vu4 = [(Vru(1) + 1); (Vru(2) + 1); (Vru(3) + 1)];
                    end
                end
            end
        end
    end
end

if 0 <= thetal && thetal < 60
    Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
    Vl2 = [(Vrl(1) + 1); Vrl(2); Vrl(3)];
    Vl3 = [(Vrl(1) + 1); (Vrl(2) + 1); Vrl(3)];
    Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
else
    if 60 <= thetal && thetal < 120
        Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
        Vl2 = [Vrl(1); (Vrl(2) + 1); Vrl(3)];
        Vl3 = [(Vrl(1) + 1); (Vrl(2) + 1); Vrl(3)];
        Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
    else
        if 120 <= thetal && thetal < 180
            Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
            Vl2 = [Vrl(1); (Vrl(2) + 1); Vrl(3)];
            Vl3 = [Vrl(1); (Vrl(2) + 1); (Vrl(3) + 1)];
            Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
        else
            if 180 <= thetal && thetal < 240
                Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
                Vl2 = [Vrl(1); Vrl(2); (Vrl(3) + 1)];
                Vl3 = [Vrl(1); (Vrl(2) + 1); (Vrl(3) + 1)];
                Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
            else
                if 240 <= thetal && thetal < 300
                    Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
                    Vl2 = [Vrl(1); Vrl(2); (Vrl(3) + 1)];
                    Vl3 = [(Vrl(1) + 1); Vrl(2); (Vrl(3) + 1)];
                    Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
                else
```

```
                    if 300 <= thetal && thetal < 360
                        Vl1 = [Vrl(1); Vrl(2); Vrl(3)];
                        Vl2 = [(Vrl(1) + 1); Vrl(2); Vrl(3)];
                        Vl3 = [(Vrl(1) + 1); Vrl(2); (Vrl(3) + 1)];
                        Vl4 = [(Vrl(1) + 1); (Vrl(2) + 1); (Vrl(3) + 1)];
                    end
                end
            end
        end
    end
end

% Calculate required dwell times
Tau = Vut(1) * Ts;
Tbu = Vut(2) * Ts;
Tcu = Vut(3) * Ts;

Tal = Vlt(1) * Ts;
Tbl = Vlt(2) * Ts;
Tcl = Vlt(3) * Ts;

Tu = [Tau, Tbu, Tcu];
Tl = [Tal, Tbl, Tcl];

Trefu = sort(Tu);
Trefl = sort(Tl);

Tu1 = Ts - Trefu(3);
Tu2 = Trefu(3) - Trefu(2);
Tu3 = Trefu(2) - Trefu(1);
Tu4 = Trefu(1);
Tu0 = Tu1 + Tu4;

Tl1 = Ts - Trefl(3);
Tl2 = Trefl(3) - Trefl(2);
Tl3 = Trefl(2) - Trefl(1);
Tl4 = Trefl(1);
Tl0 = Tl1 + Tl4;

% Switch vector output based on dwell times
if tri <= (Tu0/4)
    Vu = Vu1;
else
    if tri <= (Tu0/4) + (Tu2/2)
        Vu = Vu2;
    else
        if tri <= (Tu0/4) + (Tu2/2) + (Tu3/2)
            Vu = Vu3;
        else
            Vu = Vu4;
        end
    end
end

if tri <= (Tl0/4)
    Vl = Vl1;
else
    if tri <= (Tl0/4) + (Tl2/2)
        Vl = Vl2;
    else
```

```
        if tri <= (Tl0/4) + (Tl2/2) + (Tl3/2)
            Vl = Vl3;
        else
            Vl = Vl4;
        end
    end
end

Va = [Vu(1); Vl(1)];
Vb = [Vu(2); Vl(2)];
Vc = [Vu(3); Vl(3)];
```

APPENDIX C SVM TESTING SCRIPT

```
%Space Vector Modulation graphical tool
%Script for testing the SVM Simulink model and visualising its performance
%By Anthony Watson
%24/02/21
% Ver. 2.0

clear, clc

% Get user input parameters
MMC_Level = input('Desired Maximum MMC Switching Level \n');
switch_F = input('Desired Carrier Frequency \n');
mod_F = input('Desired Reference Frequency \n');
T_fss = input('Desired Model Sample Time \n');

% Calculate fundamental step time SVM switching period, and sim time
T_sw = 1/switch_F;
T_pk = T_sw/2;
T = 2/mod_F;

% Ask user if they want a fixed or step amplitude input
Vary_Level = 'E';
while Vary_Level ~= 'y' || Vary_Level ~= 'n'
    if Vary_Level == 'y' || Vary_Level == 'n'
        break
    else
        Vary_Level = input('Do you want a varying level reference input?
(y/n) \n','s');
    end
end
if Vary_Level == 'y'
    Vary_Level_Control = 1;
else
    Vary_Level_Control = 0;
end

% Generate all the unique switching vectors for a user selected switching
% level in abc reference frame
sum = 1;
index = 2;
level_index = 1;
Vector_Array = [0;0;0];
% Calculate the number of unique switching vectors
for ii = 1:1:MMC_Level
    sum = sum + 6 + (ii-2)*6;
end
% Generate all the unique space vectors in abc reference
Vector_AB = zeros(sum,2);
while level_index < MMC_Level
    Vector_Array = cat(2,Vector_Array,[level_index;0;0]);
    for ii = 1:1:level_index
        Vector_Array = cat(2,Vector_Array,[level_index;ii;0]);
    end
    for ii = level_index-1:-1:0
        Vector_Array = cat(2,Vector_Array,[ii;level_index;0]);
    end
    for ii = 1:1:level_index
        Vector_Array = cat(2,Vector_Array,[0;level_index;ii]);
    end
```

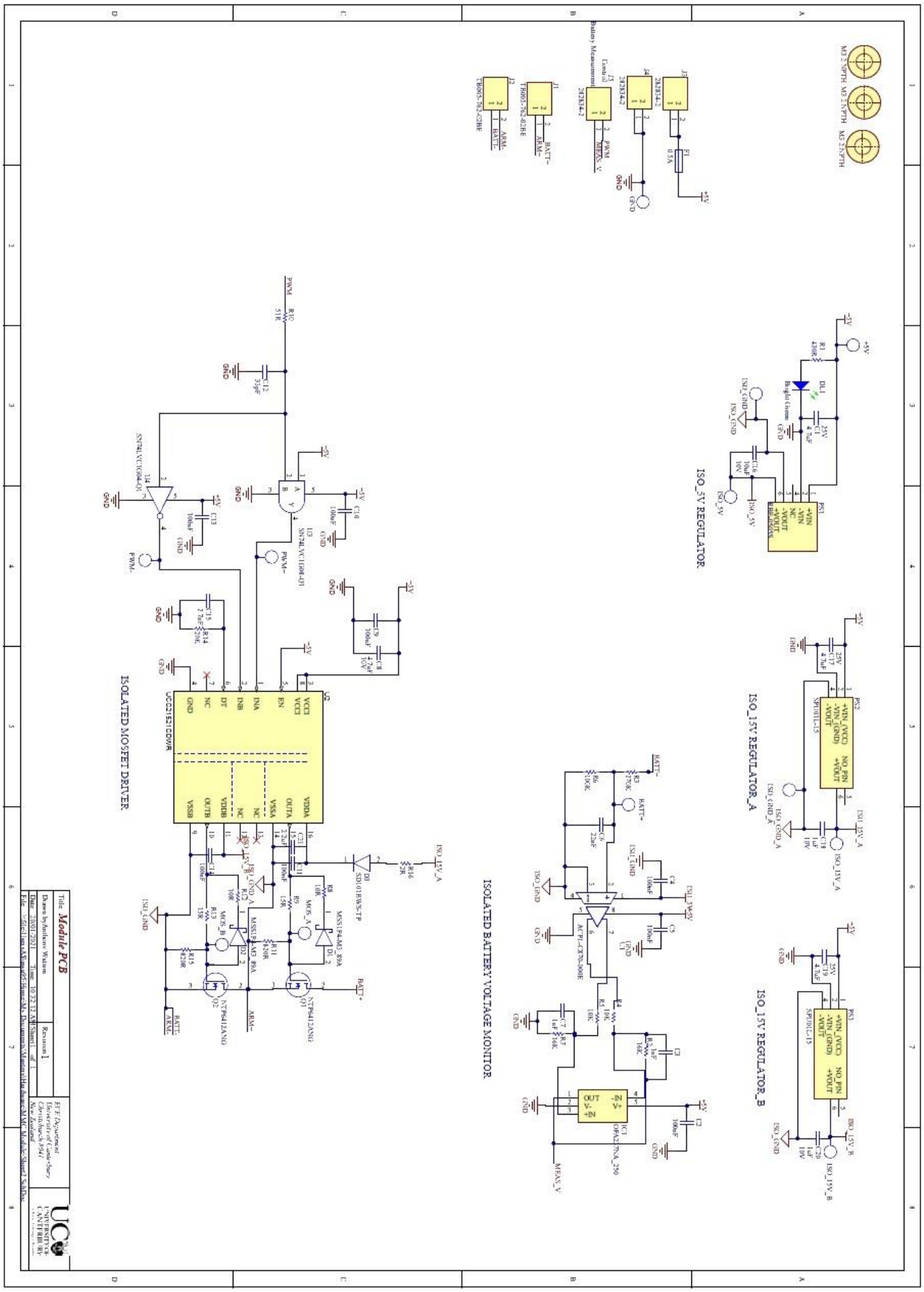
```
    for ii = level_index-1:-1:0
        Vector_Array = cat(2,Vector_Array,[0;ii;level_index]);
    end
    for ii = 1:1:level_index
        Vector_Array = cat(2,Vector_Array,[ii;0;level_index]);
    end
    if level_index > 1
        for ii = level_index-1:-1:1
            Vector_Array = cat(2,Vector_Array,[level_index;0;ii]);
        end
    end
    level_index = level_index + 1;
end
% Generate the unique switching vectors in alapha-beta reference frame
for ii = 1:1:sum
    Vector_AB(ii,:) = (2/3)*[1, -0.5, -0.5; 0, sqrt(3)/2, -sqrt(3)/2] *
Vector_Array(:,ii);
end
% Run the SVM generator interface model with the SVM embedded Matlab
% function block
sim('SVM_test',T);
% Plot the SVM output vectors, the calculated unique space vectors, and the
% reference input in the alpha-beta reference frame
hold on
plot(Vector_AB(:,1),Vector_AB(:,2),'ko')
plot(Vuab(:,2),Vuab(:,3),'b-o')
plot(Vref(:,2),Vref(:,3),'r-o')
hold off
```

APPENDIX D MODULE SWITCHING SELECTION SCHEME

```
function [G, D] = fcn(SOC, I, D, control, D_mem, G_mem)
%# Module selection based on switching vector input for a converter arm

%Initialise variables
N = 4;
G = false(4,1);
S = [0,0,0,0];
Mod = [0,0,0,0];
AI = [0,0,0,0];

% Check if PWM input has changed
if D == D_mem
    % Since PWM input is the same, maintain the same output
    G = G_mem;
else
    % Determine new module control output
    Mod(1) = (SOC(1) > SOC(2)) + (SOC(1) > SOC(3)) + (SOC(1) > SOC(4));
    Mod(2) = (SOC(2) > SOC(1)) + (SOC(2) > SOC(3)) + (SOC(2) > SOC(4));
    Mod(3) = (SOC(3) > SOC(1)) + (SOC(3) > SOC(2)) + (SOC(3) > SOC(4));
    Mod(4) = (SOC(4) > SOC(1)) + (SOC(4) > SOC(2)) + (SOC(4) > SOC(3));
    [Sort_SOC,Index] = sort(Mod);

    %Prevent modules being assigned the same switching priority by making
sure module sorting is mutually exclusive
    Sort_SOC(Index(1)) = 0;
    Sort_SOC(Index(2)) = 1;
    Sort_SOC(Index(3)) = 2;
    Sort_SOC(Index(4)) = 3;

    %Determine if module is charging or discharging
    if I >= 0
        Ad = 0;
    else
        Ad = 1;
    end

    %Arrange the switching priority based on the module SOC order and the
current direction
    AI(1) = Sort_SOC(1)*Ad+(N-1-Sort_SOC(1))*(1-Ad);
    AI(2) = Sort_SOC(2)*Ad+(N-1-Sort_SOC(2))*(1-Ad);
    AI(3) = Sort_SOC(3)*Ad+(N-1-Sort_SOC(3))*(1-Ad);
    AI(4) = Sort_SOC(4)*Ad+(N-1-Sort_SOC(4))*(1-Ad);

    %Determine if module should be switched in based on the PWM reference
input and the assigned switching priority
    if AI(1) >= N - D
        S(1) = 1;
    else
        S(1) = 0;
    end
    if AI(2) >= N - D
        S(2) = 1;
    else
        S(2) = 0;
    end
    if AI(3) >= N - D
        S(3) = 1;
    else
```

```
        S(3) = 0;
    end
    if AI(4) >= N - D
        S(4) = 1;
    else
        S(4) = 0;
    end

    %Set the output switching vector
    G(1,1) = S(1);
    G(2,1) = S(2);
    G(3,1) = S(3);
    G(4,1) = S(4);
end
%Disable the system output for start-up or error detection
if control ~= 1
    G = false(4,1);
end
```

APPENDIX E MODULE SCHEMATIC



APPENDIX F BATTERY PACK SPECIFICATION AND ISOLATED VOLTAGE MEASUREMENT CIRCUIT TUNING SCRIPT

```
% Modular Multilevel Converter Equivalent Battery Pack and Voltage
% Measurement Circuit Response Calculator
% Takes in a desired nominal pack voltage, calculates a pack size and using
% user input generates the required resistor values to get the desired
% circuit response
% Author: Anthony Watson
% Date: 30/09/2020
% Version 2.0

clear,clc

%Init. parameters
max_iso_amp_input = 2.7;
div_R2 = 100;
max_diff_amp_input = 4.24;
diff_R1 = 10;
v_step = 1;
figure_index = 1;
test_R1s = ones(1,24);
nodes = ["Input", "Div. Out", "Iso. Plus", "Output"];
nodes_1 = ["Input", "Div. Out", "Iso. Plus"];
nodes_2 = ["Iso. Plus", "Output"];
res_list = [1.0, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0,
3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1];

%Calculate battery pack parameters
des_nom_pack_volt = input('Desired nominal battery pack voltage (V) \n');
mod_num = ceil(des_nom_pack_volt/(3.6*8));
tot_mod = mod_num * 4 * 2 * 3;
max_input = mod_num * 4.2;
pack_max = max_input * 8;
nom_input = mod_num * 3.6;
pack_nom = nom_input * 8;
pack_capacity = (pack_nom * 20 *3)/1000;
target_div_volt = round(max_input/5) * 5;
target_div_ratio = max_iso_amp_input/target_div_volt;
required_R1 = round(div_R2*((1-target_div_ratio)/target_div_ratio));
test_R1 = required_R1;
div_tick_R1 = 0;
iso_tick = 0;
diff_tick = 0;
%Calculate a valid resistor sizing
while test_R1 >= 10
    test_R1 = test_R1 / 10;
    div_tick_R1 = div_tick_R1 + 1;
end
dif_R1 = res_list - test_R1;
R1_index = 1;
if test_R1 > max(res_list)
div_tick_R1 = div_tick_R1 + 1;
end
for ii = 1:1:length(res_list)
    if dif_R1(ii) > 0
        R1_index = ii;
        break
    end
```

```
    if res_list(ii) == test_R1
        req_R1_good = 1;
        break
    else
        req_R1_good = 0;
    end
end

if req_R1_good ~= 1
    check_R1 = res_list(R1_index)*10^div_tick_R1;
else
    check_R1 = required_R1;
end

%Calculate output of designed isolated amplifier
used_div_ratio = div_R2/(check_R1+div_R2);
test_div_volt = round(target_div_volt);
check_diff_input = test_div_volt*used_div_ratio;
if check_diff_input > max_iso_amp_input
    test_div_volt = test_div_volt - 1;
    check_diff_input = test_div_volt*used_div_ratio;
end
calc_diff_V_pos = 0.534*check_diff_input+1.2454;

%Calculate valid gain resistor for diff. amplifier
required_diff_ratio = max_diff_amp_input/calc_diff_V_pos;
required_R3 = round(required_diff_ratio*diff_R1);
used_R3 = required_R3;
test_R3 = used_R3;
div_tick_R3 = 0;
while test_R3 >= 10
    test_R3 = test_R3 / 10;
    div_tick_R3 = div_tick_R3 + 1;
end
diff_R3 = res_list - test_R3;
R3_index = 1;
if test_R3 > max(res_list)
div_tick_R3 = div_tick_R3 + 1;
end
for jj = 1:1:length(res_list)
    if diff_R3(jj) > 0
        R3_index = jj;
        break
    end
    if res_list(jj) == test_R3
        req_R3_good = 1;
        break
    else
        req_R3_good = 0;
    end
end

if req_R3_good ~= 1
    check_R3 = res_list(R3_index-1)*10^div_tick_R3;
else
    check_R3 = required_R3;
end

% Filter tuning
iso_filter = input('Desired Isolated Low Pass filter (Hz) \n');
```

```
diff_filter = input('Desired Differential Amplifier Low Pass filter (Hz)
\n');

divider = (1/(check_R1*1000)) + (1/(div_R2*1000));
divider = 1/ divider;
iso_c = 1/(2*pi*divider*iso_filter);
iso_c_mem = iso_c;
iso_c = iso_c * 1e9;
while iso_c > 10
    iso_c = iso_c / 10;
    iso_tick = iso_tick + 1;
end
diff_iso = res_list - iso_c;
iso_index = 1;
if iso_c > max(res_list)
iso_tick = iso_tick + 1;
end
for kk = 1:1:length(res_list)
    if diff_iso(kk) > 0
        iso_index = kk;
        break
    end
    if res_list(kk) == iso_c
        iso_c_good = 1;
        break
    else
        iso_c_good = 0;
    end
end

if iso_c_good ~= 1
    check_iso_c = res_list(iso_index);
else
    check_iso_c = iso_c_mem;
end
display_iso_c = check_iso_c*10^iso_tick;
scale = 9-iso_tick;
check_iso_c = check_iso_c * (1*10^-scale);
iso_filter = 1/(2*pi*divider*check_iso_c);

diff_c = 1/(2*pi*check_R3*1000*diff_filter);
diff_c_mem = diff_c;
diff_c = diff_c *1e9;
while diff_c > 10
    diff_c = diff_c / 10;
    diff_tick = diff_tick + 1;
end
diff_diff = res_list - diff_c;
diff_index = 1;
if diff_c > max(res_list)
diff_tick = diff_tick + 1;
end
for ll = 1:1:length(res_list)
    if diff_diff(ll) > 0
        diff_index = ll;
        break
    end
    if res_list(ll) == diff_c
        diff_c_good = 1;
        break
    else
```

```
        diff_c_good = 0;
    end
end

if diff_c_good ~= 1
    check_diff_c = res_list(diff_index);
else
    check_diff_c = diff_c_mem;
end
display_diff_c = (check_diff_c*10^diff_tick)/1000;
scale = 9-diff_tick;
check_diff_c = check_diff_c * (1*10^-scale);
diff_filter = 1/(2*pi*check_R3*1000*check_diff_c);

used_diff_ratio = used_R3/diff_R1;
test_V_out = used_diff_ratio * calc_diff_V_pos;
figure_index = run_sim (figure_index, v_step, target_div_volt, div_R2,
check_R1, used_R3, diff_R1, max_iso_amp_input, max_diff_amp_input, nodes);

comp_func = get_comp_func (figure_index, v_step, target_div_volt, div_R2,
check_R1, check_R3, diff_R1, max_iso_amp_input, max_diff_amp_input,
nodes_1);

%Print out pack parameters
fprintf('\n------------- Summary of Battery Pack Parameters ----------\n');
fprintf('| Battery Pack Peak Voltage:                    %.1f V        |\n',
pack_max);
fprintf('| Battery Pack Nominal Voltage:                 %.1f V        |\n',
pack_nom);
fprintf('| Number of Batteries per Module:               %.0f          |\n',
mod_num);
fprintf('| Total Number of Batteries Required:           %.0f          |\n',
tot_mod);
fprintf('| Battery Pack Capacity:                        %.2f kWh      |\n',
pack_capacity);
fprintf('| Maximum Module Voltage:                       %.1f  V       |\n',
max_input);
fprintf('| Nominal Module Voltage:                       %.1f  V       |\n',
nom_input);
fprintf('| Voltage Divider R1:                           %.0f  kOhm    |\n',
check_R1);
fprintf('| Voltage Divider R2:                           %.0f  kOhm    |\n',
div_R2);
fprintf('| Diff. Amp. R1 and R2:                         %.0f   kOhm   |\n',
diff_R1);
fprintf('| Diff. Amp. R3 and R4:                         %.0f   kOhm   |\n',
check_R3);
fprintf('| Iso Amp. Filter Capacitor                     %.0f   nF     |\n',
display_iso_c);
fprintf('| Diff Amp. Filter Capacitor                    %.0f    uF    |\n',
display_diff_c);
fprintf('| Iso Amp. Cut-off Freq.                        %.0f   Hz     |\n',
iso_filter);
fprintf('| Diff Amp. Cut-off Freq.                       %.0f   Hz     |\n',
diff_filter);
fprintf('| Required software compensation coefficient    %.3f         |\n',
comp_func);
fprintf('-----------------------------------------------------------\n\n');

%Plot the response of the designed circuit
```

```
function figure_index = run_sim (figure_index, v_step, target_div_volt,
div_R2, used_R1, used_R3, diff_R1, max_iso_amp_input, max_diff_amp_input,
nodes)
close
for ii = 0:v_step:target_div_volt
    v_in(ii+1) = ii;
    v_div(ii+1) = ii*(div_R2)/(used_R1+div_R2);
    if v_div(ii+1) >= max_iso_amp_input
        fprintf('WARNING: Isolation Amplifier output may saturate!\n');
    end
    v_plus(ii+1) = 0.534*v_div(ii+1) + 1.2454;
    v_minus(ii+1) = -0.541*v_div(ii+1) + 1.2575;
    v_out(ii+1) = (v_plus(ii+1)-v_minus(ii+1))*(used_R3/diff_R1);
    if v_out(ii+1) >= max_diff_amp_input
        fprintf('WARNING: Differential Amplifier output may saturate!\n');
    end
    out(ii+1,1) = v_in(ii+1);
    out(ii+1,2) = v_div(ii+1);
    out(ii+1,3) = v_plus(ii+1);
    out(ii+1,4) = v_out(ii+1);
    figure(figure_index)
    xlabel('Circuit Node')
    ylabel('Voltage at Node (V)')
    hold on
    grid on
    plot(out(ii+1,:))
    ylim([0 target_div_volt]);
end
set(gca, 'xtick',[1:4], 'xticklabel', nodes');
hold off
figure_index = figure_index + 1;
end

%Calculate the scaling factor for the control software to extract the
%measured battery voltage from the circuit output voltage
function comp_func = get_comp_func (figure_index, v_step, target_div_volt,
div_R2, used_R1, used_R3, diff_R1, max_iso_amp_input, max_diff_amp_input,
nodes_1)
 for ii = 0:v_step:target_div_volt
    v_in(ii+1) = ii;
    v_div(ii+1) = ii*(div_R2)/(used_R1+div_R2);
    v_plus(ii+1) = 0.534*v_div(ii+1) + 1.2454;
    v_minus(ii+1) = -0.541*v_div(ii+1) + 1.2575;
    v_out(ii+1) = (v_plus(ii+1)-v_minus(ii+1))*(used_R3/diff_R1);
 end
 grad = v_out(end)/v_in(end);
 comp_func = 1/grad;
end
```

APPENDIX G MODULE BATTERY SOCS FOR SIMULATION

```
SOC_1 = 90;
SOC_2 = 82;
SOC_3 = 90;
SOC_4 = 86;
SOC_5 = 90;
SOC_6 = 88;
SOC_7 = 94;
SOC_8 = 89;
SOC_9 = 93;
SOC_10 = 82;
SOC_11 = 91;
SOC_12 = 88;
SOC_13 = 95;
SOC_14 = 91;
SOC_15 = 82;
SOC_16 = 89;
SOC_17 = 96;
SOC_18 = 85;
SOC_19 = 90;
SOC_20 = 86;
SOC_21 = 97;
SOC_22 = 89;
SOC_23 = 98;
SOC_24 = 89;
```

```
---------- Summary of SOC Parameters ----------
| Total SOC:                    89.58           |
| SOC Range:                    2.63            |
| Range High:                   1.67            |
| Range Low:                    0.96            |
------------------ Arm 1 Stats ------------------
| Average SOC:                  87.00           |
| SOC Range:                    8.00            |
| Range High:                   3.00            |
| Range Low:                    5.00            |
-------------------------------------------------
------------------ Arm 2 Stats ------------------
| Average SOC:                  88.50           |
| SOC Range:                    11.00           |
| Range High:                   4.50            |
| Range Low:                    6.50            |
-------------------------------------------------
------------------ Arm 3 Stats ------------------
| Average SOC:                  89.25           |
| SOC Range:                    11.00           |
| Range High:                   6.75            |
| Range Low:                    4.25            |
-------------------------------------------------
```

Arm 4 Stats	
Average SOC:	90.25
SOC Range:	6.00
Range High:	3.75
Range Low:	2.25

Arm 5 Stats	
Average SOC:	89.25
SOC Range:	13.00
Range High:	5.75
Range Low:	7.25

Arm 6 Stats	
Average SOC:	93.25
SOC Range:	9.00
Range High:	4.75
Range Low:	4.25

Leg A Stats	
Average SOC:	88.63
SOC Range:	3.25
Range High:	1.63
Range Low:	1.63

Leg B Stats	
Average SOC:	88.88
SOC Range:	0.75
Range High:	0.38
Range Low:	0.38

Leg C Stats	
Average SOC:	91.25
SOC Range:	4.00
Range High:	2.00
Range Low:	2.00