

Field plate optimization in low-power high-gain source-gated transistors

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Abstract — Source-gated transistors (SGTs) have potentially very high output impedance and low saturation voltages, which make them ideal as building blocks for high performance analog circuits fabricated in thin-film technologies. The quality of the saturation is greatly influenced by the design of the field-relief structure incorporated into the source electrode. Starting from measurements on self-aligned polysilicon structures, we show through numerical simulations how the field plate design can be improved. A simple source field plate around 1 μm long situated several tens of nm above the semiconductor can increase the low-voltage intrinsic gain by more than two orders of magnitude and offers adequate tolerance to process variations in a moderately scaled thin-film SGT.

I. INTRODUCTION

Polysilicon field effect transistors (FETs) are the technology of choice in a number of large-area electronic applications, including flat-panel display/touch screens [1], fingerprint readers [2] and logic circuits [3]. Due to the high mobility of polycrystalline silicon [3, 4], electronic devices and circuits made with this material operate at high frequencies and have larger current densities in their “on” state when compared to those made with other thin-film technologies, such as hydrogenated amorphous silicon or amorphous carbon.

Polysilicon technology has reached a maturity which enables reliable fabrication of high performance large area circuits [5, 6], however, intrinsic to the polycrystalline nature of the material is the problem of device-to-device variations in drain current [7]. Additionally, the high carrier mobility coupled with the body of the transistor being electrically floating lead to the deleterious “kink effect” [8], also seen in silicon-on-insulator (SOI) devices [9]. This manifests itself by a rapid increase in overall current at high drain bias due to the bipolar amplification of charge generated by impact ionization. Several fabrication techniques [10-13] have been developed which improve the quality of the film in an attempt to ensure the same number of grain boundaries (or none) are present in the channel of every device and advanced device structures have been implemented in order to mitigate the

kink effect. Device engineering techniques include: lightly-doped drain (LDD) [14-15]; gate-overlapping lightly-doped drain (GOLDD) [16] and drain field plate [17]. Their main role is to reduce the drain-field dependence of drain current, the main benefits being reduced power consumption in digital circuits [18] and improved signal amplification in analog blocks [19].

Source-gated transistors (SGTs) [20] are a class of FET in which the current is controlled by the effective height of a reverse-biased potential barrier at the source. In principle, SGTs could produce drain currents with a very small dependence on the drain field (low output conductance) and, at the same time, enter saturation at comparatively low drain voltage [21]. These characteristics are inherently favorable in terms of both power consumption and signal amplification, but they largely depend on the effectiveness of the mechanism which screens the source barrier from the drain field.

We have previously shown source-gated transistors made in polysilicon and comprising Schottky source barriers with very good output characteristics [22], and high-performance devices have been made in amorphous silicon [20, 21]. These devices require small or no changes to conventional staggered-electrode processes. As a consequence, it is envisaged that SGTs and conventional FETs can be made using the same technology, and even in the same fabrication process with minimal cost implications.

In this paper we investigate by numerical simulation the effect of a simple field-relief structure integrated in the source contact and compare these findings with measurements on the polysilicon structures. We subsequently develop recommendations for maximizing low-voltage gain, while keeping the influence of process variations to a minimum.

II. POLYSILICON SOURCE-GATED TRANSISTORS

Polysilicon *n-type* SGTs have been fabricated at the MiPlaza facility in Eindhoven, according to the recipe

described in [23], with and without field plates. Micrographs of otherwise identical SGTs are shown in Figure 1. The field plate is created by allowing the source metal to overlap the edge of the source window.

A cross-section of a typical device is shown in Figure 2. The source contact comprises a Schottky barrier, while the drain is made ohmic using an n^+ implant. The source-drain gap is denoted d while the construction of the field plate (FP) has two parameters: the length that the FP protrudes above the source-drain gap (l) and the thickness of the insulator that separates the semiconductor from the field plate (h). In the case of the fabricated devices, this insulator was silicon dioxide with a thickness of 120nm and FP length according to mask design was $4\mu\text{m}$. The source metallization of the device on the left was centered on the source window in the x direction, but as can be seen from Figure 1, misalignment during fabrication has resulted in an actual l of less than $2\mu\text{m}$. This simulates conditions which might be present in a real fabrication run on a large substrate.

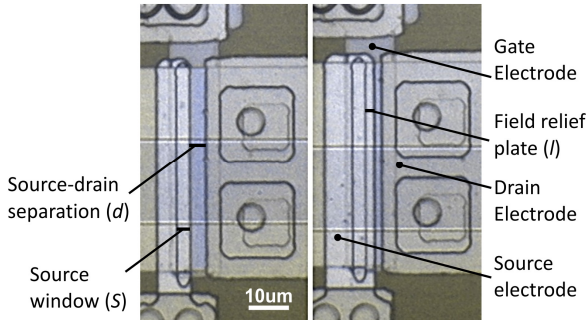


Figure 1. Micrographs of two source-gated transistors made in polysilicon, with source width $W = 50\mu\text{m}$, source length $S = 4\mu\text{m}$, drawn source-drain gap $d = 4\mu\text{m}$ (drain implant self-aligned to the gate). Left – no field plate; Right – $l = 4\mu\text{m}$ drawn ($2\mu\text{m}$ realized) field plate realized by overlapping the source electrode and the source window.

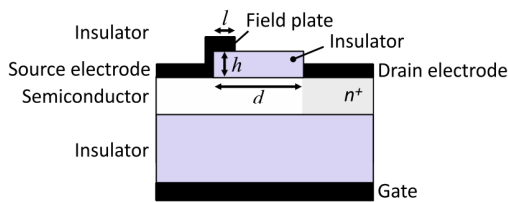


Figure 2. Schematic cross-section of an n -type source-gated transistor, showing the ohmic drain contact and Schottky source contact comprising a field plate of length l formed above an insulating layer of thickness h . The source-drain gap is denoted d .

The SGT device concept allows for very low saturation voltages and flat output characteristics [20, 23]. Due to the presence of the reverse-biased source barrier, saturation occurs when the semiconductor depletes at the source at a much lower voltage than in a conventional FET: $V_{SAT1} = (C_i / C_i + C_s) \cdot V_{SAT2}$, where $V_{SAT2} = V_G - V_T$ is the saturation voltage of a regular FET when the drain pinches off, C_i and C_s are the specific capacitances of the gate insulator and semiconductor, respectively, and V_T is the threshold voltage of the transistor [20]. Nevertheless, without adequate screening of the source from the drain field, the

saturation is poor when drain voltage is between V_{SAT1} and V_{SAT2} . Figure 3a illustrates the measured output characteristics of SGTs with and without field plate, of otherwise identical geometry and in the same bias condition. The current of the device which comprises a field plate is somewhat lower, but strong saturation begins well below V_{SAT2} , whereas in the device without the field plate, the slope of the curve in the region $\sim 1\text{V} < V_D < \sim 4\text{V}$ is substantially higher, leading to higher current by the time the FET channel saturates ($V_D > V_{SAT2}$) [20]. The intrinsic gain of both devices is shown in Figure 3b. It can be seen that the gain of the device with a field plate is around 10 times higher around $V_D = 2\text{V}$, which would allow operation as an amplifier from much lower supply voltages and thus minimize power dissipation.

Saturation in both devices is strong above V_{SAT2} , which is partly due to the SGT device architecture and partly to the fact that the source-drain gap (d) is fairly large. The curves in Figure 3a also show the absence of the kink effect which in conventional devices would lead to substantial drain current increase at high voltage, reducing amplification functionality. In fact, on similar polysilicon SGTs we have measured intrinsic gain above V_{SAT2} of up to 10^5 [24], which is several orders of magnitude higher than in conventional polysilicon FETs.

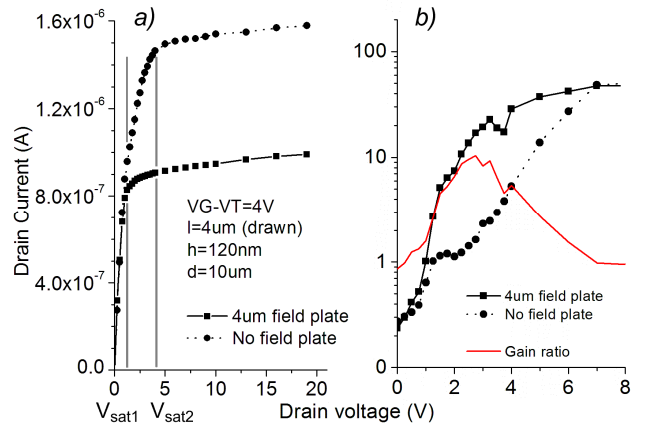


Figure 3. a) Output characteristics measured on polysilicon SGTs of identical geometry but differing in their field plate configuration; b) Intrinsic gain measured on the same structures at low drain bias. Polysilicon thickness $t_s = 40\text{nm}$; Equivalent oxide thickness $t_e = 300\text{nm}$; Cr source contact [22].

III. NUMERICAL SIMULATION

A. Simulation conditions and field plate architecture

Based on the markedly different characteristics of SGTs with and without field plate, it is of interest to investigate to what extent the field plate design (l and h) improves saturation and whether the presence of a field plate has adverse effects on other areas of device operation.

Two-dimensional (2-D) numerical simulations using Silvaco Atlas have been performed on a structure resembling the fabricated devices and the cross-section in Figure 2. The effect we are studying is generally confined to the region of operation where $V_D \leq V_{SAT2}$. Consequently, impact ionization

effects, which manifest predominantly at high drain voltage, have not been included in the simulation.

A bottom-gate structure has been generated, with 200nm SiO₂ as gate insulator and a 50nm polysilicon active layer. The drain contact was made ohmic by *n*++ doping, while the source contact was left undoped and a Schottky barrier was formed with the following parameters [25]: barrier height, $\phi_{B0}=0.3\text{eV}$; field-dependent barrier in the form of $\phi_B = \phi_{B0}(\alpha E + \beta E^{0.5})$, with $\alpha=3\text{nm}$; $\beta=0$. The metallization of the source was extended on top of the source-drain gap to form a field plate (FP) of length l and the insulator layer between the FP and the semiconductor was SiO₂, of thickness d (Figure 2). Several values were considered for these two parameters: $l = 100, 200, 500, 1000, 2000\text{nm}$ and $h = 10, 20, 50, 100, 200\text{nm}$.

B. Simulation of SGT operation

Figure 4 shows the simulated output characteristics for two devices (no FP and FP with $l = 500\text{nm}$ and $d = 50\text{nm}$) for three gate biases. It can be seen that the curves have the same shape as those in Figure 3a which were measured on the polysilicon devices. The discrepancy between the curves with and without FP is largest for higher V_G , which makes $V_{SAT2} = V_G - V_T$ larger and allows the current to increase over a larger range between V_{SAT1} and V_{SAT2} before it finally saturates due to pinch-off at the drain [20]. The same conclusion can be drawn as in the case of the measured devices: the performance of the SGT without FP is inadequate below V_{SAT2} and negates the advantage of the SGT over the FET in terms of high gain and low power.

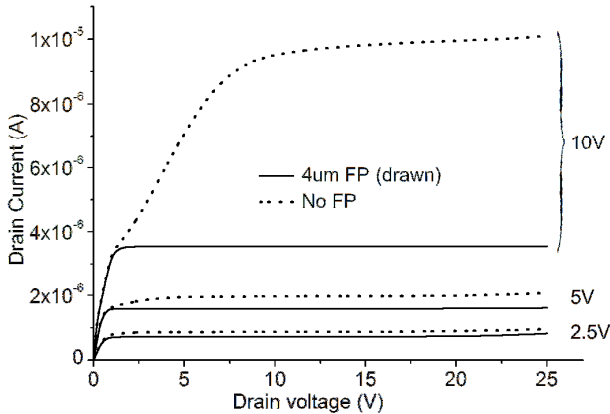


Figure 4. Simulated output characteristics showing the effect of the field plate with $l = 500\text{nm}$ and $h = 50\text{nm}$ (continuous line) at three different gate voltages. The same improvement in output impedance when V_D is between V_{SAT1} and V_{SAT2} [T-ED] shown in Figure 3 can be observed and the effect is stronger for curves for which V_{SAT2} is higher. $V_G = 2.5, 5$ and 10V .

The simulated structures show SGT behavior in other respects: a small V_{SAT1} is achieved and the drain current is modulated by the applied gate voltage.

The effect of the gate voltage for a device without source field plate can be seen in Figure 5a, where we show the effective barrier height, ϕ_B (represented by the difference

between the conduction band edge and the Fermi level in the metal; nominal value $\phi_{B0}=0.3\text{eV}$) along the length of the source electrode for different gate biasing conditions. At $V_G = 0\text{V}$, there is no gate-induced barrier lowering due to electric field, but as we increase V_G we see the barrier lowering along the length of the source. Moreover, the edge of the source closest to the drain ($x = 0$ in Figure 5a) is subject to more pronounced barrier lowering as explained by the 2-D nature of the SGT's operation [20, 26]. This confirms previous simulations in which the majority of the current was emitted by the first few hundreds of nanometers of source length [22, 26].

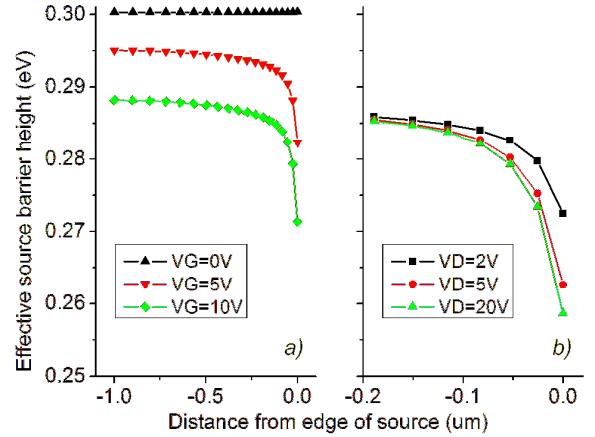


Figure 5. Simulated source barrier height vs. distance from the source edge for a SGT without a source field plate. Left: applied gate bias lowers the barrier at the edge of the source electrode ($V_D = 5\text{V}$); right: the applied drain field has an undesired barrier-lowering effect ($V_G = 12\text{V}$).

We now turn our attention to the effect on the drain bias on ϕ_B . Figure 5b illustrates the barrier-lowering effect of V_D . This effect is unwanted, since it degrades the output conductance, g_d , of the SGT in saturation, leading to poorer amplification characteristics (intrinsic gain $A_V = g_m / g_d$) and increased power consumption. From the figure we can observe that increasing V_D from 2V to 5V ($V_{SAT1} < V_D < V_{SAT2}$, where source saturation has occurred but the FET channel is still in the linear region [20]) there is a large variation of ϕ_B with V_D . However, increasing V_D further, above $V_{SAT2} = V_G - V_T$ has a minimal impact on ϕ_B ; beyond drain pinch-off, the drain-induced field at the source remains largely unchanged. As a consequence, the change in drain current with drain voltage above V_{SAT2} is small.

C. Field plate architecture and effect of drain field on source barrier

Minimizing the drain field dependence (output conductance - g_d) in the region $V_{SAT1} < V_D < V_{SAT2}$ would lead to very flat curves at drain voltages far less than $V_G - V_T$, an attractive prospect for linear drivers and low-power amplifiers. As shown in Figures 6 and 7, the source field-relief plate is an effective route for improving the output characteristics. As h decreases and l increases, the

characteristics saturate at much lower voltages, as expected for SGTs. Devices with long l or thin h are usable as constant current sources, active loads, amplifiers, etc. at much lower voltages than SGTs with no (or poorly designed: short l or thick h) field plate, allowing better power efficiency.

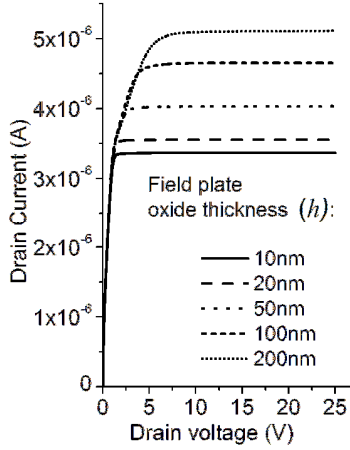


Figure 6. Output characteristics for $V_G = 5V$ and devices with different field plate insulator thicknesses; $l = 500nm$.

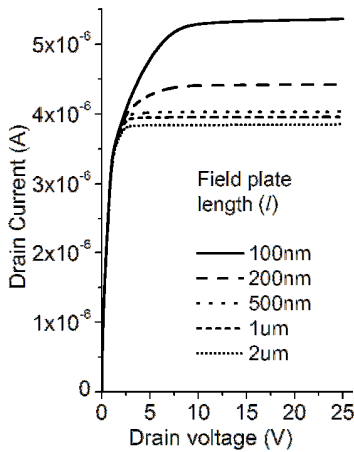


Figure 7. Output characteristics for $V_G = 5V$ and devices with different field plate lengths; $h = 50nm$.

Figure 8 shows the effective values of barrier height at the edge of the source obtained by simulation for a variety of field plate lengths (l), field plate insulator heights (h) and different drain bias conditions. It can be seen that for the very thin field plate oxide, the barrier lowering due to drain field is virtually zero (curves at high and low V_D are superimposed) for all but the shortest field plate. The effectiveness of the field plate decreases as the insulator is made thicker, resulting in a more pronounced barrier lowering at high V_D . There is little difference between the curves for $V_D = 5V$ and $V_D = 20V$ for reasons discussed in the previous section. However, these curves diverge for the shortest field plates which reside far above the semiconductor (the least effective designs). We also observe that the curve obtained at $V_D = 5V$, which is in the region of greatest interest ($V_{SAT1} < V_D < V_{SAT2}$) is strongly dependent on field plate length for low h , but is almost

completely flat when h increases to 200nm, in which case it is too distant from the semiconductor to play a role in screening the source contact from the drain field. This can also be seen in Figure 9, where we show the longitudinal potential distribution in the vicinity of the active corner of the source for the three values of h . For the given bias condition, the design with $h = 200nm$ offers effectively no screening, as the potential difference (approx. 3V) is dropped in around 100nm of semiconductor from the edge of the source, and large fields are generated in that region, leading to the barrier lowering effect seen in Figure 8c. Lower values of h permit far better screening: at $h = 10nm$, the potential drop in the x axis around the edge of the source is very small and spread around many hundreds of nanometers, producing negligible electric field in the x direction.

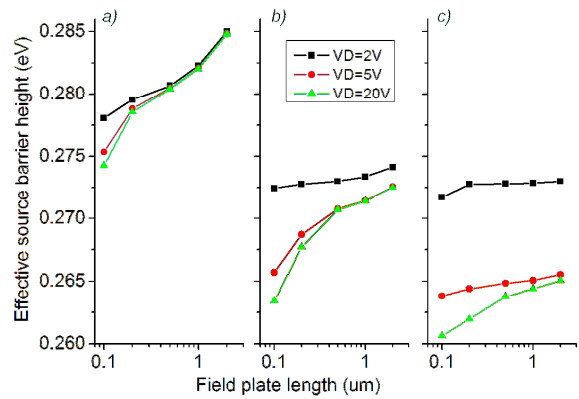


Figure 8. Effect of field plate length on the source barrier lowering due to drain field for three given field plate insulator thicknesses at $V_G = 12V$. a) $h = 10nm$; b) $h = 50nm$; c) $h = 200nm$.

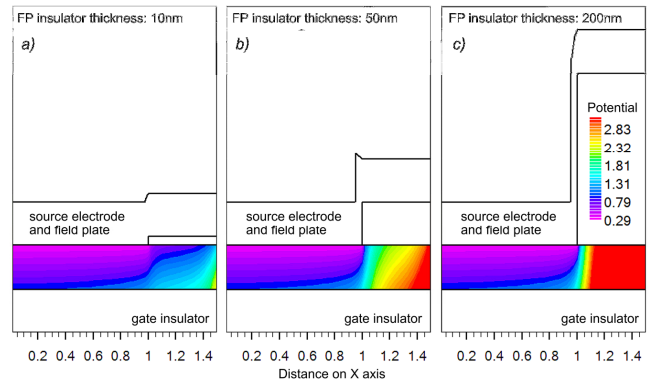


Figure 9. Distribution of longitudinal potential in the source region of the semiconductor for $l = 0.5um$, $V_D = 25V$, $V_G = 12V$ and: a) $h = 10nm$; b) $h = 50nm$; c) $h = 200nm$.

Figure 10 shows the barrier lowering effect of drain voltage versus the thickness of the field plate insulator. It is apparent that the very short field plate has a limited effect (large modulation of barrier height by V_D) regardless of h . For longer field plates and if h is lower than about 50nm, there is little drain field dependence of the effective barrier height, and the thinner the insulator, the higher the effective barrier

height at any drain bias. Above that value of h , the field plate loses its effectiveness regardless of l .

The potential distribution around the edge of the source (Figure 11) shows a large drop and a large electric field in the x direction for the short field plate. Longer field relief structures permit the spreading out of this potential drop over a much larger distance, thus reducing the magnitude of the field at the source edge.

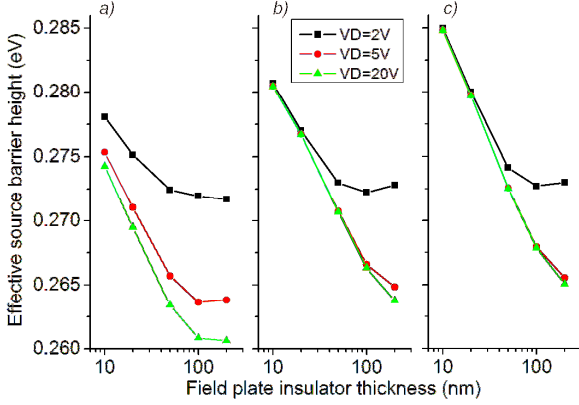


Figure 10. Effect of field plate insulator thicknesses on the source barrier lowering due to drain field for three given field plate lengths at $V_G = 12V$. a) $l = 0.1\mu m$; b) $l = 0.5\mu m$; c) $l = 2\mu m$.

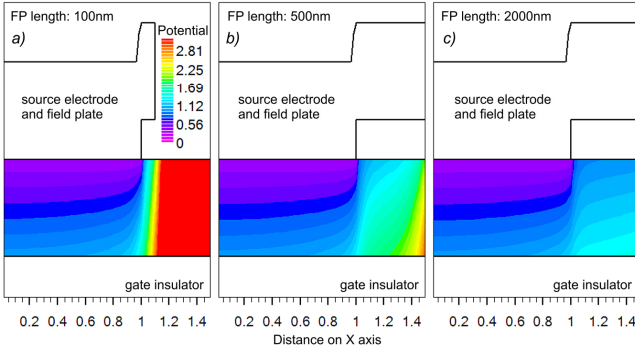


Figure 11. Distribution of longitudinal potential in the source region of the semiconductor for $h = 20nm$, $V_D = 25V$, $V_G = 12V$ and: a) $l = 0.1\mu m$; b) $l = 0.5\mu m$; c) $l = 2\mu m$.

D. Intrinsic gain increase at low drain voltage

Good field plate designs are extremely effective at screening the source from the drain field. Figure 12a shows the intrinsic gain calculated from simulations for different values of h . The low-voltage gain drastically increases as the field plate insulator becomes thinner: around $V_D = 2V$, a $\sim 20x$ is obtained when h changes from 100nm to 20nm. We expect a similar increase in gain at low voltage in the fabricated devices (Figure 3b) through the optimization of h (from 120nm to 20nm), to more than two orders of magnitude higher than in the device with no field relief structure.

We plot the minimum drain voltage at which the intrinsic gain reaches 100 in Figure 12b. Operation below 2V can be achieved if h is several tens of nm. The anomalous increase for $h=10nm$ is due to the effect of the field plate around the

threshold of the device. Figure 13 shows that the most effective field plates also behave as back gates which retard the turn-on of the device, lowering the current around threshold and implicitly g_m and intrinsic gain. At higher V_G , this effect all but disappears.

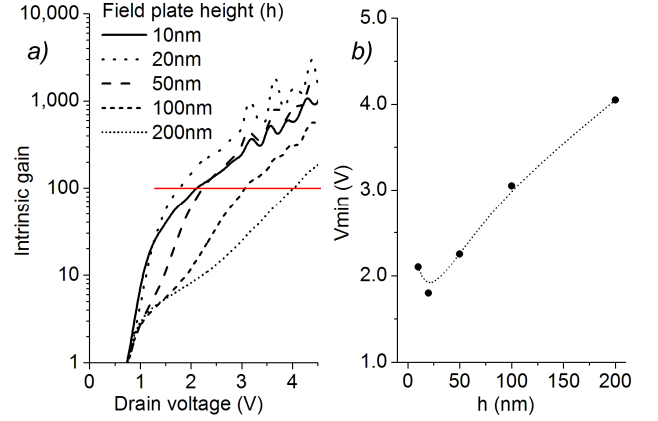


Figure 12. a) Simulated intrinsic gain vs. field plate height (h) for field plate length $l = 500nm$; b) Minimum voltage at which the curves in a) reach 100.

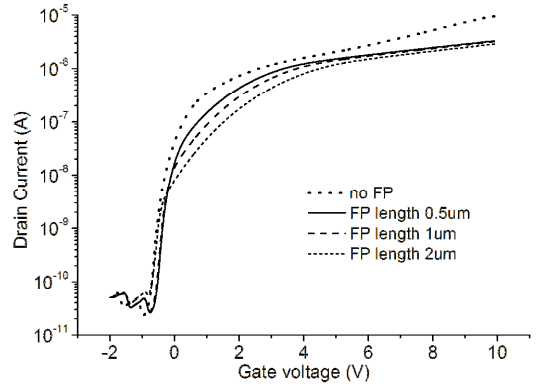


Figure 13. Simulated transfer characteristics of SGTs with different field plate lengths and $h = 20nm$. It can be seen that longer field plates degrade the characteristic around threshold and, in the extreme, lower the maximum attainable current. $V_D = 10V$.

E. Energy efficient operation

Through simulation, we have studied the minimum power dissipation in SGTs and FETs. Since $P = V_{SAT} \cdot I$, SGTs with different field plate configurations and a FET with the same geometry were biased at the same drain current and the saturation voltages recorded and compared. For this purpose, the saturation voltage was defined as the minimum drain voltage for which the current is within 1% of its saturated value. Figure 14 shows the minimum power dissipation of the SGTs as a ratio of the FET power. The curves in Figure 14a illustrate the behavior of the SGTs when biased just above threshold (see previous section and Figure 13). For higher currents, the very effective field plate configurations (small h) improve power consumption by more than 50% versus the FET.

Intrinsic gain values greater than 100 were obtained at $V_D = 2V$, which open the possibility of building high-gain SGT amplifiers with inexpensive large-area electronic techniques. Additionally, the low-voltage operation allows the design of low power linear drivers and amplifiers.

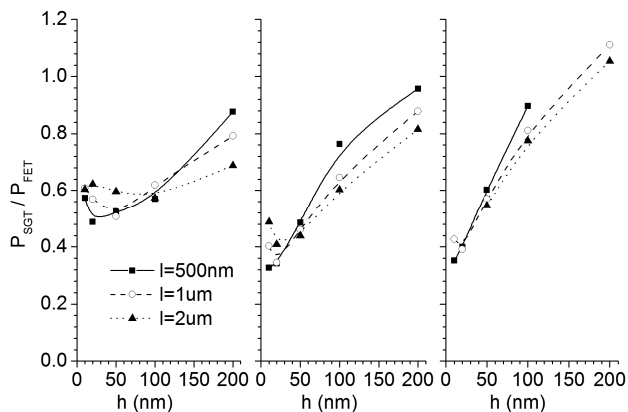


Figure 14. SGT power dissipation as a ratio of the power of a FET with identical geometry but an ohmic source contact; $I_D =$ a) $1\mu A$; b) $2\mu A$; c) $3\mu A$.

F. Design-for-manufacture considerations

The barrier-lowering effects shown in Figures 8 and 10 are numerically specific to the transistor design and material system considered, but the trends derived from the analysis are valid and independent of process.

From a manufacturability point of view, first consideration of the viability of realizing very thin field plate insulators (low h) is required. Techniques for nanometer-scale insulating layers have been proposed [27], but for more traditional materials, such as silicon dioxide, mechanical considerations, uniformity and repeatability of thickness limit the lower range of h to several tens of nm. As the analysis suggests (Figure 10b) these insulator dimensions are suitable.

The second aspect we need to take into account in fabrication is the impact of potential misalignments of the source metal (which includes the field plate) with respect to the source contact (see Figure 1) which can lead to very different output characteristics from devices designed to be identical. For instance, by looking at the $V_D = 5V$ curve in Figure 8b we can conclude that devices with field plates designed to be 200nm long but misaligned by 100nm will have a large variation in their effective source barrier heights under a given bias and, implicitly, quite different drain currents. Devices with short l will be hard to match consistently. By way of contrast, the same curve has a much lower slope around and above $l = 1\mu m$. In the technology we have used, $l = 1\mu m$ proves to be optimal, as longer field plates may have a detrimental effect on g_m around threshold (Figure 13).

IV. CONCLUSIONS

We have investigated the effectiveness of field relief

structures built into the source electrode of polysilicon source-gated transistors (SGTs) through a combination of measurements and numerical simulations.

For the given fabrication process, a source field plate $1\mu m$ long and 20nm away from the semiconductor offers good screening from drain field while minimizing the impact of misalignments during fabrication.

More generally, the presence of a good field plate leads to very low output conductance in saturation and opens up the possibility of operating these devices at very low drain voltages with good gain characteristics. Since metal layers overlapping contact windows are standard structures in semiconductor device fabrication, we expect the incorporation of source field plates to be possible in most established thin-film technologies.

Numerical simulations reveal that, compared to devices without a field plate, low-voltage gain increases by two orders of magnitude when a simple field relief structure is built into the source contact. In the SGTs considered, intrinsic gain reaches 100 around $V_D = 2V$ and rises up to more than 10,000 in strong saturation owing to the absence of the kink effect. The minimum power dissipation in these devices is more than 50% lower than in FETs made in the same technology and operating at the same drain current.

We have shown that SGTs with effective field plates can operate in regimes inaccessible to conventional FETs and so can act as energy-efficient, high-gain amplifiers and precision linear drivers for analog applications in large area electronics.

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