Polysilicon Thin-Film Source-Gated Transistors for Mixed Signal Large Area Electronics

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Abstract

As the applications of Large Area Electronics are becoming increasingly widespread, ease of fabrication of comparatively large electronic circuits and cost are important factors which favour thin-film technologies over their bulk counterparts. However, the quality of the semiconductors used in these processes is inferior to the semiconductor of choice of the industry, crystalline silicon, and this limits the speed, power efficiency and functionality of the resulting electronic devices.

The Source-Gated Transistor (SGT) is a relatively new type of Field Effect Transistor (FET). Its structure and operation are fundamentally different from the standard FET, even though both devices use the same fabrication technology. These structural changes result in higher speed, better analog performance and lower leakage currents than those of conventional FETs when SGTs are made in disordered semiconductor.

This work assesses the operation and performance of SGTs which have a Schottky source barrier, through measurements performed on polysilicon structures built at MiPlaza, Eindhoven, The Netherlands. It is found that the devices exhibit the standard characteristics of FETs, namely high output impedance in saturation, low saturation voltage and independence of drain current on source-drain gap. Additionally, intrinsic gain figures of over 10,000 were measured.

It is shown through computer simulations how the Schottky barrier can be replaced with a bulk unipolar implanted diode, with the aim of producing a barrier which is higher to start but easier to pull down. The resulting device, the bulk unipolar SGT (BUSGT) can achieve very high on/off current ratios and low activation energy for the on-current.

Finally, some analog circuit applications for source-gated transistors are proposed. These exploit the characteristics of SGTs: high output impedance and low saturation voltage are beneficial in gain stages and active load circuit blocks, while the potentially high temperature coefficient of the drain current can be exploited in high-sensitivity integrated temperature sensors.

Declaration

This thesis and the work to which it refers are the results of my own efforts. Any ideas, data, images or text resulting from the work of others (whether published or unpublished) are fully identified as such within the work and attributed to their originator in the text, bibliography or in footnotes. This thesis has not been submitted in whole or in part for any other academic degree or professional qualification. I agree that the University has the right to submit my work to the plagiarism detection service TurnitinUK for originality checks. Whether or not drafts have been so-assessed, the University reserves the right to require an electronic version of the final document (as submitted) for assessment as above.

Radu Alexandru Sporea

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A complex project is never the work of a single person, and this is particularly true in the case of a PhD studentship, when one needs to accumulate, to grow and to develop by his own strength but with the essential help of superiors and peers.

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List of publications

Journal publications

1. **R. A. Sporea**, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, "Intrinsic Gain in Self-Aligned Polysilicon Source-Gated Transistors", *IEEE Trans. Electron. Devices*, vol. 57, iss. 10, Oct. 2010.
2. X. Guo, **R. Sporea**, J. M. Shannon, S. R. P. Silva, "Down-scaling of Thin-Film Transistors; Opportunities and Design Challenges", ECS Transactions 22 (1), pp. 227-238, 2009.
3. **R. A. Sporea**, M. J. Trainor, N. D. Young, X. Guo, J. M. Shannon, S. R. P. Silva, "Performance Tradeoffs in Source-Gated Transistors", *invited for special edition of Solid-State Electronics*, under review, December 2010.

Published conference proceedings arising from oral presentations

1. **R. A. Sporea**, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, "Performance Tradeoffs in Source-Gated Transistors", *Proceedings of the European Solid State Device Research Conference ESSDERC 2010*, Seville, Spain, 13-17 Sep. 2010.
2. **R. A. Sporea**, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, "Performance Improvements in Polysilicon Source-Gated Transistors", *DRC2010 Digest*, pp. 245 – 246, South Bend, IN, USA, 21-23 Jun. 2010.
3. **R. A. Sporea**, Xiaojun Guo, J. M. Shannon and S. R. P. Silva, "Effects of Process Variations on the Current in Schottky Barrier Source-Gated Transistors", *Semiconductor Conference CAS 2009 Proceedings*, vol. 2, pp. 413 – 416, Sinaia, Romania, Oct. 2009.

Conference proceedings arising from oral presentations

1. **Radu A. Sporea**, Xiaojun Guo, J. M. Shannon and S. Ravi P. Silva, "Polysilicon Source-Gated Transistors for Mixed-Signal Systems-on-Panel", *218th ECS Meeting*, Las Vegas, Nevada, October 10-15, 2010.
2. **R. A. Sporea**, J. M. Shannon, S. R. P. Silva, "Properties of Source-Gated Transistors in Polysilicon", *PRIME2010 Digest*, Berlin, Germany, 18-21 Jul. 2010.

3. **R. A. Sporea**, Xiaojun Guo and J. M. Shannon, "Bulk Unipolar Source-Gated Transistors", *Proceedings of ITC2009*, Paris, France, 1-3 Mar. 2009.

Other oral presentations and posters

1. **R. A. Sporea**, Xiaojun Guo and J. M. Shannon, "Bulk Unipolar Source-Gated Transistors", Postgraduate student conference, University of Surrey, March 2009.
2. **R. A. Sporea,** "Source-Gated Transistors", Nanoelectronics Group Seminar, University of Surrey, January 2009.
3. **R. A. Sporea,** "Source-Gated Transistors", Postgraduate student poster competition, University of Surrey, June 2008.

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Glossary of terms

Symbol	Significance	Value	Unit*
E, $\mathcal{E}$	Electric field		V/m
ε_0	Permittivity of free space	8.854×10^{-12}	F/m
ε_s	Permittivity of the semiconductor		-
ε_i	Permittivity of the insulator		-
J	Current density		A/m^2
k	Boltzmann's constant	1.381×10^{-23}	J/K
μ	Carrier mobility		$cm^2/V.s$
N_D	Dopant atom concentration		cm^{-3}
Φ	Height of potential barrier		eV
Φ_{Bn}	Schottky barrier height on *n-type* semiconductor		eV
Φ_B'	Effective barrier height		eV
Φ_m	Work function of metal		eV
q	Magnitude of electronic charge	1.602×10^{-19}	C
T	Temperature		K
t_i	Insulator thickness		m
t_s	Semiconductor thickness		m
C_i	Insulator capacitance per unit area		F/m^2
C_S	Semiconductor capacitance per unit area		F/m^2
V	Voltage		V
χ_S	Electron affinity of semiconductor		V
I_D	Drain current		A
V_{DS}	Drain – source voltage		V
V_{GS}	Gate – source voltage		V
V_{SAT}	Saturation drain voltage		V

List of abbreviations

BUSGT	Bulk unipolar source-gated transistor
CMOS	Complementary metal-oxide-semiconductor
FET	Field-effect transistor
LDD	Lightly doped drain
GOLDD	Gate-overlapping LDD
LTPS	Low temperature polysilicon
MOS	Metal-oxide-semiconductor
PECVD	Plasma-enhanced chemical vapour deposition
SBSGT	Schottky barrier source-gated transistor
SGT	Source-gated transistor
TFT	Thin-film transistor
FESGT	Field emission SGT

Chapter 1. Introduction

1. 1. Background and motivation

Since the middle of the last century the field of electronics has evolved from being the enabler of telephony, television and radio to the cornerstone of modern society. What is more remarkable is that the majority of the world's population has unprecedented access to information at manageable cost. Indeed, it is hard to imagine how the contemporary tasks of complex telecommunications, transportation, data handling and storage could be performed without the use of computers and electronic devices.

The transistor, a device deemed by its inventors to be no more than a laboratory curiosity, made its first appearance as a real device in Bell Laboratories in 1947 and soon became an indispensable component in electronic circuits. But the transistor reached its extraordinary prevalence through the development by Noyce and Kilby of arguably the finest application of a component with no apparent purpose: the integrated circuit.

Building several transistors on the same piece of semiconductor material enables faster and more reliable operation and lower costs due to economies of scale. Silicon has emerged as the preferred semiconductor owing to its electrical properties (and to its highly desirable insulating oxide), availability and ease of processing, and the field-effect transistor (FET) architecture has gained unanimous acceptance by virtue of its defining characteristics, such as zero bias current. As fabrication technology improved over the decades, the development of general-purpose silicon circuits has followed two major paths.

The first direction is high speed, highly integrated circuits with areas ranging from a few hundreds of square microns to a few square centimetres. These circuits are fast, precise and represent the state of the art in miniaturization. Over the past forty years, the industry has remained faithful to a self-imposed roadmap of technological improvements which see the doubling of component density roughly every two years, known as Moore's Law. The cost and speed of individual transistors have followed similar trends,

to the point where chips with hundreds of millions of transistors are now computing and storing data in a wide array of applications, from personal multimedia devices and information access platforms, to traffic control systems, weather modelling and space-going vehicles. We refer to the forefront of this technology as ultra-large-scale integration (ULSI).

The second path taken by electronics is that of large area applications, where speed and component density take a secondary role to the size requirement of man-machine interface devices. Flat-panel display screens found in media players, computers and television sets are the perfect example; they are essential components in the visually-rich, information-driven society of the 21st Century. In designing and making these circuits the emphasis is put on reliability and cost, which in turn is driven by the speed at which manufacture can take place.

The performance gap between large area electronics and highly integrated circuits is considerable, particularly in the area of analog signal processing, sensing and control. With the emergence of new technologies such as those based on organic semiconductors, in which low cost is favoured even more, this gap is likely to widen. This gap exists in the first place as a result of the vastly inferior quality of the semiconductors used in large area circuits in contrast to the extremely good electrical properties of crystalline silicon grown for high performance ULSI chips.

As technology develops, it is to be expected that large-area electronic technology will simultaneously evolve into densely packed high speed digital applications built on large substrates and into very low cost disposable chips. However, analog applications will continue to remain a problem if the standard FET continues to be used. The FET's limitations arise as it is scaled down (leakage current, low tolerance to manufacturing errors, poor saturation and kink effect, etc.) or when built in poor quality semiconductors (low switching speed, stability issues, etc.).

Over recent decades, most of the advances in microelectronics and its applications have been due mostly to the development of semiconducting materials and insulators. Here we address the transistor structure itself and examine how changing its constitution and mode of operation can improve the performance of many electronic circuits.

1. 2. Aim of this work and original contribution

A form of transistor called the source-gated transistor (SGT) has been developed over the past few years. Its electrical characteristics enable it to perform better than the standard field-effect transistor (FET) in some aspects of circuit operation.

This work investigates the performance of SGTs with a Schottky barrier source built in polysilicon, with the aim of establishing the areas where the SGT improves circuit performance compared with the FET. Some appropriate applications are proposed and performance gains are examined.

Polysilicon technology was chosen on account of its balance between costs and electrical characteristics as a potential carrier for mixed-signal (analog and digital) circuits built using a combination of SGTs and FETs.

An original contribution to the advancement of the state of the art has been made in the following:

- Characterisation and analysis of self-aligned polysilicon Schottky barrier source-gated transistors;
- Measurements of SGT and FET electrical characteristics on the same device;
- Description of the double saturation mechanisms in SGTs;
- Analysis of SGT gain characteristics in relation to controlled doping and other process parameters;
- Simulation of a new structure: the bulk unipolar source-gated transistor (BUSGT);
- Outline the suitability of polysilicon SGTs for circuit applications and proposals for such applications.

1. 3. Structure of the Thesis

A brief overview of Semiconductor Physics is presented in Chapter 2. This section outlines the properties of the most prevalent semiconductor, silicon, including the specific characteristics of amorphous silicon and polysilicon, which was used for making the devices characterised in Chapter 5. Also described are the mechanisms through which unipolar devices achieve their practical operation, with an emphasis on Schottky barriers, bulk unipolar diodes and field-effect transistors (FET). Some of the performance characteristics of FETs which are relevant to low power mixed signal circuits are briefly introduced.

The hardware setup and software tools employed for electrical measurements and subsequent data analysis are described in Chapter 3. The numerical simulation package used for SGT device modelling and mixed-mode circuit simulation is also briefly presented.

Chapter 4 explains the operating principles of the source gated transistor and includes an analysis of prior published results.

The measurements on polysilicon Schottky barrier source-gated transistors (SBSGTs) designed and fabricated in collaboration with Philips Research are discussed in Chapter 5. The devices are proved to be in fact operating as SGTs and an assessment is made on current uniformity temperature effects. Measured results are compared to the theoretical figure that one expects for the barrier lowering constant in metal-silicon contacts. The consequences of doping on the electrical characteristics, and specifically on intrinsic gain, are investigated with a view to establishing the suitability of polysilicon SGTs for high performance mixed-signal large area electronic circuits. The second part of this chapter describes the first simulation results of the novel BUSGT structure. The potential advantages of this type of device compared to the SBSGT are emphasised.

In Chapter 6, several circuit applications using SGTs are investigated: integrated temperature sensors, current mode logic, gain stages and active loads. It is shown that considerable performance improvements can be obtained if these circuits are built with SGTs in the key areas. The effects of process variability on source-gated transistors are examined and recommendations made.

The final chapter presents the conclusions of this work and a summary of what has been accomplished. This section also contains an outlook on future developments following this project.

Chapter 2. Semiconductors and unipolar devices

2.1. Introduction

The year 2010 has seen the creation of an integrated circuit having over three thousand million transistors for a consumer-level commercial application [1], the computation power of which surpasses that of leading edge supercomputers of 10 years ago and at a production price of a few hundred dollars. Without the use of low-power circuit techniques, state of the art digital chips would suffer thermal damage from the excessive leakage current alone.

The technology used to make them is the mature, reliable, high performance and rapidly-evolving CMOS (complementary metal-oxide-semiconductor). Silicon field effect transistors (FETs) of *n* and *p* type are combined to create the logic gates for data processing. Because the transistors are used as switches and as a requirement for fast tripping time and high density of logic circuitry, these devices have been scaled down continually in the past 40 years. On average, a doubling of density occurs every 18 – 24 months, following a trend observed by Gordon Moore [2] and known as Moore's Law. Circuit operating speeds have been following the same trend, but recently the speed increase has been tempered by constraints imposed by interconnect delays [3] over ever-bigger dice and power density [4]. A growing proportion of the average dissipated power is in the form of idle power consumption due to leakage currents [5] (notably: gate leakage by tunnelling through the insulator, drain-induced barrier lowering – DIBL, leakage current in weak inversion, gate induced drain leakage – GIDL, diffusion junction leakage current, parasitic bipolar punch-through, etc).

MOSFET scaling has its proven benefits in terms of increasing functionality in digital applications, but as feature sizes go below a few hundreds of nanometres, leakage currents due to a multitude of phenomena start to contribute significantly to overall

power consumption. In analog circuits problems relating to transistor performance arise once channel lengths venture below about 1μm, most notably through degradations in saturation characteristics and device matching.

While CMOS can be used successfully to create increasingly complex, ultra-large scale integration (ULSI) circuits, the high costs per unit area of finished chip make the technology unsuitable for applications such as:

- Very cheap circuits for mainstream electronics;
- Disposable circuits;
- Ubiquitous electronics and man-machine interfaces;
- Large area electronics.

For these applications other technologies are more suited and are either in use or being investigated as alternatives.

By the nature of its atomic array, silicon can exist in an amorphous state and a crystalline one, both suitable for making electronic devices, but targeted at different types of applications. Crystalline silicon's main advantage is high performance (operating frequency, integration density, small process variations) and an established set of technological processes, hence its widespread use in highly integrated electronic applications such as general use microprocessors (CPUs), application specific integrated circuits (ASICs) and digital signal processing (DSPs) chips.

Amorphous silicon and polycrystalline silicon are well suited to large-area electronics and have been successfully used to create applications such as backplanes for large area display screens, solar cells and image sensors. The main advantages of these technologies are the large throughput in manufacturing and relatively low cost of production stemming from economies of scale.

2.2. Semiconductors

2.2.1. Crystalline silicon

Silicon is a group four element in the periodic table. Atoms are covalently bonded with four neighbours in a tetrahedral crystalline configuration. The band gap [6],

$$E_G = E_C - E_V = 1.12eV \tag{2.1}$$

is high enough to impede the random thermal excitations of charge carriers from the valence band to the conduction band, but low enough to allow carriers excited by thermal or optical energy to reach the conduction band. As such, at thermal equilibrium and in the absence of an electrical field, the valence band is completely occupied and no carriers exist in the conduction band at absolute zero temperature [7].

In its pure state, crystalline silicon is an intrinsic semiconductor, that is to say the semiconductor contains no electrically active impurities. The Fermi energy level, $\mathbf{E_F}$, which represents the energy at which there is a probability of ½ of finding a free carrier, is halfway between the valence and conduction band edges (Figure 2.1).

Intrinsic carrier concentrations in silicon at room temperature are on the order of $\mathbf{n_i} = 10^{10}\text{cm}^{-3}$. The number of *n-type* and *p-type* carriers is equal so that:

$$np = n_i^2 \tag{2.2}$$

The semiconducting properties of silicon are tuned by doping with impurities, which are atoms that have a different number of valence electrons. To become electrically active, they are introduced into the crystalline structure of the silicon, and in this process they dislodge one of the silicon atoms and form bonds with the neighbouring atoms.

Group V elements, like nitrogen, phosphorus or arsenic, have five valence electrons. When they are introduced into a silicon lattice, they use four of their valence electrons to bond with four neighbouring silicon atoms. For every donor atom there is one free electron which can participate in current transport. Donors create a shallow energy state in the band gap close to the conduction band, and in the process shift the Fermi level to a higher energy (Figure 2.1).

Similarly, Group III elements, such as boron, have three valence electrons, which they use to bond covalently to neighbouring silicon atoms. The absence of a fourth electron is called a hole and can be visualised as a positively charged particle which is free to participate in current transport due to its delocalised nature. Elements in Group III are called acceptors and their presence brings the Fermi level closer to the valence band edge.

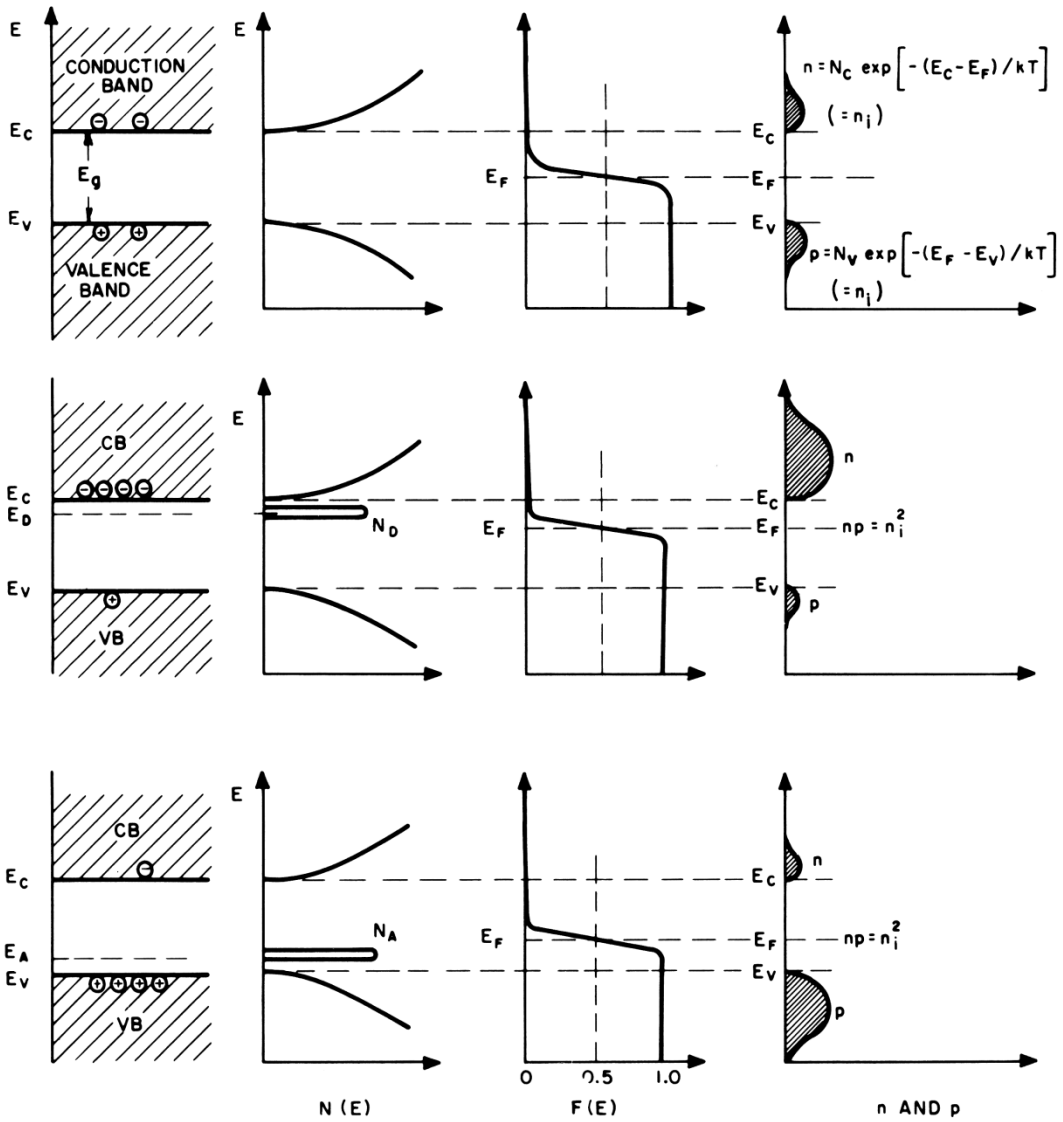


Figure 2.1. Schematic band diagram, density of states, Fermi-Dirac distribution and carrier concentration plot for intrinsic (top), n-type (middle) and p-type semiconductor (bottom) at thermal equilibrium. [7]

To conserve charge neutrality, the following equation needs to be satisfied:

$$n + N_A = p + N_D, \tag{2.3}$$

where $\mathbf{N_A}$ and $\mathbf{N_D}$ are the concentrations of ionised acceptor and donor states, respectively; **n** and **p** denote the concentration of donors and acceptors.

For a highly *n-type* doped semiconductor

$$n_{n0} \approx N_D \tag{2.4}$$

and

$$p_{n0} \approx \frac{n_i^2}{N_D}. \tag{2.5}$$

If we assume $\mathbf{E_C}$ to be the energy at the bottom of the conduction band, $\mathbf{N_C}$ is the effective density of states in the conduction band edge and $\mathbf{E_I}$ the intrinsic energy level (middle of the band gap), then:

$$E_C - E_F = kTln\left(\frac{N_C}{N_D}\right) \tag{2.6}$$

and

$$E_F - E_I = kTln\left(\frac{n_{n0}}{n_i}\right). \tag{2.7}$$

Similarly, for high *p-type* doping:

$$p_{p0} \approx N_A, \tag{2.8}$$

$$n_{p0} \approx \frac{n_i^2}{N_A}, \tag{2.9}$$

$$E_F - E_V = kTln\left(\frac{N_V}{N_A}\right) \tag{2.10}$$

and

$$E_I - E_F = kTln\left(\frac{p_{p0}}{n_i}\right), \tag{2.11}$$

where $\mathbf{N_V}$ is the density of states in the valence band and $\mathbf{E_V}$ is the energy at the top of the valence band.
In a doped semiconductor, the Fermi level changes and Equation 2.2 is always satisfied.

Initially, doping was achieved by diffusion from a substrate, but ion implantation has been common practice in the past three decades, mainly due to the degree of control and to the repeatability it provides [8].

A parameter which is important in electronic devices is the charge carrier mobility in the semiconductor. Mobility is defined by:

$$\mu = \frac{v}{\mathcal{E}} \tag{2.12}$$

where v is the carrier drift velocity and $\mathcal{E}$ is the electric field.

High mobility is desired in order to obtain high operating speed of devices. Intrinsic silicon has a bulk mobility of 1400 $cm^2/V \cdot s$ for electrons and 450 $cm^2/V \cdot s$ for holes. Mobility is dependent on factors such as lattice scattering (with pronounced temperature dependence – $\propto T^{-2.4}$ for electrons in silicon) and dopant concentration [7]. Surface mobility can be much smaller than the bulk value due to surface scattering, and this has consequences on the operation of field-effect transistors which rely on a thin inversion layer at the semiconductor-insulator boundary for current transport.

For nearly half a century, crystalline silicon has been the semiconductor of choice in the majority of electronic applications, owing to its combination of electronic properties (and the ease with which these are controlled) and fabrication costs. Large ingots of single-crystal silicon with extremely low defect densities are grown [9] for use in high performance integrated circuits. The absence of defects and the lattice order over vast areas allow the fabrication of fast, very high density and reliable devices and implicitly complex electronic circuits. The earliest designs included single devices, such as rectifiers and transistors, and small-scale integration (SSI) of several components which formed logic gates, latches, and analog circuit blocks. Today's state of the art is represented by ultra-large-scale integration (ULSI) circuits such as multi-core general-use microprocessors (CPU) [10] and highly parallel vector processing engines (GPGPU) [11].

2.2.2. Amorphous silicon (a-Si)

The economic viability of crystalline silicon for large-area electronic applications, such as display screens, is greatly reduced due to the cost of the processing equipment needed for large wafers and by the loss of yield that results from building larger circuits on a substrate with a small but non-zero density of defects. For large-area electronics, amorphous or polycrystalline silicon are preferred, due to the comparatively low cost of fabrication, low temperature processing and less stringent performance requirements of the applications.

The amorphous state of silicon is characterised by long range disorder (Figure 2.2). The bonds of the atomic lattice vary in terms of their lengths and angles. As a result of this distribution of bond angle and length, the valence and conduction band are not precisely delimited in energy, as is the case in crystalline silicon. Rather, there are energy states that extend into the band gap both up from the valence band and down from the conductance band. (Figure 2.3) [12] There are also a significant proportion of unfulfilled (or dangling) bonds which further worsen the electronic quality of the material. These can be suppressed by bonding to hydrogen atoms in a process called hydrogenation [13-15]. The electronic devices made with the resulting material, hydrogenated amorphous silicon (a-Si:H), show improvements in leakage current, stability, etc. Just like crystalline silicon, a-Si can be doped to change its electrical characteristics [16].

In a-Si:H carrier mobility is orders of magnitude lower than in the case of crystalline Si (on the order of 1 $cm^2/V \cdot s$ for electrons and 0.01 $cm^2/V \cdot s$ for holes), precisely due to the disordered nature of this material which causes scattering and trapping[12-14].

To fabricate amorphous silicon electronics, several processes are available. The most widely used is Plasma Enhanced Chemical Vapour Deposition (PECVD) [17, 18]. The method exploits the energy added to the system by the plasma, which contributes to the breakup of precursor silane (SiH_4) molecules. By this route molecules split at a much lower temperature than otherwise needed. The silicon adsorbs onto the surface and the hydrogen and other gaseous compound diffuse and are extracted. Only moderately high temperatures ($250^{O}C$) are required, which makes the process compatible with glass substrates. Hot wire chemical vapour deposition (HWCVD) requires even lower temperatures, around $150^{O}C$ and is well suited for silicon deposition on plastic substrates [19, 20].

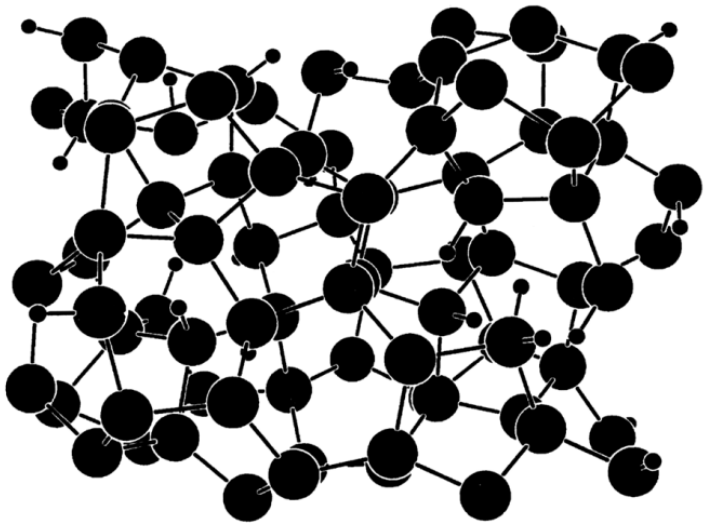


Figure 2.2. Amorphous structure of a-Si:H. [12]

Amorphous silicon has long been the material of choice for building large-area electronics. Electronic devices such as thin-film transistors (TFTs) and complex circuits can be fabricated on inexpensive glass [21-23] or polymer [24, 25] substrates. Moreover, as there is no need for precise control of lattice growth, the cost of fabrication of amorphous silicon active layers is significantly lower than that of crystalline Si. Large area electronics, such as liquid crystal display (LCD) screens [21], and more recently organic or polymer light emitting diode (OLED/PLED) display screens use amorphous silicon technology for the electronic control of the brightness and colour of each picture element (pixel). Other applications, such as solar cells, benefit from its good absorption characteristic of radiation in the visible spectrum, a property which enables a-Si photovoltaics to achieve high energy conversion efficiency [14, 22, 26].

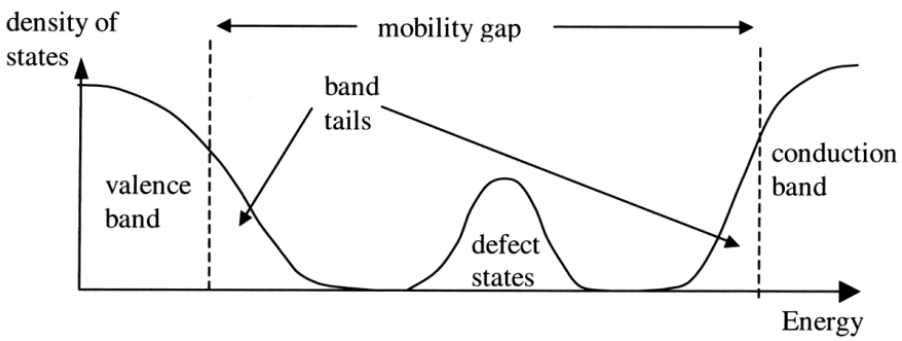


Figure 2.3. Band structure of amorphous silicon. [12]

2.2.3. Polycrystalline silicon (poly-Si)

The principal downside of amorphous silicon technology is the relatively low carrier mobility that can be achieved. Lower defect density and a more crystalline structure are two areas that need to be pursued for increased mobility.

Electronics-grade polycrystalline silicon (or polysilicon) is used for gate electrodes in CMOS technologies (and is heavily doped in order to make it highly conductive) and as an active layer in thin-film transistor (TFT) technology. Large area electronics can benefit from this latter use. In applications such as image sensors and flat-screen displays, it has become both desirable and feasible to integrate the high-performance control circuitry onto the panel using polysilicon TFTs.

Polysilicon is derived from the amorphous state through a process of crystallisation which leads to the formation of a more uniform material, with fewer defects and mobility on the order of 100 $cm^2/V \cdot s$.

The fabrication of polysilicon [27] begins with a precursor layer of hydrogenated amorphous silicon, usually deposited on buffer silicon oxide on a glass substrate. As the high content of hydrogen in a-Si:H (usually 10 at%) can degrade the quality of the finished polysilicon, a thermal dehydrogenation is first performed. The laser crystallisation process itself relies on melting the a-Si and on creating the growth conditions for polycrystalline silicon.

Historically, solid phase crystallisation (SPC) has been used for producing polysilicon. The method relies on heating the entire substrate to temperatures of $600^{O}C$ to allow crystal growth. The resulting polysilicon has an electron mobility an order of magnitude greater than that of a-Si:H [28]. However, the relatively low temperature required to ensure that the glass substrate is not damaged means that the heating step takes more time than is economically viable. As a consequence, another method of producing polysilicon has become widespread.

Laser crystallisation involves delivering bursts of energy from a laser to the a-Si film. Ultraviolet-emitting lasers, such as the 308nm XeCl radiation, are preferred due to the

high absorption by silicon of these wavelengths (Figure 2.4). The end-goal is to achieve large crystals (or grains) with minimal intra-grain defects. The fewer grain boundaries and defects, the higher the mobility of the material [29]. The laser pulses have a high enough energy to melt the silicon, but are short enough to ensure that the generated heat does not damage the underlying substrate [27].

Oxide damage increases the roughness of the semiconductor-insulator interface, which in turn provides nucleation sites for the crystallisation and smaller crystals are formed. Very large grains (over 1μm in diameter) can be grown laterally if the silicon is melted completely while keeping the number of nucleation sites to a minimum. However, as the density of molten silicon is higher than that of the solid [30], large hillocks can form at the boundaries between the large grains when the melt crystallises. Surface roughness is highly detrimental to carrier transport, but which of the two surfaces of the semiconductor will be used for conduction is determined by the type of structure which is made (top- or bottom-gate). A balance between grain size and surface roughness can be achieved if the laser beam is scanned in steps smaller than the beam width and several (tens of) lower energy pulses, or shots, are delivered.

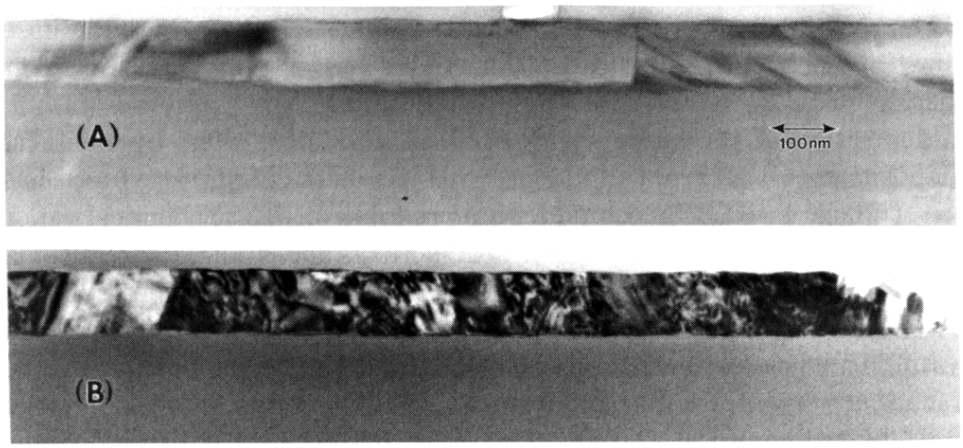


Figure 2.4. Laser crystallisation (A) produces larger polysilicon grains than thermal crystallisation (B) does. [27]

Polysilicon can be doped by ion implantation followed by a thermal anneal. The alternative, laser doping, relies on partly melting the surface of the semiconductor in a dopant-rich ambient. Both methods are designed to promote the diffusion and chemical activation of impurity atoms.

Although polysilicon is far less disordered than a-Si, strained and unfulfilled bonds at grain boundaries and intra-grain defects create trapping states in the band gap. When compared to single-crystal technology, these traps lead to higher threshold voltages, less abrupt sub-threshold slope, poorer stability and decreased mobility in transistors made in polysilicon. Excess carriers from doping can become trapped at the energy barriers formed between grains and fail to participate to carrier transport. Hydrogen passivation

of dangling bonds at the grain boundaries helps decrease the number of trap states by a factor of ten. Grain boundary energy barriers are thus lowered and the mobility is substantially improved [31].

Extensive studies have investigated the charge transport mechanisms and the optimizations required in order to produce the highest quality electronics-grade polysilicon [32-36]

As transistors are scaled down below several micrometers, it is possible to ensure that the channel contains exactly one [37] or no grain boundaries. The micro-Czochralski (micro-CZ) process relies on creating a single grain in the region where the transistor channel will lay [38]. The limiting performance factors for transistors made using this process are surface roughness and intra-grain defects. Another polysilicon technology that allows the fabrication of high mobility devices and high speed large area electronics is continuous grain silicon (CG-Si). [39, 40]

2.3. Unipolar devices

Electronic devices which rely on only one type of charge carrier for their operation are said to be unipolar. In these structures, minority carriers only have a minor role.

This section introduces the metal-semiconductor contact, the Schottky effect, bulk-unipolar diodes and field-effect transistors.

2.3.1. Metal-semiconductor (MS) contacts and the Schottky effect

When a semiconductor contacts a metal its Fermi level shifts to equal that of the metal (Figure 2.5). In the process, a depletion region is formed in the semiconductor (when the work function in the metal is larger) and a potential barrier is created at the interface. In an ideal system without interface states, the height of this barrier is the difference between the work function of the metal and the electron affinity of the semiconductor.

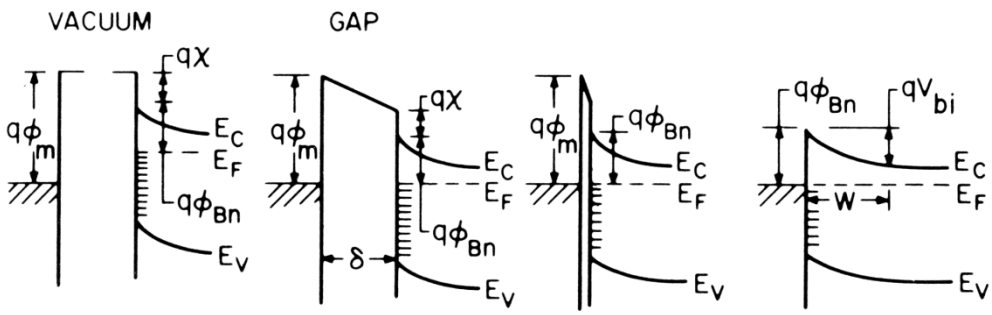


Figure 2.5. Energy-band diagrams for metal-semiconductor contacts [41].

When an electric field is applied across the metal-semiconductor interface there is an additional lowering of the potential barrier due to the image force (Figure 2.6) [41]. The effective barrier height will be lowered by the combined effect of the field and the image force. This process is called the Schottky effect.

In the simple case of a metal in free space, the image force lowering occurs at [41]

$$x_m = \sqrt{\frac{q}{16\pi\varepsilon_0\mathcal{E}}} \quad [cm] \tag{2.13}$$

and has a magnitude of

$$\Delta\phi = \sqrt{\frac{q\mathcal{E}}{4\pi\varepsilon_0}} = 2\mathcal{E}x_m \quad [V] \tag{2.14}$$

where ε_0 is the permittivity of vacuum and $\mathcal{E}$ is the applied field.

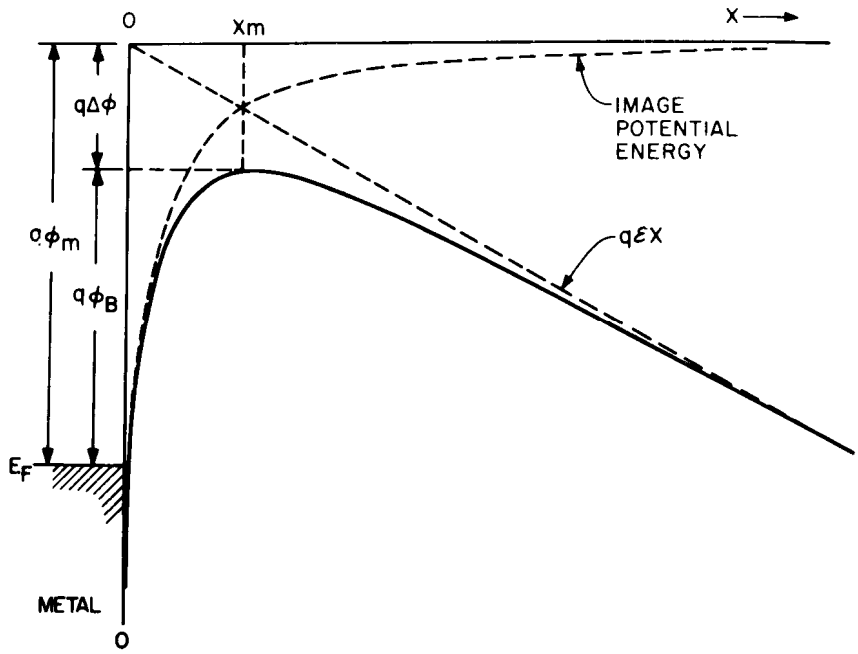


Figure 2.6. Energy band diagram between a metal and a vacuum; reproduced from [41].

For a metal-semiconductor contact, the lowering occurs within the semiconductor and therefore the permittivity of the semiconductor ($\varepsilon_s = \varepsilon_0\varepsilon_r$) is used in (2.13).

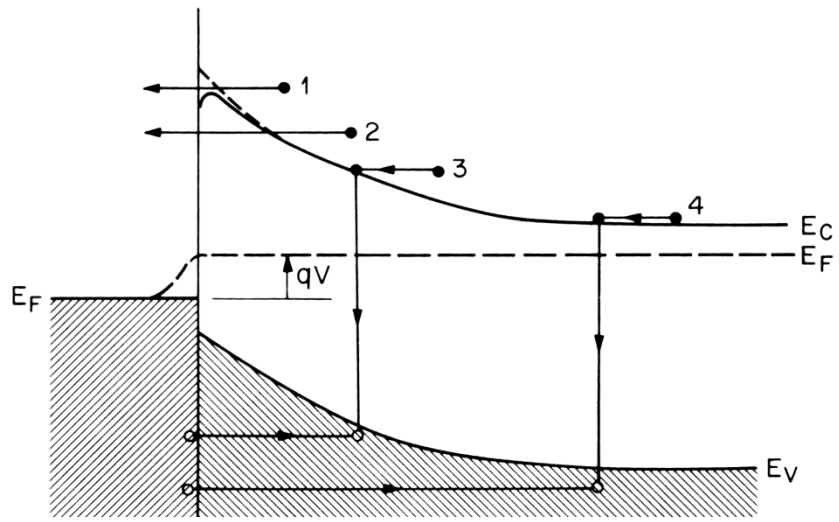


Figure 2.7. Transport mechanisms across the barrier in forward bias. In reverse bias, (1) and (2) are of interest; reproduced from [41].

In metal-semiconductor contacts, the current transport processes are due to majority carriers and can be [41] (Figure 2.7):

- Transport of electrons over the barrier (thermionic emission – diffusion model);
- Quantum transport through the barrier (tunnelling model);
- Recombination in the space-charge region (similar to *p-n* junctions) and

- Recombination in the neutral region (hole injection from the metal into the semiconductor).

The total current flowing through the barrier is due to a combination of these processes.

For high mobility semiconductors, transport over the barrier can be explained using thermionic emission theory. In the case of low mobility materials, the diffusion theory is used and a generalised thermionic emission – diffusion theory exists [41]. Tunnelling between localized states, or hopping, is an important charge transport process in disordered materials. Charges can become trapped in the states present in the band gap for relatively long periods of time and, for this reason, mobility is decreased.

If the Schottky barrier is reverse biased, as it is in the SBSGT, then the current flow across the barrier is of a quantum-mechanical tunnelling nature and takes into account the barrier lowering which occurs due to the image force (Figure 2.8). This is usually expressed using an effective barrier lowering constant, α, which includes the effects of thermionic emission, image-force barrier lowering and quantum mechanical tunnelling and which for silicon has been measured at α ≈2.7nm. [42]

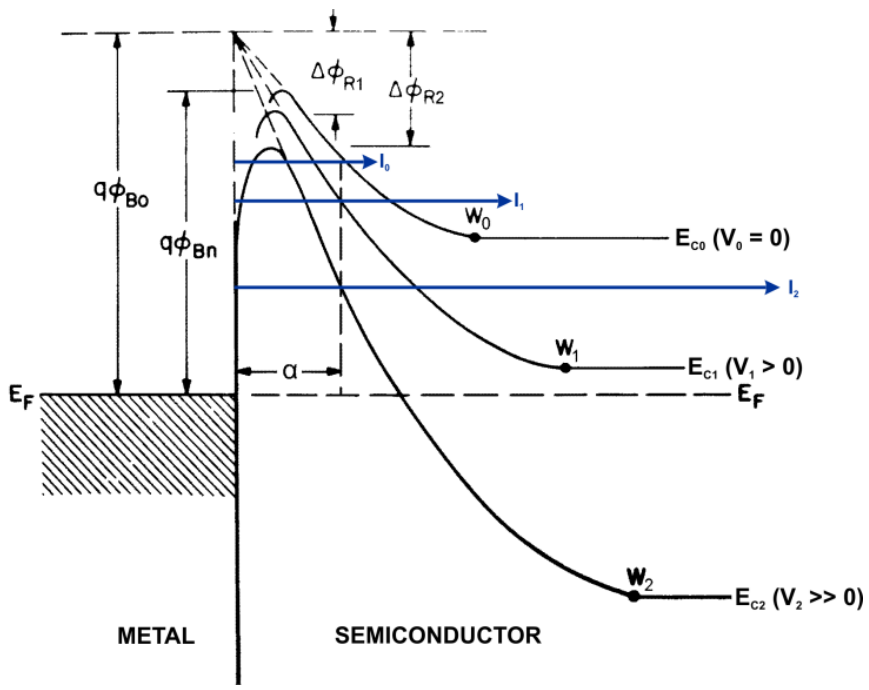


Figure 2.8. Energy band diagram for a metal – n-type semiconductor interface, incorporating the Schottky effect under different reverse biasing conditions, adapted from [41].

According to [41], at low temperatures, or for heavily doped semiconductors, tunnelling is the dominant mechanism of charge transport. In silicon, around 300K the contribution of tunnelling to the total current becomes significant for doping exceeding 1e17 cm^{-3}.

For high doping, the ratio between tunnelling and thermionic current can vary as much as two orders of magnitude per 100 Kelvin.

Free charge in the metal decreases exponentially with energy above the Fermi level; the current flowing due to tunnelling is then proportional to product of the carrier density and the occupational probability at the energy considered, and also to the effective barrier thickness. When pulling down the barrier slightly, the effective thickness decreases and additional carriers of lower energies, which are far more numerous, obtain a higher tunnelling probability. Therefore, large variations in tunnelling current are observed for small changes in barrier height.

It has been shown by Shannon [42] that the current through a reverse biased Schottky barrier on silicon can be approximated by the expression:

$$J \approx J_0 \exp\left(-\frac{q}{kT}\left(\Phi_{B0} - \alpha E_S\right)\right), \tag{2.15}$$

where T is the temperature, Φ_{B0} is the height of the source barrier, α is a barrier lowering constant and $\mathbf{E_S}$ is the electric field at the metal-semiconductor interface and $\mathbf{J_0}$ depends on the transport mechanism through the barrier. Therefore the amount of barrier lowering is simply proportional to the electric field at the barrier.

Equation 2.15 can also be written:

$$lnJ = lnJ_0 - \frac{q}{kT}\left(\Phi_{B0} - \alpha E_S\right). \tag{2.16}$$

If we differentiate with respect to the reverse bias, we obtain:

$$\frac{\partial lnJ}{\partial V_R} = \frac{q\alpha}{kT}\frac{\partial E_S}{\partial V_R} \tag{2.17}$$

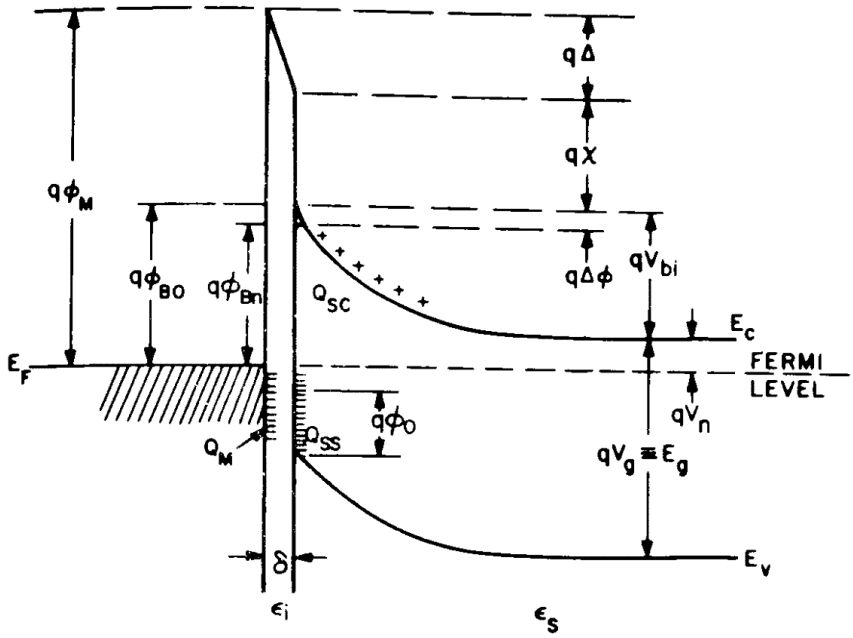
and the expression for the barrier lowering constant:

$$\alpha = \frac{kT}{q}\left(\frac{\partial lnJ}{\partial V_R} / \frac{\partial E_S}{\partial V_R}\right) \tag{2.18}$$

J has an exponential dependence on temperature. Depending on the application, this could be a disadvantage or a useful characteristic of devices incorporating Schottky barriers, such as the Schottky Barrier Source-Gated Transistor (SBSGT).

Characterisation and control of Schottky barrier height

Figure 2.9 describes the energy band diagram of a metal-semiconductor contact having an insulating interfacial layer of a thickness δ of the order of an atomic distance.



ϕ_M = WORK FUNCTION OF METAL
ϕ_{Bn} = BARRIER HEIGHT OF METAL-SEMICONDUCTOR BARRIER
ϕ_{BO} = ASYMPTOTIC VALUE OF ϕ_{Bn} AT ZERO ELECTRIC FIELD
ϕ_O = ENERGY LEVEL AT SURFACE
$\Delta\phi$ = IMAGE FORCE BARRIER LOWERING
Δ = POTENTIAL ACROSS INTERFACIAL LAYER
χ = ELECTRON AFFINITY OF SEMICONDUCTOR
V_{bi} = BUILT-IN POTENTIAL
ϵ_S = PERMITTIVITY OF SEMICONDUCTOR
ϵ_i = PERMITTIVITY OF INTERFACIAL LAYER
δ = THICKNESS OF INTERFACIAL LAYER
Q_{SC} = SPACE-CHARGE DENSITY IN SEMICONDUCTOR
Q_{SS} = SURFACE-STATE DENSITY ON SEMICONDUCTOR
Q_M = SURFACE-CHARGE DENSITY ON METAL

Figure 2.9. Energy band diagram for a metal-semiconductor (n-type) contact with a thin interfacial layer, reproduced from [41].

The barrier height can be measured with the following procedures, described in [41]:

- Current-voltage measurement;
- Capacitance-voltage measurement;
- Activation energy measurement; and
- Photoelectric measurement.

The activation energy technique is used for data analysis in this work. This simple method of obtaining the activation energy requires measuring the change in the reverse

current crossing the barrier with varying temperature for a given applied reverse bias. From Equation 2.15, the change of current with temperature is mostly determined by the exponent rather than the temperature dependence of the pre-factor $\mathbf{J_0}$. Therefore, if we assume $\mathbf{J_0}$ to be constant, it follows that:

$$\frac{\partial lnJ}{\partial\left(\frac{1}{kT}\right)} \approx -\Phi_{B0} + \alpha E_S = \Phi_B^{'} \tag{2.19}$$

and the field dependence of the effective barrier height, Φ_B', can be determined by measuring the slope of the lnJ vs. $\frac{1}{kT}$ curve at different bias voltages.

The effective height of a Schottky (metal-semiconductor) barrier can be adjusted through:

- Choosing a metal with a suitable work function [41];
- Controlled doping of a thin layer on the semiconductor surface (on the order of nanometers) [41, 42-45];
- Alterations to the work function of the metal surface [46].

2.3.2. The bulk unipolar diode

An alternative means of creating a potential barrier is to build it inside the semiconductor, rather than at the surface. Using ion implantation [42, 47-51] one can create a thin doped layer away from the surface of the semiconductor, which forms a bulk unipolar barrier to charge transport (Figure 2.10).

Two main features distinguish the operation of the bulk unipolar barrier from that of a Schottky contact [52]. Firstly, the barrier can be tuned to an arbitrary but very precise value, irrespective of the contact work function or surface states. Secondly, the pull-down due to applied field in reverse bias, which is relevant to this work, can be designed to be much more pronounced than in Schottky barriers (bulk unipolar barriers can be softer).

In a Schottky barrier in which the dominant current transport mechanism is tunnelling, the change in barrier height with applied reverse field is [52]:

$$\frac{d\Phi_{\mathbf{B}}}{dV_R} = -\alpha\left(\frac{qN_D}{2\varepsilon\varepsilon_0}\right)^{\frac{1}{2}} V^{-\frac{1}{2}} \tag{2.20}$$

In bulk unipolar diodes, the equation has the form:

$$\frac{d\Phi_B}{dV_R} = -t\left(\frac{qN_D}{2\varepsilon\varepsilon_0}\right)^{\frac{1}{2}} V^{-\frac{1}{2}} \tag{2.21}$$

where t is the thickness of the doped layer and $\mathbf{N_D}$ is the bulk dopant concentration, n region in Figure 2.10.

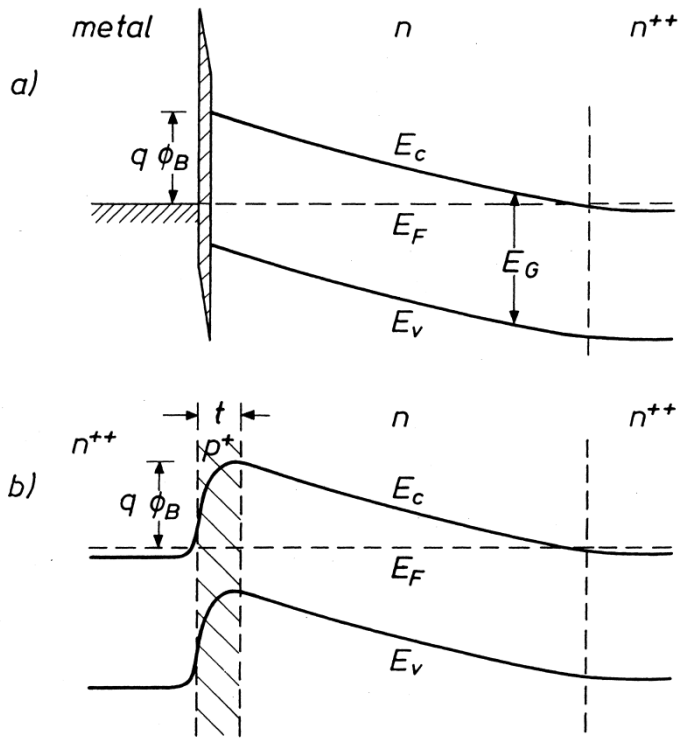


Figure 2.10. Band diagrams for a) metal-semiconductor contact and b) bulk-unipolar diode; after [52].

It can be seen that if $\mathbf{t > \alpha}$, the bulk unipolar barrier becomes more susceptible to changes in effective height due to the effect of the field. With values of $\boldsymbol{\alpha}$ in the range of 2 to 3 nanometres for silicon, this is easily achieved using standard ion implantation, in which the depth and the vertical distribution of dopants is accurately controlled.

2.3.3. The field-effect transistor (FET)

The FET [53] is a type of unipolar device that has either three or four terminals and can be used as:

- A digital switch;
- A voltage controlled current source;
- A variable resistor;
- A capacitor.

The most common structure is the planar metal-oxide-semiconductor FET (MOSFET) (Figure 2.11), which comprises a semiconductor layer, which forms the body of the transistor, an insulating layer and a conductive gate electrode. At the extremities of the device, a source and a drain contact allow electrical access to the structure. The role of the insulator is to provide a non-conductive way for the gate to act electrostatically on the charge carriers in the semiconductor. In some technologies, such as the traditional bulk silicon, the potential of the bulk itself can be controlled, and it acts as the fourth terminal of the device. For this reason it is sometimes referred to as the "back gate".

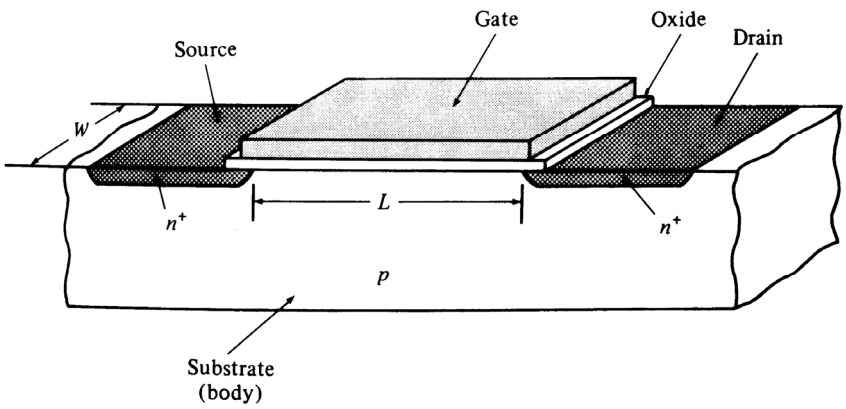


Figure 2.11. Structure of a conventional n-channel MOSFET, reproduced from [54].

The FET relies on majority carriers for current transport. These carriers only exist in sufficient numbers if the semiconductor is doped with either donor or acceptor impurities. Depending on the type of dopants, *n-type* or *p-type* devices can be created, in which the majority carriers are electrons or holes, respectively.

The name of this type of device reflects the mode of operation. A voltage applied on the gate electrode creates an electric field which modulates the conductance of a channel formed between the source and drain electrodes. Current flows between the two electrodes when a potential difference is created between the drain and the source.

We can analyse the various operating regimes [54-57], with the aid of Figure 2.11, which depicts an *n-type* device, starting from an initial condition in which all terminals are at 0V. Excess carriers are distributed uniformly inside the device with no current flowing, and now if we apply a small voltage on the gate ($\mathbf{V_G}$, positive with respect to the source), the negative charges will be attracted to the semiconductor-insulator interface and will begin to form a conductive (*n-type*) bridge called the channel between the source and the drain. This is the weak inversion regime. The threshold voltage ($\mathbf{V_T}$) is an empirical quantity which separates the inversion regimes. For $\mathbf{V_G > V_T}$, we enter the strong inversion region in which the channel (of length **L**) is very conductive.

For any value of $\mathbf{V_G}$, the drain terminal can be biased positively relative to the source, which allows current to flow from the source to the drain through the channel which acts as a resistor (Figure 2.12a). This drain current at low fields depends on the drain voltage, $\mathbf{V_D}$, and to the channel conductance [58]:

$$I_D = \mu C_{ox} \frac{W}{L}\left(\left(V_G - V_T\right) V_D - \frac{V_D^2}{2} \right) \tag{2.22}$$

where $\mathbf{C_{ox}}$ is the insulator capacitance per unit area, μ is the field-effect mobility in the semiconductor and **W** and **L** are the width and length of the FET channel, respectively.

We call this operating mode the linear or ohmic region.

Increasing the drain bias further (Figure 2.12b) until $\mathbf{V_D} = \mathbf{V_G} - \mathbf{V_T}$ results in the so-called pinch-off at the drain. The semiconductor area around the drain contact is depleted of free carriers and the channel no longer touches the drain.

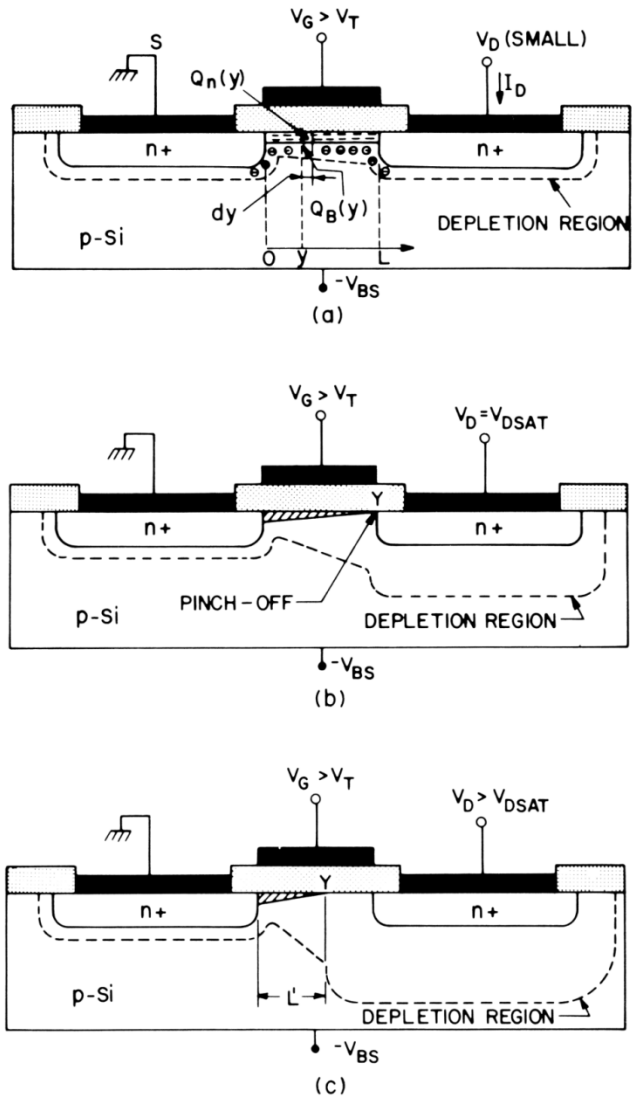


Figure 2.12. Saturation of the metal-oxide-semiconductor field-effect transistor (MOSFET): a) small V_D; b) $V_D = V_G - V_T$; c) $V_D > V_G - V_T$; from [55].

Above this drain voltage (Figure 2.12c), $\mathbf{V_{SAT}}$, the current saturates to a value of:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_G - V_T\right)^2 \tag{2.23}$$

The excess drain voltage is dropped on the pinch-off region which widens with increasing $\mathbf{V_D}$. As a consequence, the effective channel length becomes smaller (**L' <L**).

Output and transfer characteristics, which show the change of drain current with drain and gate voltage, respectively, are exemplified in Figures 2.13 and 2.14.

The field effect transistor is a transconductance device; a voltage applied on the gate modulates the current at the drain.

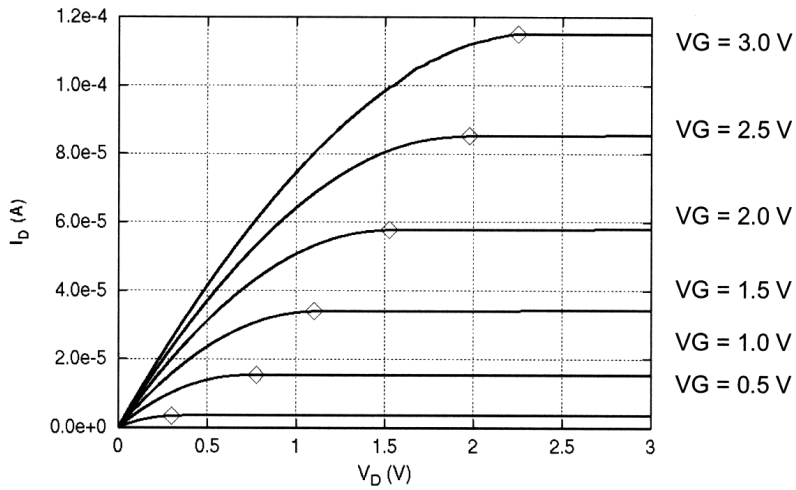


Figure 2.13. Output characteristic of a typical MOSFET, showing the saturation voltage for each gate bias [57]

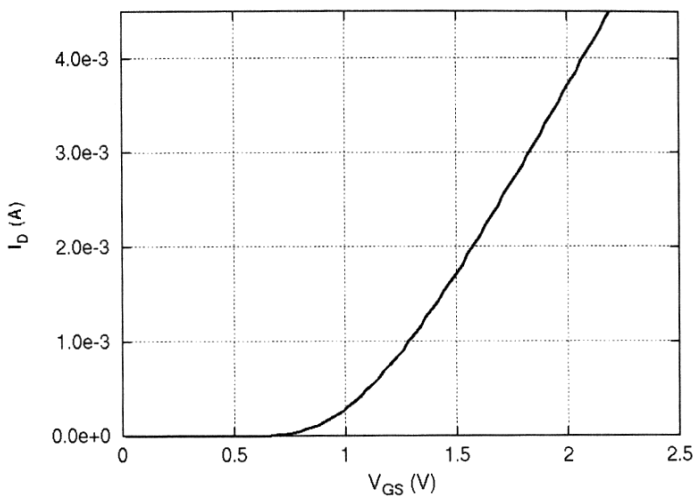


Figure 2.14. Transfer characteristic of a typical MOSFET. Drain current is negligible below the threshold voltage and increases quadratically with $V_G - V_T$ above threshold [57].

Metal-oxide-semiconductor field-effect transistor (MOSFET) is a term that generally refers to a high performance transistor fabricated in single-crystal silicon and is created in a sequential process having as a substrate the bulk semiconductor itself. Alternative technologies create islands of silicon on an insulated wafer (Silicon on Insulator – SoI), in an attempt to eliminate bulk effects and substrate leakage [59-61].

By far the most used technology for very-large-scale integration (VLSI) and ultra-LSI (ULSI) electronic circuits, complementary MOS (CMOS) has the built-in capability of creating both *n*-type and *p*-type transistors on the same wafer. For digital circuits, the main advantage is that switches can be made that consume no power in either stable state (apart from losses by leakage currents). In analog circuits, functionality is increased and less chip area is used when designing with complementary devices.

2.3.4. The thin-film field-effect transistor (TFT)

Thin-film transistor technology has a long and successful history [62], as a result of its ability to create transparent large area electronics at a very low cost when compared to the bulk silicon process. TFTs can be made using almost all semiconducting materials. The most common of these are polysilicon, amorphous silicon, semiconducting nanowires [63-64], semiconducting carbon naotubes [65], and a number of organic semiconductors. These devices are made on an insulating substrate and require manufacturing steps that will not damage the substrate (e.g. temperature constraints, chemical compounds). A thin layer of semiconductor is deposited through various procedures (evaporation, sputtering, spin-coating, chemical vapour deposition - CVD) on the substrate. The cross section and components of a typical TFT are shown in Figure 2.15, while Figure 2.16 illustrates the various thin film transistor topologies.

The main advantage of TFT technology is the ability to produce electronic circuits on large-area substrates far more cost-effectively than using crystalline semiconductor fabrication. The price paid is the relative device size and level of circuit integration (minimum features on the order of hundreds of nanometres).

When augmented with transparent interconnects made from conductive materials, such as indium-tin oxide (ITO) films, this technology enables the fabrication of transparent electronics and is widely used for display screen manufacturing. Components which were, in the past, built using crystalline silicon are now being integrated onto the same substrate along with the traditional TFT electronics, leading to System-on-Panel designs (Figure 2.17) [66-68].

By replacing the conventional glass substrate with one made of plastic, thin-film technology can produce flexible electronics with potential applications in display screens

which can be rolled up into a cylinder [70], printed and wearable electronics [71 -73], disposable sensors and electronic product identification tags [74].

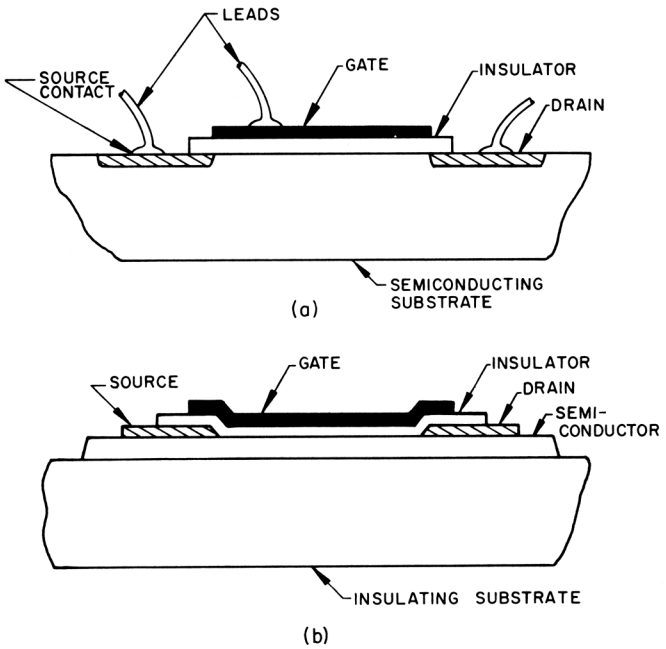


Figure 2.15. Schematic cross sections revealing the differences between the TFT and the bulk MOSFET [62].

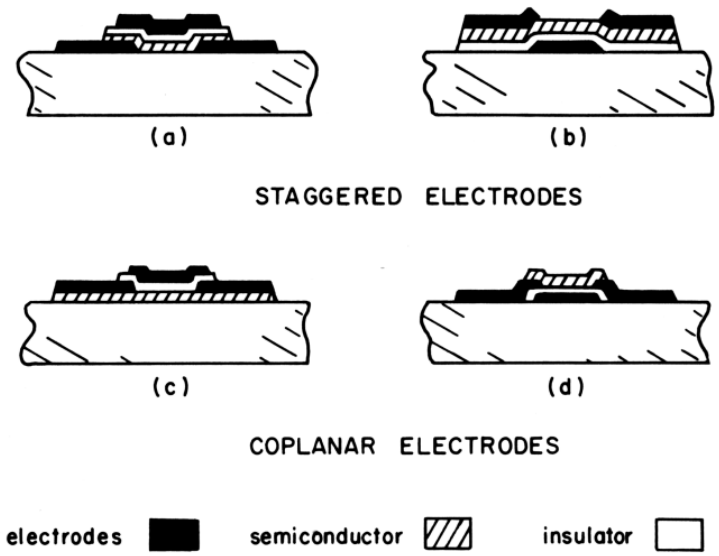


Figure 2.16. TFT topologies. (b) and (d) are inverted (or bottom gate) structures [62].

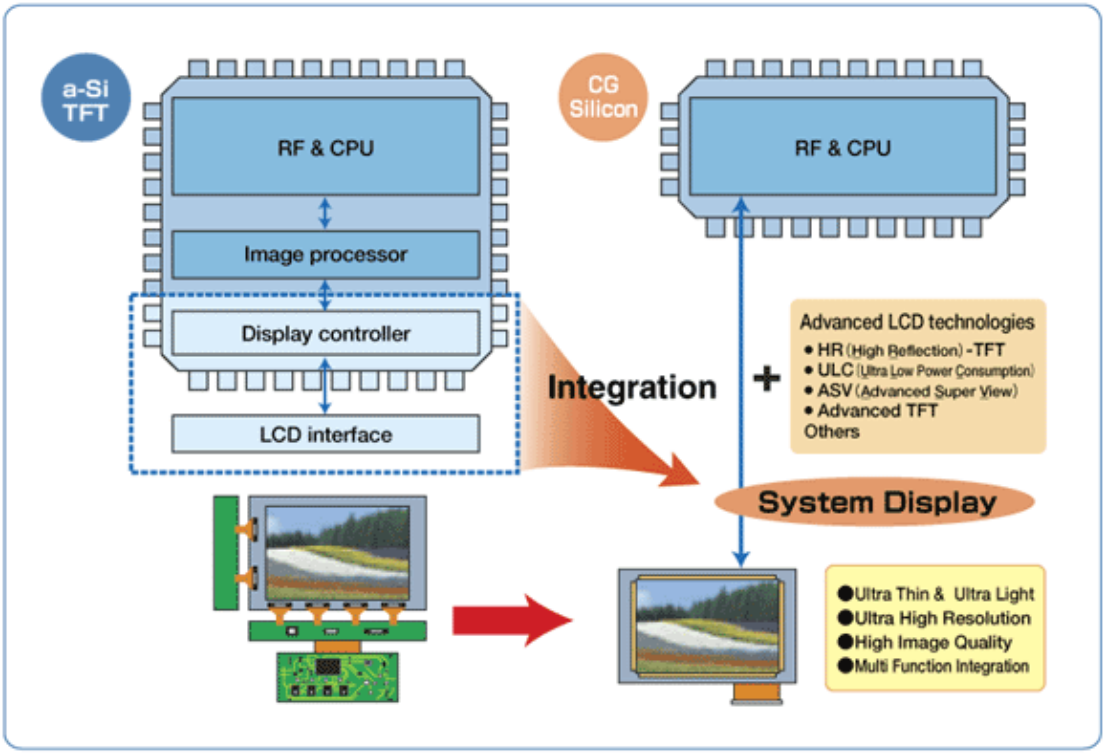


Figure 2.17. High performance thin-film electronics allow for better integration of system components [69].

2.4. Performance characteristics of FETs

2.4.1. Saturation

In MOSFETs, saturation occurs once the drain pinches off, at a drain voltage equal to $\mathbf{V_G}$ - $\mathbf{V_T}$. Any additional voltage applied to the drain is then dropped onto the depleted semiconductor area; the source "feels" the same drain field and current remains constant. For every volt applied on the gate, the saturation voltage $\mathbf{V_{SAT}}$ will also increase by one volt, therefore at high gate voltages the voltage drop and power dissipation in saturation can be high. However, for very short channel lengths, several effects which are detrimental to current saturation can occur.

The first one is the saturation of the carrier drift velocity. At values of the electric field higher than $3 \cdot 10^6$ V/cm, brought about by the application of high drain bias in devices with short channels, the drain reaches a maximum lower than that predicted by the saturated current equation, (2.23). Saturation also occurs at a drain voltage lower than $\mathbf{V_G}$ - $\mathbf{V_T}$, and it is said that the device is operating in the velocity saturation regime.

The second consequence of a short channel is a dependence of the saturated drain current on the drain field. The parameter λ is introduced in Equation 2.23 and gives a measure of this dependence [57]:

$$I_D = I_{Dsat}\left(1 + \lambda V_D\right). \tag{2.24}$$

Drain-induced barrier lowering (DIBL) is the name given to the phenomenon whereby the conductance of a very short channel is not controlled solely by the electric field generated by the gate, but also by the drain field [54].

2.4.2. Output conductance

The "quality" of the saturation regime is given by a parameter named output conductance ($\mathbf{g_d}$). This is an important parameter, particularly in signal amplification applications and can be calculated at every point of the output characteristic of the transistor:

$$g_d = \frac{\partial I_D}{\partial V_D}. \tag{2.25}$$

Alternately, one can use in calculations the output resistance (impedance):

$$r_O \equiv Z_O = \frac{1}{g_d}. \tag{2.26}$$

Output conductance should be as low as possible, ideally zero. A constant value of $\mathbf{g_d}$ denotes a certain dependence of the current on drain voltage, and in thin-film transistors on insulating substrates an increase in $\mathbf{g_d}$ at higher drain voltage reveals the so-called kink effect [75-77] or its precursor: generation of carriers by avalanche. Charge carriers are created in the high field regions near the drain and contribute to the overall current. Bipolar amplification can occur, leading to avalanche multiplication of carriers and consequently, a very large increase in drain current (kink effect) which compromises the output conductance figure. Techniques such as gate-overlapping lightly doped drain implants (GOLDD) [78] have been developed in order to reduce the field near the drain and thus to reduce the kink effect.

2.4.3. Transconductance or mutual conductance

Transconductance (denoted $\mathbf{g_m}$) is another parameter of interest in transistor applications. It is a measure of the change of output current produced by a change of gate voltage [56]. From equation 2.23:

$$g_m = \frac{\partial I_D}{\partial V_G} = \sqrt{2 I_D \mu C_{ox} \frac{W}{L}} \,. \tag{2.27}$$

The value of $\mathbf{g_m}$ is affected by the thickness and dielectric constants of both the gate insulator and the semiconductor and by the semiconductor doping.

2.4.4. Intrinsic Gain

The ratio $\mathbf{g_m/g_d}$ (or the product $\mathbf{g_m \cdot r_O}$) is called intrinsic gain ($\mathbf{A_V}$) and represents a defining quality of the transistor. Desirably, a large gm and a small gd produce a high value for intrinsic gain.

Intrinsic gain deteriorates due to the kink effect and when scaling down the channel. Through $\mathbf{g_m}$, it also depends on the quality of the semiconductor.

Deep sub-micron silicon-on-insulator MOSFETs typically have maximum intrinsic gain of 30, but improved structures can yield $\mathbf{A_V}$ of over 100 [79]. Early long-channel polysilicon thin-film transistors were demonstrated with maximum $\mathbf{A_V}$ of several hundred [80].

2.4.5. Current on/off ratio

The following discussion refers to the drain current. It is desirable for a transistor acting as a switch to have as little leakage current (in the off-state) and as much on-current at a given bias as possible.

Off-current is limited by the choice of semiconductor, channel doping and insulator quality. On-current depends primarily on the channel geometry and layer thicknesses and carrier mobility, and will increase quadratically with gate voltage (Equation 2.23). Ideally, the on-current will be independent of drain bias in saturation, but short channel effects introduce some dependence on drain field.

In order to perform meaningful comparisons between structures and technologies, the **W/L** ratio, or at least the device width should be specified. The on-to-off ratio in well designed transistors is greater than 10^6.

2.4.6. Threshold voltage

In MOSFETs, the threshold voltage ($\mathbf{V_T}$) is defined as the voltage applied to the gate which is necessary to invert the carrier population in the channel. This figure is proportional to the number of charge carriers to be depleted and consequently, on the doping level in the semiconductor. $\mathbf{V_T}$ also depends on the dielectric properties and thickness of the gate insulator [56].

$$V_t = \Phi_{ms} + 2\Phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}, \tag{2.28}$$

where Φ_f is bulk potential (2.29), Φ_{ms} is the metal-semiconductor work function, $\mathbf{Q_b}$ is the bulk depletion layer charge, $\mathbf{Q_{SS}}$ is the concentration of surface state charge and $\mathbf{C_{ox}}$ is the insulator capacitance per unit area.

$$\Phi_f = \frac{E_F - E_I}{q}. \tag{2.29}$$

Short channels lower the threshold voltage, as the free carriers in the channel are partly depleted by the proximity of the drain to the source. Very narrow channels can lead to an increase in $\mathbf{V_T}$ due to insulator thinning and edge effects [54].

2.4.7. Parasitic capacitance

In a staggered configuration, the gate overlaps the source and the drain to some extent. This has the effect of increasing the overall gate capacitance and is detrimental to the switching speed of the device (Figure 2.18). A small overlap is generally required to

ensure good conductivity at the ends of the channel; otherwise a fixed series resistance is seen in the transistor characteristics. This overlap can be optimized during the lithographic process and techniques such as back exposure have been developed to ensure perfect alignment of the drain and source to the gate (Figure 2.19) [81]. The resulting self-aligned structure is optimized for minimum parasitic gate capacitance and, at the same time, ensures a good channel is formed between the source and the drain.

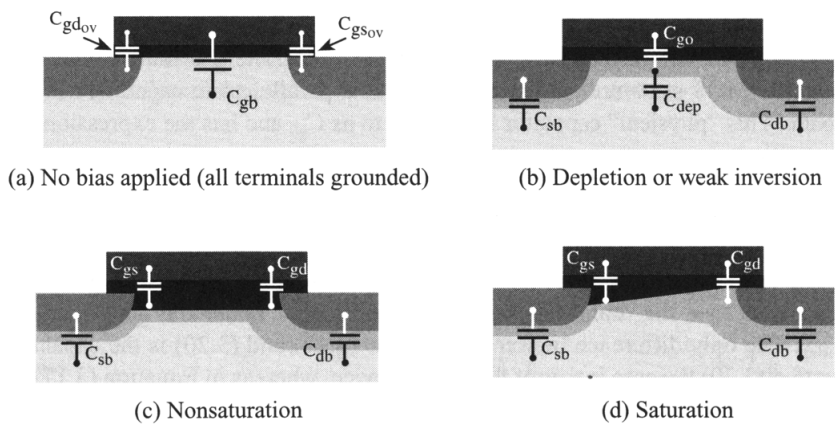


Figure 2.18. Capacitances in the FET under various bias conditions [57].

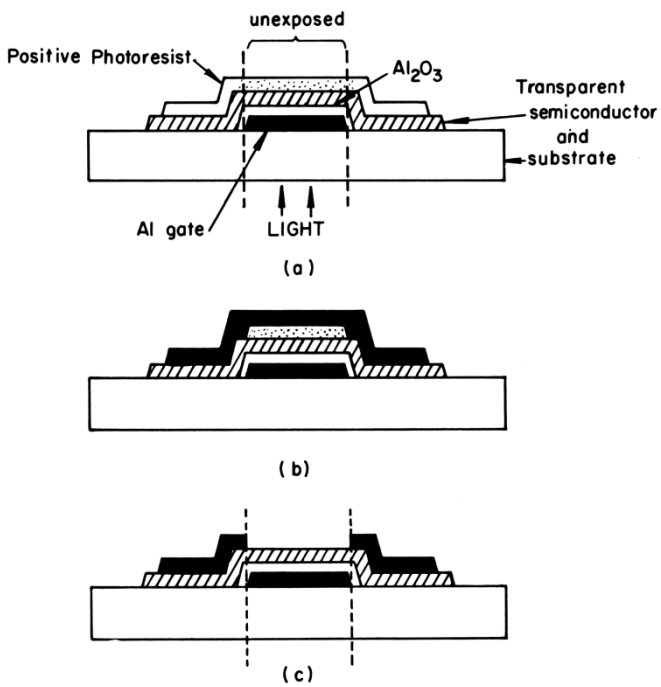


Figure 2.19. Self-aligning the top contacts to the bottom gate by back exposure through the substrate [62, 81].

2.4.8. Subthreshold slope

The turn-on characteristic of MOSFETs is dictated by the subthreshold slope, which represents the voltage that needs to be applied to the gate in order to increase the subthreshold current by one order of magnitude [82]:

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_D}{C_i} \right). \tag{2.30}$$

This equation, in which C_D is the capacitance per unit area of the depletion region, shows that thin insulators are needed for minimal subthreshold swings. In the limit, if $C_D \to 0$ then $S \cong 60\text{mV/dec}$; this is a fundamental limit for standard FET devices.

2.4.9. Stability to electrical stress

Device stability refers to the variation of threshold voltage, and implicitly output current over time.

In hydrogenated amorphous silicon, the dominant mechanism through which stability is degraded is different (Figure 2.20). The large number of excess carriers increases the probability of hydrogen atoms being pulled out of the lattice which leads to the formation of dangling bonds.

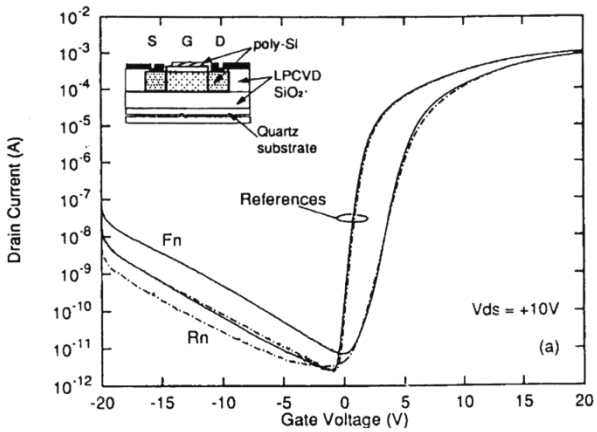


Figure 2.20. Amorphous silicon TFTs suffer from positive threshold shifts and lower on-currents after being subjected to bias stress; after [27].

Another process which affects the stability of FETs, particularly in high-mobility semiconductors is hot carrier injection. High drain field can cause carriers to acquire very high energy. Due to the combined effect of the drain and gate electric fields, some of these "hot" carriers can impact the insulator at the interface with the semiconductor and may become trapped (hot carrier injection) [83]. This process has been exploited in non-volatile memory technology [84, 85], but it can compromise the performance of standard field-effect transistors. Carriers trapped in the insulator diminish the effectiveness of the gate in its action upon free carriers and the threshold voltage increases. During electrical stress hot electron injection occurs mainly in the high-field area near the drain; the channel gradually becomes asymmetrical and swapping the source and drain terminal leads to large variations in $\mathbf{V_T}$ and drain current [27]. The effect can be partially reversed by temporarily biasing the gate at a voltage opposite to normal. It can be minimised by ensuring the drain field is kept low, either by operating the device at a low drain voltage or by incorporating field relief structures such as LDD [78].

2.5. Power efficiency in electronic circuits

2.5.1. Introduction

The penetration of electronic devices into everyday life continues to increase. In recent years, an area of high growth was that of portable electronics, in which the computational power, number of features and integration have increased substantially. By using power-optimized devices and low-power circuit techniques this trend can be maintained. A low-power approach to circuit design will enable next generation electronic systems to benefit from any number of the following:

- Increased autonomy, desirable for consumer products, essential for some medical and remote sensing applications;
- Longer operating times for portable, battery-operated applications;
- Augmented feature set;
- Migration of certain applications from desktop to mobile;
- Better integration of features;
- Better user interface;
- Lower manufacturing cost for the application, eventually ending in disposable electronics;
- Lower losses in the form of heat, and in some cases, savings from employing less complex cooling solutions;
- Increased miniaturization of the application through integration and reduced battery bulk, with the possibility of more appealing, innovative product designs;

The following techniques have found their uses mostly in MOSFET technologies, but some can be used regardless of technology.

2.5.2. Scaling as a low power technique in digital integrated circuits

Several well known and emerging routes for reducing power consumption in digital circuits are presented in [86], with an in-depth analysis of the implications in [5].

Device scaling or technological miniaturization represents the most frequently used technique and has been driving the microprocessor revolution of the 1990s and early 2000s. The reduction in device dimensions has the effect of decreasing the delay x power product by up to the fourth power of the scaling factor. However, especially as feature sizes go below 100nm, simple device scaling creates additional problems, the biggest of which is the increased static power dissipation. Moreover, the benefits of scaling are

somewhat minimized by the fact that, as circuit complexity grows, interconnects play an increasing role in both signal delay and power dissipation.

With the scaling of transistor dimensions, a reduction in operating voltage can be applied. The dynamic power dissipation is given by:

$$P \sim C_L \cdot V_{DD} \cdot V_{drive} \cdot a \cdot f \,, \tag{2.31}$$

where $\mathbf{C_L}$ is the average load capacitance per logic gate, $\mathbf{V_{DD}}$ is the supply voltage, $\mathbf{V_{drive}}$ is the output voltage swing of a logic gate, **a** is the activity factor and **f** is the switching frequency. Assuming $\mathbf{V_{drive} = V_{DD}}$, the significant decrease in dynamic power due to supply voltage scaling can be observed.

The evolution of the various technological parameters due to scaling from one generation to another, while maintaining a constant field across the device according to [54] is shown in Table 2.1.

TABLE 2.1. CONSTANT FIELD SCALING, REPRODUCED FROM [54]

Quantity	Scaling factor
Device dimensions (L, W, d_{ox}, junction depth)	$1/\kappa$
Area	$1/\kappa^2$
Packing density (devices per unit of chip area)	κ^2
Doping concentration, N_A	κ
Bias voltages and V_T	$1/\kappa$
Bias currents	$1/\kappa$
Power dissipation for a given circuit	$1/\kappa^2$
Power dissipation per unit of chip area	1
Capacitances, C	$1/\kappa$
Capacitances per unit area, C'	κ
Charges, Q	$1/\kappa^2$
Charges per unit area, Q'	1
Electric field intensity	1
Body effect coefficient, γ	$1/\sqrt{\kappa}$
Transistor transit time, τ	$1/\kappa$
Transistor power-delay product	$1/\kappa^3$

2.5.3. Low power techniques in analog integrated circuits

Adaptive biasing

Operating currents can be tailored to the operating conditions at a specific time by bias control.

Sub-threshold operation

By operating the transistors in weak inversion, very low currents can be drawn.

Selective supply voltage increase

Some parts of a circuit may need to be operated at higher supply voltage for various reasons. By using dc-dc converters or integrated (multistage) charge pumps, the desired supply voltages can be obtained. The rest of the circuit can still be operated at a lower voltage thereby minimizing loss.

Cascading gain stages

In order to enable low supply voltage operations, analog functions may be implemented by cascading several stages instead of relying on a 'tall' string of transistors for that purpose (e.g. cascoding for high gain).

Rail-to-rail design techniques

Generally, the input and output signals are limited to a range between the two supplies (or supply and ground). Rail-to-rail techniques allow either input or output signals, or both, to swing between the supplies with no loss of functionality or linearity at the extremities. As a result, the supply voltage range is used more efficiently.

2.5.4. Considerations on device characteristics

A real transistor that is to be used in low power applications should have some of the following properties:

- Negligible gate leakage current and overall off-state current;
- High current output per unit area;
- High sensitivity to gate (drive) voltage – high transconductance;
- Low sensitivity to voltage drop across the device in saturation – high output impedance;
- Low saturation voltage;
- Predictable variations of saturation voltage and output current with gate voltage;
- Little or no degradation in performance as the device is scaled down (e.g. weak DIBL effect);
- A structure that is inexpensive and easy to fabricate.

Several of these characteristics can be tailored by the circuit designer to suit the needs of the application. For instance, low saturation voltage can be achieved by operating the device below or slightly above threshold and off currents can be minimised by adequately choosing device dimensions.

A number of materials, device structures and circuit techniques exist for increasing energy efficiency in electronic circuits. The suitable combination of these elements needs to be chosen by the designer to suit the needs of the application. This work presents several advances in device technology and circuit design which, directly or indirectly are contributing to lowering the power consumption of electronic circuits and that allow the fabrication of devices which are less susceptible to the undesirable side-effects of scaling.

2.6. Summary

Semiconductors are an essential component from which virtually all modern electronics are made. Among them, silicon holds a prime place due to its technological maturity and electrical characteristics.

The highest quality silicon is used in circuits where speed and component density are paramount, such as general-purpose processors. In large area electronics, hydrogenated amorphous silicon and polysilicon are the materials of choice, owing to the low cost of fabrication. Polysilicon is fabricated from amorphous silicon, most commonly by laser crystallisation and due to its grain structure has higher carrier mobility than its precursor. As such, it is preferred for building the speed-critical parts of large area electronic circuits, such as row and column drivers in flat panel display screens.

One exploits the electronic properties of silicon by building devices and circuits. The most versatile and widespread electronic component is the field-effect transistors (FET). It is a type of unipolar device which can act either as a switch, or as a resistor, or as a current source, depending on the application. FETs made in crystalline silicon are at the forefront of electronic technology, pushing the limits of integration. For large area applications, thin-film FETs (TFTs) are created from the respective semiconductor on an insulating substrate (usually glass, but more recently flexible polymeric substrate have been investigated).

Polysilicon and amorphous silicon TFTs suffer from speed degradation and stability issues due to the nature of the semiconductor, but also from effects such as the so-called "kink" which results from device architecture.

Other unipolar devices such as Schottky contacts and bulk barriers have been introduced. Their usefulness is varied, but in the context of this work they are used to create electronic components which address some of the limitations of standard TFTs.

Chapter 3. Research methods

3. 1. Introduction

During this project, the following investigations have been performed:

- Characterization and performance assessment of electronic devices (source-gated transistors) fabricated off-site;
- Numerical simulation of electronic devices using material and device simulation software;
- Mixed-mode numerical simulation of electronic circuits comprising several electronic devices. Standard devices (resistors, current sources) were represented using standard mathematical models; others, such as the source-gated transistor were described by physical device simulation and embedded into the containing circuit.

3. 2. Electrical measurements

A number of electrical measurements have been performed on the devices-under-test (DUT) in order to characterize their performance. The setup consisted of (Figure 3.1):

- A probe station with four passive microprobes;
- A heated stage;
- A Keithley model 6485/E picoammeter for measuring the source current of the DUT;
- A Keithley model 2400 source/meter which supplied the voltage necessary to bias the gate and with the capability to measure the gate leakage current;
- An identical Keithley model 2400 source/meter used for biasing the drain(s) of the DUT ;
- Measurement automation software written in LabView for replicating the functionality of an electronic curve tracer.

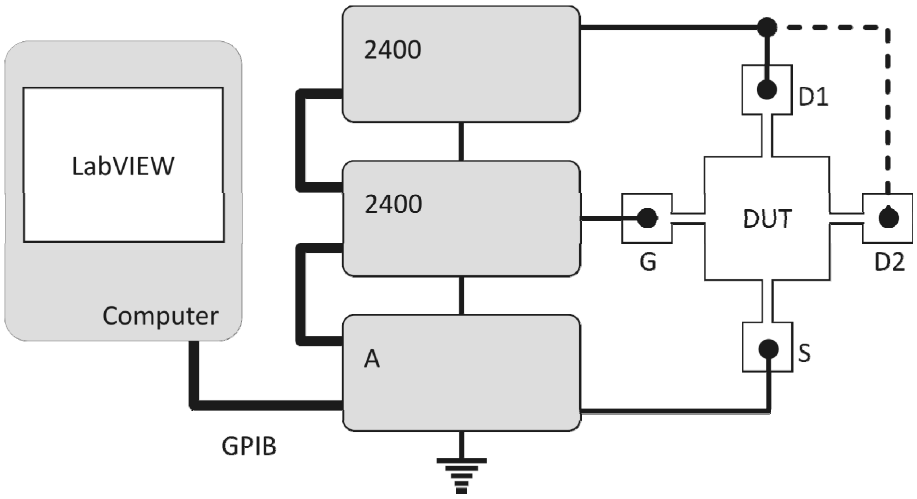


Figure 3.1. Diagram of the transistor measurement setup. A –picoammeter; 2400 – source-meter; V – voltage supply; DUT – device under test; G – gate; S – source; D1, D2 – drains with optional connection to the second drain.

The DUT were electrically isolated permanently from the stage by their glass substrate.

Gate leakage was found to be in the order of the sensitivity of the measuring equipment, which is expected due to the design and structure of the DUT. As a result, no analysis was done on the gate current values and the source current data was taken to represent the drain current.

The measurements consisted mainly of transistor (or output) characteristic scans, in which the gate is stepped from low to high voltage. For each step, the drain current is swept in fine increments and the corresponding drain current is recorded.

Data was analysed and represented using the Origin package (ver. 8) from OriginLab and Microsoft Excel (ver. 2007). The measured current data were somewhat noisy. In preparation for output conductance and intrinsic gain evaluation, the measured output characteristics were smoothed in Origin using the built-in Savitzky-Golay routine [87], using a 7-data point window and a first order polynomial as parameters. This method was chosen due to its ability to effectively eliminate noise while retaining the shape of the curves, with little mismatch between the measured data and the result of the smoothing process in the region of interest. Figure 3.2 shows a typical transistor characteristic and the corresponding smoothed curve. There are large discrepancies between the measured and smoothed data just in the linear region of transistor operation and just as the current approaches saturation. However, in this analysis we are only concerned with the behaviour in the saturated regime and the approximation is accurate in the region of interest. The plot on the right in Figure 3.2 shows the same curve as the left plot, but zoomed in to show the saturation region. The shape of the characteristic is kept, but the noise is suppressed.

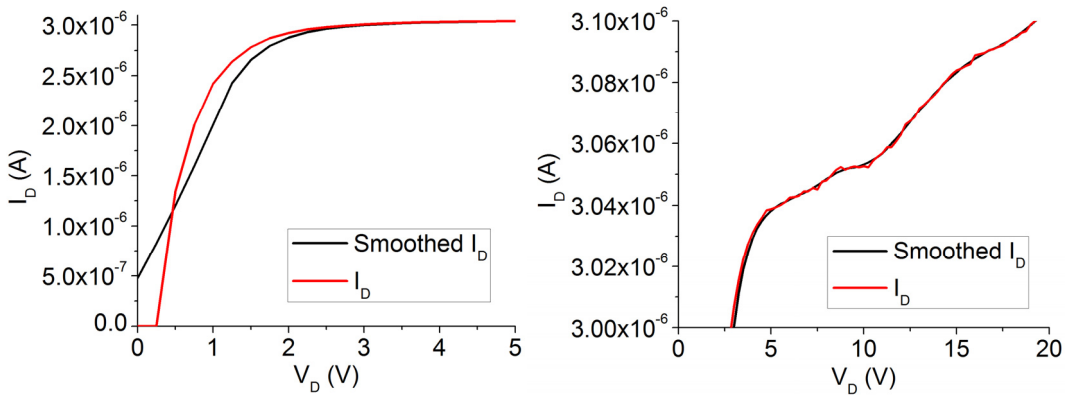


Figure 3.2. Outcome of the smoothing of a measured output characteristic. Left: the smoothed curve only approximates the raw data in the region of interest (in saturation, in this case above 4V); right: a detail of the characteristic in saturation shows that the smoothing operation effectively removes noise from the data, while preserving the actual variations of the current.

3. 3. Electronic circuit simulation using the SPICE environment

From the very beginning of integrated circuit design, the complexity of circuits with more than a few components posed problems to the designers. Solving circuits by hand or with the aid of a calculator soon proved to be a very time-consuming task, even when using simple mathematical models with relatively few parameters. By the early 1970s, computers were beginning to be used intensively to accelerate circuit design by reducing the time needed for the calculations. The most successful simulator, Simulation Program with Integrated Circuit Emphasis (SPICE) [88], was developed at the University of California at Berkeley and its various embodiments are still used today.

SPICE is generally used to:

- Describe the electronic circuits in terms of their components and the connections between them in a text file called a "netlist";
- Attach properties to the electronic components via models extracted from real devices or via abstract description of behaviour;
- Apply electrical stimuli to the circuit;
- Set the temperature at which the simulation is performed, along with other initial conditions;
- Perform analyses by solving the equations describing the devices using the specified values for the stimuli.

The most frequently used analyses are:

- Nonlinear direct current (DC) simulation for calculating the steady-state effects of the stimuli on the behaviour of the circuit;
- Transient time analysis, useful for visualising the effect of large changes in the stimuli (such as applying power to the circuit), delays and general circuit behaviour in time;
- Alternative current (AC) simulation which is particularly useful in determining the frequency response and stability of the circuit;
- Noise analysis;
- Monte Carlo and corner analysis for statistical analysis of the performance impact of process variations.

During this project, SPICE analysis of electronic circuits with standard transistors was performed using the Silvaco SmartSpice simulation software version 3.6.8 R [89].

The usefulness of SPICE as a tool for circuit design can hardly be overstated. Today's transistor models can have many hundreds of parameters [90]. As such, the use of

computer simulation software is mandatory. However, large circuits cannot be described reliably and easily into a *netlist* by hand and for this reason, graphical interfaces have been developed that allow the effortless extraction of the SPICE *netlist* from schematics drawn by the designer. They give the user the opportunity to:

- describe the circuit graphically;
- create hierarchies of sub-circuits;
- assign models to the devices;
- create stimuli;
- initiate analyses;
- set up post-simulation measurements, such as signal period or minimum amplitude of oscillation, and stop conditions (e.g. a signal exceeds a certain value).

Silvaco Gateway is such a graphical tool for circuit schematic design; version v 2.6.4 R was used during this project.

The results of SmartSpice simulation can be easily represented using the SmartView tool and later saved in standard formats which can be read by Origin.

3. 4. Electronic device simulation with Silvaco Atlas

The complexity of current electronic technologies has led to the development of Technology Computer-Aided Simulation (T-CAD) tools which facilitate the visualisation and development of electronic, optoelectronic and microelecromechanical (MEMS) devices. Accurate mathematical representations of the reality are applied to computer-generated entities, allowing design optimization and performance prediction prior to structures being made. With the increasing power of computers, fabrication test runs have increasingly been traded for computing time, leading to large economies and improved production cycles.

The behaviour of the source-gated transistor has been calculated using two-dimensional (2D) physical simulation provided by the Silvaco Atlas [91] environment (version 5.10.0R). Silvaco Deckbuild is an intuitive Atlas front-end which allows changes to be made to the *netlist* and input files, and simulations to be performed and monitored. Atlas simulation results can be visualised using the TonyPlot tool.

Device simulation using Atlas relies on finite element computation, which maps the 2D device representation onto a user-defined grid. The potential and carrier density at each node in the grid are computed iteratively using a non-linear Newton algorithm, and final values are obtained when the results of successive steps converge to within a set tolerance. The computation aims to solve the fundamental equations of semiconductor physics [7, 91]:

- Poisson's equation:

$$\nabla^2\varphi = \frac{\rho}{\varepsilon} = \frac{-q\left(p - n + N_D - N_A\right) - \rho_S}{\varepsilon} \tag{3.1}$$

- Charge carrier continuity equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}_n - U_n \tag{3.2}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}_p - U_p \tag{3.3}$$

- Charge transport, or current, equations:

$$\vec{J}_n = -q\mu_n nE \tag{3.4}$$

$$\vec{J}_p = -q\mu_p pE \tag{3.5}$$

where:

φ is the electrostatic potential, ρ is the charge density (ρ_S being the fixed charge due to trapping or interface states). ε is the permittivity, q is the electric charge, and n and p are the number of charge carriers. N_D and $N_A$the concentration of donor and acceptor impurities, $U_n$and U_p- the net recombination rates for electrons and holes, $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ represent the electron and hole current densities, μ_n and μ_p are electron and hole mobilities and E is the electric field.

Several physical models for electrical behaviour of the material exist [91]. The most often used of these are described below:

- The **carrier generation-recombination model** can be invoked in Atlas using the `SRH` and `Auger` parameters. This model represents the system as it recovers from an electrical perturbation and falls back to its equilibrium state. Mechanisms such as carrier generation/recombination at an interface and trap-assisted tunnelling are modelled.
- **Carrier mobility models** exist to describe charge transport through the materials in the presence of a low field or a high field. Parameters such as `MUN` and `MUP` set the low-field mobility. A number of parameters describe the temperature and field dependence of mobility. Non-planar devices can be simulated with the Lombardi model using the `CVT` option.
- Free carriers of high energy can dislocate other charge carriers upon impact with lattice atoms. Several **impact ionization models** exist.
- **Gate current models,** including Fowler-Nordheim Tunnelling and Hot Electron Injection, are used for assessing the gate leakage of deep-sub-micron CMOS transistors and the functionality of EEPROM and FLASH devices.

In Atlas, boundaries can be [91]:

- insulated contacts, such as the ones of the above mentioned FLASH devices;
- reflecting (Neumann) boundaries, which bound the device in areas where no contacts have been defined. These represent limits where the electric field normal to the boundary becomes zero in the absence of surface charge, or interfaces between two non-insulating materials where the difference between normal components of the electric field must match the effect of surface charge.

- ohmic contacts, for which carrier concentrations and surface potential are fixed, and carrier quasi-Fermi potentials are equal to the bias applied at the contact
- Schottky contacts, which are of interest when simulating source-gated transistors.

The material properties of the semiconductor are specified using the available options, as described in Appendix 1.

Schottky contacts describe the barrier that is formed due to the difference in work function at metal-semiconductor interfaces. The height of the Schottky barrier can be set manually by choosing the value of the metal work function, with the electron affinity of the semiconductor as a given. To create a barrier of 0.45eV, one would use the following syntax [91]:

```
material region=2 mun=300 mup=30 affinity=4.17
contact name=source SURF.REC BARRIER alpha=9e-7 beta=0 \
workfunction=4.17+0.45
```

Barrier lowering mechanisms, including image force and dipole lowering, are modelled using the following equation [91]:

$$\Delta\Phi_B = \alpha E^{\gamma} + \beta\sqrt{\frac{q}{4\pi\varepsilon_S}}\sqrt{E}\,, \tag{3.6}$$

where $\Delta\Phi_B$ is the effective barrier lowering and E is the electric field at the metal-semiconductor interface. α, β and γ are parameters with default values of 0, 1 and 1 respectively.

In simulating Schottky Barrier SGTs, we need $\Delta\Phi_B$ to be of the form:

$$\Delta\Phi_B = \alpha E\,, \tag{3.7}$$

in accordance with equation 2.15. For this reason, the values for β and γ need to be 0 and 1, respectively. α is the barrier lowering constant, which for metal contacts on silicon was shown to be around 3nm [42], thus a value of $3\cdot10^{-7}$cm would need to be used. However, in previous SGT simulations $\alpha = 9\cdot10^{-7}$cm was used successfully, even though there is no empirical reason for doing so. It was found that changing the value of α in the simulator has little effects on the behaviour of the resulting source-gated transistors, for reasons which are not clear at this time. $\alpha = 9\cdot10^{-7}$cm was also used in this work.

The `SURF.REC` parameter in the `CONTACT` statement forces a finite surface recombination velocity.

The main difference between physical and SPICE simulation is represented by the way the device is described. In SPICE, models extracted from real devices. Mathematical approximations are used to simulate the response to electrical stimuli of devices the behaviour of which is given by models. Physical simulation, on the other hand, relies on fundamental mathematical representations of the electronic properties of matter in order to investigate the behaviour of devices. In conjunction, these approaches allow the development of electronic components with novel characteristics and their integration into design flows.

3. 5. Mixed-mode simulation

Prototype devices in their early development stage usually do not have precise numerical models associated with them, which makes it difficult to integrate them directly in SPICE-type circuit simulations. The solution is mixed-mode simulation, which computes the device using physical simulation and uses mathematical models for the part of the circuit described with SPICE. In this type of simulation, the device is treated as a black box by SPICE and the physical simulations are performed at run-time according to the conditions of the whole circuit. This has the advantage of performing time-consuming physical computations only on the parts of the circuit for which SPICE models do not exist.

There is currently no SPICE model for source-gated transistors. For this reason, mixed mode simulations need to be undertaken for circuits which contain SGTs. The technique has been successfully applied in the past to the simulation of current-mode logic using SGTs made in organic semiconductors.

Silvaco Atlas has the capability of describing circuit elements using SPICE and of interfacing them with others which are simulated using the physical models (in this case the source-gated transistor).

An example of mixed mode code for SPICE/Atlas simulation is shown in Appendix 2. It represents a circuit containing several SPICE components, three Atlas components, stimuli and a transient time analysis of the resulting circuit. The four sections described in Figure 3.3 are highlighted.

Many Electronic Design Automation (EDA) and TCAD companies like Silvaco now offer complete packages that facilitate electronic circuit design [89], from material and design simulation to circuit simulation, layout, verification and preparation for fabrication (Figure 3.3). These tools greatly aid the circuit designer by providing seamless transitions between different types of simulation (for example device and circuit analysis or analog and digital block simulation).

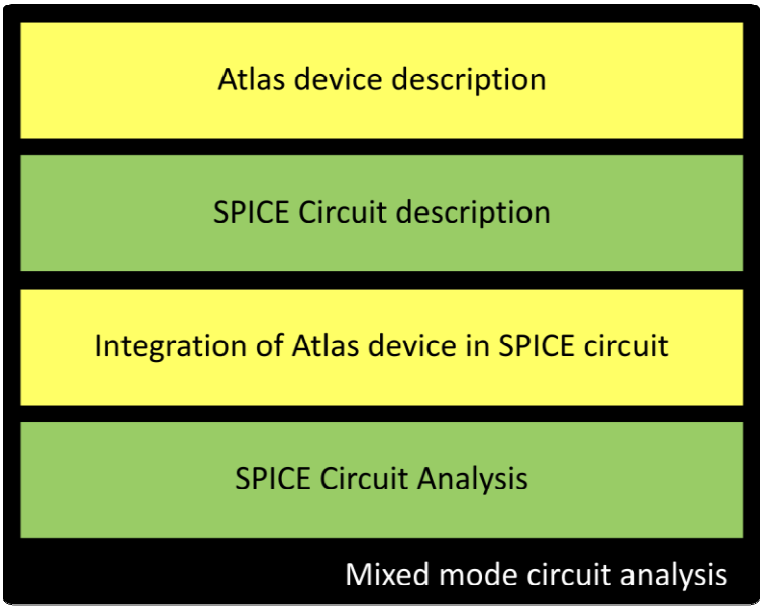


Figure 3.3. The structure of the simulation code for mixed-mode SPICE/Atlas analysis

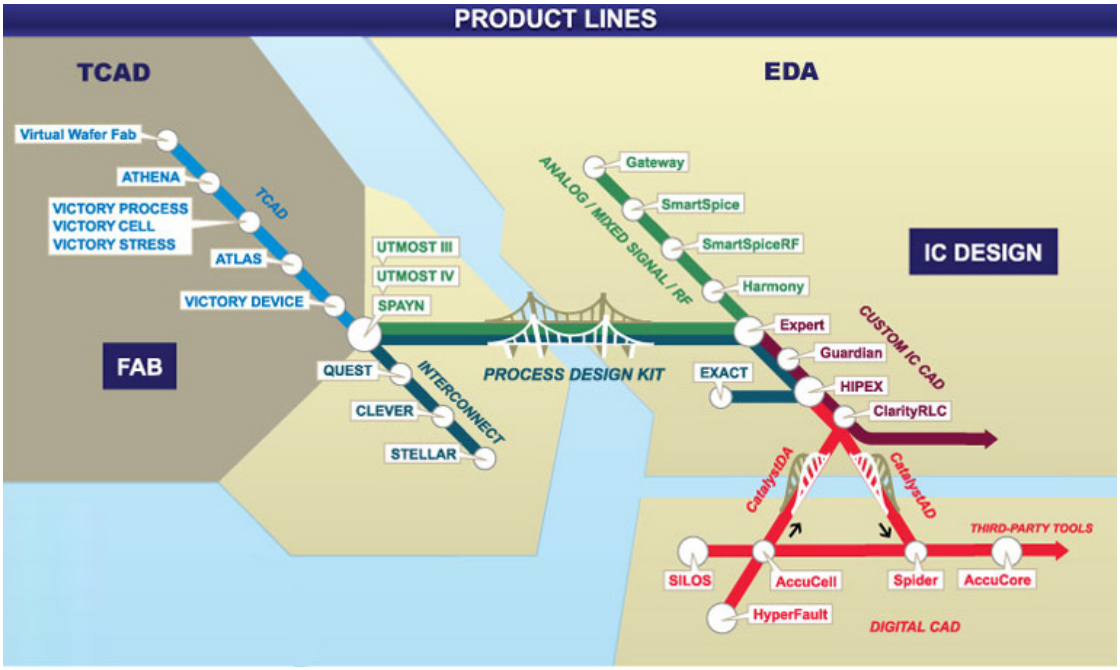


Figure 3.4. The Silvaco product line for electronic and optoelectronic design, circa 2010.

3. 6. Device fabrication and technology

Self-aligned source-gated transistors (SGTs) were made on glass substrates at the Philips Research MiPlaza facility in Eindhoven, The Netherlands. Figure 3.5 shows a microphotograph of a typical structure. A schematic cross-section of the structure is shown in Figure 3.6.

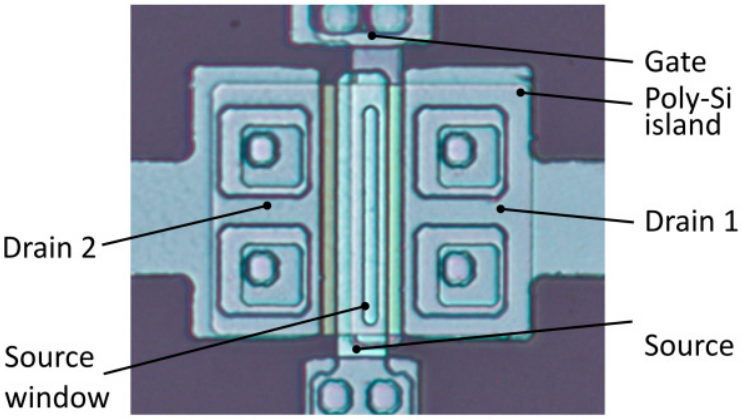


Figure 3.5. Micrograph of a typical self-aligned polysilicon source-gated transistor

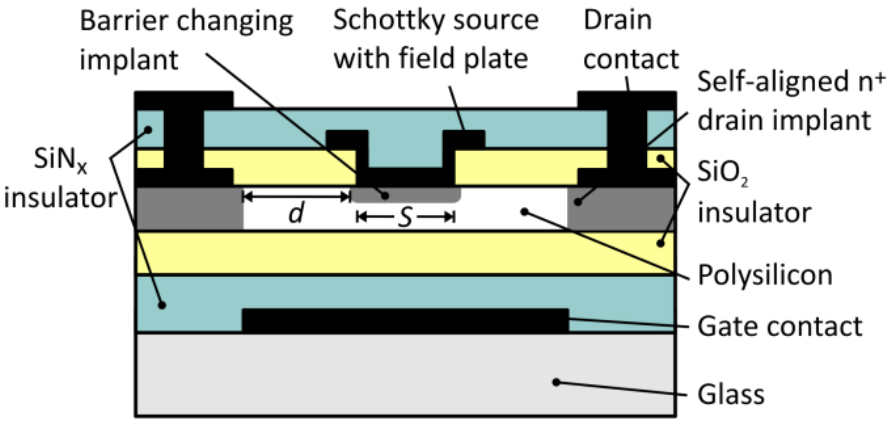


Figure 3.6. Schematic cross-section of the self-aligned polysilicon source-gated transistor

The processing steps involved in creating these structures are as follows:

- Deposition and definition of a chromium metal which forms the gate of the device and is used as a light shield for back exposure when defining the self-aligned drain contacts;
- Deposition of 200nm SiN_x and 200nm SiO_2 using PECVD, which constitute the gate insulator for the SGTs; approx. 300nm equivalent oxide thickness (EOT);

- Deposition of 40nm of a-Si:H as the semiconductor;
- Dehydrogenation of the amorphous silicon by baking at $450^{O}C$
- Doping of the semiconductor with BF_2 or P were used to give a range of doping levels in the polysilicon (bulk doping), as shown in Table 3.1. Bulk doping level varies across devices on the same substrate.

TABLE 3.1. BULK DOPING CONCENTRATION

Bulk doping level	Type	Effective concentration
Very high	*n-type*	$3.5 \cdot 10^{12} cm^{-2}$
High		$2.5 \cdot 10^{12} cm^{-2}$
Moderate		$1.5 \cdot 10^{12} cm^{-2}$
Low		$0.5 \cdot 10^{12} cm^{-2}$

- Back exposure through the glass, using the gate metal as a mask to define a positive resist;
- Chemical removal of the exposed resist regions;
- Drain contact regions formed by a high dose P implant; the resulting contacts are self-aligned to the gate;
- Formation of polysilicon using an excimer laser, producing grains of approximately 300nm in size;
- Definition and dry etching of the polysilicon to form islands;
- Deposition of 120nm SiO_2 as passivation;

TABLE 3.2. BARRIER MODIFICATION IMPLANTS USED

Barrier modification implant	Type	Target concentration
1	-	0
2	*n-type (P)*	$0.5 \cdot 10^{13} cm^{-2}$
3		$1.0 \cdot 10^{13} cm^{-2}$
4	*p-type (BF_2)*	$0.5 \cdot 10^{13} cm^{-2}$
5		$1.0 \cdot 10^{13} cm^{-2}$
6		$2.5 \cdot 10^{13} cm^{-2}$
7		$5.0 \cdot 10^{13} cm^{-2}$
8		$7.5 \cdot 10^{13} cm^{-2}$

- Opening of source windows by etching of the SiO_2;
- Implanting 5keV BF_2 or P impurities through the source window in order to modify the source barrier profile, as illustrated in Table 3.2. Different substrates (wafers) received different barrier modification implants;
- Annealing of the implants at $500^{O}C$;
- Deposition and definition of Cr and AlTi metal layers to form a Schottky source and field plate structure (Figure 3.6);
- Passivation using a 0.6μm nitride layer;
- Contacts made to the source, drain and gate pads using Cr/AlTi/Cr metallisation via contact holes.

Table 3.3 summarises the geometry parameters and their possible values.

TABLE 3.3. DEVICE GEOMETRY

Parameter	Possible values	Observations
W – device width	50μm	-
$\mathbf{W_{eff}}$ – eff. source window width	44μm	Source window does not overlap the polysilicon
S – source window length	2, 4, 8μm	-
d – Source-drain separation	4, 6, 10μm	Designed values; variations due to processing
Field relief plate	0, 4 μm	Overlap on either side of the source window

Since the width of all fabricated devices is the same, throughout this work the drain current, rather than the drain current per micron width, will be shown. To obtain the drain current per micron of device width, divide the drain current by the effective device width, $\mathbf{W_{eff}}$ = 44μm.

Before studying the electrical characteristics of these devices, several points have to be made.

Substrate compaction

Firstly, the samples suffered from severe compaction of the glass during the high temperature annealing steps. As a consequence, the alignment of layers which were separated in the lithographic process by the annealing stage is somewhat compromised. Misalignments of up to 7 microns are not uncommon between the designed and the fabricated structures, with as much as 6 microns of mismatch across a single substrate, depending on the position of the device relative to the centre of the glass plate.

These processing errors would be critical for standard FETs, but SGTs are rather resilient to the majority of these effects, as will be revealed in this chapter.

Ideally, the structure should be symmetrical, with a drain on either side of the source. As shown by the micrograph of Figure 3.5, this is not the case, with the source-drain separation (**d**) to the left drain being much smaller than that to the drain on the right. However, a useful property of the SGT is that the current is independent of **d**, since it is controlled by the source barrier. A self-aligned structure has the advantage that it minimizes gate-drain capacitance.

Effect of the field plate

Secondly, and related to the first point, in some devices which have a field plate, the source-drain separation to the left drain may be smaller than 4μm due to the combined effects of misalignment and compaction. When this happens, the field plate sits on top of the drain, with detrimental effects on device performance.

Double-drain measurements

In order to have reliable data for analysis, the drain to the left of the source was left unconnected for the majority of measurements, across all devices and substrates. Unless explicitly specified, all measurements were done by connecting only the right drain. Since all devices are on the same axis, the effective separation between the source and the right drain is be *at least* the designed value (d), with a spread of several microns. For a device with d=4μm, this could mean a doubling in source-drain gap, but given the functioning of the SGT, this will have a minor impact on several performance aspects.

Nevertheless, a small number of double-drain measurements have been successfully performed to illustrate the effect of a symmetrical structure on frequency performance and to highlight several properties of SGTs in general.

Uniformity of electrical performance

Due to the large number of possible permutations in terms of geometry, bulk and barrier changing implant, only a limited number of identical devices have been made. Wafer-to-wafer comparisons cannot be made reliably at this stage, given that each substrate is allocated a different doping level under the source barrier and the operation of the same device on different substrates is intentionally quite different.

On the same substrate, only six identical devices of each type exist. The evaluation of uniformity is complicated slightly by the large distance between identical devices (at least

0.3cm and several cm at most), which exacerbates differences created by glass compaction.

Dopant activation

Finally, the doping process used for creating the barrier modification implant through the source window is controllable and precise. However, in order to become electrically active, a high temperature annealing step is required. This creates a conflict between the requirement of minimising glass compaction and the high temperatures needed for impurity activation. A middle ground solution was attempted, in the form of baking the devices at 500 ^{O}C.

The method was only marginally successful, as compaction was still severe and it is highly probable that not all impurities were activated. In this chapter, the discussions will highlight the dose of dopants. Disagreements between the theory and measured results are most likely to stem from a presumed low percentage of activated impurities combined with damage, caused to the atomic lattice of silicon during implantation, which was not repaired during the anneal.

Chapter 4. The source-gated transistor

4.1. Introduction

Field effect transistors (FETs) are the electronic device of choice for the vast majority of electronic circuits, owing to their versatility, to their zero-current biasing capability, to their higher speed compared to bipolar devices and to the remarkable technological evolution of the past half a century. In addition to that, the cost of manufacture over the same period has dropped from a few tens of dollars per transistor to several tens of cents per million. However, this type of device has certain limitations which restrict the performance or applicability of particular technologies for certain applications.

In bulk silicon and silicon-on-insulator (SOI) technology, scaled fabrication processes have produced feature sizes of less than 1μm for over 25 years. With each improvement in lithography resolution, maintaining good transistor characteristics becomes increasingly difficult, due to an assortment of deleterious processes, collectively referred to as short-channel effects. These include increased leakage current, lower on/off ratio, lower output impedance and increased dependence of the current on the drain field.

Thin-film devices made in amorphous silicon [23, 24, 92] enable the fabrication of large area electronics, but due to the electronic properties of the material, charge carriers can be trapped and dangling bonds can form during prolonged device operation. Consequently, these transistors generally suffer from poor stability, manifested in large threshold shifts and decreased output current and as such, they cannot be used (without employing complex correction circuits) in applications where performance variations over time are not tolerated (such as display drivers, data converters, etc.) The amorphous structure leads to carrier scattering at virtually every atomic site and therefore carrier

mobility is low. Polysilicon thin-film devices [93-98] have far better stability and higher carrier mobility, as a consequence of fewer defects and improved long-range order. Nevertheless, their useful drain voltage range is limited at the top end by the kink effect [75-77].

Field-effect transistors are also made in disordered or poor quality semiconductors, such as organics. These materials are being increasingly used in the fabrication of cost-effective, and sometimes flexible, large area electronics [99-103]. However, they suffer from very low charge carrier mobility (as low as 10^{-3} $cm^2/V \cdot s$); combined with the fabrication techniques used for this type of electronics, which only allow comparatively long channels, this leads to very low operating frequencies for FET devices and circuits.

These technological limitations impose restrictions on FET applications.

4.2. The principle of operation of the source-gated transistor

A relatively new type of device, called the Source-Gated Transistor (SGT) [104], addresses these limitations of standard structures. Two main differences distinguish the SGT from an FET.

First, whereas in an FET the source and the drain are usually ohmic, the source of the SGT comprises a reverse biased potential barrier.

Second, the primary role of the gate is to modulate the effective height of the source barrier and, as such, the gate electrode is situated opposite the source, as shown in Figure 4.1. A parasitic FET of length **d** will form between the source and the drain of the device. To ensure that the current is controlled entirely by the potential barrier at the source, the conductance of the parasitic FET needs to be high enough to allow the source current to flow to the drain unimpeded. This can be achieved by heavily doping the channel of the FET or by extending the gate so that it overlaps the channel (the case in Figure 4.1).

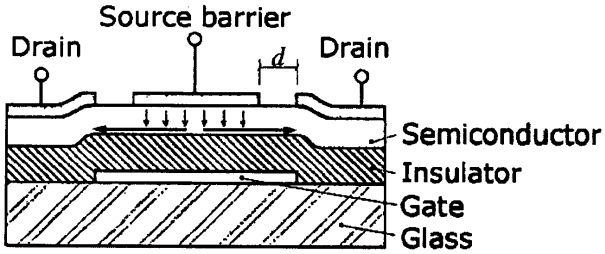


Figure 4.1. Schematic cross section of the source-gated transistor (SGT); reproduced from [105].

As a consequence of the source barrier controlling the current, the gap between the source and the drain has little influence on the magnitude of the current. In general, for a given gate bias the channel is conductive enough to play no role in restricting the drain current in the on-state, assuming the channel is not pinched off.

The SGT can be made, in principle, in any semiconductor and in any technology, as long as there is a way to produce a potential barrier of controllable height at the source. The source barrier can be a Schottky contact (Schottky barrier SGT – SBSGT), a bulk unipolar diode (bulk unipolar SGT – BUSGT), or a tunnelling barrier (field-emission SGT – FESGT) [106].

In operation, some of the differences between the SGT and a standard FET are [104]:

- Lower saturation voltage;
- Higher output impedance in saturation;
- Better performance when scaling down geometry;

- Potentially higher internal electric fields leading to higher device speed.

These characteristics make the SGT well suited to low power, large area electronic circuits, and more so in technologies where FET behaviour is significantly less than ideal, such as in poor quality, low mobility semiconducting materials.

Aside from the advantages mentioned above, the SGT has the following drawbacks compared to standard FETs:

- Lower current output for the same gate bias;
- Lower transconductance;
- Lower current output for the same device dimensions;
- Potentially high temperature dependence of drain current.

However, whether these are indeed disadvantages will depend on the application. If one wants to perform voltage amplification, for example, then it is the output impedance that is essential rather than the magnitude of the drain current. Besides, the effect of these limitations can be, in fact, much reduced due to the proper use of the advantageous features described earlier, or even be used to augment the functionality of particular applications.

The mode of operation is explained in the next section using a Schottky barrier-type device (SBSGT).

4.3. The Schottky barrier source-gated transistor (SBSGT)

4.3.1. Mode of operation

Source-gated transistors can be made with a metal-semiconductor contact at the source. The choice of the metal and careful processing give a known barrier height for the resulting Schottky contact [41].

Figure 4.2 illustrates the energy band diagram between the source and the gate of a typical SBSGT made in an *n-type* semiconductor. When a positive drain bias is applied, the drain field sweeps away free carriers and eventually depletes the semiconductor under the source. When this happens, the semiconductor and the gate insulator act as two capacitors in series. If a gate bias is now increased, the electric field it generates acts on the Schottky contact, lowering the effective barrier height ($q\Phi_B'$ Figure 4.2 and $q\Phi_{Bn}$ Figure 2.8).

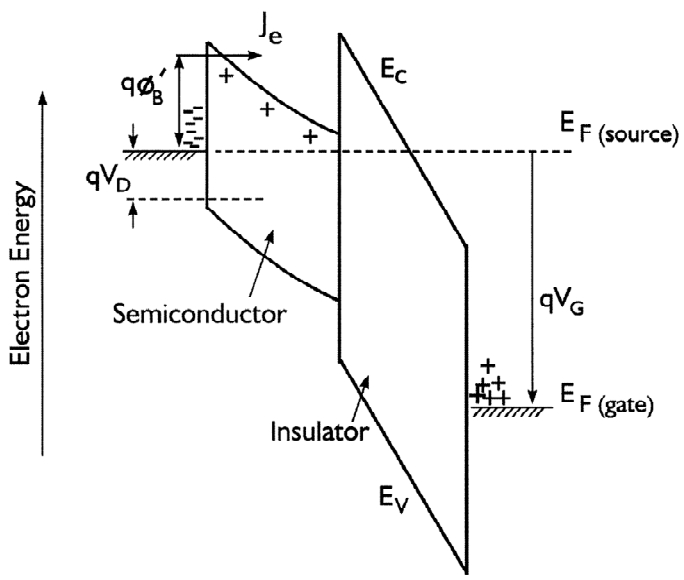


Figure 4.2. Energy band diagram between the source and the gate of a SBSGT. Φ_B is the height of the Schottky barrier at the source; reproduced from [104].

4.3.2. Saturation of the drain current

In a standard FET, saturation occurs when the semiconductor pinches off at the drain end of the channel, at a drain voltage equal to [54]:

$$V_{SAT2} = V_G - V_T \,, \tag{4.1}$$

where $\mathbf{V_G}$ is the applied gate voltage and $\mathbf{V_T}$ is the threshold voltage of the device. For every additional volt applied to the gate, $\mathbf{V_{SAT2}}$ changes by 1V.

In the SGT, the semiconductor first pinches off at the source, at a drain voltage much lower than $\mathbf{V_{SAT2}}$:

$$V_{SAT1} = \frac{C_i}{C_i + C_s}\left(V_G - V_T\right) + K\,, \tag{4.2}$$

where $\mathbf{C_i}$ and $\mathbf{C_S}$ are the insulator and semiconductor capacitances per unit area respectively and **K** is a constant which represents the drain voltage needed to deplete the interface charge at the semiconductor-insulator boundary [105]. The change in $\mathbf{V_{SAT1}}$ with applied gate voltage is then:

$$\partial V_{SAT1} / \partial V_G = \frac{C_i}{C_i + C_s} \tag{4.3}$$

The Schottky barrier at the source is reverse biased by the gate field and current transport happens through thermionic-field emission [41, 105].

4.3.3. SGT on-current and gate action

The on-current is exponentially dependent on gate field. Using Equation 2.15, the current density through the source is [41, 105, 106]:

$$J_S \approx A^* T^2 \exp\left(-\frac{q}{kT}\left(\Phi_{B0} - \alpha E_S\right)\right), \tag{4.4}$$

where $\mathbf{E_S}$ is the electric field at the surface of the semiconductor (Equation 4.5), **T** is the temperature, Φ_{B0} is the height of the source barrier and α is the barrier lowering constant given by Equation 4.7.

Since

$$E_S = \left(\frac{C_i\left(V_G - V_T\right)}{C_i + C_S} + K\right)\frac{1}{t_s} \tag{4.5}$$

and

$$\frac{\partial E_S}{\partial V_G} = \frac{\partial V_{SAT1}}{\partial V_G}\frac{1}{t_S}, \tag{4.6}$$

the barrier lowering constant is:

$$\alpha = \frac{kT}{q}\left(\frac{\partial \ln J_S}{\partial V_G} / \frac{\partial E_S}{\partial V_G}\right) = \frac{kT}{q}\frac{C_S}{\varepsilon_S \varepsilon_0}\left(\frac{\partial \ln J_S}{\partial V_G} / \frac{\partial V_{SAT1}}{\partial V_G}\right). \tag{4.7}$$

4.3.4. SGT off-current

In an SGT, the source barrier is connected in series with a parasitic FET which forms between the source and the drain. The device is designed so that the source barrier is high enough to ensure that it is the barrier that restricts the current, rather than the parasitic FET, but low enough to permit substantial current to flow when the device is on. Because of this latter constraint, it is the leakage current of the FET which generally determines the subthreshold and off-characteristic of the SGT.

4.3.5. SGT frequency characteristic

The barrier height of the Schottky source can be lowered through ion implantation [43-45, 107], to give an effective barrier height:

$$\Phi_B^{'} = \Phi_{B0} - \left(\frac{\alpha q D \gamma}{\varepsilon_S \varepsilon_0} \right), \tag{4.8}$$

where α is the tunnelling constant given by Equation 4.5, **D** is the impurity dose and γ represents the proportion of impurities which are electrically active.

Ion implantation can also be used to raise the height of the source barrier [45]:

$$\Phi_B^{'} = \Phi_{B0} + \frac{qN_D}{2\varepsilon_0 \varepsilon_S} t_d^2 \qquad \left(N_D \gg N_A \right) \tag{4.9}$$

where $\mathbf{N_D}$ and $\mathbf{N_A}$ are the donor and acceptor concentrations, respectively, $\mathbf{t_d}$ is the thickness of the doped layer and **q** is the electronic charge.

The small-signal equivalent circuit of the SGT is shown in Figure 4.3.

From Equations 4.4 and 4.5 we can derive the expression for the transconductance of the SGT [105]:

$$g_m = \frac{\partial I_S}{\partial V_G} \approx \frac{\alpha J_S S}{\varepsilon_S \varepsilon_0} \frac{q}{kT} \frac{C_S C_i}{C_S + C_i}, \tag{4.10}$$

where **S** is the source area.

The cut-off frequency of a transistor represents the frequency at which the current through the current source, $g_m V_I$, is equal to the current through the input capacitance C_{GS} (unity current gain), where $\mathbf{g_m}$ is the transconductance of the reverse biased source barrier and $\mathbf{V_I}$ is the input voltage applied to the gate. (Figure 4.3)

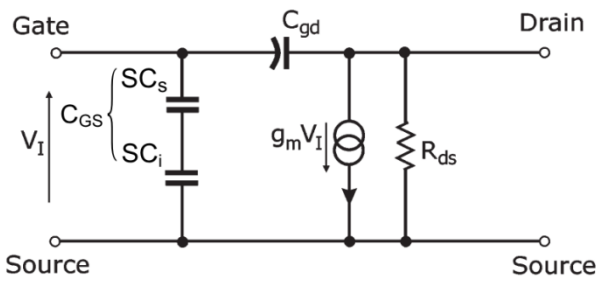


Figure 4.3. Small signal equivalent circuit of the SGT, adapted from [108].

As described in [109], the cut-off frequency is:

$$f_T = \frac{g_m}{2\pi C_{GS}} \tag{4.11}$$

which for the SGT is:

$$f_T = \frac{g_m(C_i + C_S)}{2\pi S C_i C_S} \tag{4.12}$$

and substituting $\mathbf{g_m}$ from Equation 4.10 we obtain:

$$f_T \approx \frac{q}{kT}\frac{\alpha J_S}{2\pi\varepsilon_s\varepsilon_0}, \tag{4.13}$$

where $\mathbf{J_S}$ is the average current density through the source.

It is seen that the cut-off frequency is proportional to α and $\mathbf{J_S}$ and is higher for semiconductors with lower permittivity. Furthermore, for a given average current density, $\mathbf{f_T}$ is independent of $\mathbf{C_S}$, $\mathbf{C_i}$ and layer thicknesses.

4.4. A review of published results on Schottky barrier source-gated transistors (SBSGT)

This section presents a brief review of the literature concerning Source-Gated Transistors. All devices discussed below have a Schottky source barrier.

Source-Gated Transistors have been made and measured in both amorphous [104, 105, 110, 111] and polycrystalline [112] silicon technologies. Early results revealed the much lower values for saturation voltage compared to a standard FET (e.g. a change of saturation voltage with gate voltage of 0.21V/V). Hydrogenated amorphous silicon (a-Si:H) was used as a semiconductor (100nm) and a 300nm layer of silicon nitride as an insulator, in a bottom gate technology. The source barrier was made using chromium over a semiconductor surface implanted with 10keV phosphorus for barrier modification purposes [104, 105].

The change in saturation voltage with respect to the change in gate voltage was in accordance with calculations based on the dielectric model. Values for the effective tunnelling constant α [105] were in the range 2 – 3.5nm and are in agreement with measurements on a-Si:H diodes [113-114], decreasing with implant dose, as more damage is created in the semiconductor. As predicted, for relatively short parasitic FET channels, source-drain separation was found to be practically of no consequence on the magnitude of the saturated drain current. Additionally, the authors reiterate in [111] the independence of drain current on source drain separation in saturation and show the linear dependence of the saturation current on source width.

Further studies on devices fabricated in a-Si:H [111] have revealed much better stability of the SGT compared to the FET under gate bias in the 'strong inversion' region. Stability is also somewhat improved in 'weak inversion'. This is due to a much lower number of excess carriers in the SGT which reduces the probability of dangling bond creation.

The frequency behaviour of amorphous silicon SGTs was studied in [106]. The measurements on a-Si:H devices show a linear dependence of the device time constant on average current density though the source. A theoretical study on high frequency operation of the Schottky barrier SGT [108] showed that the cut-off frequency is proportional on the average current density through the source. It was assumed that the gate-to-drain capacitance is negligible and that the current is entirely controlled by the source barrier (short **d**, highly conductive channel).

Source-gated transistors have also been implemented in polysilicon (poly-Si) [112]. A silicon oxide layer of 150nm and a layer of poly-Si 40nm thick were used. Poly-Si was formed using an excimer laser from amorphous Silicon. The metal used for the source

barrier was again chromium. All devices had a field-relief plate built into the source electrode and source-drain separation was between 2 an 60 microns. Saturation current has been found to be independent of source-drain separation. Output resistance in the range of $10^9\Omega$ was measured in saturation ($\mathbf{V_{SAT}} < 2V$). At high drain voltage, operation is adversely affected by the presence of the field plate passivation structure.

So far the SGT has been fabricated using thin-film silicon technology. A similar concept has been demonstrated in crystalline silicon. nMOS Schottky Tunnelling Source devices have been made starting from a Schottky source MOSFET by overlapping the gate electrode and the source implant [115]. The device shows higher output impedance and higher intrinsic gain than conventional Silicon-on-Insulator MOSFETs. The study also concludes that the device is less prone to threshold changes as the source-drain separation is decreased into the deep-sub-micron region.

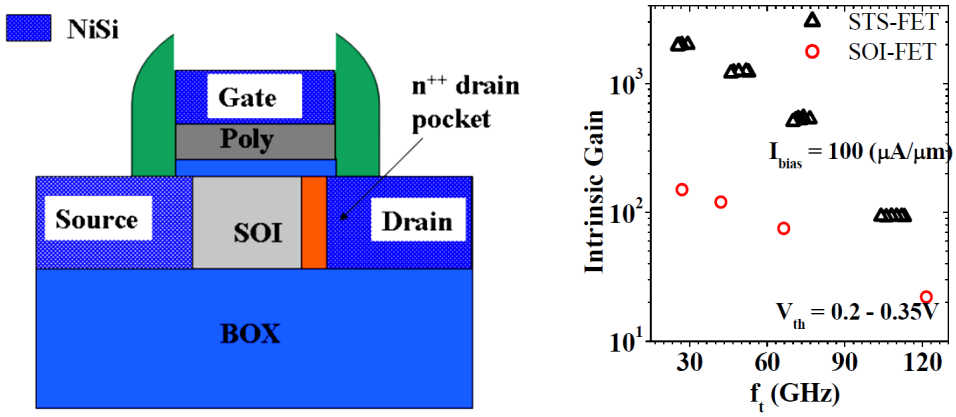


Figure 4.4. nMOS Schottky Tunnelling Source device (left) and its gain plot compared to a standard SOI transistor (right), from presentation of [115].

Guo and Shannon present in [116] the results of mixed-mode circuit simulations involving organic SGTs. A current-mode inverter in pentacene was modelled and its switching performance was inspected. Source-gated transistors can perform much better than regular FETs when the source-drain gap is scaled below 1μm; the authors found that the field-dependent mobility of pentacene, albeit low, can be increased enough by using small source-drain gaps to permit inverter operation in the MHz range, which is far higher than what full-swing inverters with OTFT can achieve. They also show that the circuit has a wide input dynamic range and that performance deteriorates if the source length is increased, in accordance with [108].

More information on the SGT can be found at [117].

Chapter 5. Self-aligned poly-Si source-gated transistors

5.1. Introduction

Thin-film polysilicon layers enable large area, inexpensive devices and circuits to be fabricated for use in systems concerned with the man-machine interfaces [118, 119] or cheap, disposable portable devices, resulting from the economies of scale.

To date, the application of polysilicon devices is almost entirely restricted to digital circuits. In this thesis we are concerned with analog circuits, and in particular the amplification factor or intrinsic gain of the thin-film transistor. It is difficult to obtain high intrinsic gain in conventional polysilicon FETs because the output characteristic is degraded by the so-called "kink effect" in which minority carriers generated in the high field region at the drain under saturation drift back toward the source and increase the drain current via bipolar amplification [75-77]. Therefore, the output impedance is only large for small drain voltages. In a source-gated transistor, however, we have a reverse biased barrier at the source [110] that extracts any minority carriers. Furthermore, saturation is far stronger because it occurs at both the source and the drain and the output impedance can be very large.

In this chapter we examine source-gated transistors made from polysilicon on glass substrates. These devices have drain contact regions which are self-aligned to the gate and the source barrier is a Schottky contact (SBSGT). A summary of the technological process used for fabrication is presented in Section 3.6. Subsequent sections prove that the devices that were fabricated behave like SGTs, as expected, and describe the different means of tuning some of the electrical parameters; the metrics important for circuit operation, such as intrinsic gain and frequency behaviour, are examined.

The final sections describe the working of SGT devices with a unipolar barrier at the source (BUSGTs). These initial simulations outline the advantages and disadvantages of devices this type of barrier.

5.2. Basic electrical characteristics of the polysilicon SBSGT

Source-gated transistors (SGTs) based on the previous section were designed, fabricated and tested. To be specific, there is a potential barrier at the source which exclusively controls the current between the source and the drain. The magnitude of the current is controlled by the effective barrier height, which in turn is modulated by the voltage applied on the gate.

This first set of electrical measurements attempts to validate the hypothesis that the devices are in fact SGTs. In order to accomplish this, we look for the tell-tale signs of SGT operation:

- Low saturation voltage ($\mathbf{V_{SAT1}}$) as described by equation 4.2;
- Low value of the change in saturation voltage with gate bias, as per equation 4.3;
- High output impedance in saturation;
- Absence of kink effect;
- Drain current independent of source-drain separation;

5.2.1. SGT versus FET

The SGT is made up of a reverse biased Schottky barrier at the source (with a barrier changing implant) in series with a parasitic FET of length d. Since the drain contact of a SGT is forward biased in the on-state, it can be a barrier just like the source. The source and the drain can therefore be reversed to give symmetrical SGT characteristics. However, in the structure made here, the drain contact is ohmic. By swapping the source and drain terminals and operating the SGT in reverse, one can obtain the characteristics of a FET. This FET has an ohmic source (the drain of the SGT) and a forward biased Schottky barrier at the drain (the SGT's source). By running the device in both SGT and FET mode, we can study the behaviour of both types of structure on the same device and make a direct comparison between the performance of the two device topologies.

The output and transfer characteristics were measured on devices similar to that shown in Figure 3.5, accounting for all permutations of source length (**S**), source-drain separation (**d**), bulk doping and barrier changing implant.

Figure 5.1 shows the output and transfer characteristics of a typical device for both modes of operation at the same saturation current. In this side-by-side comparison the defining features of the SGT can be observed [104]:

- Lower saturation voltage;
- Far higher output impedance in saturation;

- Lack of kink effect;
- Lower leakage in the off-state;
- Lower transconductance above the threshold (where the barrier controls the current);
- Good on-off ratio, exceeding that of the FET at high voltage.

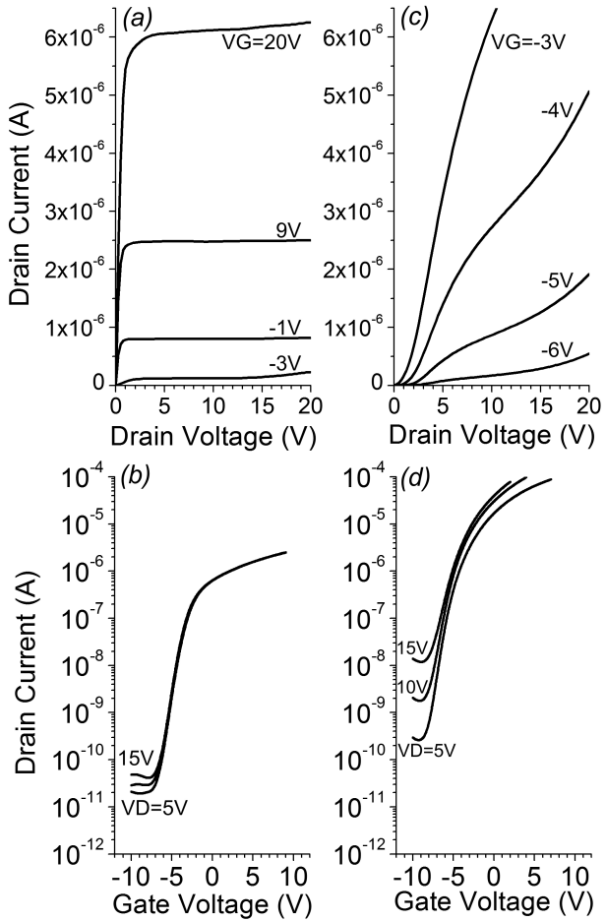


Figure 5.1. Characteristics of SGT (a), (b) and FET (c), (d) behaviour, at a similar current, obtained by interchanging the source and the drain on the same device. W=50μm, S=8μm, d=10μm, $1\cdot10^{13}cm^{-2}$ BF_2 barrier modification implant.

The FET is somewhat at a disadvantage in this setup, as the *p-type* implant which is used to tune the barrier profile in the SGT makes the drain of the FET very resistive. It is conceivable, however, that a structure with good performance in both SGT and FET modes can be devised and fabricated.

From the FET characteristics, the field-effect mobility can be extracted using the formula for drain current in the linear region. The calculated value based on Figure 5.1 is $\mu=33cm^2/Vs$.

It can be observed that the kink effect [75-77] is negligible in the SGT and very pronounced in the FET. The reason for the excellent performance of the SGT is that the

reverse biased source barrier extracts the minority carrier and thus prevents bipolar amplification. Some degradation due to carrier generation is still present, but the suppression of the amplification process makes the SGT far superior at high voltages.

5.2.2. Saturation mechanisms

In an FET the output conductance in saturation is determined by channel length shortening with increasing $\mathbf{V_D}$, combined with the effect of carrier generation in the high-field pinch-off region at the drain (the so-called "kink effect"). In the SGT one expects both these physical mechanisms to play a role but the saturation is more complicated because as $\mathbf{V_D}$ increases, pinch-off and current saturation first occurs under the source, as shown schematically in Figure 5.2a and then, at higher $\mathbf{V_D}$, the device also pinches off at the drain end of the parasitic FET (Figure 5.2b).

As the drain voltage increases from a low value, more free carriers are swept away from the area underneath the source. As a result of the presence of the source barrier, depletion occurs at the source at a voltage (see Section 4.3):

$$V_{SAT1} = \frac{C_i}{C_i + C_S}\left(V_G - V_T\right) = \frac{C_i}{C_i + C_S} V_{SAT2}\,. \tag{5.1}$$

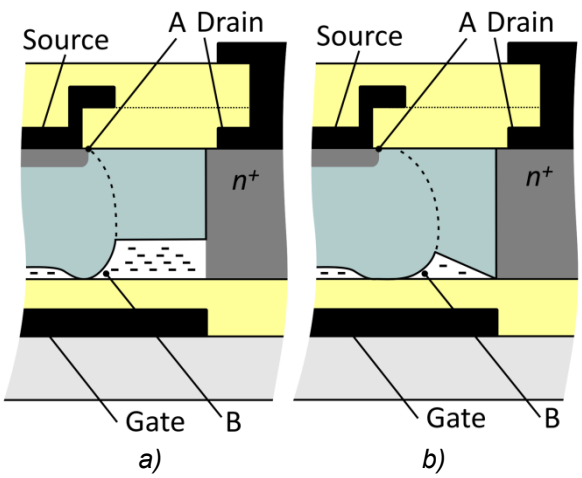


Figure 5.2. Schematic showing the two pinch-off states of the SGT. In (a) the semiconductor is pinched-off at the source. In (b) when $V_D = V_G - V_T$ the semiconductor pinches off at both the source and the drain. A is the corner of the source most sensitive to drain field. B is the position of the floating source of the parasitic FET.

The channel of the parasitic FET pinches off at the known value

$$V_{SAT2} = V_G - V_T\,. \tag{5.2}$$

There are four regions defining the output characteristic of an SGT, as illustrated in Figure 5.3:

1) $\mathbf{V_D} < \mathbf{V_{SAT1}}$. In this region, the parasitic FET is in the linear region. The current going through the source barrier is controlled by the depletion region which forms under the source contact and grows with increasing $\mathbf{V_D}$.

2) $\mathbf{V_{SAT1}} < \mathbf{V_D} < \mathbf{V_{SAT2}}$. The parasitic FET is in still in the linear region. The semiconductor is pinched off at the source and output impedance is governed by the effectiveness of the field relief structure [109] in protecting the source barrier from the drain field.

3) $\mathbf{V_D} > \mathbf{V_{SAT2}}$. The parasitic FET is also saturated. Output impedance is very high, since the excess drain voltage is dropped on the depletion region at the drain end of the FET channel. As a consequence, there is no change in the lateral field seen by the source barrier regardless of $\mathbf{V_D}$, apart from that induced by the shortening of the FET channel [54].

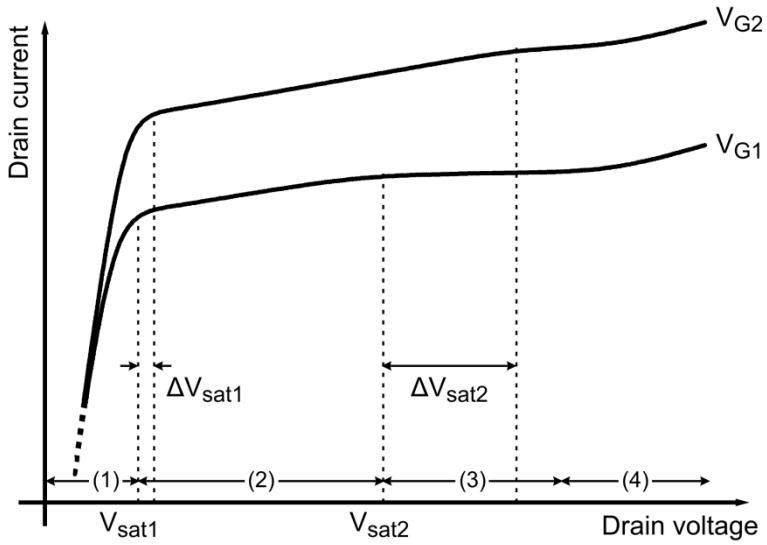


Figure 5.3. Schematic showing the saturation behaviour of the SGT [120].

4) $\mathbf{V_D} \gg \mathbf{V_{SAT2}}$. Carriers are generated in the high field region around the drain and they contribute to drain current. This would be the "kink" portion of a thin-film TFT's output characteristic, where output impedance degrades rapidly due to bipolar amplification of the current [75-77]. In an SGT, however, bipolar amplification does not occur, since the reverse biased source barrier extracts minority carriers and, as a result, there is only a slight decrease of output impedance.

Figure 5.5 also shows the shifts in $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$ which take place when the gate bias is increased. $\mathbf{V_{SAT2}}$ shifts to higher $\mathbf{V_D}$ at 1V for each additional volt applied on the gate. At the same time, the shift in $\mathbf{V_{SAT1}}$ is far less, due to the capacitive voltage divider that forms between the source and the gate, equalling $\frac{C_i}{C_i+C_s}$ V/V.

Exceptions are identified for high drain bias operation or for extreme values of **d**. At very high drain voltage, the high electric field in the pinch-off area near the drain of the parasitic FET generates additional carriers which deteriorate the output impedance of the device (region (4) in Figure 5.3). For very small source-drain gaps, the drain field can modulate the effective source barrier height and the drain current experiences pronounced drain field dependence.

Conversely, a very long source-drain separation creates the situation of the source barrier being in series with a long, resistive channel and as a consequence the output characteristic of the SGT is controlled by a combination of the two, as described schematically in Figure 5.4. The characteristic of the long channel parasitic FET has a lower slope in the linear regime, and the SGT has to follow this curve until the current is limited by the source barrier, resulting in a shift in $\mathbf{V_{SAT1}}$ to higher voltage than predicted by Equation 4.3.

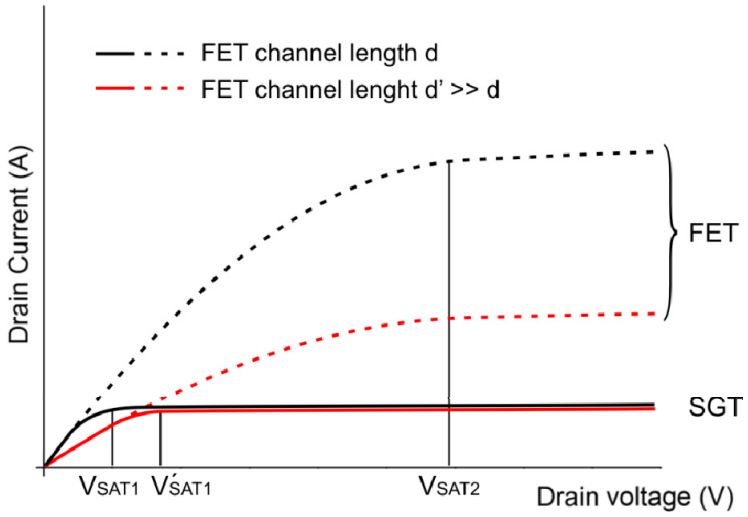


Figure 5.4. Schematic showing shift in V_{SAT1} due to increased parasitic FET channel length.

The change in carrier density in the semiconductor in each saturation regime can be studied from the results of numerical simulations. Figure 5.5 illustrates the amount of charge under the source, in the channel of the parasitic FET and the fact that saturation at the source occurs at the extremity of the source region which is closest to the drain and is not uniform over the whole source length. This is due to the way the semiconductor region under the source is depleted by the gate field and is an important observation which impacts source length scaling and frequency behaviour. Additionally, Figure 5.5 shows the concentration of carriers in the bulk of the semiconductor and in the channel of the parasitic FET. For high drain voltages and in particular for $\mathbf{V_D} > \mathbf{V_{SAT2}}$, the carrier concentration becomes very low across the whole thickness of the semiconductor layer, leading to a reduction in capacitance which should also lead to improvements in the frequency characteristic.

$V_D < V_{SAT1}$

$V_{SAT1} < V_D < V_{SAT}$

$V_{SAT2} < V_D$

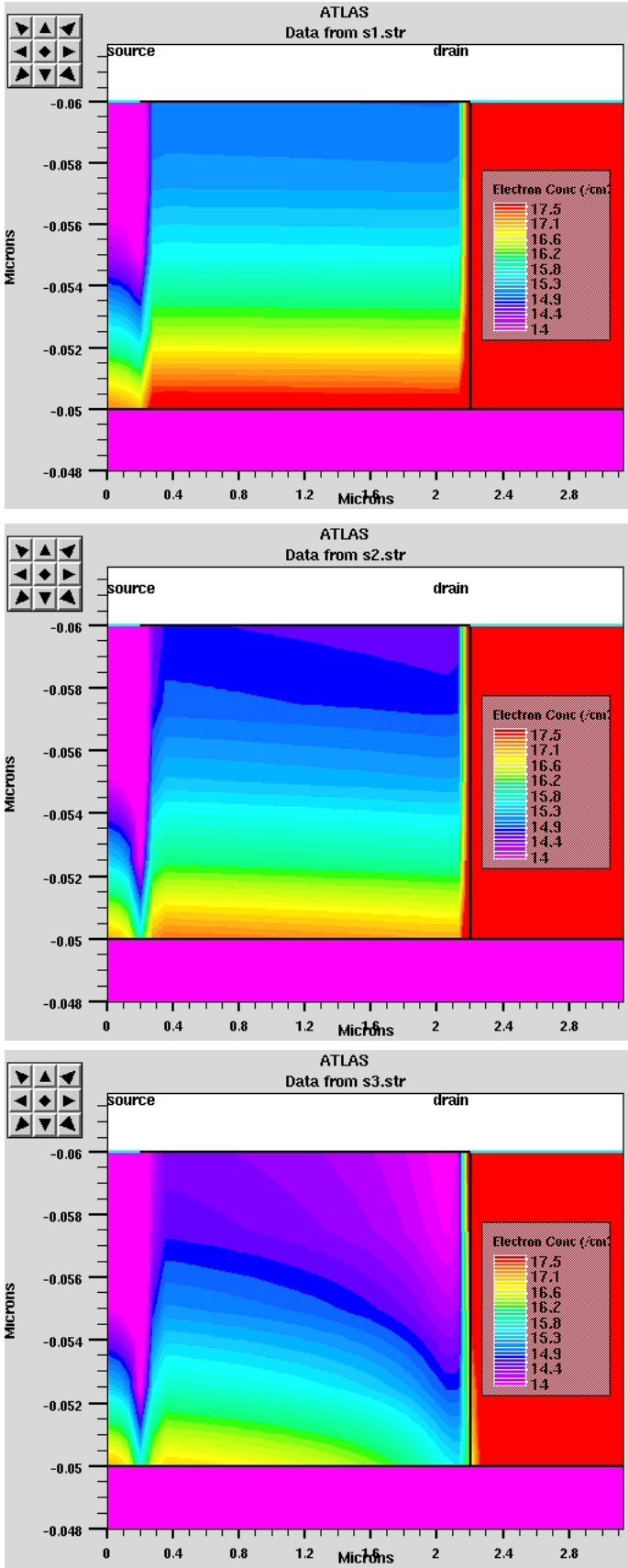


Figure 5.5. Simulation showing the electron density in the semiconductor under the source and in the channel region of the parasitic FET for three values of drain bias.

The depletion region at the source extends slightly toward the drain over an area which changes with drain bias, thus the source of the parasitic FET (point B in Figure 5.2) will change position depending on operating conditions. The actual change in saturation voltage for real devices, which will be identified as γ from this point onwards, is *at least* $\frac{C_i}{C_i+C_s}$. Depending on several factors which are discussed below, γ can be much larger than the value predicted by the electrostatic model.

The value of $\partial V_{SAT1}/\partial V_G$ for a range of insulator and semiconductor thicknesses is plotted in Figure 5.6. It can be seen that if a thick insulator is used, $\partial V_{SAT1}/\partial V_G$ can easily be less than 100mV/V. However, thick insulators are not mandatory for low $\partial V_{SAT1}/\partial V_G$ as long as the semiconductor is kept thin (tens of nanometres).

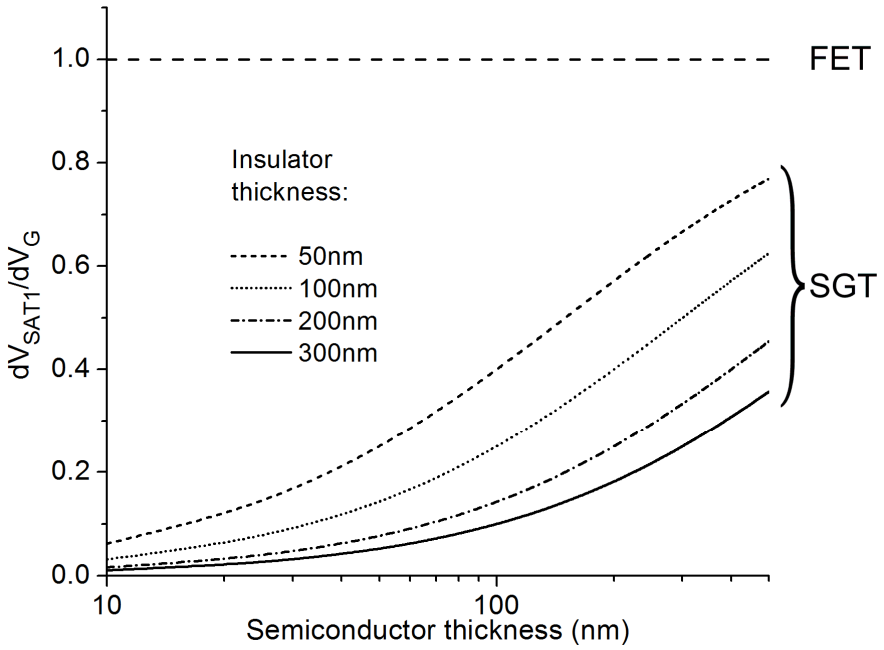


Figure 5.6. Calculated values of $\partial V_{SAT1}/\partial V_G$ (denoted SGT) and $\partial V_{SAT2}/\partial V_G$ (denoted FET) for different insulator and semiconductor thicknesses.

For the technology used in this study, $\frac{C_i}{C_i+C_s}$ = 0.041V/V, which is much lower than the change in $\mathbf{V_{SAT2}}$ with gate voltage, which is 1 (V/V) for a device which is not operating in velocity saturation. Measured values for γ at low gate bias are around 40mV/V, which agrees well with the calculation (Figure 5.7). The plot also shows the evolution of $\mathbf{V_{SAT2}}$ with gate voltage; as expected, $\mathbf{V_{SAT2}}$ shifts to higher voltage at the rate of about 1V/V.

The higher the bulk doping, the larger the value of γ, since it higher voltage is needed to deplete the semiconductor under the source. The output characteristics of two devices with identical geometries but different bulk doping are compared in Figure 5.8. While the saturation of the device in Figure 5.8b is sharp and well defined, the device in Figure 5.8a

shows a more rounded feature, with current increasing abruptly but taking comparatively high drain voltage to reach saturation.

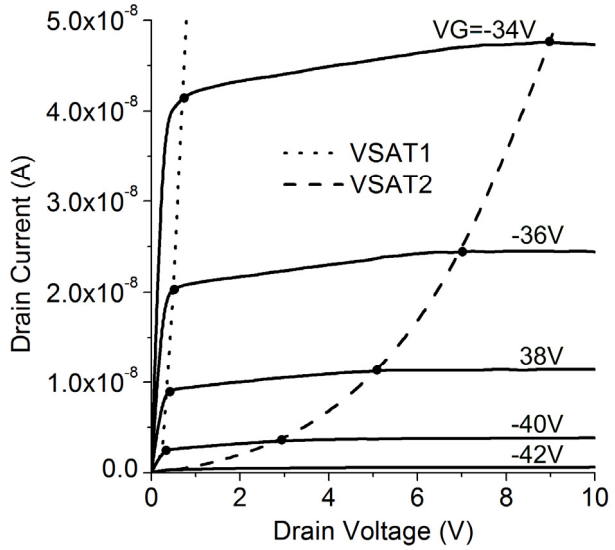


Figure 5.7. Measured output characteristic showing V_{SAT1} and V_{SAT2} envelopes. W=50μm, S=2μm, d=10μm; barrier changing implant: $7.5\cdot10^{12}cm^{-2}$ p-type; bulk doping: $10^{13}cm^{-2}$.

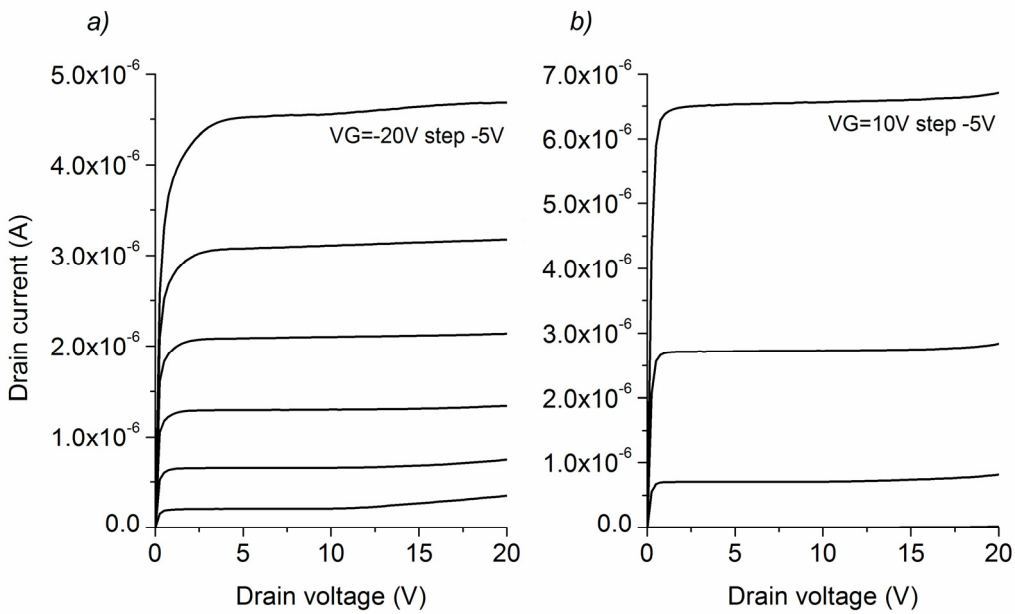


Figure 5.8. Output characteristics showing rounding of the curves before the current saturates for the device with the higher bulk doping. W=50μm, S=2μm, d=4μm; barrier changing implant: $10^{13}cm^{-2}$ p-type; bulk doping: (a) $3.5\cdot10^{12}cm^{-2}$, (b) $0.5\cdot10^{12}cm^{-2}$.

γ is also higher than $\frac{C_i}{C_i+C_s}$ when barrier modification implant is used (Figure 5.9). This is most probably due to the high dose BF_2 implant below the Cr source and the resulting doping profile. Since the annealing temperature for this implant was limited to 500°C to prevent glass compaction, there will be some residual damage centres and inactive boron making depletion more complicated.

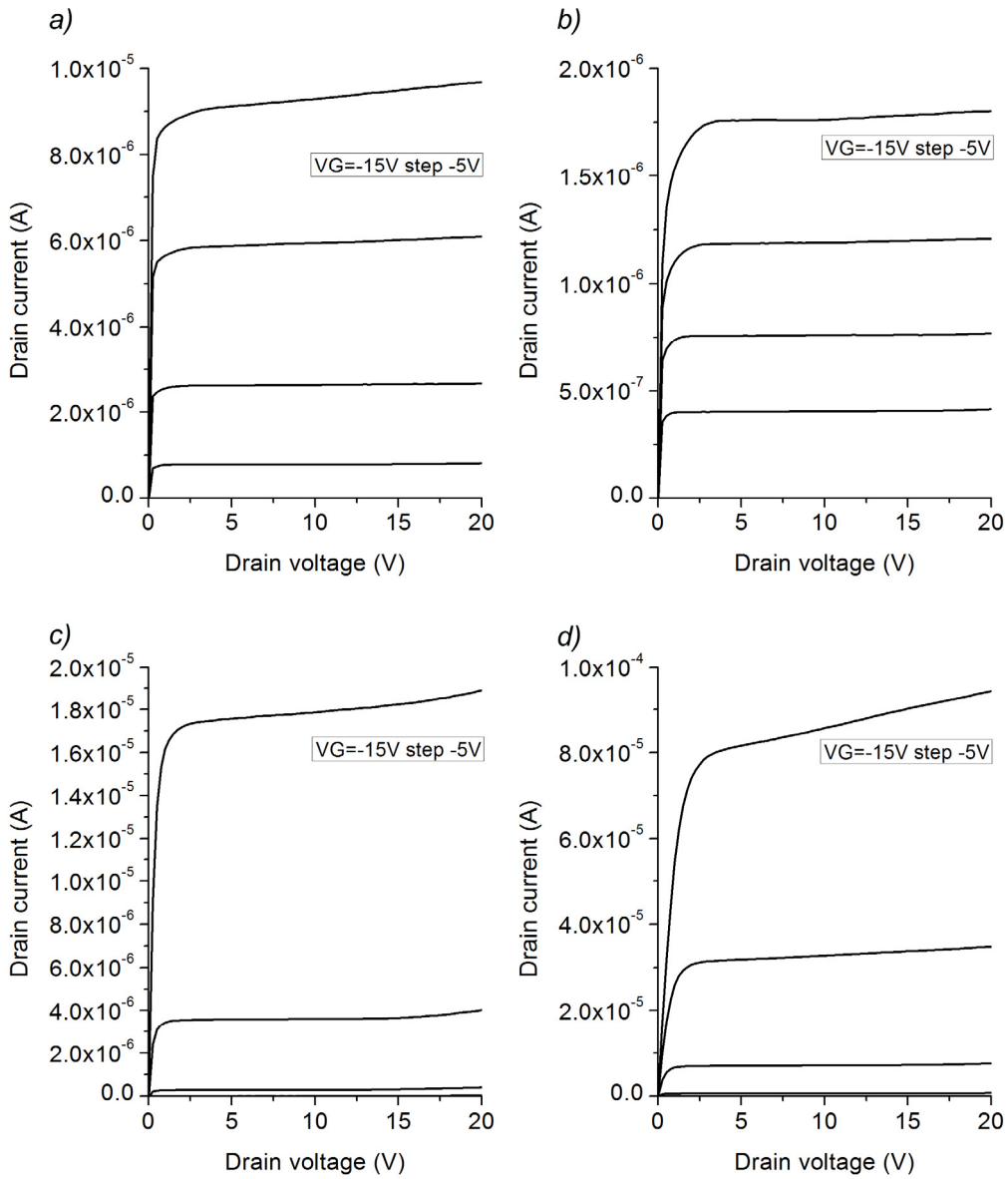


Figure 5.9. Output characteristics showing rounding of the curves before the current saturates for the device with the higher barrier modification implant. W=50μm, S=2μm, d=4μm; bulk doping: 2.5·10^{12}cm^{-2}; barrier changing implant: (a) 0, (b) 7.5·10^{13}cm^{-2} p-type, (c) 0.5·10^{13}cm^{-2} n-type, (d) 10^{13}cm^{-2} n-type.

Figure 5.10 plots the measured value **γ** of for the devices in Figures 5.8 and 5.9 against the theoretical value of 41mV/V.

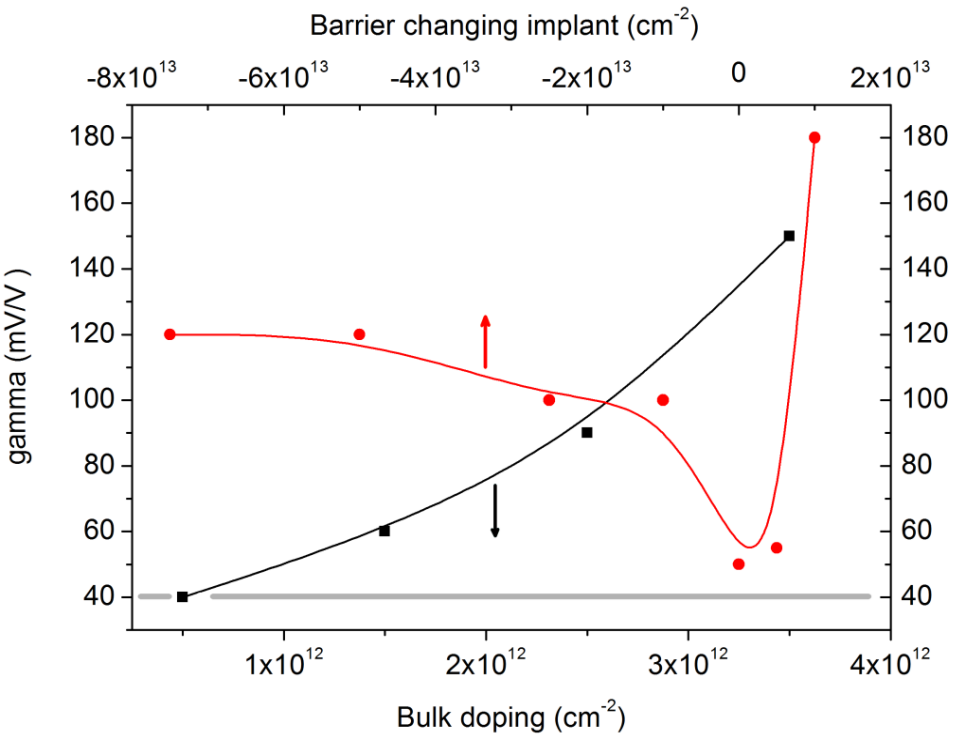


Figure 5.10. Measured γ for different values of bulk doping and barrier modification implant (equivalent n-type*), compared to the theoretical value of 41mV/V. For the red curve, the bulk doping is $2.5\cdot10^{12}cm^{-2}$* n-type*; for the black curve, the barrier modification implant is: $10^{13}cm^{-2}$* p-type.

From Figure 5.10 it is apparent that the measured **γ** is proportional to bulk doping and can go as low as the value calculated from the electrostatic model of the SGT, for the lowest bulk doping equivalent to $1.25\cdot10^{17}/cm^{-3}$.

Low barrier changing implants have practically no effect on the way the devices saturate. Lowering the barrier by using a high implant increases drain current dramatically to the point where it is comparable to that of the FET, and in this case there is a big increase in **γ**. On the other hand, **γ** increases somewhat but is relatively insensitive to the concentration when implants designed to increase the barrier height are used. As described above, damage centres and inactive impurity atoms are probably the cause of this phenomenon.

Lastly, γ is higher in devices with large source-drain separations, as the voltage drop along the channel of the parasitic FET (which is operating at this point in the linear region) becomes significant. This effect is shown in Figure 5.11, where two identical devices, except for source-drain gap were operated in the same conditions. The drain current saturates at the same value, but saturation occurs at higher $\mathbf{V_D}$.

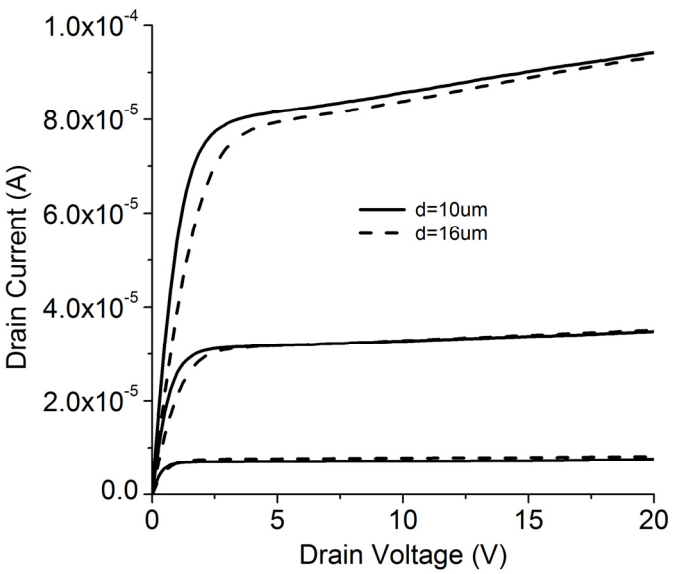


Figure 5.11. For high current devices, the dependence of the saturation point on parasitic FET channel length is not negligible. The value for d *is the approximate effective source-drain separation obtained in silicon.*

5.2.3. Output impedance in saturation

For $\mathbf{V_D}$ between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$, the parasitic FET is still in the linear region, but the SGT current is saturated due to the pinch-off which occurs at the edge of the source. (Table 5.1).

TABLE 5.1. OPERATING REGIONS OF THE SGT AND PARASITIC FET

Drain voltage	Parasitic FET region	SGT region
$V_D < V_{SAT1}$	Linear	Linear
$V_{SAT1} < V_D < V_{SAT2}$		Saturation
$V_D > V_{SAT2}$	Saturation	

For a given gate bias, the source barrier experiences an electric field composed of the components induced by the gate and by the drain. Thus, in this regime, the saturated current of the SGT will have a drain voltage dependence which varies according to several parameters.

Firstly, the longer the source-drain separation, the smaller the drain field for a given drain voltage.

Second, the field relief plate (Figures 3.6 and 5.2) acts by spreading the drain field away from the area of the source which is most exposed (point A in Figure 5.2).

Finally, the *p-type* doping underneath the source of some devices acts itself like a field relief structure around the periphery of the source, which impedes the drain field from reaching the sensitive area of the Schottky barrier. The *n-type* barrier changing implant in the other devices creates a lower effective barrier height and the saturated current increases which leads to the condition described in the previous paragraph.

The output impedance in saturation when $\mathbf{V_{SAT1}} < \mathbf{V_D} < \mathbf{V_{SAT2}}$,

$$Z_O = \frac{1}{g_d} = \left(\frac{\partial I_D}{\partial V_D} \right)^{-1} \tag{5.3}$$

has a drain field dependence which varies with device geometry, effective barrier height and efficacy of the field relief structure. Measured values for $\mathbf{Z_O}$ in this region vary between 10^{10} and 10^6 **Ω**, depending on these factors. Substantial $\mathbf{Z_O}$ is a very desirable device characteristic for applications in signal amplification, reference signal generation and biasing schemes.

The large output impedance of a typical device operating at low current just above the threshold can be observed in Figure 5.7.

When $\mathbf{V_D}$ reaches $\mathbf{V_{SAT2}}=\mathbf{V_G} - \mathbf{V_T}$, the output impedance can be extremely high (well above the several 10^{10} noise floor of the measuring setup) for all devices. This figure is deteriorated somewhat at very high drain bias by the generation of carriers in the high field area around the drain, as explained in Section 2.4.2. It is worth noting, however, that though in an FET minority carrier current tends to be amplified because the source junction becomes forward biased and there is a bipolar effect (the kink effect), in the SGT the source is reverse biased, minority carriers are extracted and no amplification occurs. Far better high voltage characteristics can be observed when comparing the SGT with the equivalent FET (Figure 5.1).

As a final comment it should be noted that due to the thick insulator in these devices, the gate bias has to be relatively high in order to get good current output. As such, most devices will operate in the region between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$ even at high drain voltage. In order to benefit from the extremely high impedance that can be obtained from these structures, a mix of operating voltage, gate voltage, barrier modifying implant and device width needs to be chosen carefully, to make possible operation just above the threshold voltage of the FET. For most applications, however, the output impedance delivered between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$ is sufficient.

5.2.4. Barrier lowering by gate action

The effective height of a reverse-biased Schottky barrier can be lowered by applied electric field. Shannon [42] has demonstrated that the barrier lowering constant, α, has a value of approximately 2.7nm for silicon and we expect to obtain results of similar nature from the source barrier of these polysilicon devices.

The barrier lowering constant was extracted from measurements using Equation 4.5. For the device in Figure 5.1, α = 2.8nm, which is in good agreement with the theory [42].

We can calculate the change in barrier height with gate voltage. From Equation 2.18:

$$\frac{\partial \Phi_B}{\partial V_G} = -\alpha \frac{\partial E_S}{\partial V_G}, \tag{5.4}$$

and Equation 4.6 gives the change in electric field with gate voltage at the metal-semiconductor interface:

$$\frac{\partial E_S}{\partial V_G} = \frac{\partial V_{SAT1}}{\partial V_G} \frac{1}{t_S}. \tag{5.5}$$

For this technology $\frac{\partial V_{SAT1}}{\partial V_G} = 0.04$ and $\mathbf{t_S}$ = 40nm, which lead to $\frac{\partial \Phi_B}{\partial V_G} = -2.8 meV/V$.

5.2.5. Dependence of saturated drain current on source-drain separation

Figure 5.12 illustrates the dependence of saturated drain current on source-drain gap. Provided that the parasitic FET is turned on strongly enough to allow the current to pass unimpeded, the output characteristic in saturation is independent of the source-drain separation, **d**.

The measurement results confirm the theoretical predictions. There is some spread in the data, most probably due to mismatches between what was designed and the fabricated devices, not in terms of **d**, but rather in general alignment (for example, the position of the field plate and drain metallisation over the parasitic FET channel). This assertion is supported by the fact that devices with identical currents for both drains have been measured; for an in-depth discussion of double-drain measurements, see Section 5.6.

We can conclude that in well designed SGTs the current in saturation is independent of **d** when the source-drain gap is in the micron range.

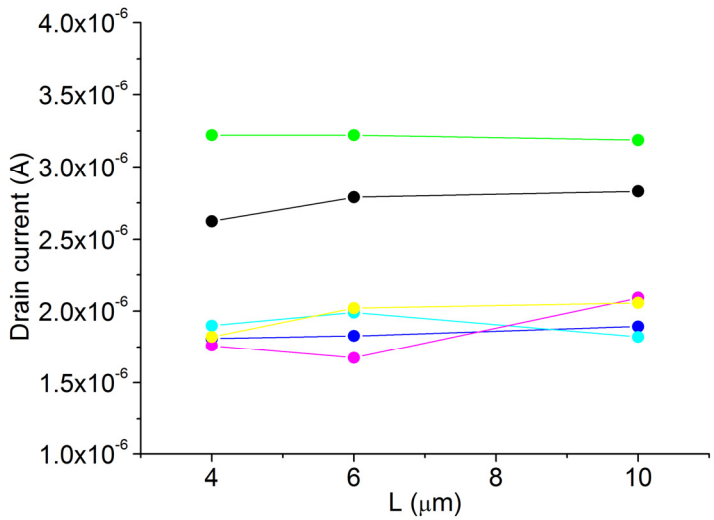


Figure 5.12. Variation of drain current with source-drain separation for otherwise identical devices.

5.2.6. Verdict on SGT behaviour

The fabricated polysilicon devices exhibit all the defining characteristics of source-gated transistors. We can conclude that these polysilicon thin-film transistors are SGTs.

The sections that follow explore the means of controlling the electrical characteristics of the polysilicon SGTs.

5.3. Control of barrier height

We have seen in section 5.2.4 that the measured barrier lowering constant, α, of about 2.8nm matches with the value expected from theory and prior measurements on Schottky barriers on silicon.

In an SGT, α is a measure of the change in effective source barrier height with applied gate voltage. Its value being greater than zero shows that an increase in gate bias results in a lowering of the effective barrier height which allows more current to be sourced.

The positive biasing of the gate relative to the source is the method used to modulate the height of the source barrier to electrons and therefore to change the current during SGT operation. At the design stage, the height of the barrier and its pull-down characteristics can be modified by making shallow implants through the source window. Depending on the type and concentration of impurities, the barrier height can be lowered or raised by precise amounts by controlling the magnitude of the electric field at the interface.

Figure 5.13 shows the normalised transfer characteristics (translated on the *x* axis to remove differences in threshold voltage) for devices with identical geometries but with different barrier modification implants.

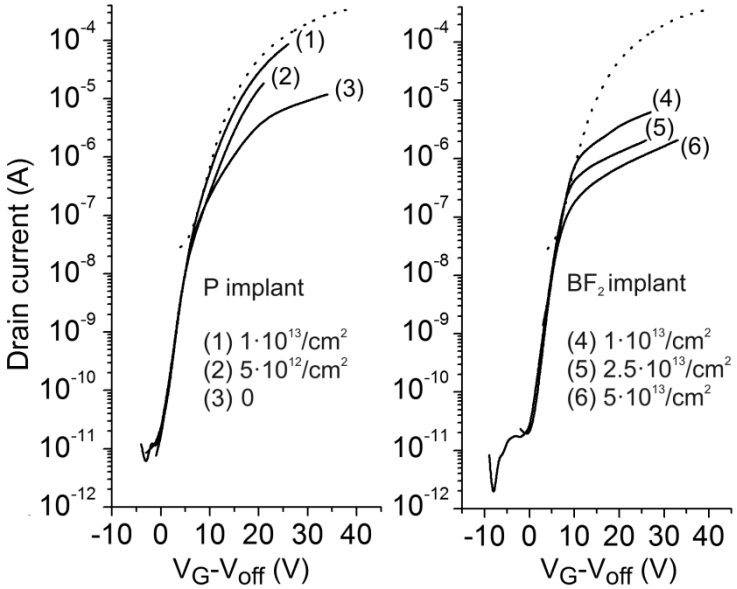


Figure 5.13. Transfer curves for different barrier implants at V_D=5V. Dotted line – FET, continuous line – SGT.

On the left, the plots show the effect of *n-type* doping. With increased concentration, the electric field increases and source barrier becomes narrower, effectively permitting carriers from lower energy levels, which are more numerous (see Figure 2.1), to tunnel into the conduction band of the silicon; the current increases with *n-type* doping. This trend is limited, however, by the envelope of the transfer characteristic of the parasitic

FET (shown as the dotted line in Figure 5.13). The FET channel has a finite conductivity at every gate voltage and if the source barrier is more conductive, an equilibrium situation is reached whereby the current is controlled both by the source barrier and the parasitic FET and so alpha is difficult to define in this regime.

Figure 5.13 also shows the consequences of increasing *p-type* doping concentrations in the barrier modification layer. *P-type* doping reduces the electric field, so the barrier becomes effectively higher at the higher doping levels, leading to less current flow. However, α remains largely unchanged at slightly below 2.5nm. This value is marginally lower than expected, and the variations are not monotonic with doping concentration. The discrepancies are probably due to a thin oxide layer in the source window and to the poor quality of the polysilicon layer following the BF_2 implant, respectively. The reader is reminded that the barrier modification implant was activated at low temperature which almost certainly resulted in partial activation and unrepaired damage to the polysilicon (see discussion on dopant activation in Section 3.6).

It has been shown that the barrier height can be changed by ion implantation. Carefully tuning the height of the source barrier can influence other electrical characteristics, such as temperature dependence of the current and gain curves, as shall be discussed later on in this chapter.

5.4. The effects of bulk doping on threshold voltage and off-current

Doping the bulk of the transistor is an effective means of controlling the threshold voltage ($\mathbf{V_T}$) and the subthreshold slope in FETs. Since the subthreshold region of the SGT characteristic is governed by the parasitic FET, this region of SGT operation can be controlled by the same means.

Figure 5.14 shows the change in the transfer curve with bulk implant for otherwise identical SGTs. As the *n-type* doping concentration increases, so does the subthreshold slope, and the threshold itself shifts to more negative voltages.

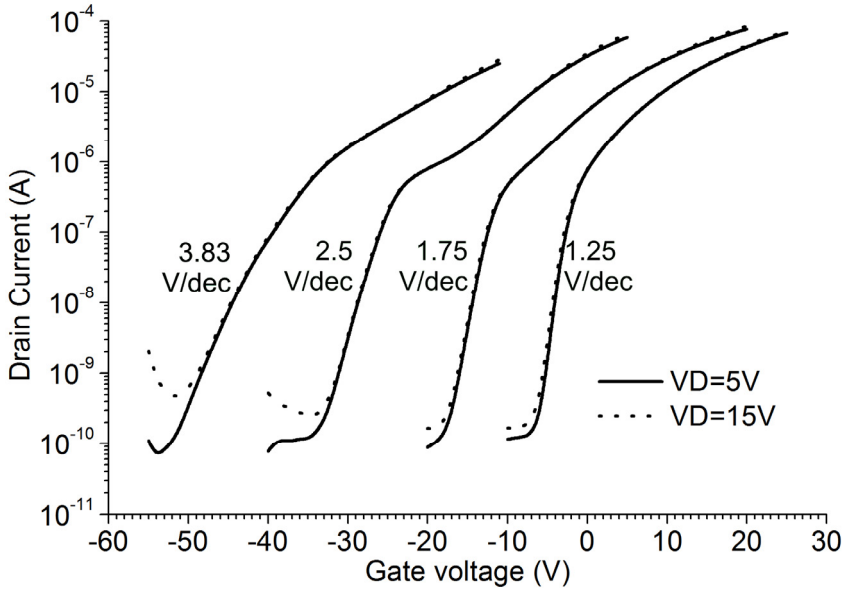


Figure 5.14. Transfer curves of SGTs with different substrate doping. W=50μm, S=8μm, d=10μm, 5·10¹² P barrier modification implant; areal doping, left to right: 3.5·10¹², 2.5·10¹², 1.5·10¹², 0.5·10¹² /cm² n-type.

The measured changes in average subthreshold slope are compared to the calculated values and the results are plotted in Figure 5.15. A certain discrepancy is observed between the two curves. The most probable cause is the fact that some of the measured devices were stressed prior to this experiment, whereas others were pristine. Threshold and slope changes are common during high field stress.

The change of threshold with bulk doping is not easily assessed in SGTs due to the fact that the knee of the transfer characteristic is due to the source barrier which limits the current and not to the threshold voltage as it is in a regular FET.

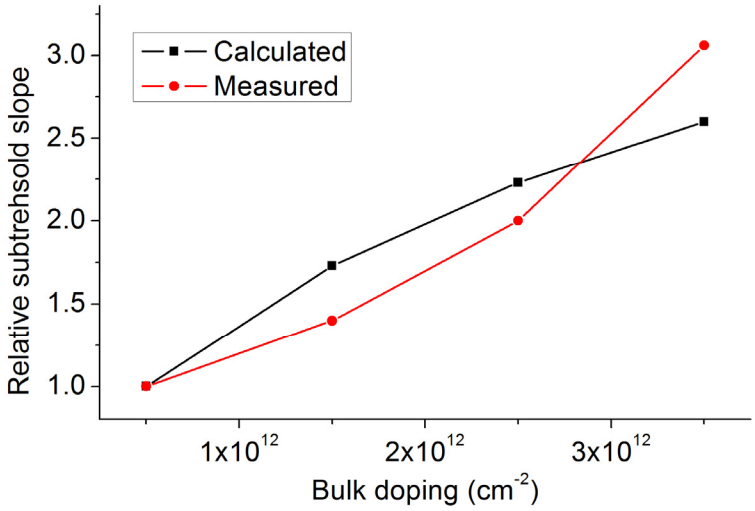


Figure 5.15. Normalised subthreshold slope (expressed in V/dec) against bulk doping.

Depletion-mode FETs, in which the threshold is made negative by bulk doping, are the harder to turn off, the higher the doping (Figure 5.16). The SGTs with the same bulk implant, however, turn off very well regardless of doping concentration. Moreover, from Figure 5.17 it can be seen that the off-current of the SGT does not increase considerably at smaller source-drain separations or at high drain voltage.

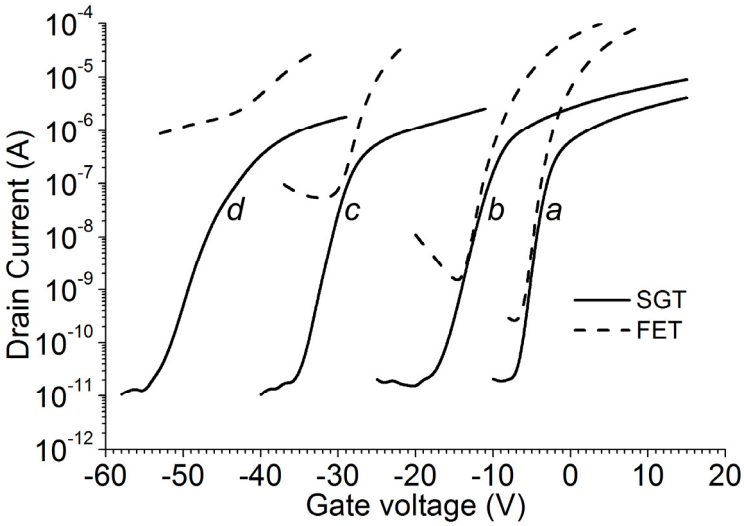


Figure 5.16. Transfer curves for different barrier implants at V_D=5V. Dotted line – FET, continuous line – SGT; Areal doping: a) $0.5\cdot10^{12}$; b) $1.5\cdot10^{12}$; c) $2.5\cdot10^{12}$; d) $3.5\cdot10^{12}$ /cm^2 n-type; $1\cdot10^{13}$ BF_2 barrier modification implant; W=50μm, S=2μm, d=4μm.

This performance improvement in terms of off-current relative to the FET is due to the presence of the reverse biased barrier at the source. As a negative gate voltage is applied on the gate of an *n-type* FET, there is accumulation of negative charges in the bulk of the semiconductor, resulting in a highly resistive, yet conductive path for leakage current.

The reverse biased source barrier in a SGT, however, impedes the flow of electron current in the off state when the drain is positive relative to the source, even though the parasitic FET is conductive (Figure 5.18).

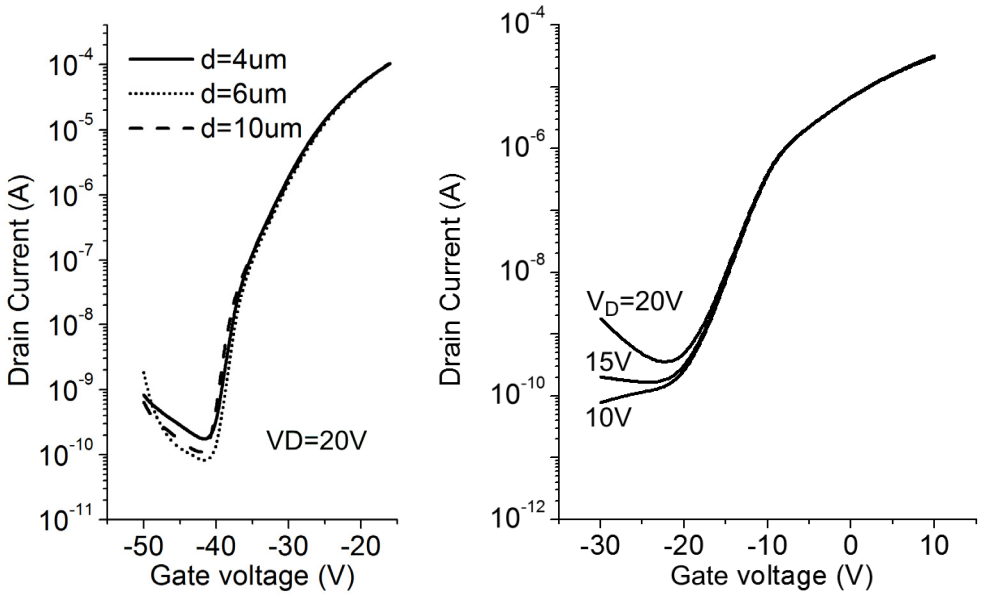


Figure 5.17. Measured transfer characteristics showing that the current is virtually independent of d or drain voltage.

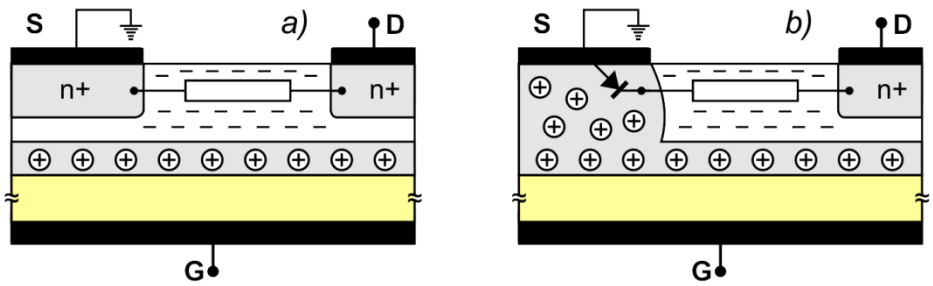


Figure 5.18. Schematic showing why a FET (a) cannot be switched off when the substrate is highly doped, whereas a SGT (b) can.

5.5. Other geometrical considerations

5.5.1. Dependence of drain current on S

The change of current with source length (**S**) has been measured in the past and it has been shown that the current is concentrated at the edge of the source as shown in Figure 5.19 [116].

The explanation can be found in the manner in which the drain field depletes the semiconductor under the source (Figure 5.5). This depletion region forms at the edge of the source closest to the drain, and it is in this region that the majority of the current flows. The rest of the source area has a minor contribution to the current, and as a consequence, the current does not increase substantially with source length, as long as **S** is larger than a saturation value (empirically found to be in the region of 0.5 – 1μm in an unpublished study).

This has important implications because the average current density ($\mathbf{J_S}$) will not have a linear dependence on **S**.

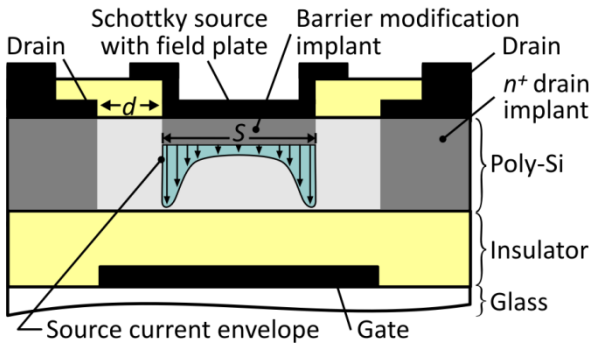


Figure 5.19. Schematic cross-section of the self-aligned SGT showing current crowding at the edge of the source.

The drain current was measured for SGTs with different source length, **S**, but otherwise identical. The results for several devices biased at the same $\mathbf{V_G}$ are shown in Figure 5.20. Figure 5.21 shows the dependence of drain current on source length at different gate biases. From the two figures, it can be seen that, allowing for process variations, the current hardly changes as the source length is increased from 2 to 8 microns.

In Figure 5.22 the results obtained from computer simulations are plotted for drain current over a range of source lengths. Figure 5.22a shows that, as source length increases, the drain current saturates ($\mathbf{S_{SAT}}$). Therefore, increasing **S** reduces $\mathbf{J_S}$, since the current becomes almost independent of **S**. If high $\mathbf{f_T}$ is required, the source should be less than $\mathbf{S_{SAT}}$, for optimum $\mathbf{J_S}$ (to maintain maximum current density during operation).

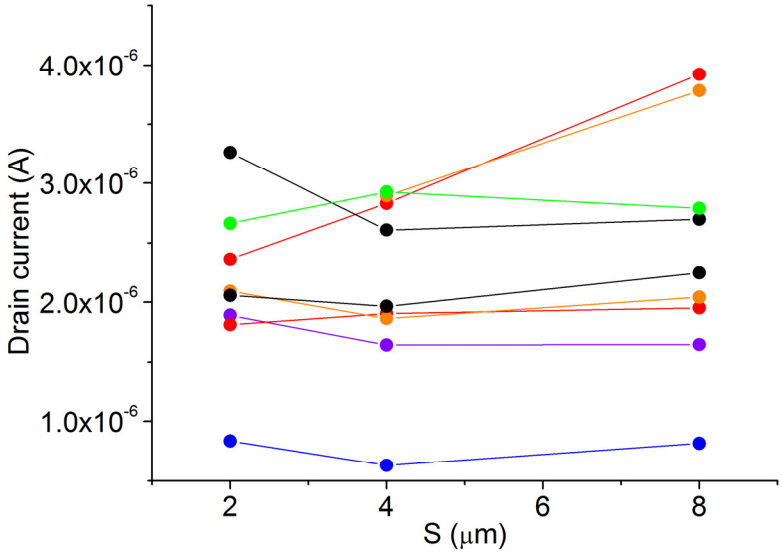


Figure 5.20. Measured variation of the drain current with source length.

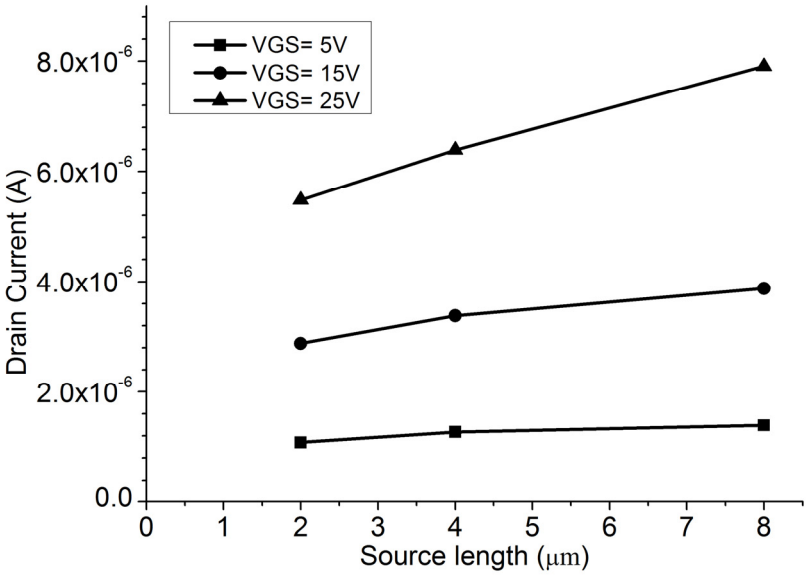


Figure 5.21. Measured dependence of the drain current on source length. Most of the current flows at the edge of the source opposite the drain; W=50μm, d=6μm.

It is worth highlighting that if current uniformity is desired rather than high operating frequency, **S** should be greater than $\mathbf{S_{SAT}}$, so that variations in **S** due to processing produce minimal changes in drain current. The current mismatch between two devices with a change of 0.1μm in source length is shown in Figure 5.22b.

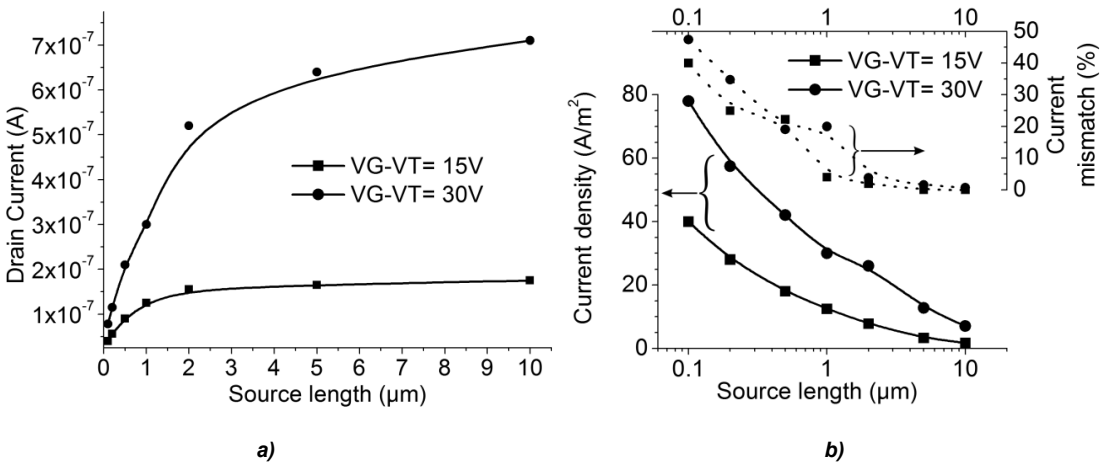


Figure 5.22. Computed variation of current (a) and current density (b, bottom) through the source as a function of source length. Current mismatch was calculated (b, top) for a 0.1μm change in source length.

We conclude that the current is virtually independent of source length for **S** > 2μm; an important point which contributes to the discussion on frequency behaviour in Section 5.8. It is easily seen that as **S** increases, so does the gate to source capacitance, whereas the current does not. This greatly affects the time constant of the device.

5.5.2. Double-drain measurements

The current crowding at the edge of the source (Figure 5.19), has a major advantage. For source lengths larger than $2 \cdot \mathbf{S_{SAT}}$, a device with a drain on each side of the source will draw double the current from the same source area. Each drain has its own area of the source from which it draws the majority of its current, and does not interfere with the current generation on the other side of the source.

To test the hypothesis of doubling average current density when both drains are connected experimentally, with some measurements being repeated, contacting either drain independently and both drains together. This is illustrated in Figure 5.23 where the current to each drain of an SGT with **S**=2μm is measured separately and compared with the current achieved when both drains are connected at the same time.

It can be seen that the currents to each drain are identical at low $\mathbf{V_D}$, and significantly, the sum of the currents measured with one drain connected is identical to the current obtained when both drains are used. This is an indication that there is no current sharing between the two drains, and that the current density exactly doubles for the double-drain structure.

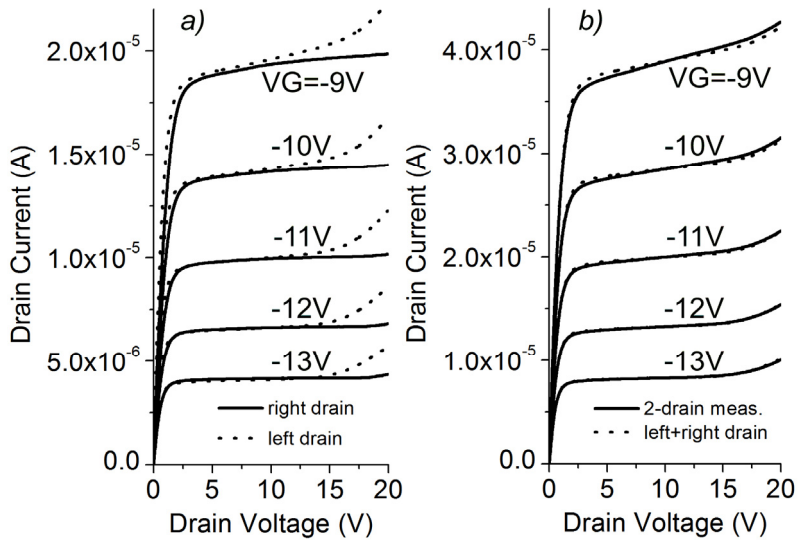


Figure 5.23. Output characteristics for the left and right drains on the same device (a), compared with drain current when both drains are connected (b). W=50μm, S=2μm, d_1=16μm, d_2=4μm.

A closer look to the device measured to obtain the characteristics of Figure 5.23 reveals that there is a large difference between the source-drain separations to the right and to the left of the source (around 6 microns, which is the largest of all the measured devices), as shown by the micrograph inset in Figure 5.24. The same figure shows the transfer characteristics obtained with either drain connected. As we expect, the off-current and the on-current are independent of **d**. The output characteristics shown in Figure 5.23 reveal the slight degradation in output impedance of the shorter-**d** device.

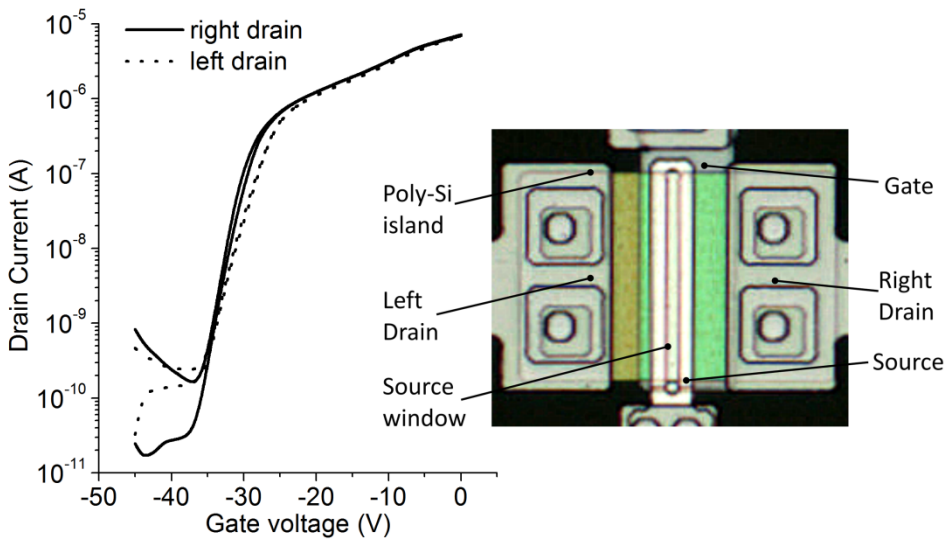


Figure 5.24. Left: Transfer curves for the left and right drains on the same device. Right: Micrograph of the measured device, showing the large discrepancy between the two source-drain separations. W=50μm, S=2μm, d_1=16μm, d_2=4μm.

The absence of current sharing between the two drains is of consequence in the frequency behaviour of the SGT, as will be shown in Section 5.8. When both drains are connected, the current doubles and so does $\mathbf{J_S}$; this effectively doubles the operating frequency of the device.

5.5.3. Current uniformity

With only six devices of each type on a substrate, uniformity is not easy to assess reliably. However, some information can be obtained from a limited number of measurements and compared with the theory.

Figure 5.25 shows the structure of the region of interest of each substrate. The area consists of six identical repetition of the same block of devices, labelled A to F. C and F are closest to the centre of the physical substrate; D is farthest away. The blocks are rectangular in shape, with a large aspect ratio, so identical devices in C and F are very close to each other, while the same device in block d is several centimetres away.

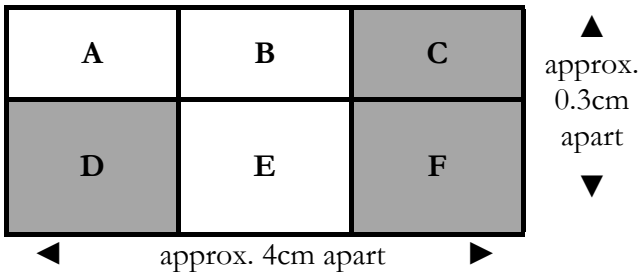


Figure 5.25. Each substrate contains six identical blocks, identified by the respective letter. Devices from the shaded blocks were compared to assess uniformity.

Nine devices were measured in each block and compared to identical ones in the other two blocks, focusing on the saturated drain current at high and low gate bias. The results are plotted in Figure 5.26.

The misalignment between blocks F and C is small and is mostly perpendicular to the direction of the current, and the results show little difference. Between block D and F there are mismatches of several microns in the longitudinal direction, and the differences are larger. Nevertheless, such large variations would never happen in a well controlled production run. These measurements prove that short range uniformity is good, but long range performance is only adequate. Vast improvements should be seen if the process would include a pre-compaction stage to eliminate the largest of the mismatches.

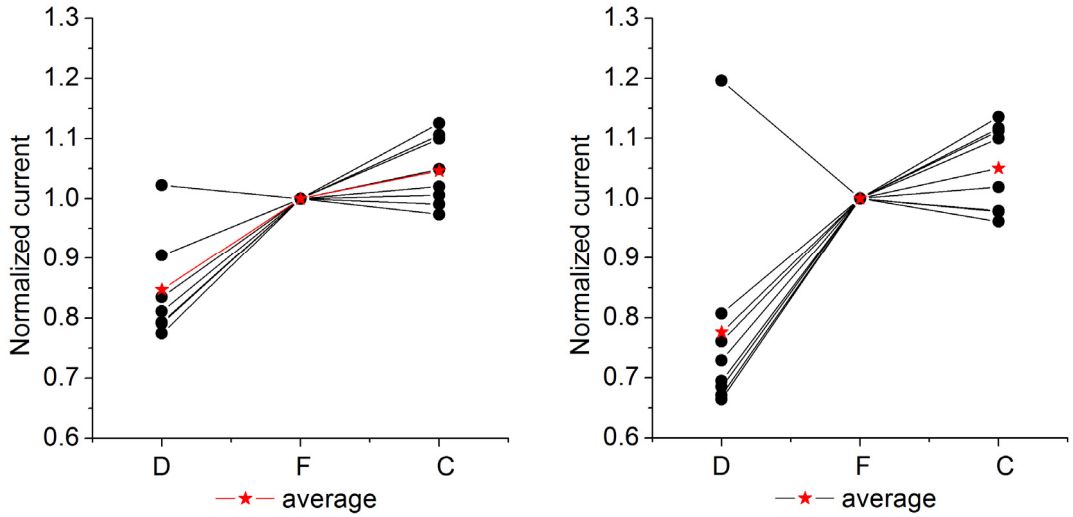


Figure 5.26. Current uniformity across the substrate for high (left) and low (right) gate bias; bulk doping $10^{13}cm^{-2}$; barrier modification implant: $2.5 \cdot 10^{12}cm^{-2}$ p-type.

5.6. Activation energy of the current

One potential disadvantage of the SGT with Schottky source compared to a FET is the temperature coefficient of the drain current. Since there is a metal-semiconductor barrier at the source, the current over/through the barrier will be thermally activated [41]. Large temperature coefficients are generally undesirable in most electronic circuit applications and this warrants an investigation into ways of improving the temperature dependence of the drain current in SGTs.

A typical plot of activation energy versus gate bias is shown in Figure 5.27a. The result is typical of a Schottky source SGT: the barrier is pulled down by the gate as expected, but the activation energy of the current ($\mathbf{E_A}$) is ≈0.25eV and a lot more than one would expect in an FET. A solution to this problem would be to make a field emission source in which at a large gate voltage the barrier would become transparent, with carriers tunnelling through the barrier at the Fermi level of the metal [106]. Using the highly developed technology available for polysilicon, it should be possible to achieve this by a combination of thin insulating films and precise doping.

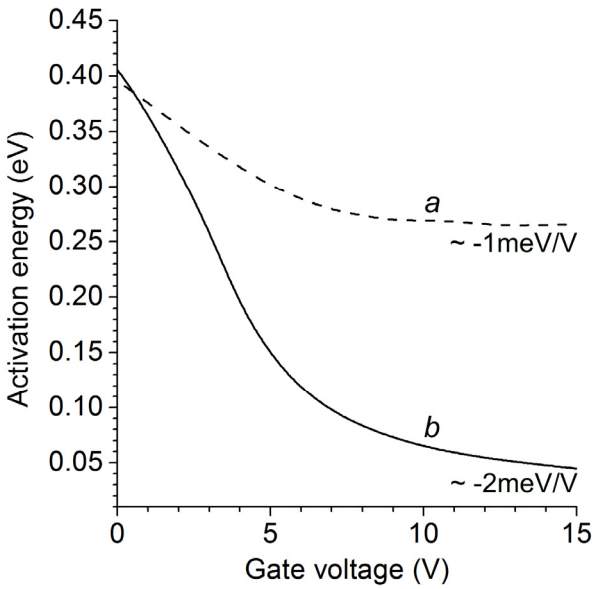


Figure 5.27. Change of activation energy for current transport for a) a SGT operating at low current and b) a SGT with barrier lowering implant (n-type), operating at high current.

Figure 5.27b shows the result of an attempt to reduce $\mathbf{E_A}$ by using an *n-type*, barrier lowering implant at the source. The implant has the effect of lowering the barrier and increasing the efficacy of the gate action in modulating the effective barrier height. The lower barrier increases the current through the device and, at the same time, lowers the

temperature coefficient of the current. At $\mathbf{V_G}$ =15V, $\mathbf{E_A}$ is ≈0.04eV; in this case, the current increases by only 30% between 30 and 100°C.

The above curves were extracted using the method explained in Section 2.3.1. From the measured values of α, the effective barrier lowering with gate voltage should be approx. –1.5meV/V for Figure 5.29a and –2.5meV/V for the plot in Figure 5.27b. The inconsistency may be due to errors in the estimation of α on curves that have a progressively lower slope as $\mathbf{V_G}$ increases (see Figure 5.13) and in rounding errors during processing.

Figure 5.28 shows the Arrhenius-type plots for the two devices described previously. It can be seen that current of the *p-type* barrier implant device changes less with gate voltage and is lower at maximum $\mathbf{V_G}$ than the other. The *n-type* barrier modification implant makes the device far more responsive to gate action and at high $\mathbf{V_G}$ the current achieved is higher, but the lines become almost horizontal, as a result of a weak dependence on temperature.

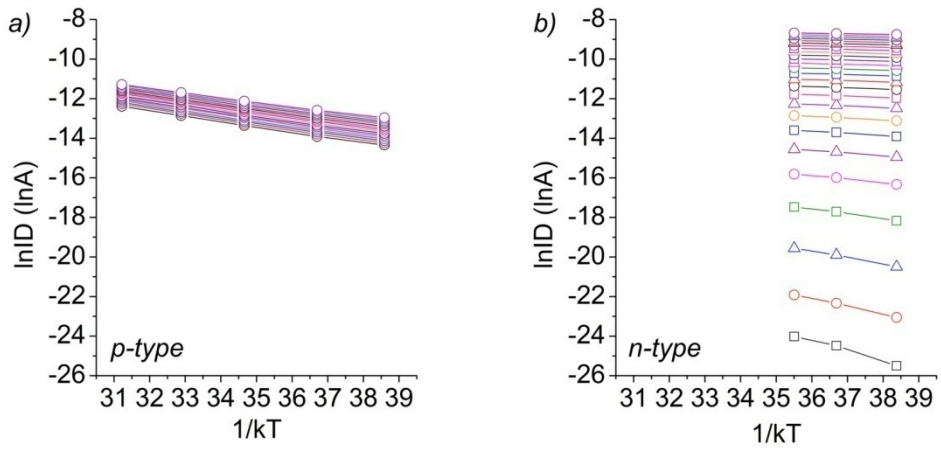
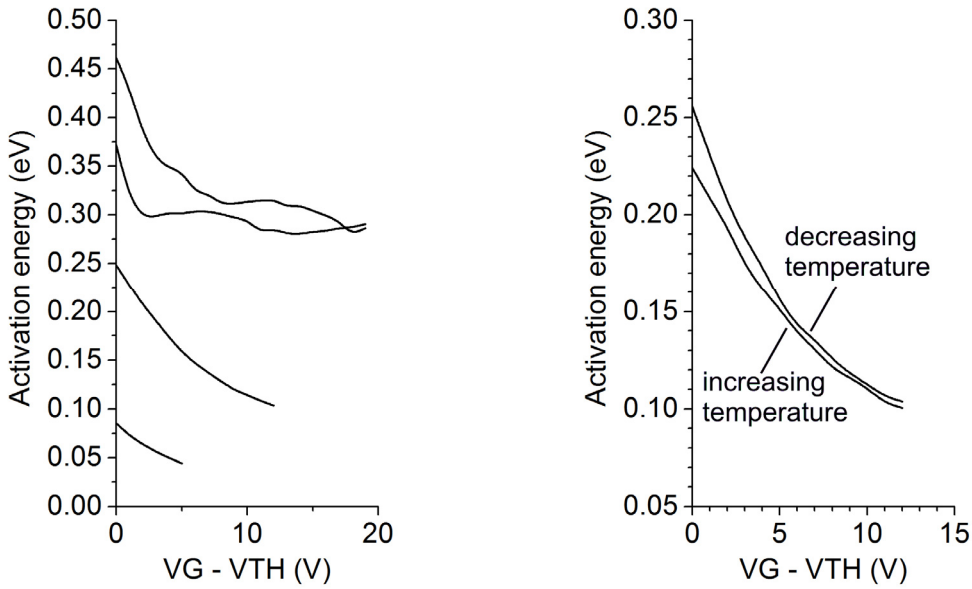


Figure 5.28. Activation energy plots from which the curves in Figure 5.28 were extracted, calculated for a number of gate voltages. At the top, V_G=15V.

The very low activation energy measured in the high current devices is unlikely to be due to the source barrier. The current is high enough to allow the channel of the parasitic FET to play a substantial role, and a non-negligible increase in $\mathbf{V_{SAT1}}$ is observed. We conclude, therefore, that these devices operate in a hybrid mode in which the on-state is partly controlled by the source barrier and partly by the parasitic FET. It seems that there is a negative feedback effect in which the FET, with its very low activation energy of the current restricts the change of current through the source. This hybrid mode could be very important when small changes of current with temperature are required. The trade-off is a small increase in $\mathbf{V_{SAT1}}$. To fully understand the interaction between the source barrier and the parasitic FET in this situation requires a further 2D analysis.

Figure 5.29a illustrates the way in which the barrier is pulled down by the gate field for different barrier modification implants. The effects of the different types of doping are

apparent: *p-type* implants increase the effective barrier height and make it difficult to pull down. *n-type* implants have an opposite consequence, leading to very high current to the point where the Schottky barrier ceases to be the sole or dominating factor in establishing the magnitude of the current.



a) *b)*

Figure 5.29. Activation energy versus gate voltage. a) Barrier pull-down profile for different barrier modification implants; top to bottom: $7.5\cdot10^{13}/cm^2$, $5\cdot10^{13}/cm^2$ p-type, $0.5\cdot10^{13}/cm^2$ and $10^{13}/cm^2$ n-type. b) Temperature hysteresis measured on the device with $0.5\cdot10^{13}/cm^2$ n-type implant.

The measurements were performed both while heating and cooling the device in order to test for temperature hysteresis. The results, shown in Figure 5.29b suggest that the device behaviour does not change irreversibly at increased temperatures. The plots are within the error margin which results from the precision of the calculations and from the temperature gradients inherent in the measurement setup.

To summarise, the activation energy of the current and the pull-down characteristic can be changed using barrier modification implants under the source. The activation energy can be made very low by means of an *n-type* implant, leading to low temperature coefficients and high current output which becomes limited due to a hybrid mode of operation.

P-type implants can be used to increase the temperature dependence of the current, a feature which may be exploited in temperature sensing applications.

5.7. Intrinsic gain

5.7.1. SGT intrinsic gain characteristic

The intrinsic voltage gain is given by the ratio of the transconductance $\mathbf{g_m}$ and the output conductance $\mathbf{g_d}$. It is an important performance criterion of field effect transistors, as it governs the maximum amplification which can be obtained from a single gain stage. Greater, desirable values are obtained when the transconductance of the transistor is large and when the influence of drain voltage on the current is minimised.

$$A_V = \frac{g_m}{g_d} \tag{5.6}$$

$$g_m \equiv \frac{\partial I_D}{\partial V_G} \tag{5.7}$$

$$g_d = \frac{1}{r_O} = \frac{1}{Z_O} \equiv \frac{\partial I_D}{\partial V_D} \tag{5.8}$$

In an FET the output conductance in saturation is determined by channel length shortening with increasing $\mathbf{V_D}$, combined with the effect of carrier generation in the high-field pinch-off region at the drain (the so-called "kink effect"). In the SGT we expect both these physical mechanisms to play a role, but a third region of interest is represented by operation between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$.

An analysis of the SGT with a Schottky barrier source shows that the transconductance is proportional to the average source current density $\mathbf{J_S}$ and the capacitance per unit area of the gate insulator [108]. Therefore $\mathbf{g_m}$ will increase with decreasing source barrier height and gate insulator thickness.

Intrinsic voltage gain ($\mathbf{g_m}/\mathbf{g_d}$) measurements were made on the polysilicon transistors having a range of source lengths and source-drain separations. The study includes the influence of bulk doping and the impact of variations in the characteristic of the Schottky source barrier due to implantation of dopants below the source barrier.

In general, the transconductance of the devices was poor in comparison to an equivalent FET because firstly the barrier lowering constant was low, presumably due to a thin oxide layer in the source window, and secondly the insulator was thick (200nm SiO_2 + 200nm SiN_x) compared to that in a typical polysilicon FET. This meant that $\mathbf{J_S}$ and $\mathbf{C_i}$ were much smaller than optimum. The output conductance, however, was very low for certain values of $\mathbf{V_D}$ and strongly $\mathbf{V_D}$ dependent. This led to voltage gains higher than a thousand in some devices.

An example of the drain voltage dependence of the intrinsic gain in these polysilicon SGTs is shown in Figure 5.30 for three different gate voltages.

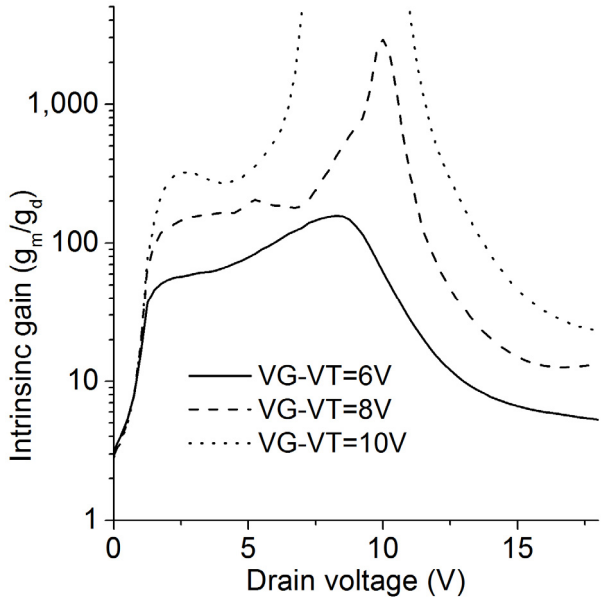


Figure 5.30. Intrinsic gain against drain voltage showing high gains around V_{SAT2}; W=50µm, S=2µm, d=10µm; 0.5·10^{13}/cm^2 n-type doping under the source barrier and 2.5·10^{12}/cm^2 n-type bulk doping.

The SGT gain characteristic has several distinguishing features.

It is apparent from Figure 5.31 that for a given $\mathbf{V_G}$ there are large variations in the gain with drain voltage. Since $\mathbf{g_m}$ does not change very much, these variations are due to changes in $\mathbf{g_d}$.

Most notably there are two peaks in each gain curve. The one at the lower drain voltage is associated with $\mathbf{V_{SAT1}}$, while the one at high $\mathbf{V_D}$ corresponds to $\mathbf{V_{SAT2}}$. The first peak occurs as the SGT saturates, and it can be seen that increasing gate voltage leads to an increase in gain in this region. This is due to the larger transconductance. The characteristic remains virtually flat until the second peak. At this point, the source barrier is completely isolated from the drain field by the pinched-off channel of the parasitic FET and $\mathbf{g_d}$ decreases rapidly to almost zero, leading to a very large gain figure. Gain in excess of several thousand was routinely observed, but it remains to be seen if these very high gains are practically useful. For higher gate bias, the increased transconductance improves the characteristic in this operating regime much the same way it does around $\mathbf{V_{SAT1}}$.

Increasing the drain voltage further beyond $\mathbf{V_{SAT2}}$ is detrimental to intrinsic gain. The degradation in $\mathbf{g_d}$ (which is far less than in a FET but potentially significant) which results from carrier generation compromises the gain, but the beneficial influence of $\mathbf{g_m}$ which results from higher gate bias is still observed.

Figure 5.30 also depicts the evolution of the two peaks as the gate bias is increased. The second peak shifts to the right at about 1V/V as predicted from the behaviour of $\mathbf{V_{SAT2}}$, while the first peak shifts only slightly, as is characteristic for $\mathbf{V_{SAT1}}$.

Comparing the performance with varying **d** (Figure 5.31), an improvement in the gain around and above $\mathbf{V_{SAT2}}$ is observed. This is to be expected, since in this region, $\mathbf{g_d}$ is entirely influenced by the parasitic FET and a longer channel results in a flatter characteristic. Gain peaks at higher values than in the shorter-**d** device, although it decreases rapidly at high $\mathbf{V_D}$ due to carrier generation. The devices contain a BF_2 implant, which should also aid passivation, since the polysilicon region around the edge of the window will be less *n-type*. The source-drain separations were 4 and 10 microns, respectively.

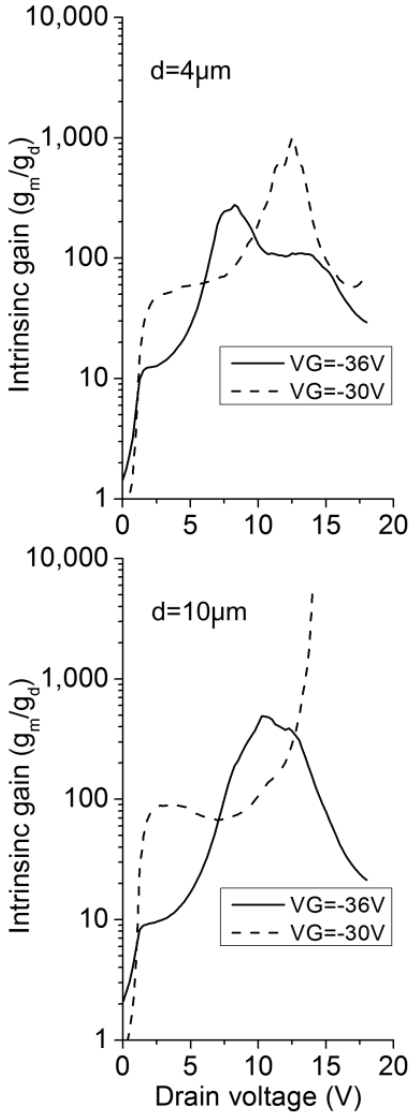


Figure 5.31. Intrinsic gain measurements on two identical devices apart from the source drain separation. W=50µm, S=2µm, $V_T \approx$ -40V. $7.5 \cdot 10^{13}/cm^2$ p-type doping under the source barrier and $2.5 \cdot 10^{12}/cm^2$ n-type bulk doping.

In Figure 5.31a, the gain around $\mathbf{V_{SAT1}}$ increases by around 5 for higher gate bias, due to a similar increase in $\mathbf{g_m}$. The gain at the second peak also increases fivefold. For the longer device in Figure 5.31b, the gain increase at the first peak is about 8, so we expect maximum gain around $\mathbf{V_{SAT2}}$ to be around 4,000.

5.7.2. Dependence of gain on bulk doping

Figure 5.32 shows intrinsic gains for identical devices at the same gate bias, but for different *n-type* doping levels in the polysilicon.

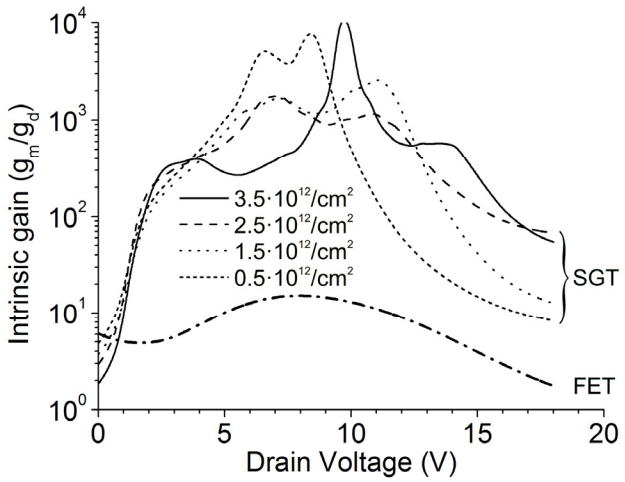


Figure 5.32. Measured intrinsic gain of the SGT at approx. 1μA drain current as a function of drain voltage for different substrate doping levels and compared to that of an FET. W=50μm, S=2μm, d=10μm; 1·10¹³/cm² n-type doping under the source barrier.

It is seen that the gain at low $\mathbf{V_D}$ above $\mathbf{V_{SAT1}}$ increases with decreasing substrate doping levels. This can be explained by a decrease in the electric field at the periphery of the source as $\mathbf{V_D}$ increases and the depletion layer expands towards the drain. For higher doping levels in the polysilicon, the increase in electric field with drain voltage will be greater, as will the increase in $\mathbf{g_d}$. At higher $\mathbf{V_D}$, however, gains are greatest for higher substrate doping. Since $\mathbf{g_m}$ is the same, this effect must be due to a reduction in carrier generation in the high field regions.

We now extend the investigation to devices with identical geometry and different bulk doping and study the gain characteristic at the same drain current (Figure 5.33). In Figure 5.33a, at low current, the devices behave as explained above, with less degradation at high drain voltage in the devices with higher doping. As the current increases (Figure 5.33b and Figure 5.33c), there is a lowering of intrinsic gain and a shift of the first peak due to the increase in $\mathbf{V_{SAT1}}$. At lower drain voltage, the characteristics at a given current are similar, regardless of bulk doping.

It is observed that the reduction of gain at high $\mathbf{V_D}$ becomes less pronounced as the current increases. This can be justified by considering the operating regions of the SGT and parasitic FET. Due to reduced $\mathbf{g_m}$, a significant increase in $\mathbf{V_G}$ is required for high drain current, and this means that $\mathbf{V_{SAT2}}$ will be large enough so that even at $\mathbf{V_D}$=20V, the SGT will be operating between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$. The gain in this region is lower, but since the parasitic FET is not pinched off, there is no additional generation of carriers (which is responsible for the increase in $\mathbf{g_d}$ and the loss of gain). The result is that the gain is lower, since we are operating around the first peak, but constant across the operating $\mathbf{V_D}$.

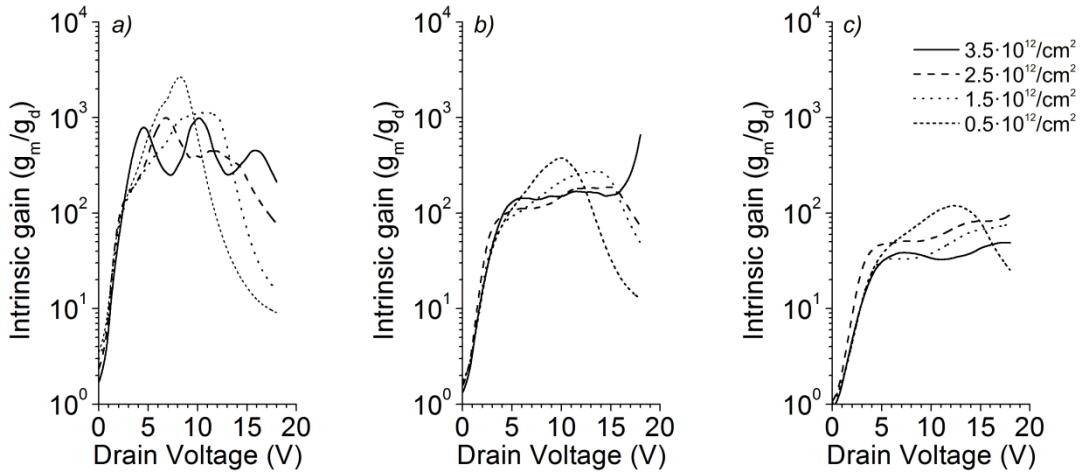


Figure 5.33. Measured intrinsic gain of the SGT as a function of drain voltage for different substrate doping levels at the same drain current: a) 3μA, b) 10μA, c) 30μA. W=50μm, S=2μm, d=10μm; 1·10¹³/cm² n-type doping under the source barrier.

The results above are reinforced by the plots in Figure 5.34 which show the evolution of gain against drain voltage and drain current, for different bulk doping. In every case, the gain becomes lower as the current gets higher. It is also shown that the gain around $\mathbf{V_{SAT2}}$ decreases with increasing concentration of the *n-type* bulk doping and that the envelope of high gain is widest for the highest *n-type* doping. Carrier generation at high $\mathbf{V_D}$ and its deleterious effects on $\mathbf{g_d}$ are strongest for the more lightly doped silicon.

Figure 5.35 shows the dependence of intrinsic gain – measured just above $\mathbf{V_{SAT1}}$ – on drain current and bulk doping. The gain falls almost linearly with increasing current at the lower currents. This decrease in gain could be due to:

a) Reduction in $\mathbf{g_m}$;

b) Generation of carriers in the high field peripheral region of the source;

c) Reduction of barrier at the periphery of the source with increasing current.

An analysis of these three phenomena based on the present understanding of device operation is as follows.

a) We expect $\mathbf{g_m}$ to be proportional to current (Equation 4.10). However, high gains are obtained close to threshold. In this regime, the barrier lowering constant, α, changes from a high value to a lower one as $\mathbf{V_G}$ and $\mathbf{I_D}$ increase. Therefore, $\mathbf{g_m}$ does not increase very much, but here is no evidence that $\mathbf{g_m}$ actually decreases and can account for the decrease in gain.

b) We expect the generation of carriers to be sensitive to electric field in the periphery. Figure 5.35 shows that the gain is not sensitive to the carrier concentration in the polysilicon, and since increased doping levels lead to higher electric fields, this suggests that carrier generation is not the mechanism responsible for the reduction in gain.

c) If we assume a model in which the peripheral barrier is related to the barrier in the body of the source and that it is also affected by the lateral field due to $\mathbf{V_D}$, it can be shown that a situation arises when $\mathbf{g_d}$ is proportional to $\mathbf{I_D}$. Moreover, the device studied here has a *n-type* barrier modification layer, which degrades the quality of the passivation at the edge of the source by increasing the lateral electric field.

Let $\mathbf{I_V}$ be the vertical component and $\mathbf{I_L}$ the lateral controlled component of the current.

From Equation 2.15:

$$I_V \approx I_{V0} \exp\left(-\frac{q}{kT}\left(\Phi_{B0} - \alpha E\left(V_G\right)\right)\right). \tag{5.9}$$

The lateral current includes a component which depends on the field as controlled by bulk doping and drain voltage and which is larger in poorly passivated devices. This field is applied to a restricted area of the source, given by the proportionality constant, A:

$$I_L \approx \frac{I_{V0}}{A} \exp\left(-\frac{q}{kT}\left(\Phi_{B0} - \alpha E\left(V_G\right) - \beta E\left(V_D, N_D\right)\right)\right). \tag{5.10}$$

Substituting $\mathbf{I_V}$ in Equation 5.10 we obtain:

$$I_L = \frac{I_V}{A} \exp\left(\frac{q}{kT} \beta E\left(V_D, N_D\right)\right), \tag{5.11}$$

thus:

$$\frac{\partial I_L}{\partial V_D} = \frac{I_V}{A} \exp\left(\frac{q}{kT} \beta E\left(V_D, N_D\right)\right) \frac{\partial}{\partial V_D} \beta E\left(V_D, N_D\right). \tag{5.12}$$

For given V_D and N_D, $g_d = \frac{\partial I_L}{\partial V_D} \propto I_V$.

The explanation of the results in Figure 5.35 is, therefore, that $\mathbf{g_m}$ does not change much at lower current, so gain falls due to the increase in $\mathbf{g_d}$. At higher currents and higher $\mathbf{V_G}$, α is constant, since $\mathbf{g_m}$ is proportional to the current, as is $\mathbf{g_d}$. For this reason the gain tends to remain constant.

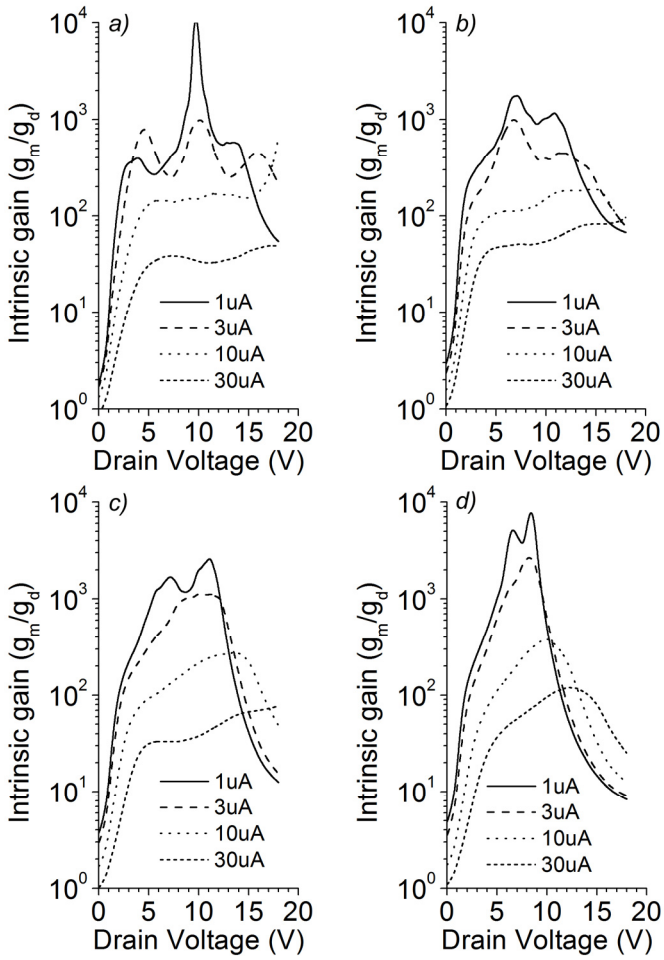


Figure 5.34. Measured intrinsic gain of the SGT as a function of drain voltage for different drain currents at the same substrate doping levels: a) $3.5\cdot10^{12}$, b) $2.5\cdot10^{12}$, c) $1.5\cdot10^{12}$, d) $0.5\cdot10^{12}$ /cm^2 n-type*; $1\cdot10^{13}$/cm^2* n-type *doping under the source barrier; W=50μm, S=2μm, d=10μm.*

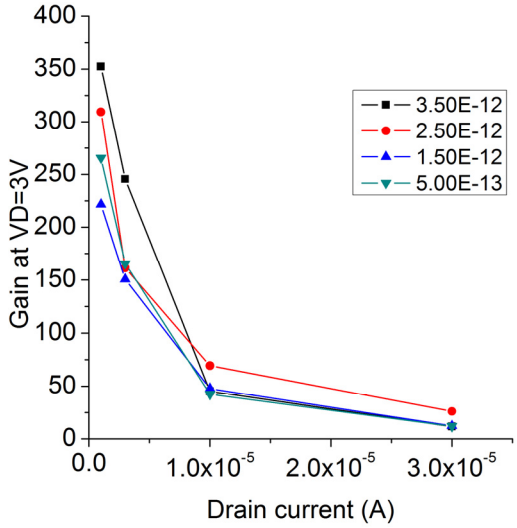


Figure 5.35. Measured intrinsic gain versus drain current for different values of **n-type** *bulk doping. $1\cdot10^{13}/cm^2$* **n-type** *doping under the source barrier; $W=50\mu m$, $S=2\mu m$, $d=10\mu m$.*

5.7.3. Dependence of gain on the barrier modification implant

In Figure 5.36, intrinsic gains are shown for two transistors with the same doping level in the polysilicon but with different barrier modification implants.

Both are operating at the same current, but $\mathbf{g_m}$ in (a) is larger than in (b), which explains its higher intrinsic gain. In this case, while the peaks and the dips are due to changes in $\mathbf{g_d}$, the downward shift of (b) relative to (a) results from a change in $\mathbf{g_m}$. For comparison, the intrinsic gain of the FET is around 10.

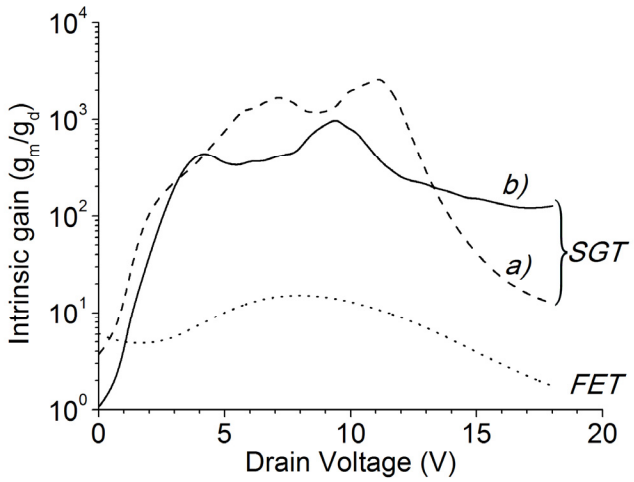


Figure 5.36. Intrinsic gain for a) $1\cdot10^{13}/cm^2$ n-type and b) $5\cdot10^{13}/cm^2$ p-type measured at $1\mu A$. $W=50\mu m$, $S=2\mu m$, $d=10\mu m$, $0.5\cdot10^{12}/cm^2$ n-type bulk doping. Also shown is the gain of an equivalent FET.

5.7.4. Dependence of gain on temperature

The influence of temperature on the drain current of the SGT can be significant if the barrier is high. From a circuit design point of view this may be detrimental to the amplification performance. For this reason, it is of interest to characterise the temperature dependence of intrinsic gain.

One device was measured at a constant gate bias but at different temperatures (Figure 5.37). The plot shows that temperature has a minimal effect on intrinsic gain. The largest discrepancy between the curves is observed at low $\mathbf{V_D}$, where $\mathbf{V_{SAT1}}$ changes with temperature, as the current increases. This is due to the altered characteristic of the parasitic FET which operates in the linear region. The gain is then similar between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$, and above $\mathbf{V_{SAT2}}$. Any differences in this high gain region may be down to noise in the measurement setup ($\mathbf{g_d}$ is very low and very prone to noise).

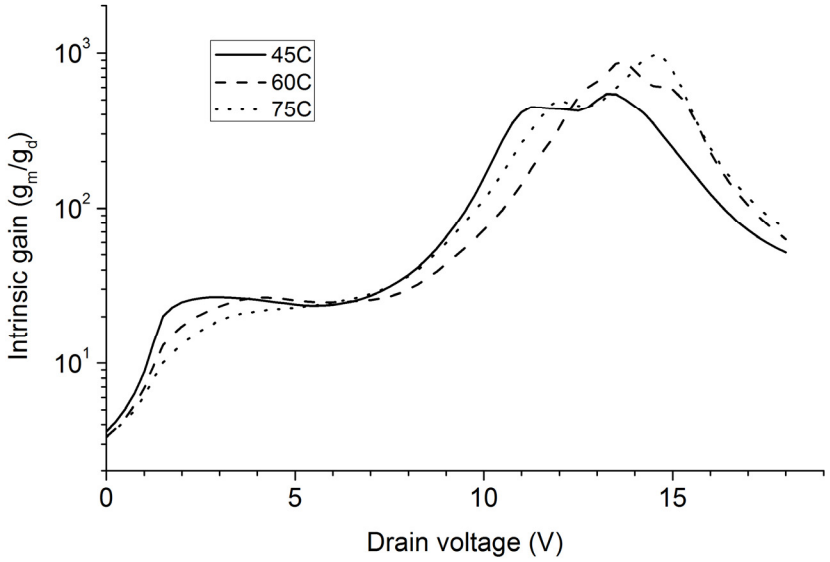


Figure 5.37. Intrinsic gain of the SGT at a set gate bias as a function of drain voltage for different temperatures. W=50μm, S=2μm, d=10μm; 0.5·10^13/cm^2 n-type doping under the source barrier and 2.5·10^12/cm^2 n-type bulk doping.

This behaviour can be explained by the evolution of $\mathbf{g_m}$ and $\mathbf{g_d}$ with temperature at a constant gate bias. As the temperature increases, the current increases and so does $\mathbf{g_m}$, so the gain has a tendency to increase but this trend is opposed by the increased output conductance, which itself is proportional to the drain current.

Even though the current changes by one order of magnitude over 50°C, the gain is unchanged above $\mathbf{V_{SAT1}}$, which makes it easy to design gain stages with the SGT. Admittedly, the current consumption may increase when the temperature rises, but the gain remains constant.

5.8. Frequency behaviour

So far, the analysis of the polysilicon SGT has been confined to *d.c.* operation. In practice, the majority of circuit functions involve either oscillation or some kind of transient and even purely *d.c.* applications have transient regimes during power-up before they reach their steady state. With this in mind, it is useful to characterise the frequency behaviour of the SGT and describe the parameters which influence performance.

Assuming that the current is controlled exclusively by the source barrier, the cut-off frequency of the SGT is given by: (see derivation in Chapter 4)

$$f_T \approx \frac{q}{kT}\frac{\alpha J_S}{2\pi\varepsilon_s\varepsilon_0}. \tag{5.13}$$

From the above we can derive the response time to an abrupt step signal:

$$\tau = \frac{1}{2\pi f_T} \approx \frac{kT}{q}\frac{\varepsilon_s\varepsilon_0}{\alpha J_S}. \tag{5.14}$$

The factors that influence the cut-off frequency and the step response time are:

- Operating temperature
- Average current density through the source, which is itself dependent on temperature
- Semiconductor permittivity
- Barrier lowering constant

At a given temperature, the cut-off frequency has a linear dependence on $\mathbf{J_S}$ and is inversely proportional to the permittivity of the semiconductor, as illustrated in Figure 5.38.

In the case of the polysilicon devices, ε_S is fixed to 11.9, which leaves $\mathbf{J_S}$ and α as the two parameters that can impact the frequency characteristic. Computed $\mathbf{f_T}$ values based on measured $\mathbf{J_S}$ and α are shown in Figure 5.39.

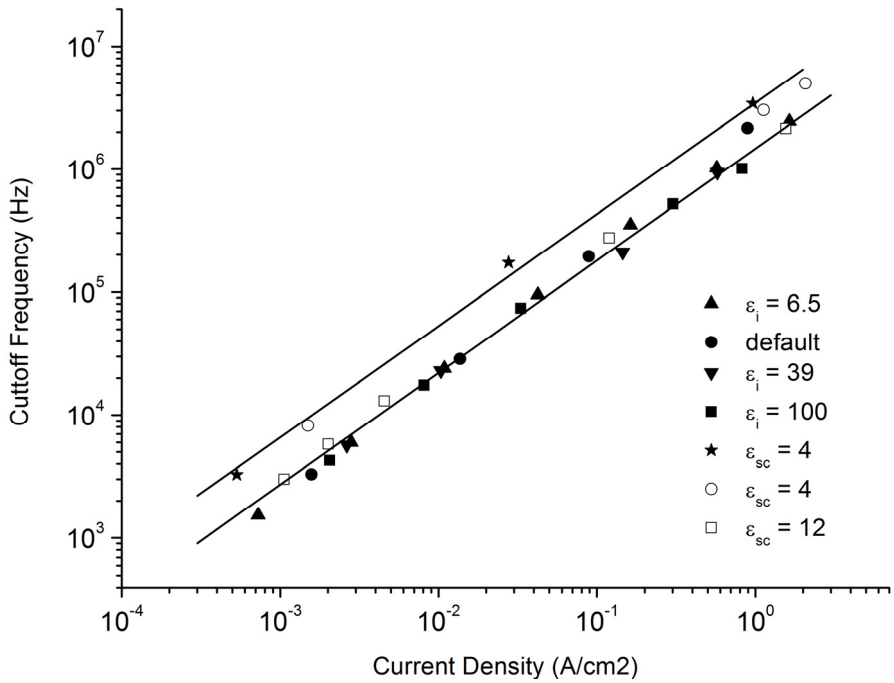


Figure 5.38. Cut-off frequency simulation results for different layer thicknesses and permittivities. The closed symbols are for t_i = 300nm and t_S = 100nm while the open symbols are for t_i =60 nm and t_S = 20nm. Simulation performed for [108].

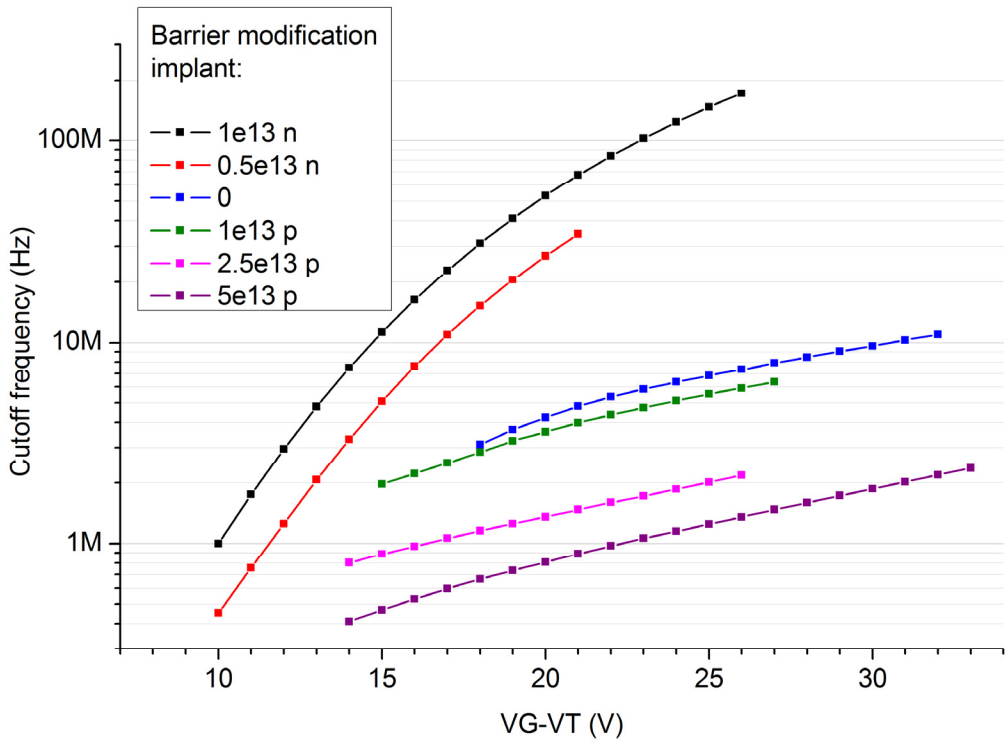


Figure 5.39. Cut-off frequency versus gate bias for different barrier modification implants; S=2μm.

As expected, $\mathbf{f_T}$ increases as the current density grows due to source barrier height lowering (brought about either by increased gate field or by changes to the barrier profile after implantation of impurities.

Figure 5.40 corroborates these statements; the cut-off frequency is lower for higher barriers (*p-type* implant) and increases as the barrier accommodates more charge carriers. However, the same plot shows that increasing the source length has a negative impact on the frequency. With larger S comes an increase in source area and in gate-to-source capacitance. Since the current does not increase proportionally, the cut-off frequency becomes lower. (See also Equation 4.11.)

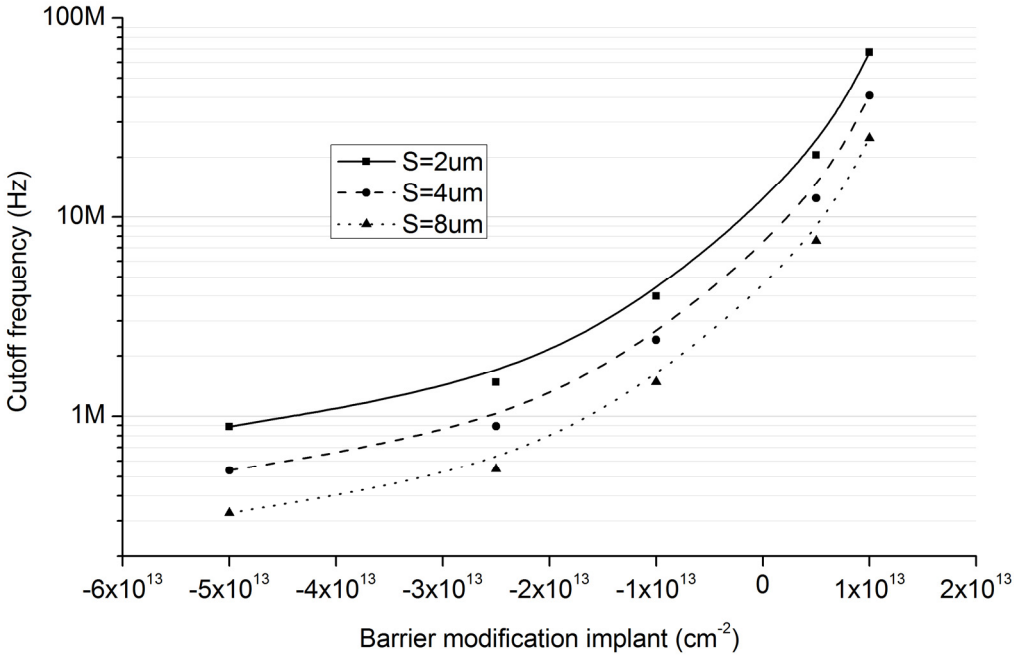


Figure 5.40. Cut-off frequency versus barrier modification implant for different source lengths. V_G - V_T = 21 V.

When both drains of the device are connected, the current effectively doubles due to the fact that the overwhelming majority of the current to each drain originates from a different part of the source (current crowding at the edge of the source closest to the respective drain). As the current doubles, so does the average current density through the source, which leads to a twofold increase in cut-off frequency.

In conclusion, the cut-off frequency of the SGTs is proportional to $\mathbf{J_S}$ and α. $\mathbf{J_S}$ is the average current density though the source and depends on gate bias. The current density can be improved by decreasing the source length and by using a double drain topology. The barrier lowering constant (α) is controlled by doping the semiconductor under the source contact.

For the self-aligned devices with the highest *n-type* barrier modifying implant, the calculated $\mathbf{f_T}$ is well in excess 100MHz with both drains connected (double the results in Figure 5.39).

5.9. SGTs with other barrier types – the Bulk Unipolar SGT (BUSGT)

5.9.1. Introduction

To date, Schottky barrier source-gated thin-film transistors (SBSGTs) [104] have only been fabricated in amorphous silicon and polysilicon. The on-current is determined by the source which comprises a Schottky barrier whose effective height is controlled using a gate located opposite the source (SBSGT) (Figure 5.41a). The SGT has been shown to have several important advantages compared with a standard thin-film FET. In particular, in the on state it has a higher output impedance, a lower saturation voltage, is less sensitive to short channel effects and is more stable [106]. Furthermore, the SGT can be a lot faster than the conventional FET since source-drain separations can be smaller and electric fields larger [103, 106].

A parameter which is important in many circuits is the temperature coefficient of the on-current. Although the temperature coefficient of a SBSGT in some cases can approach that of a FET, in most instances it is worse because the source current is thermally activated. Another parameter, the dynamic range of the on-current is also much less in a SBSGT compared with an FET, owing to the fact that the barrier restricts the current flowing from the source to the drain of the device and the barrier is difficult to pull down. In addition, if we have a barrier that can easily be pulled down, then it might be possible to increase the on-to-off current ratio and also use the source barrier to control the off-current, thereby reducing short channel effects even further.

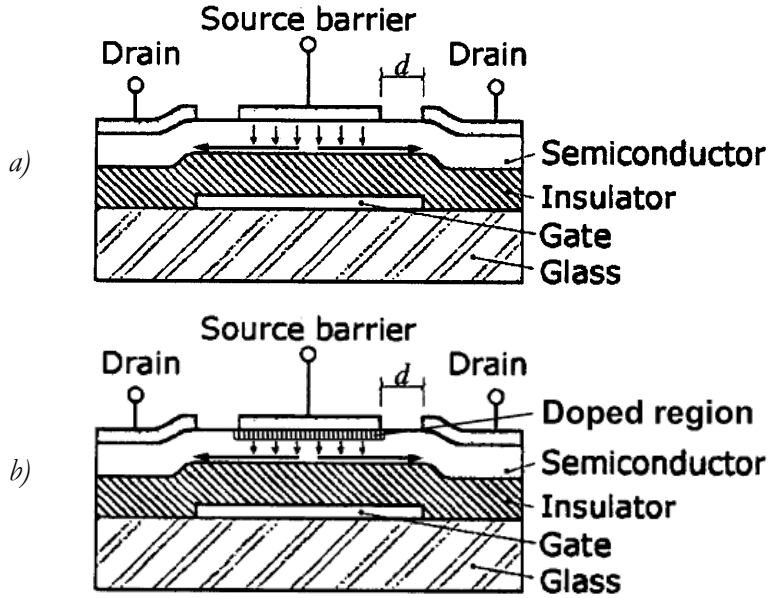


Figure 5.41. Schematic showing cross-section of (a) SBSGT and (b) BUSGT.

In SBSGTs, the on-state is controlled by the Schottky barrier at the source, while the off-state is mostly controlled by the parasitic FET in series with the source barrier. The

increase in off-current for small source-drain separations is fundamental to the SBSGT because the source barrier is difficult to pull down by the gate, and so has to be low if high on-currents are to be obtained, and the off-current is controlled by the parasitic FET.

A possible route to reducing off-currents, increasing dynamic range and reducing temperature coefficients is to engineer a unipolar barrier at the source that is high in the off state and low in the on-state. Therefore, a weaker barrier, which is easy to pull down using the gate, is needed.

One such barrier is the bulk unipolar barrier formed by doping. [52] (See section 2.3.2.) Ideally the source contact is ohmic, but a barrier is created by doping the semiconductor with acceptors for an electron source or with donors for a hole source. This type of barrier replaces the Schottky-type contact used in standard SGTs and, in common with unipolar barriers, the doped region is fully depleted in thermal equilibrium. The resulting device has been called the Bulk Unipolar Source-Gated Transistor (BUSGT) (Figure 5.41b). Other barrier types with possible uses within a SGT structure have been identified in [106].

5.9.2. Design and Operation of the BUSGT

In a BUSGT, a source barrier is created using a bulk doping just as in a bulk unipolar diode. [52] (See section 2.3.2.) The doping concentration and thickness of the doped layer is such that in thermal equilibrium the Fermi level does not approach either band edge so there are not a large number of free carriers and the layer is fully depleted by the natural band bending caused by the doping. The band diagram through a section of the device between the source and the gate (Figure 5.41) is shown in Figure 5.42. Figure 5.42a shows the band diagram of the SGT with a source barrier created by the source Schottky contact, while Figure 5.42b has a highly doped *p-type* layer of thickness $\mathbf{t_d}$ below the ohmic source contact. This forms a barrier of height Φ_B' to electrons relative to the source contact. The gate voltage $\mathbf{V}_G$ pulls down the barrier when a positive drain voltage is applied to deplete any free electrons at the semiconductor-insulator interface and the system effectively acts as two insulating layers in series [104]. Under these conditions, the change of voltage at which the semiconductor pinches off at the source ($\mathbf{V_{SAT1}}$) with gate voltage is simply given by Equation 4.3. [105]

The advantage of the bulk unipolar barrier compared with the Schottky barrier in the context of the SGT is that it can be pulled down more easily by the gate.

This leads to higher on-currents, larger transconductance and higher dynamic range. Furthermore, all the SGT configurations considered so far have an on-current determined by the source barrier and an off-current determined by the parasitic FET of

length **d** (Figure 5.41) in series with the source barrier. With a unipolar, source barrier one has the option to design the SGT so that both the off and on currents are determined by the source barrier or an SGT where the off-current is determined by the source barrier and the on-current by the parasitic FET, as described in Table 5.2.

TABLE 5.2. CONTROL OF THE ON- AND OFF-STATES BY THE SOURCE BARRIER

	Off-state controlled by	**On-state controlled by**
SBSGT	Parasitic FET	Source Barrier
BUSGT	Source Barrier	Source Barrier

The electrostatic configuration of the SGT is complicated by the two dimensional nature of the depletion layers as shown schematically in Figure 5.43. Under a large drain voltage, pinch-off occurs at the end of the source opposite the drain (point A). Here the electric field and the current density under the source barrier are highest since the barrier height is lowest.

The parasitic FET of length **d** has a virtual source at point B which floats at a potential that is positive with respect to the source contact (for an electron barrier) but negative with respect to the drain. This complicated situation means that the division of the drain voltage between the source depletion layer and the parasitic FET can be very dependent on device design. Most will be dropped across the source barrier when the source controls the current and most will be dropped across the parasitic FET when this controls the current. A sort of hybrid situation can occur when both the source barrier and the FET have a significant role in determining the current.

5.9.3. Simulation of the BUSGT

Computer simulations of the BUSGT were made using the Silvaco Atlas programme. This 2D package has been shown to give very good agreement between measured and simulated characteristics for SBSGT devices made in amorphous silicon [121]. Figure 5.44 shows the output and transfer characteristics of a BUSGT made in a thin film of silicon. The parameter values used for the simulation are given in Table 5.3.

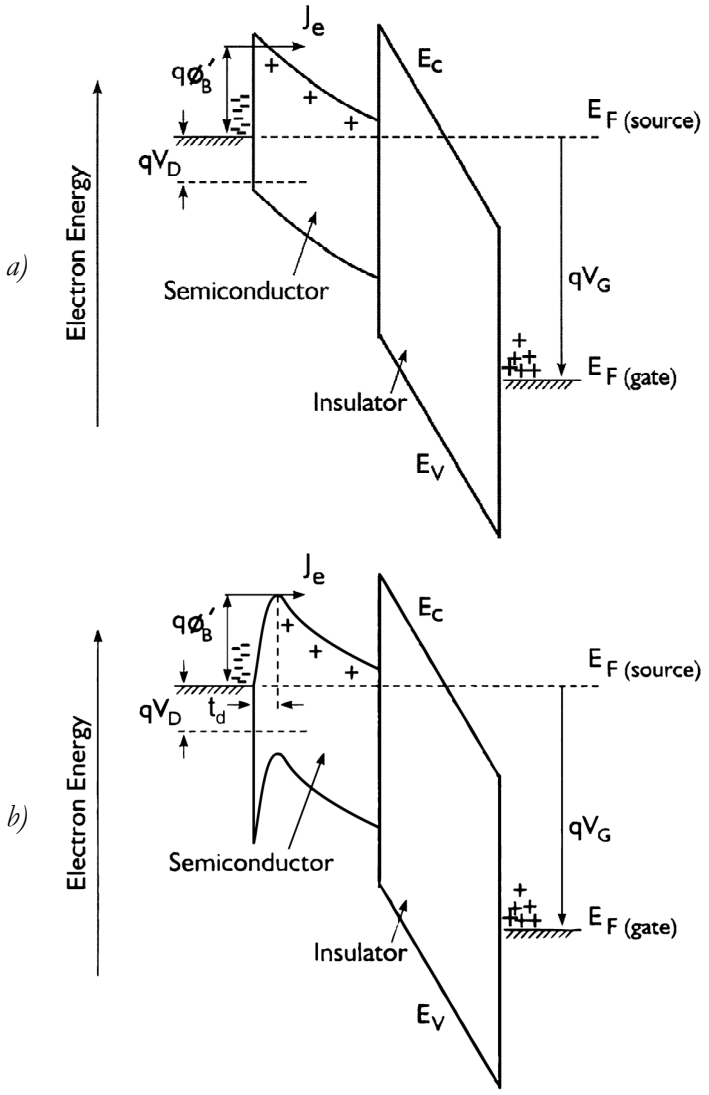


Figure 5.42. Band diagrams for (a) SBSGT and (b) BUSGT.

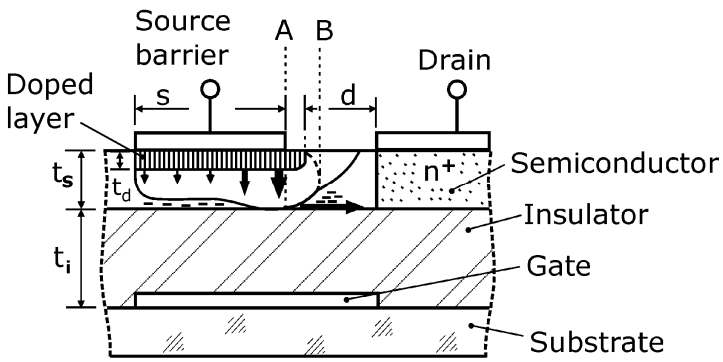


Figure 5.43. Lateral section of a BUSGT showing the 2D nature of the device and parasitic FET in series with the gated source.

TABLE 5.3. SIMULATION PARAMETERS AND THEIR DEFAULT VALUES

Parameter	Symbol	Default Value
Source length	S	1μm
Source-drain gap	d	250nm
Device width	W	1μm
Thickness of the doped layer	t_d	10nm
Thickness of the insulator	t_i	20nm
Thickness of the semiconductor	t_s	10nm
Source barrier p-type implant	p	0.5, 0.9 and $1.3 \cdot 10^{19}$ cm^{-3}
Material:	*Crystalline silicon*	

The unipolar source barrier to electrons is formed using a 10nm-thick uniformly doped p-type layer under the source contact. The doped layer extends sideways towards the drain (Figure 5.43) so as to provide field relief at the edge of the source contact. In practice, there is a Schottky barrier at the metal-semiconductor contact, as it is difficult to find a metal with such a work function as to have an ohmic contact to silicon. This Schottky barrier is made transparent to electrons by n^+ doping near the surface to the effect that the only barrier that the electrons see is the bulk unipolar one. In this simulation, a fictitious metal was chosen which allows an ohmic contact to be formed. The end result is similar: only the bulk barrier, which in this case is located near the surface of the semiconductor, is impeding the flow of carriers at the source.

As the doping level increases, there is a decrease in the on-current and a reduction in the saturation voltage. This is consistent with an increase in the height of the source barrier, and as the doping concentration is increased, the source barrier takes control over the on-current. The downside of having a *p-type* implant under the source contact is that there is a resistive effect in the output characteristic; this effect gets stronger with doping, as show in Figure 5.44. The slope of the transfer characteristic below ≈1V is consistent with that expected from the sub-threshold of the FET for the two lowest doping concentrations, but for the highest dose (1.3×10^{19} cm^{-3}), where the device behaves like an SGT (Figure 5.44c), the slope is much lower, suggesting that the sub-threshold and off-current are influenced by the unipolar barrier.

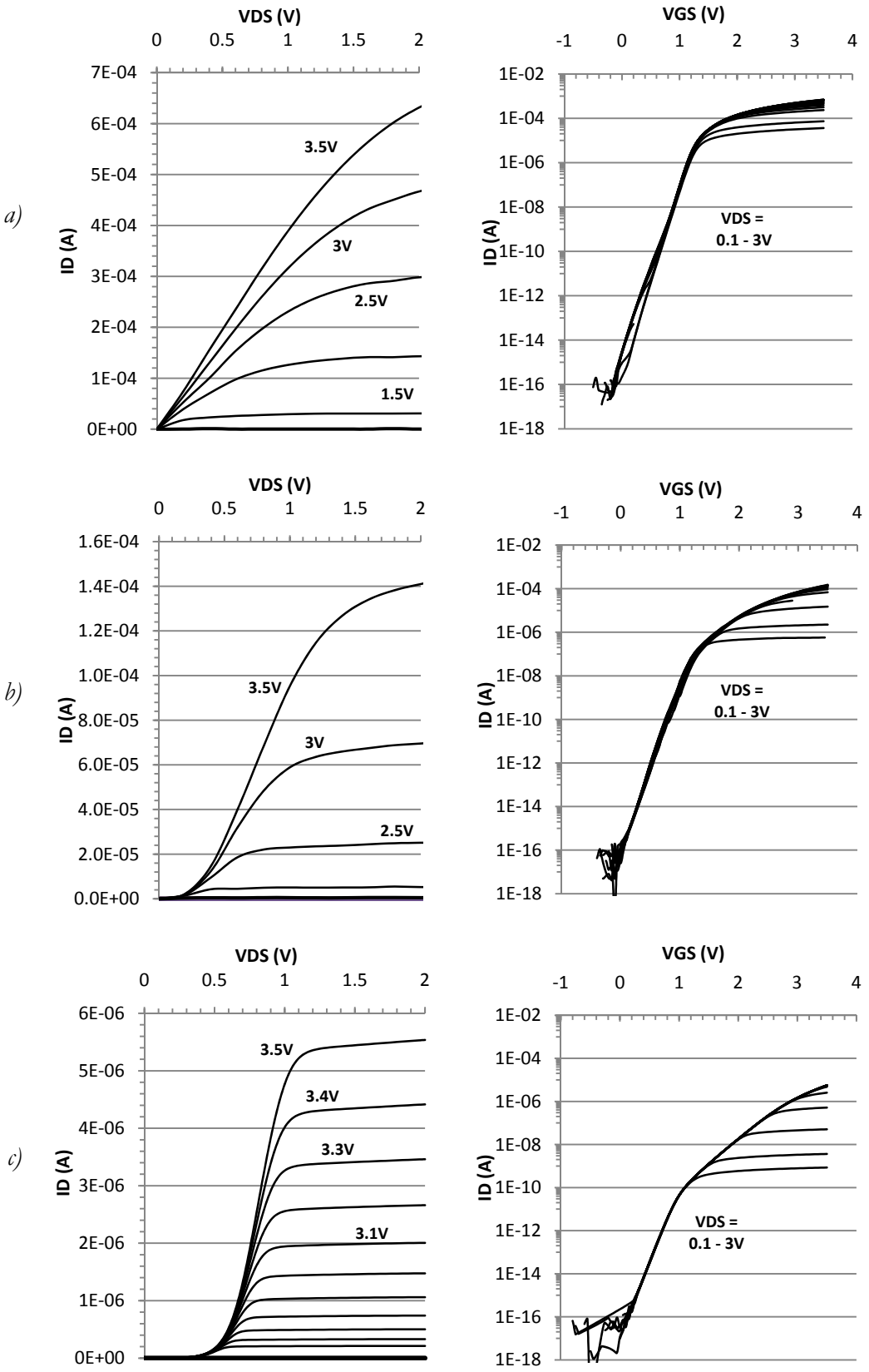


Figure 5.44. BUSGT characteristics: (a) $p = 5x10^{18}$ cm^{-3}; (b) $p = 9x10^{18}$ cm^{-3}; (c) $p = 1.3x10^{19}cm^{-3}$ ($t_s = 20nm$, $t_i = 5nm$, $t_d = 10nm$).

The on-characteristic shows a strong increase in current as the unipolar barrier is pulled down. Activation energy calculations for the current transport show that the barrier is pulled down by almost 0.5eV for a change of gate voltage of 2.5V. This potentially leads to much higher on/off ratios than would be possible if a Schottky source would be used.

At $\mathbf{V_G}$=3.5V the barrier can be very low (≈0.1eV) leading to a low temperature coefficient for the on-current, similar to an FET. This most likely happens because as the gate voltage increases the current is becoming limited by the parasitic FET, since its current increases quadratically with gate voltage, while the current over the barrier increases exponentially. One therefore has the possibility of a BUSGT where the off-state is controlled by the source barrier while the on-state is determined by the parasitic FET. This situation is completely opposite to that in a SBSGT.

If a device is working as an SGT and if $\mathbf{C_i} \ll \mathbf{C_S}$, the saturation voltage $\mathbf{V_{SAT1}}$ will be very much smaller than $\mathbf{V_{SAT2}} = \mathbf{V_G} - \mathbf{V_T}$, which is the drain voltage at which the current of a standard FET. Simulation results show the electron concentration in the semiconductor, as illustrated in Figure 5.45 for the three possible operating regimes.

The figure shows the semiconductor region underneath the source and between the source and the drain. As $\mathbf{V_D}$ is increased and approaches $\mathbf{V_{SAT1}}$, the area at the edge of the source implant starts to deplete. This depletion region extends downward and toward the drain and the semiconductor pinches off at $\mathbf{V_D}=\mathbf{V_{SAT1}}$. A further increase in $\mathbf{V_D}$ extends the source depletion region at the source to the right and extracts carriers from the parasitic FET channel. At $\mathbf{V_D}=\mathbf{V_{SAT2}}$, the semiconductor is pinched off at both the source and the drain. Higher $\mathbf{V_D}$ leads to FET channel shortening while the excess voltage is dropped across the short depletion region around the drain.

Figure 5.46 shows the characteristics for a structure with a much thicker gate oxide and therefore lower $\mathbf{C_i}$. It can be seen that $\mathbf{V_{SAT1}}$ is less than 0.7V for $\mathbf{V_G}$=15V. The change of $\mathbf{V_{SAT1}}$ with gate voltage is ≈0.12 and close to the calculated value of 0.14 ($\mathbf{C_i}/(\mathbf{C_i}+\mathbf{C_S})$).

The envelope formed by the drain current at low drain voltage and at different gate voltages is the reverse biased characteristic of the source barrier. Once again, very little drain voltage dependence of the current over the whole current range can be seen (Figure 5.46b).

A further test to verify that this device is working as an SGT is to examine the source length dependence of the current. If the device would be operating as a JFET [55], then the current would decrease with **S**, whereas for an SGT the current would increase with **S**. Figure 5.47 shows that the device does indeed behave like an SGT.

$V_D < V_{SAT1}$

$V_{SAT1} < V_D < V_{SAT}$

$V_{SAT2} < V_D$

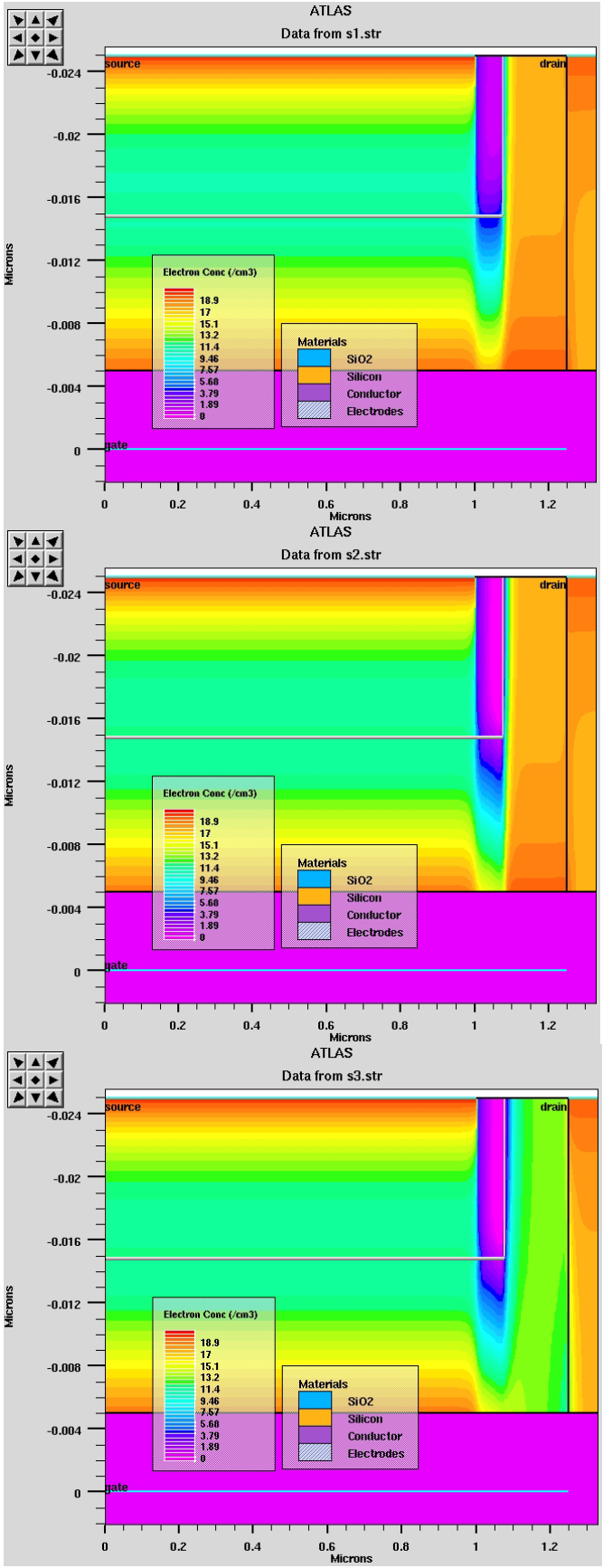


Figure 5.45. Electron concentration in the semiconductor for a BUSGT with: t_S = 20nm; t_i = 5nm; t_d = 10nm; p = 1.3x10^{19}cm^{-3}; d = 0.25μm. p = 1.3x10^{19}cm^{-3}. The outline of the source barrier doping area is also shown.

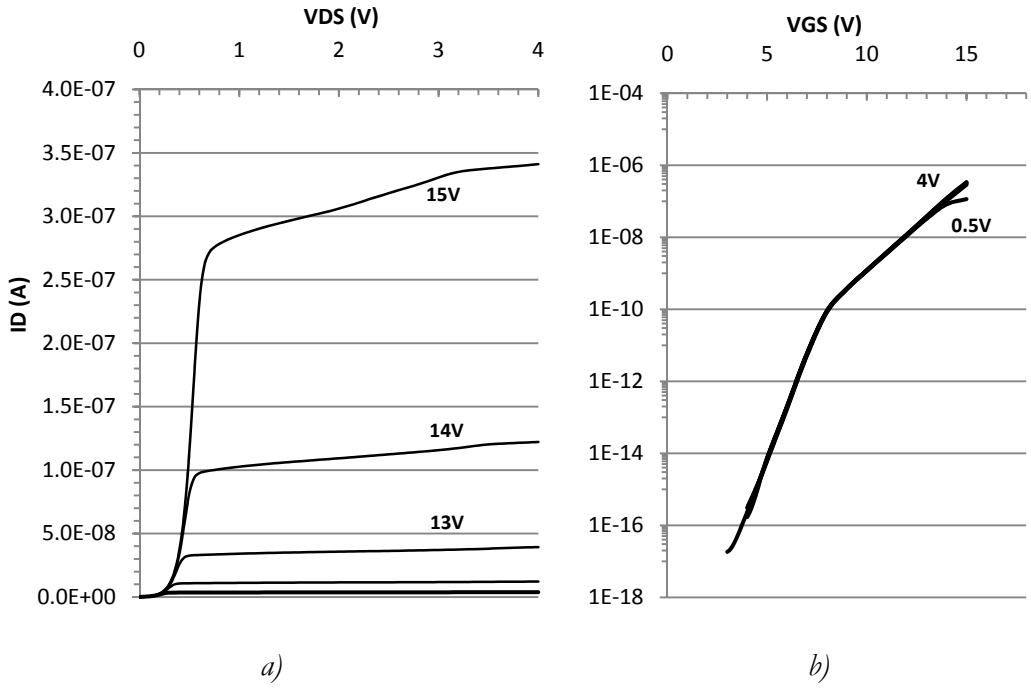


Figure 5.46. Output and transfer characteristics of a BUSGT with: t_S = 20nm; t_i = 40nm; t_d = 10nm; p = 1.3x10^{19}cm^{-3}; d = 0.25μm.

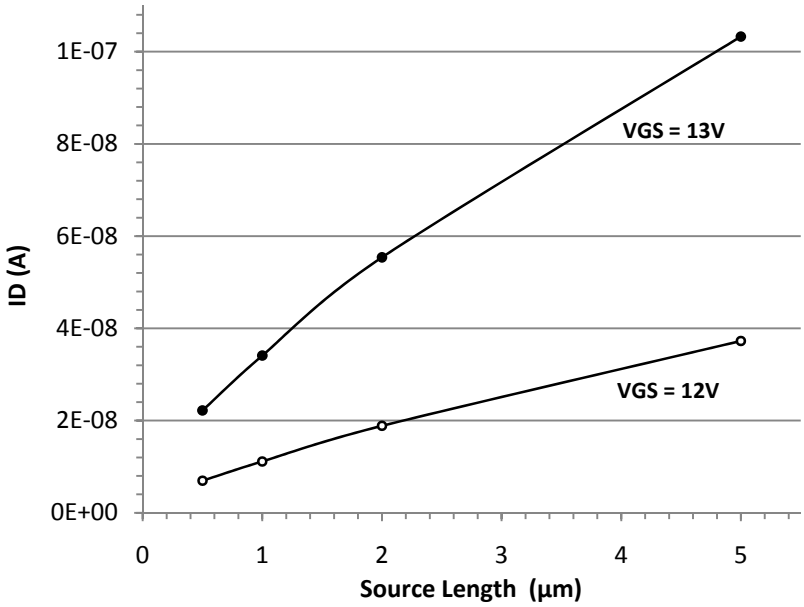


Figure 5.47. Variation of drain current with source length for a BUSGT; parameters as in Figure 6.6; V_{DS} = 1V.

Simulation results of the transfer characteristic of a polysilicon BUSGT and activation energy for current transport are illustrated in Figure 5.48 for two different doping concentrations in the *p-type* layer.

The transfer characteristic for the lowest barrier shows a strong drain voltage dependence of the current, while the higher barrier is relatively insensitive to drain field except at the lowest gate voltage. The reason for this can be seen in the activation energy plots. Since polysilicon has much lower field effect mobility than crystalline silicon, the off-current is expected to be determined by the parasitic FET.

Figure 5.48 shows that the activation energy at the lowest voltage is strongly dependent on drain field. This is interpreted as being due to short channel effects, where the barrier between the source and drain is pulled down by the drain field.

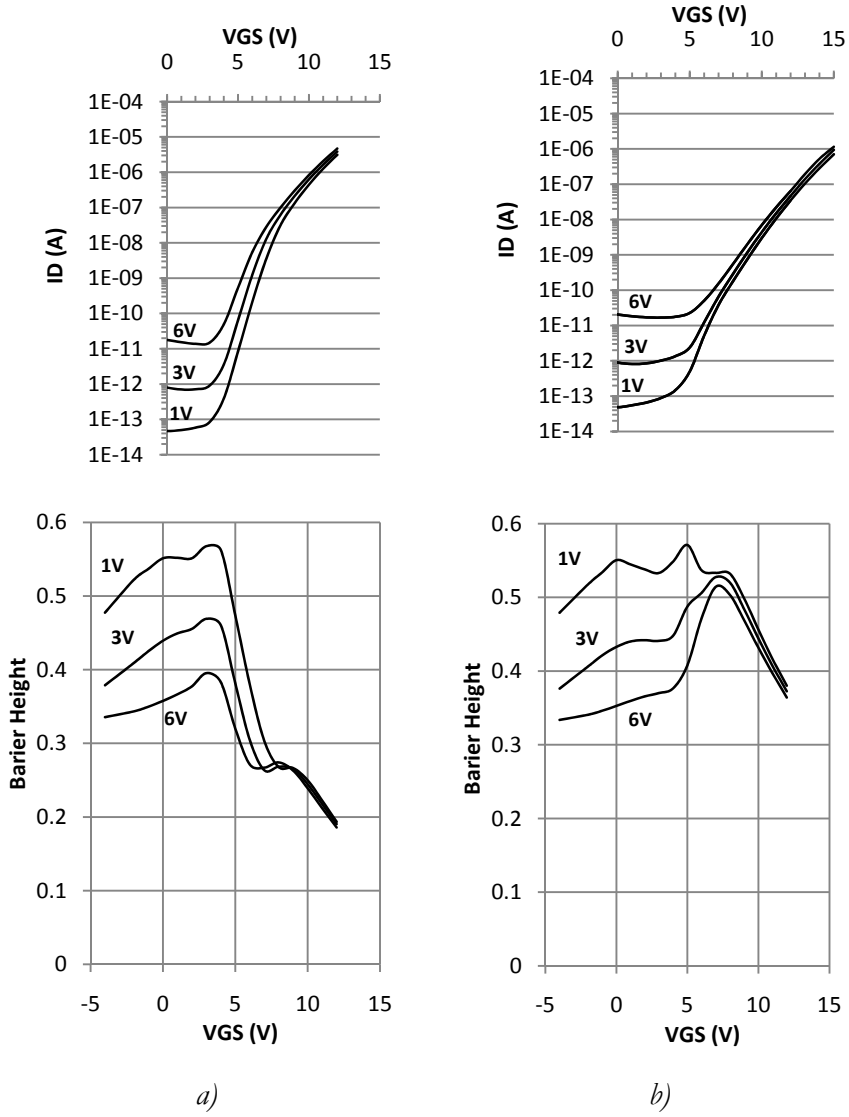


Figure 5.48. Transfer characteristic and activation energy for a polysilicon BUSGT. The device geometry is as in Figure 6.6; (a) $p = 9x10^{18}$ cm^{-3}; (b) $p = 1.3x10^{19}$ cm^{-3}.

As the gate voltage is increased, the barrier is pulled down but is still strongly drain field dependent until, at $\mathbf{V_G}$≈9V, the current becomes limited by the source barrier and the activation energy becomes independent of drain field. With a higher source barrier,

however, the source begins to influence the current and the activation energy as low as $\mathbf{V_G}$≈3V and the field dependence of the current is reduced. Above $\mathbf{V_G}$≈7V the current is determined by the source barrier and its gate field dependence.

5.10. Review of the properties of the SGT in various semiconductors and with different barrier types and comparison with the FET

In designing SGT devices, the choice of type of barrier is of a prime importance, as it is the factor that most influences the device behaviour [117].

In Figure 5.49 we represent schematically the transfer characteristic of a SGT (in black). This curve is limited either by the source barrier, the parasitic FET channel, or a combination of both. For a given height of the source barrier in the absence of modulation by the gate field, the current crossing the source barrier is represented by the red dotted line. If we include the effect of the gate field, which is essential in SGT operation, we obtain an exponential dependence of the current on the gate voltage (red line), in proportion to the barrier lowering constant, α. Also depicted, in blue, is the transfer characteristic of the parasitic FET.

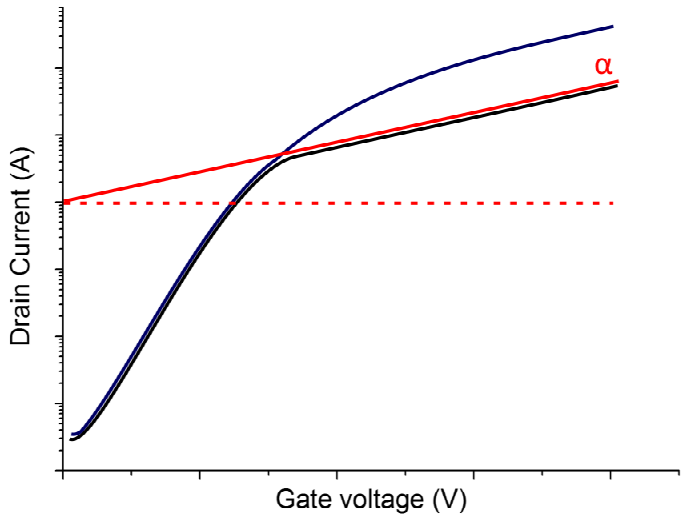
Referring to Figure 5.49, three situations can arise, as discussed below. The fourth, trivial situation would be a barrier so low that it would influence neither the off-state nor the on-state; a device comprising such a source barrier would in fact behave like a FET with an ohmic (or low barrier Schottky contact) source, and is of no relevance to the present analysis.

Barrier of average height, difficult to pull down

A moderately high source barrier would let through more current at zero reverse bias than the off-current of the parasitic FET. In this case the off-state is controlled by the FET leakage and the on-state by the source barrier. This is the behaviour of the standard SGT concept, and a Schottky barrier is well suited to building such a device (Schottky barrier SGT - SBSGT). The gate field pulls down the barrier enough to produce a modulation of the on-current above the knee of the transfer curve of at least one order of magnitude. In silicon technology creating Schottky contacts of a known barrier height is a relatively mature process. The effective height of the barrier at zero bias can be changed by ion implantation, interfacial layers or creation of a silicide. In organic semiconductors the surface can be functionalised, a process which changes the work function and enables barrier height control [117]. When designing SGTs in low mobility materials with the intention that the on-current be controlled by the source barrier, it is essential to ensure that the parasitic FET is turned on as much as possible. This can be achieved by extending the gate to overlap the FET channel so that gate bias turns on the FET while pulling down the barrier [117].

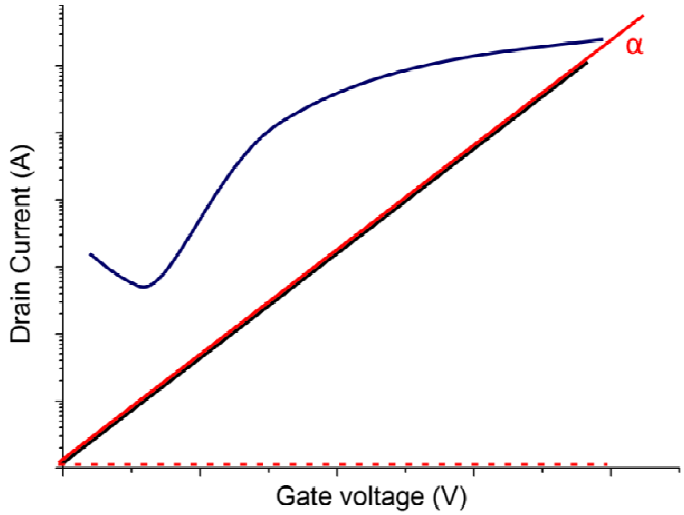
On-current
controlled by:
Source barrier

Off-current
controlled by:
Parasitic FET



On-current
controlled by:
Source barrier

Off-current
controlled by:
Source barrier



On-current
controlled by:
Parasitic FET

Off-current
controlled by:
Source barrier

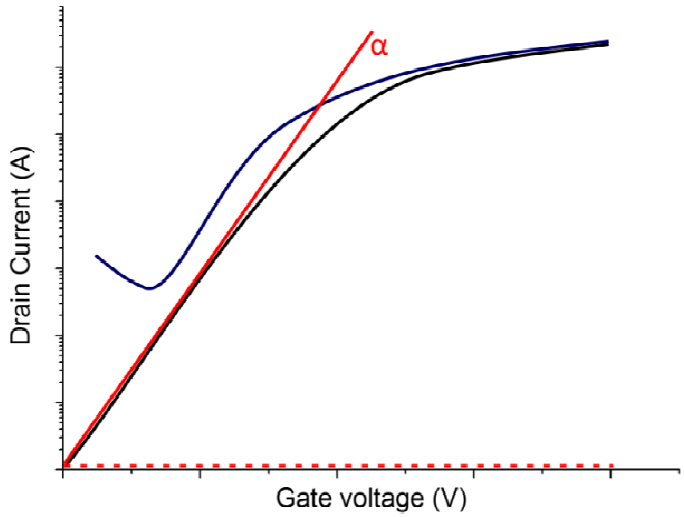


Figure 5.49. By appropriately engineering the height and pull-down characteristics of the source barrier, three types of SGT device behaviours can be, in theory, obtained.

High barrier which is moderately difficult to pull down

The barrier design could also be such that the barrier is very high but is very easily pulled down by the gate field, leading to improved transconductance in the on-state. In this case, the current is controlled by the barrier in both the on- and off-states. The bulk unipolar SGT (BUSGT) structure can be engineered for this type of operation. A unipolar barrier is created by ion implantation underneath the metal-semiconductor contact at the source, while the source contact itself is ohmic or a very low Schottky barrier. It is also speculated that the noise of BUSGT devices would be less than that of equivalent SBSGTs due to the fact that the barrier is formed inside the semiconductor, away from the metal-semiconductor interface. Unipolar barriers also have the advantage of being more versatile than Schottky contacts; barriers of either polarity and of any height can be made by implanting suitable ions and without the need of finding materials with specific work functions [117].

High barrier which is easy to pull down

If a high unipolar barrier becomes low enough when the gate field is applied, the third mode of operation can occur, in which the source barrier limits the off-current and controls the off-state and the parasitic FET governs the on-state. Devices of this nature would have very high on/off ratios, low leakage and a comparatively low temperature coefficient of the current in the on-state. It might not, however, have the defining characteristics of the SGT, namely high output impedance in saturation and low saturation voltage, due to the fact that the source barrier would have become virtually transparent to charge carriers in the on-state.

Another concept of SGT, as yet unrealised is a device with a field emission source (FESGT), which would have a barrier that becomes completely transparent to the charge crossing it under reverse bias. Current transport would happen at the Fermi level of the metal, a process which is not temperature activated. This in turn would enable the fabrication of devices with very low temperature coefficients of the on-current. Such field emission sources could be created by heavy doping under a Schottky contact or by the presence of an interfacial layer between the metal and the semiconductor. [117]

Compared to an FET, the SGT exhibits:

- Far less dependence of the current on source-drain separation. This implies:
    - better tolerance to fabrication errors,
    - smaller devices,

    - higher frequency operation for the same output impedance (or intrinsic gain),
    - better integration and
    - less susceptibility to short channel effects.
- Higher output impedance in saturation for the same output current, leading to:
    - higher intrinsic gain and
    - improved performance in analog circuits.
- Lower saturation voltage, which enables:
    - lower supply voltage operation or
    - higher output voltage swing.
- Lower number of excess carriers, which implies less defect generation in disordered semiconductors, and as an effect:
    - better device stability.
- Higher values of the minimum electric field in the area around the source, enabling:
    - higher carrier velocity, particularly in organic semiconductors where carrier mobility is dependent on the electric field and
    - faster device operation.
- Depending on the type of barrier, potentially higher temperature coefficient of the drain current, which implies either:
    - the need for more complex compensation schemes in most circuits, or
    - the ability to make very sensitive on-panel temperature sensors.

From the above it is seen that the SGT concept is extremely versatile and can be targeted to improving particular performance metrics by making the right design choices.

5.11. Conclusions

Source-gated transistors (SGTs) have been fabricated on glass using polysilicon technology. The devices have Schottky barriers at the source and barrier modification implants. A variety of geometries and bulk doping concentrations have been used in order to assess the behaviour of these *n-type* SGTs.

The devices show the basic characteristics of SGTs: low saturation voltage and high output impedance in saturation and an absence of the kink effect. The gate action is manifested by source barrier lowering, with a value of α which was measured to be in the range of 2 – 3nm, as predicted by theory and results from Schottky diodes on silicon. The effective barrier height decreases with applied gate bias and thus the current over the barrier, and through the whole device, becomes larger.

The on-current current is independent of parasitic FET channel length, **d**, as has been proven by double-drain measurements on the same structure or single-drain measurements on devices with different drawn **d**.

The saturated current also has a weak dependence on **S**, which shows that current density is not proportional to source length. Current crowding can be observed at the edge of the source closest to the drain. The two drains do not share the current if the source is longer than a saturation value of about 0.5 – 1μm, so when both drains are connected at the same time, the current density through the source effectively doubles. These observations can be exploited in order to maximise the cut-off frequency: with a short source and both drains connected, high current devices should operate at more than 200MHz.

The threshold of these SGTs can be set using bulk doping, just as in standard FET devices. The SGTs turn off completely regardless of the bulk implant, whereas off-current of the equivalent FETs increases with *n-type* bulk doping.

The on-current can be controlled at design time by modifying the source barrier with *n-type* (barrier lowering) or *p-type* (barrier raising) implants. For a large *n-type* implant, the barrier becomes low enough, particularly when the applied gate potential is high, to become less restrictive to current flow than the parasitic FET. A hybrid mode of operation is identified, when both the source barrier and the FET channel simultaneously control the current.

Since the current across the barrier is temperature activated, the drain current of the SGT can have a large temperature dependence. This temperature coefficient is less for smaller barrier heights. The activation energy of the current shows that the *n-type* doped, high current devices have very low temperature coefficients due to the low barrier. *p-type* doped devices, on the other hand, show small variations of the effective barrier height

with gate voltage and comparatively high activation energy. These SGTs have lower drain currents with strong temperature dependence, which may be detrimental to some applications, but makes them ideal components of integrated high-sensitivity temperature sensors. However, SGTs with low temperature coefficients of the drain current can be made if source barrier heights are low.

The fabricated SGTs have an ohmic contact at the drain and a reverse-biased Schottky source barrier. If the current through the device is reversed by swapping these two terminals, the resulting structure is a FET with an ohmic source and a forward-biased Schottky contact at the drain. This useful property allows us to measure the same device in two modes of operation, SGT and FET, and directly compare the results, which we have done throughout this chapter.

In contrast to the FET, the SGT has much lower saturation voltage, far higher output impedance to higher drain voltages (facilitated by the absence of the kink effect), lower leakage current, but also lower transconductance. The SGT drain current is usually controlled by the source barrier, which means that the current output is less than that of an equivalent FET.

In terms of SGT intrinsic gain, the lower transconductance is more than balanced by the very high output impedance, to give several orders of magnitude more gain than the similar FET. The intrinsic gain has a double peak characteristic. Around the drain voltage where the source region pinches off ($\mathbf{V_{SAT1}}$), the gain is governed by transconductance. Above the saturation point of the parasitic FET ($\mathbf{V_{SAT2}}$), the gain can be very high due to the high output impedance. At high drain voltage, the drain deteriorates slightly as a result of carrier generation in the high field regions. The gain is highest around the gate voltage where the source barrier takes over the control of the drain current (SGT threshold voltage), and falls with increasing current. *n-type* bulk doping results in better high-$\mathbf{V_D}$ gain characteristics, but peak gain figures of almost 10,000 are obtained around $\mathbf{V_{SAT2}}$ when bulk doping is low.

We can conclude that the fabricated polysilicon SGTs operate as expected from a source-gated transistor architecture. Properties such as high output impedance, high cut-off frequency and high intrinsic gain could enable the fabrication of large-area, flexible or disposable electronic circuits with good analog performance, which would not be possible if the standard FET structure were to be used. The temperature coefficient can be varied from very low values to highly activated. In the latter case, the large temperature coefficient of the current, which is undesirable in the majority of circuit applications, can be taken advantage of in highly responsive temperature sensors.

Computer simulations show that thin-film transistor structures in which a unipolar source barrier is created by doping the region under the source contact can operate as a source-gated transistor. These transistors should therefore have all the benefits of source-gated transistors, namely low saturation voltage, high output impedance and less sensitivity to short channel effects when compared to a standard FET.

Because the source barrier can be pulled down more easily in a BUSGT than in a SBSGT, the former has a larger dynamic range and can operate at higher currents, with higher transconductance and lower activation energies for current transport, leading to lower temperature coefficients.

The presence of a large source barrier can lead to less drain field sensitivity; therefore this device concept is one of the solutions that make it possible to design short-channel devices with low off-currents.

Chapter 5 has presented the measurement results of Schottky barrier SGTs (SBSGTs) fabricated in polysilicon and an analysis of device behaviour compared to standard polysilicon TFTs. An alternative way of realising the source barrier has been described (BUSGT), together with the performance characteristics which one should expect from a device comprising such a barrier.

In Chapter 6, the reader is introduced to some basic analog circuit blocks built with SGTs with the aim of outlining the potential performance benefits of this device structure in real world applications.

Chapter 6. Circuit design with the SGT

6.1. Introduction

The research and development of electronic devices has a key deliverable: to improve the performance (be it power efficiency, speed, precision, flexibility, ruggedness and cost of manufacture) of circuits made using them. A single device by itself hardly has any application, and this is especially true at this time of high integration, of building whole systems on the package and of unprecedentedly pervasive use of electronics.

Both digital and analog circuits built using CMOS silicon technology have reached a maturity which enables the fabrication of very complex, high performance applications for a sensible cost. Nonetheless, device technology is far from its development limits, as transistors keep reducing in size, allowing for more speed and increased integration. Devices used for digital circuits at present suffer from leakage, negative bias temperature instability, and other short channel effects. Scaled analog transistors are increasingly difficult to match and suffer even more from fabrication variability. Device research plays an essential role in mitigating these shortcomings for the current and future generations of CMOS technology, while at the same time improving energy efficiency, increasing yield and reducing costs.

In large-area electronics (LAE), there is currently a record demand for high definition display screens for television sets, computers, smartphones, etc. Polysilicon, amorphous silicon and increasingly organic semiconductor technologies are very attractive in terms of costs. Additionally, these technologies are being proposed for adaptation to plastic substrates in large-volume manufacturing, with the aim of producing flexible electronics. It is very likely that fabrication will soon reach the level of refinement that opens up the

possibility of integrating more of the functionality of the application onto the panel, rather than employing specialised CMOS chips. Very high speed digital and high performance analog applications would then be possible using LAE technologies.

The balance between cost and performance is biased toward price in LAE, and due to fabrication technology and material properties, it is difficult to engineer high performance analog circuits with these materials using the standard TFT structure. However, the properties of the source-gated transistor (SGT) open up new design possibilities for improving performance in existing applications or for enabling new applications with materials which are in principle not suitable.

This chapter presents some introductory thoughts and preliminary conclusions into the use of SGTs in analog electronic circuit blocks which would be impossible to build with LAE technologies due to the incapacity of the standard field-effect transistor to deliver the required performance. The discussion also outlines the benefits and considerations when undertaking such a design challenge.

6.2. Effects of process variability

The performance of integrated circuits can be severely compromised by variability. Due to the nature of the technological process, parameters can vary between devices in the same circuit, on the same substrate (or wafer) or on different substrates, sometimes unpredictably. This has the effect of changing circuit behaviour from the designed specification. As a measure of improving yield and reliability, circuit designers opt for sizeable margins of safety.

Large gains in overall performance can be obtained by reducing these safety margins owing to optimizations of process control and parameter uniformity. A thorough understanding of the limiting factors specific to a particular electronic device is essential, especially for newly developed structures such as the Schottky Barrier SGT (SBSGT).

To date, SBSGTs have been made in polysilicon and hydrogenated amorphous silicon but this type of device has never been integrated in a circuit. The following sections describe the tolerance to process variability of the drain current of the SBSGT and attempt to formulate a set of basic design rules for high performance large area integrated circuits containing SBSGTs.

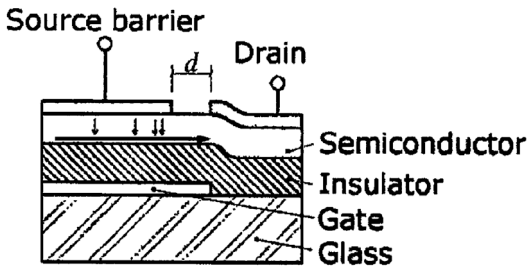


Figure 6.1. Cross section of a source-gated transistor (SGT).

To this end, a standard SBSGT structure [104] has been investigated using the Silvaco Atlas 2D physical simulation environment. The semiconducting material is n-type polysilicon and the insulator is silicon oxide. For the default structure the drain contact is ohmic, there is a metal-semiconductor barrier at the source and the gate overlaps the source completely (see Figure 6.1). Table 6.1 describes the symbols used and the nominal values of the basic parameters. Figure 6.2 depicts the output and transfer characteristics for the default structure.

It should be noted that this is not a circuit design exercise, but rather an attempt to illustrate the possible effects of process variations; parameters which are not under the circuit designer's control have been included in the investigation, and the range of parameter values has been widened in order to establish meaningful trends.

TABLE 6.1. GEOMETRICAL AND ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Default value
Source length	S	1μm
Source-drain separation	d	1μm
Device width	W	1μm
Insulator layer thickness	t_{ox}	50nm
Semiconductor thickness	t_{si}	10nm
Schottky barrier height	Φ_B	0.35eV

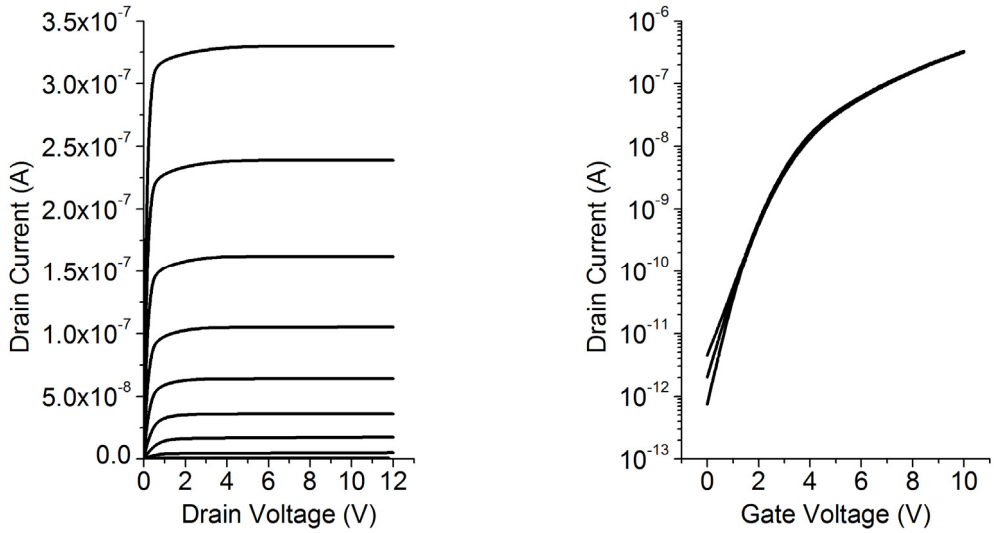


Figure 6.2. Output and transfer characteristics of the simulated SGT.

6.2.1. Source length simulation

The source window is opened by etching the insulator and edge defects or differing etch rates can result in mismatches between devices. The width of the window represents the device width and can be likened to the width of a FET, **W**. The source window length (**S**) has a direct impact on frequency behaviour, as shown in Section 5.8.

Simulations have shown that the current transport over the potential barrier has the largest magnitude at the edge of the source closest to the drain, as expected, based on the device electric field. This has been corroborated by measurements [106], as described in Section 5.6.2.

Figure 6.3 shows the dependence of saturated drain current on **S**, where **S** is measured from the edge of the source closest to the drain. It can be seen that, for a given gate bias, $\mathbf{V_{GS}}$, there is a certain value of **S** above which the current has very little sensitivity to process variations (on the order of tenths of a micron) of **S**. This value increases with gate bias. An explanation can be found by observing that, at higher $\mathbf{V_{GS}}$, conductivity

under the source is larger and therefore the contribution to current transport from regions further from the source edge is increased.

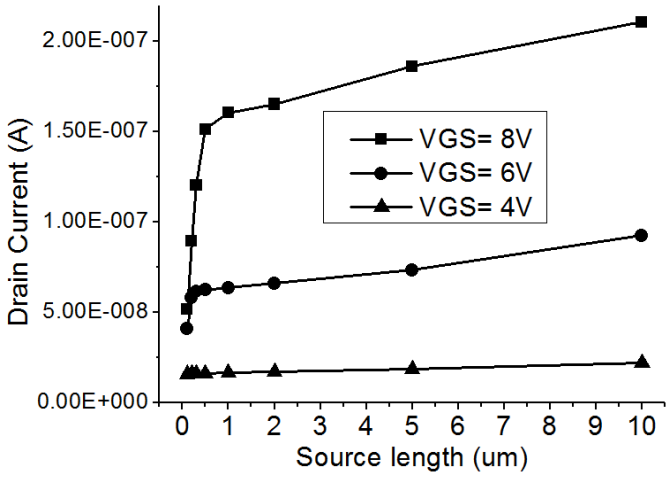


Figure 6.3. Variation of drain current with source length for three values of gate voltage.

We conclude that, in order to minimize the error in drain current caused by source length variations between transistors, **S** should be made greater than 0.5μm. This value will change slightly with gate bias and with the relative insulator and semiconductor layer thickness. In practical terms this means that using the minimum feature size of current polysilicon technologies (around 1-2μm) for **S** guarantees good current uniformity across devices. This recommendation is further supported by the effective source length having a large impact on high frequency performance, and with this in mind, it should be minimised.

6.2.2. Source-gate overlap simulation

This simulation is an extension of the one discussed in the previous section. In this scenario, the source has a length of 1μm but the gate does not overlap the source completely. The results are plotted in Figure 6.4. For a large overlap, the simulation shows the same results as in Figure 6.3. The effective source length is in fact the length of the source-gate overlap.

Such a situation can occur in fabrication as a result of unintentional misalignment between the source and the gate, for example due to glass substrate compaction during an intermediate process step. The resulting alignment error is most detrimental to large-area circuits in which devices are separated by a comparatively large distance, or between small circuits made on a large substrate.

The smallest overlap in Figure 6.4 corresponds to the case when the structure is a regular FET with a Schottky source barrier and no (or minimal, accidental) source-gate overlap.

In this case the gate field does not fully function in lowering the effective barrier height and the drain current is thus severely limited.

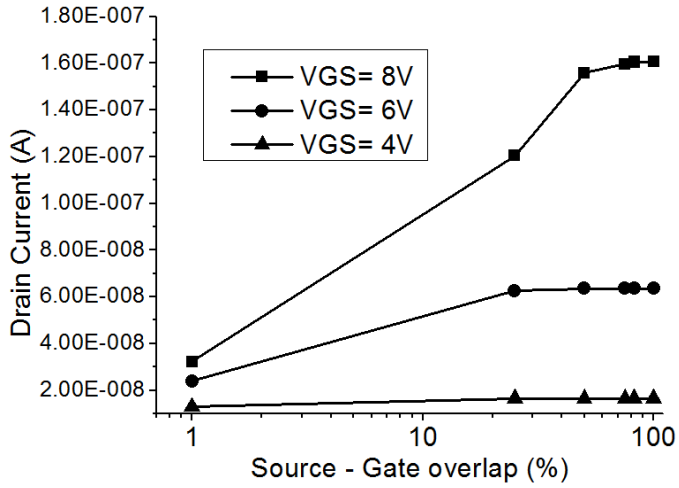


Figure 6.4. Variation of drain current with source-gate overlap for three values of gate voltage

Even for zero overlap, the current changes slightly with gate bias, indicating that there is some barrier lowering. This can be attributed to the fringe fields at the gate which act on the source even when the two do not overlap physically. The design recommendation given in the previous section still applies. The transistor should be designed so that the source-gate overlap value is well within that required to maximize the current (e.g. 50% for $\mathbf{V_{GS}}$=6V in this case, which translates into 0.5μm).

6.2.3. Source-drain separation simulation

One of the main advantages of SGTs is the fact that the drain current is independent of source-drain separation (**d**, equivalent to the length of the parasitic FET in series with the source barrier) [105]. This means that the high output impedance in saturation and the low saturation voltage are maintained even when **d** is decreased to well below 1μm.

As can be observed from Figure 6.5, at high gate bias the drain current remains constant when **d** is varied from 2μm to 0.2μm. For longer source-drain gaps, the current starts to decrease, more so for $\mathbf{V_{GS}}$=6V than for $\mathbf{V_{GS}}$=8V. The reason for this drop can be attributed to the reduced conductance of the parasitic FET channel for longer **d**. This is confirmed by the $\mathbf{V_{GS}}$=4V plot.

From an integration point of view, smaller devices are beneficial. Keeping **d** under 1μm also has some other advantages such as the possibility of operating at lower gate bias for high current output and high switching speed. In organic materials in which the effective carrier mobility is drain field dependent, a short source-drain gap leads to increased electrical field and faster device operation [103, 121].

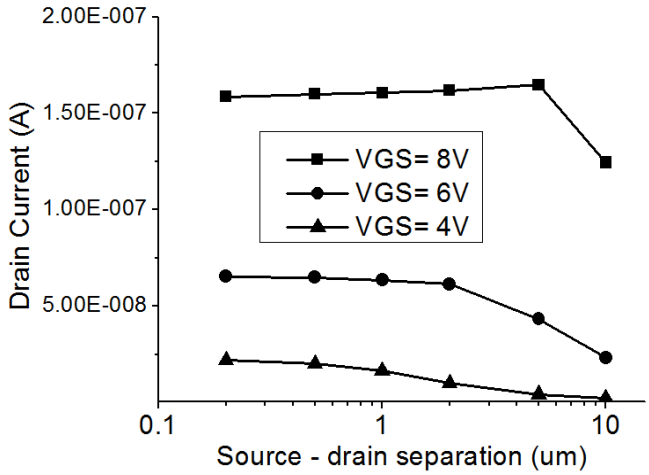


Figure 6.5. Variation of drain current with source-drain separation (parasitic FET channel length) for three values of gate voltage.

It can be concluded that the on-current of the SBSGT is independent of d in saturation. The most important consequence of this fact is that SGTs are well suited to be made with consistent performance in large-volume techniques (such as inkjet printing, stamping or lift-off) in which high accuracy is difficult to achieve due to the speed of manufacture of the large area processes and to cost implications.

Since none of these technologies can produce deep-sub-micron features yet, d should be chosen at the lower limit of the design rule. One caveat of this affirmation is related to high voltage operation, where minority carrier generation in high-field regions is exacerbated as the source-drain separation decreases.

Figure 5.24a shows the measured output characteristic for two polysilicon SGTs having different source-drain separations. There is an obvious degradation in the output impedance of the shorter device for gate voltages exceeding approx. 12V. Even though the performance loss is minimal, it could impact critical applications such as accurate current copying. The relative decrease in output impedance for the two devices is plotted in Figure 6.6, for $\mathbf{V_D}$=20V. The longer device exhibits no degradation at high drain voltage. For shorter **d**, the magnitude of the additional current decreases as the gate voltage is raised further from the threshold, which is consistent with the theory of hot-carrier generation [77].

However, too long a **d** can have detrimental effects on the low voltage operation of the SGT. The device may enter in a hybrid mode in which the large d separation decreases the conductance between the source and the drain, leading to the current being controlled predominantly by the parasitic FET. The output characteristic becomes rounded for $\mathbf{V_D}$=$\mathbf{V_{SAT1}}$ and low voltage operation is slightly compromised. Measurements on the polysilicon structures, for identical devices but with different source-drain gaps confirm this assumption. (Figure 6.7)

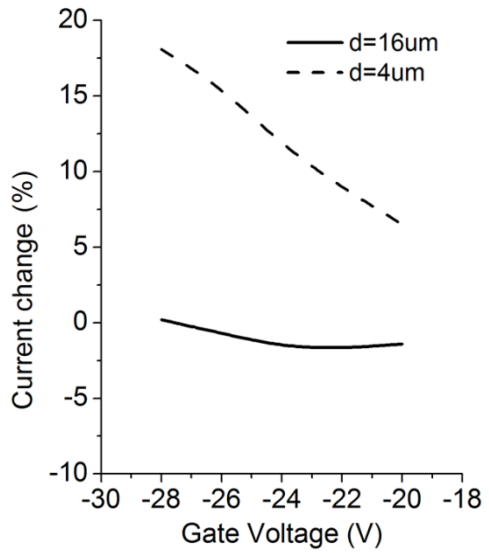


Figure 6.6. Excess current generated at V_D=20V for two source-drain separations, measured on a double-drain, asymmetrical device. See also Figure 5.24.

In conclusion the choice of **d** should be based on the desired operation regime. The lowest drain voltages can be successfully employed if d is at the minimum required by the technology ($\mathbf{d}_{min}$); empirical observations show that good output characteristics are obtained for $\mathbf{d} > 5 \cdot \mathbf{d}_{min}$. Apart from optimising frequency behaviour, there is little reason to choose an intermediate value between these two extremes.

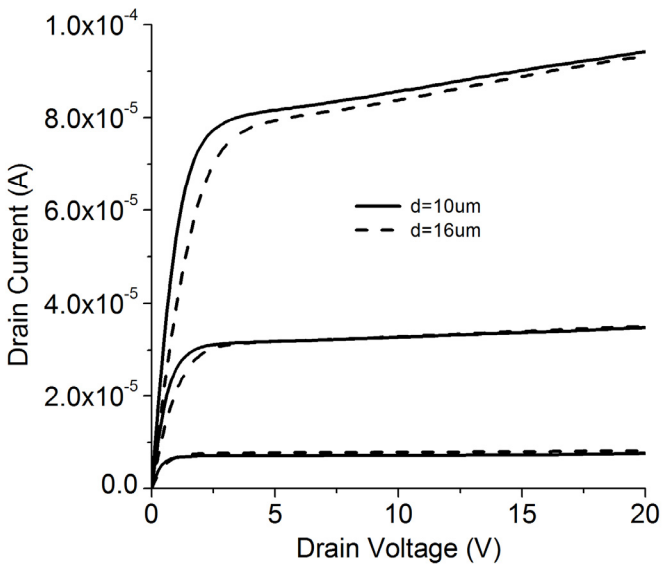


Figure 6.7. Output characteristics measured on polysilicon SGTs showing the influence of source-drain separation on saturation voltage.

6.2.4. Insulator thickness simulation

The dependence of drain current on insulator thickness is shown in Figure 6.8.

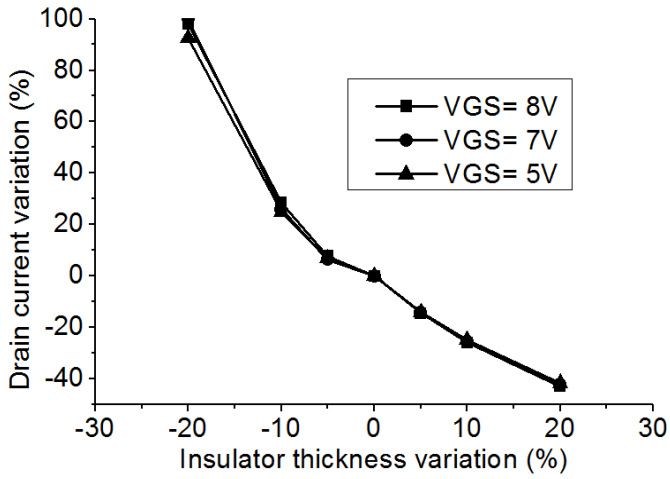


Figure 6.8. Variation of drain current with insulator thickness for three values of gate voltage

It can be observed that even small changes in insulator thickness can have a significant effect on the on-current. $\mathbf{t_{ox}}$ influences both the FET channel conductivity and the magnitude of the field that pulls down the source barrier. Since for this structure the on-current in saturation is limited by the source barrier, we can state that it is the latter effect that has the greatest contribution, and the effect is identical regardless of the gate bias.As a result, the current is very sensitive to insulator thickness, and good $\mathbf{t_{ox}}$ uniformity across the wafer is desired.

In practice, the actual sensitivity to insulator thickness variations will depend, of course, on the thickness of the semiconductor, as the field at the source is proportional to $C_i / (C_i + C_S)$ (see Equation 4.5). The usual matching techniques should be used during the circuit design stage to ensure repeatability across the wafer. Good process control is necessary for wafer-to-wafer reproducibility.

6.2.5. Semiconductor thickness simulation

As with $\mathbf{t_{ox}}$, the thickness of the semiconductor, $\mathbf{t_{si}}$, has an impact on both the channel conductance and the barrier-lowering gate field. The behaviour of the SGT is also influenced by the relative ratios between the semiconductor layer capacitance and insulator capacitance [105].

In this particular structure it can be observed (Figure 6.9) that the change of drain current with semiconductor thickness is dependent on gate voltage. For this simulation, this dependence is at a minimum around $\mathbf{V_{GS}}$=4.8V. The change increases as the gate

voltage is raised above 4.8V and the current increases. Therefore, for high current small variations of $\mathbf{t_{si}}$ may result in unacceptable changes of the on-current.

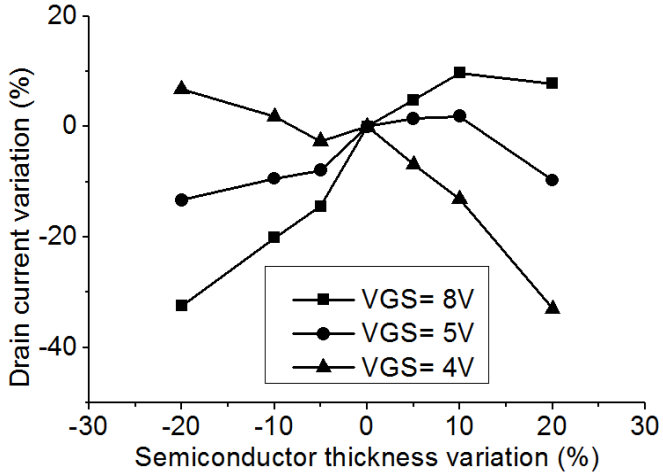


Figure 6.9. Variation of drain current with semiconductor thickness for three values of gate voltage.

The existence of a value of the gate bias for which the drain current dependence on $\mathbf{t_{si}}$ is minimal prompts the analytical investigation of this phenomenon. Establishing variability-aware design rules for any given $\mathbf{t_{si}}$, $\mathbf{t_{ox}}$ and dielectric properties of these layers would help ensure optimum performance in large area, low-cost technologies.

Interestingly, if uniform frequency response is required rather than uniform drain current then it is found that variations in insulator and semiconductor thicknesses are not important, as the cut-off frequency depends only on the current density through the source contact [108]. (See Section 5.8.)

6.2.6. Schottky barrier height simulation

Figure 7.10 shows the dependence of the saturated on-current on the source barrier height, Φ_{B0}. This type of plot is useful in visualizing the effect of having a source barrier in series with a finite conductance FET channel. For low barriers, the FET channel limits the current at low gate biases and the device is in a hybrid mode. At higher $\mathbf{V_{GS}}$, the channel becomes very conductive and the current becomes limited by the source barrier. For high barriers, the FET channel does not play a part in restricting the current and the influence of the gate field on the source barrier can be seen clearly: increasing the gate bias lowers the effective barrier height and current increases exponentially.

In order to achieve moderately high on-currents, a balance needs to be achieved between the two, but as the barrier gets lower and the device behaves more as an FET the high output impedance in saturation starts to suffer and saturation occurs at a higher drain voltage.

We see from Figure 6.10 that the drain current is very sensitive to the magnitude of the source barrier height. The barrier itself is controlled by the choice of contact metal [41] and doping [45], but processing of consecutive substrates needs to be consistent (e.g. complete removal of interfacial layers in the source window).

Furthermore, current transport across the barrier is thermally activated [41] and on-chip temperature variations can lead to significant changes of drain current. Circuit design techniques such as matching, differential signal processing, current driving and temperature compensation should be used. Special attention should be paid to the conditions (gate bias, supply voltage, $\mathbf{t_{si}}$, $\mathbf{t_{ox}}$, source metal) needed for maintaining the SGT-like operation at high temperature where the barrier is lower.

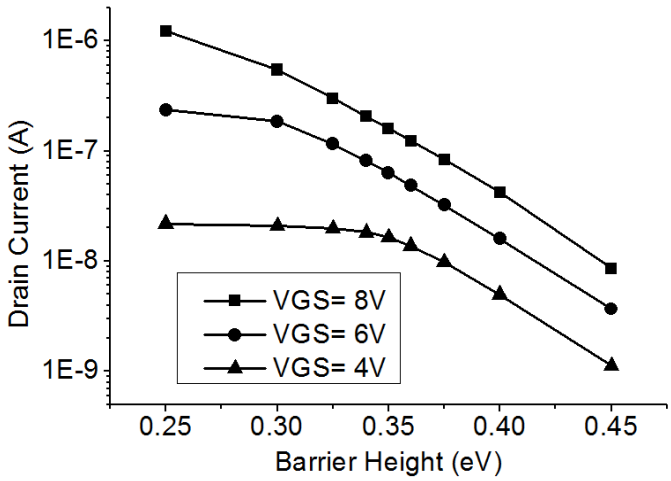


Figure 6.10. Variation of drain current with Schottky barrier height for three values of gate voltage

6.3. Temperature sensing with source-gated transistors

6.3.1. Introduction

In sensing systems, the magnitude of the quantity to be measured is inferred from changes to electrical parameters in the measuring circuit (resistance, current or voltage). Mixed signal sensors translate the analog electrical quantity correlated to the measurand into a number. For easy manipulation of this data, it is important that the electrical parameter has a linear dependence on the physical quantity which is measured. This linearity is usually achieved by analog operations based on the properties of electronic components, such as transistors, and circuit blocks.

6.3.2. The SGT as temperature sensor

From the principles of operation of the Schottky source SGT, it is inevitable that the current will be temperature activated. In most electronic circuits this is detrimental, particularly by the increase in power consumption. Yet there is one obvious application where a high temperature coefficient is in fact desirable: temperature sensor circuits.

Measurements have been performed on the polysilicon source-gated transistors with a Schottky source barrier which were described in Section 3.6. The device was biased so that a constant 100μA drain current was obtained. The gate voltage required at this operating point was noted as the temperature was changed and the results are plotted in Figure 6.11. It is immediately noticeable that, over a limited temperature range, the gate voltage has a fairly linear dependence on temperature, with minor nonlinearities. Moreover, there is a large change of gate voltage with temperature.

We can now begin to look for ways in which temperature can be measured with precision and repeatability using SGTs. The targets are high performance mixed-signal large area electronic applications, remote sensing and disposable sensors, conceivably built on plastic using organic semiconductor technology.

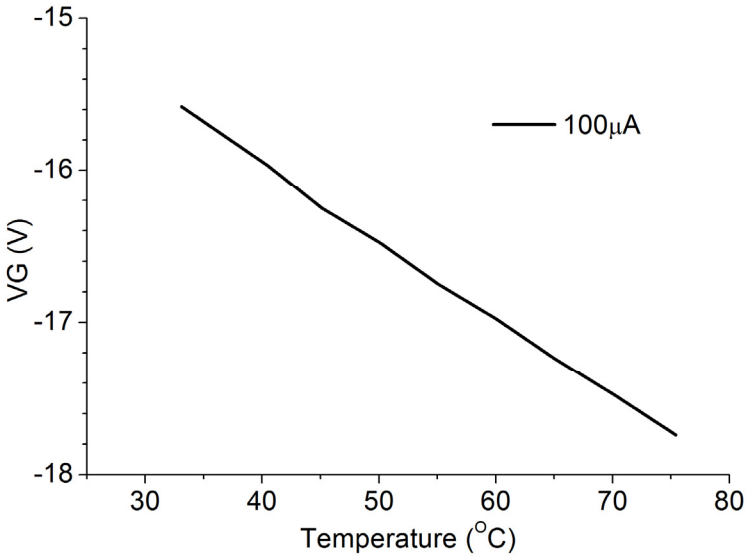


Figure 6.11. Gate voltage against temperature at a fixed drain current for an SGT with W=50μm, S=4μm, d=4μm; $1\cdot10^{13}/cm^2$ n-type doping under the source barrier and $2.5\cdot10^{12}/cm^2$ n-type bulk doping.

6.3.3. The basic topology of a mixed-signal electronic temperature sensor

Modern integrated electronic temperature sensors have a digital output in order that the temperature can be read by system management controllers. A block diagram of a standard temperature measurement circuit is shown in Figure 6.12 [122].

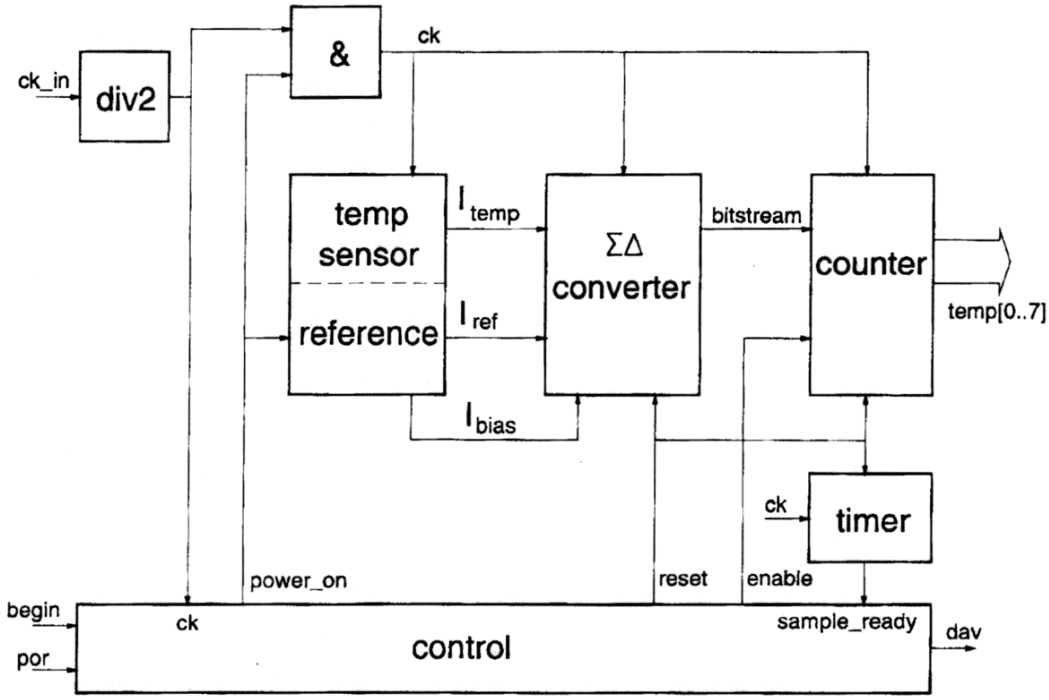


Figure 6.12. Integrated CMOS temperature sensor architecture, after [122].

These typically use the temperature-induced change of forward voltage in diode-connected lateral *pnp* bipolar transistors (easily achieved in n-well CMOS processes) to sense the local temperature of the silicon. The temperature is translated into a current rather than a voltage in order to improve the dynamic range of the analog to-digital conversion, as the supply voltage is in the range of 1.2 to 2.5V in CMOS circuits.

A current which is proportional to absolute temperature ($\mathbf{I_{PTAT}} \equiv \mathbf{I_{TEMP}}$) and one which is either constant or complementary to absolute temperature ($\mathbf{I_{CTAT}} \equiv \mathbf{I_{REF}}$) are generated in the analog block. They are alternately fed to an integrator which outputs a saw tooth voltage based on the relative ratio of the two currents. For example, $\mathbf{I_{TEMP}}$ is used to charge a node and $\mathbf{I_{REF}}$ discharges the same node, so that the ratio is expressed in the time it takes to reach certain thresholds while charging and discharging.

A ΣΔ (sigma-delta) converter is used for analog-to-digital conversion, the output of which is a one-bit digital signal. Finally, the bitstream coming from the converter is counted. If the count is zero, then the minimum temperature is reported. The temperature is found to be the maximum value (for which the circuit was designed) when at the end of the conversion cycle the counter is full, in other words a pulse was received from the ΣΔ converter for every clock cycle.

Linearity of the electrical signal against absolute temperature is achieved at design time in the analog sensing scheme. Slope errors are corrected by changing the amount of discharge current during final testing after manufacture. Offset corrections can be achieved by setting a reset value other than zero for the counter register (digital) or, more commonly, by tuning the voltage reference block. ΣΔ modulator topologies exist that permit noise shaping and improved accuracy for a large dynamic range, to the point that very high accuracy can be attained [123].

6.3.4. Temperature sensing schemes with the SGT.

In order to create a SGT-based temperature sensor we need to understand the technological limitations. The scheme in Figure 6.12 requires a clock signal in the order of 10KHz to 1MHz, depending on the desired resolution if several measurements are to be performed every second. This can, in principle, be achieved in polysilicon technology and if the requirements are relaxed, the sensing application can be integrated in amorphous silicon and organic semiconductor large area circuits. The digital part of the circuit would then be made using standard polysilicon FETs, while the analog part would contain SGTs in the $\mathbf{I_{PTAT}}$ generation block ("temp sensor" block and part of "reference" block in Figure 6.12).

There are several ways in which the required $\mathbf{I_{REF}}$ and $\mathbf{I_{TEMP}}$ can be generated by taking advantage of the following properties of the SGT:

- The current is exponentially dependent on temperature;
- The current is exponentially dependent on gate-source voltage;
- Gate-source voltage is linearly dependent on temperature;
- The effective barrier height changes with gate-source bias, and implicitly the temperature dependence of the current varies with gate-source bias.

The simplest topologies require that the reference current is generated separately as in a standard circuit [122] and one SGT biased at constant current. Figure 6.13 illustrates the principle of generating a current which is proportional to temperature from the variation of the SGT's gate-source voltage.

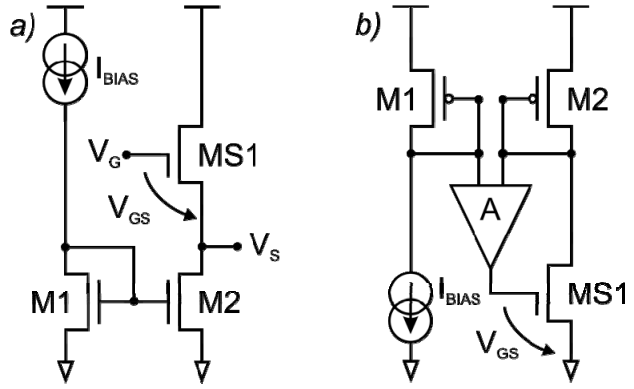


Figure 6.13. Circuit topologies for generating a voltage which has a linear dependence on temperature using a SGT. This voltage is then converted into a PTAT current.

The SGT is biased at constant current through the current mirror, and its gate voltage is fixed. The gate-source potential drop self-adjusts to bias the SGT to this operating point. Assuming the bias current is constant with temperature, $\mathbf{V_{GS}}$ will decrease as the temperature increases. $\mathbf{V_{GS}}$ or $\mathbf{V_S}$ can be buffered onto a resistor to create currents which are PTAT or complementary to absolute temperature, respectively.

Another option is to bias the SGT at constant current by using a differential gain stage. The amplifier drives the gate of the SGT so that diode-connected FETs **M1** and **M2** are operating under identical conditions. Setting the temperature-independent current through **M1** and assuming that the amplifier and FET action are not sensitive to temperature, the gate voltage of the SGT will decrease with an increase in temperature. $\mathbf{V_G}$ can be repeated in the same way as above using a buffer to generate a current which varies linearly with temperature.

In Section 5.6 it was described how the activation energy of the current through the SGT changes with gate voltage. Another way of expressing the same conclusion is: for a given drain current, the temperature coefficient of the gate voltage will be different depending on the bias point of the device. Figure 6.14 presents measured variations in gate-source

voltage and shows how the slope changes depending on biasing conditions (and drain current).

By appropriately choosing the width of the device and the bias point, we can exploit this behaviour to generate voltages (and currents as explained above) with different temperature coefficients. Furthermore, these quantities can be generated using a single device with chopped input (Figure 6.15), which eliminates errors which arise from geometrical mismatches between individual transistors.

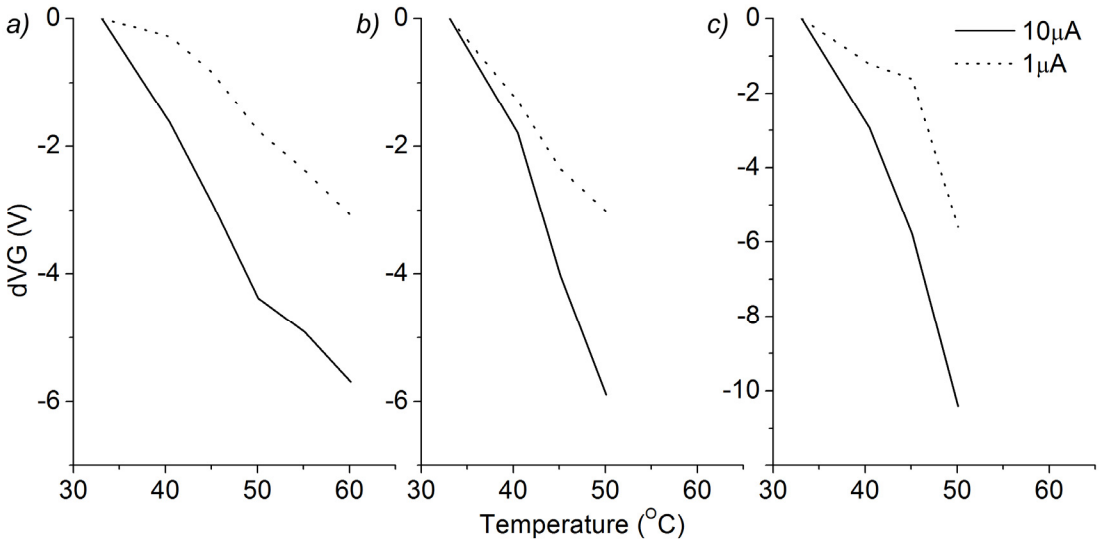


Figure 6.14. Change in gate voltage with temperature at a fixed drain current for SGTs with W=50μm, S=4μm, d=4μm and $2.5\cdot10^{12}/cm^2$ n-type bulk doping; p-type doping under the source barrier: a) 0, b) $1\cdot10^{13}$ and c) $5\cdot10^{13}/cm^2$.

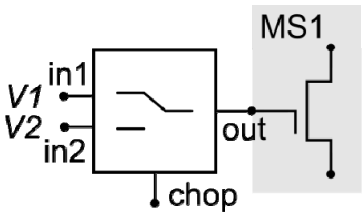


Figure 6.15. Two input voltages can be multiplexed at the gate terminal of the SGT to produce two distinct temperature variations. The practical scheme would include a feedback loop to control V1 and V2 so that the drain current of MS1 remains constant.

Advancing this reasoning further, a PTAT and a CTAT current can be generated using one device, by changing the polarity of the current through the transistor. This effectively switches the structure between SGT and FET operation (Figure 6.16), one with strong temperature coefficient, and the other with a comparatively weak one.

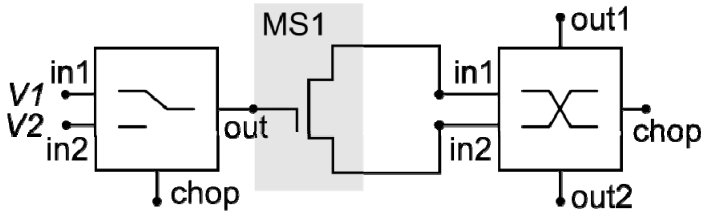


Figure 6.16. The SGT can be operated in reverse (as a FET) and with a corresponding gate voltage. This allows the generation of a PTAT and a CTAT current using one device.

The barrier modification implant can be used to change the activation energy of the SGT drain current at a given gate voltage (see Section 5.6). For devices with different barrier changing implants, the gate voltage needed to keep current at a constant value changes with temperature as shown in Figure 6.17. It can be seen that at high current, where the barrier is pulled down strongly, the barrier modification implant has a significant influence on the temperature coefficient. Heavier *p-type* doping increases the effective height of the barrier and requires larger gate voltage swings to keep the current constant with temperature.

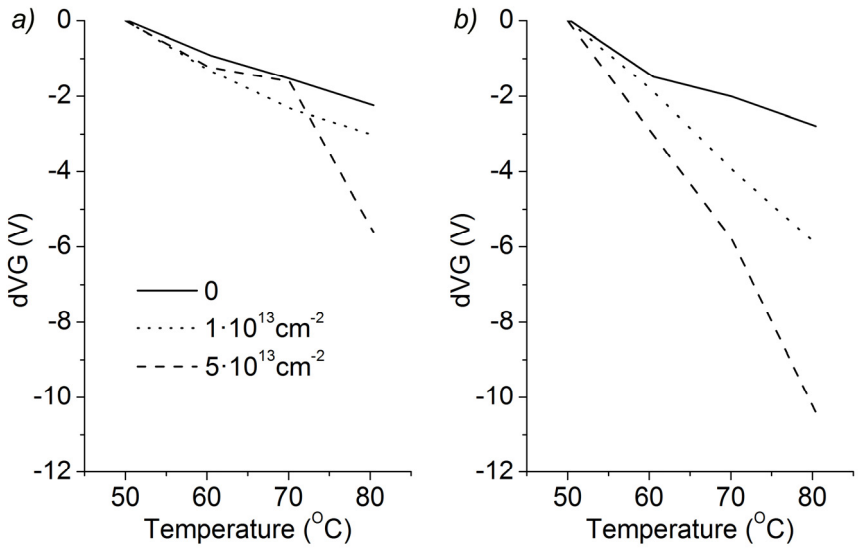


Figure 6.17. Change in gate voltage with temperature and p-type barrier modification doping for SGTs with W=50μm, S=4μm, d=4μm and $2.5\cdot10^{12}/cm^2$ n-type bulk doping. Drain current: a) 1μA, b) 10 μA.

The temperature coefficient of the gate voltage is plotted against barrier modification implant in Figure 6.18 at two drain currents. It is seen that the change in gate voltage for each degree of temperature variation increases with *p-type* doping (or effective barrier height). For the *n-type* implant, the current is not controlled solely by the barrier (as explained in Section 5.6) and so the temperature coefficient is very low.

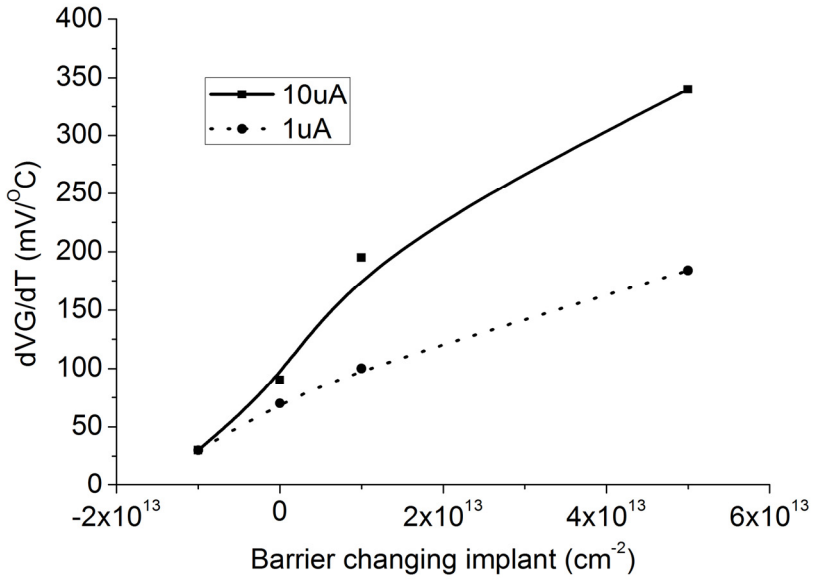


Figure 6.18. Absolute value of the gate voltage temperature coefficient against barrier modification implant at two drain currents for SGTs with W=50μm, S=4μm, d=4μm and 2.5·10¹²/cm² n-type bulk doping.

Nevertheless, the combination of thick layers and high *p-type* doping produces temperature coefficients far larger, in absolute value, than the -2mV/^{O}C one expects from semiconductor diodes in CMOS technology [124]. By changing the current through the device and the concentration of the barrier modification implant, it is possible to adjust the sensitivity of the temperature sensor containing the SGT.

For instance, a sensing circuit with two SGT temperature sensors could provide a coarse temperature reading across a wide range and a finer one in a designated range of temperatures (Figure 6.19). Several high-sensitivity temperature sensing circuits comprising SGTs can be included in the overall sensing scheme. Only one would be active at one time and would sense within its range. As the temperature reaches the end of its sensing range, the next block would become active and take over the sensing operation. This way, the whole temperature span can be sensed with a high sensitivity and accuracy (Figure 6.20).

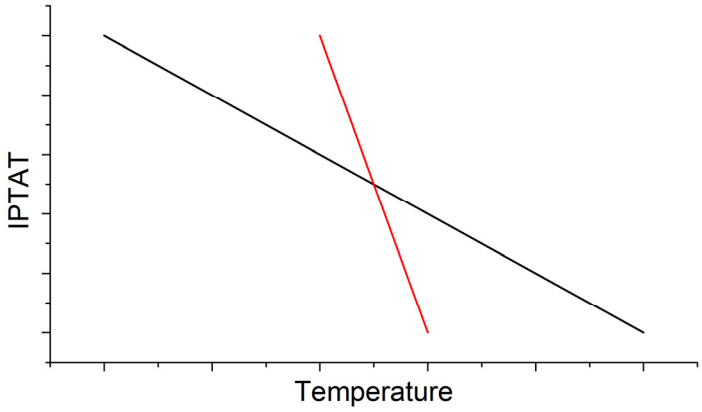


Figure 6.19. Schematic showing a low-sensitivity (black) and a high-sensitivity (red) temperature sensor.

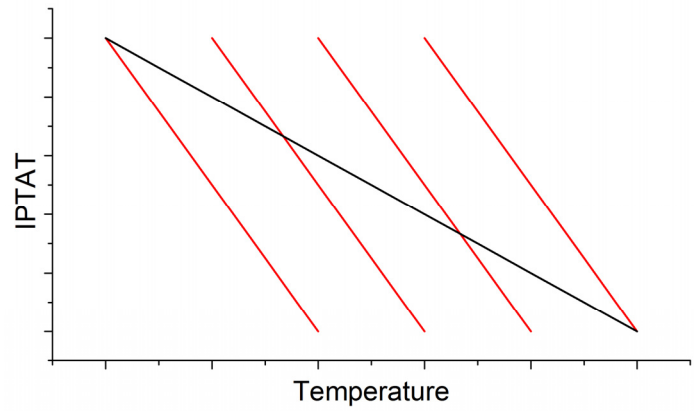


Figure 6.20. Schematic showing the improved sensitivity of a multiple-range temperature sensor (red) compared to a standard single-range sensor (black).

Care should be taken in the design of SGT temperature sensors in order to avoid errors and nonlinearities due to self-heating. If the current density through the sensor is high, self-heating can pose significant problems, especially in devices with a very high temperature coefficient. Schemes which include multiple SGTs operating at different currents are most affected, so good layout and an understanding of the extent of self-heating effects are necessary.

6.4. Gain stages and active loads

6.4.1. SGT active loads

Thin-film polysilicon technology is widely used in large area electronics, such as flat panel displays and touch-sensitive input devices [118] due to its ability to deliver large scale integrated circuits at a comparatively low cost. Significant research efforts have been made recently towards integration of complex electronic circuitry directly onto the flat panel, resulting in System on Panel (SoP) architectures [119]. However, polysilicon thin-film field-effect transistors (FETs) have generally modest performance when being used in analog circuits. The source-gated transistor (SGT), has the potential to extend the applicability of disordered semiconductors to analog and mixed signal circuits.

A Schottky barrier SGT is comprised of a metal-semiconductor barrier at the source terminal in series with a parasitic FET transistor. The gate extends over the source and, apart from its usual role of modulating the FET channel conductance, controls the effective height of the source barrier. The relevance of the SGT to analog circuits is a consequence of the defining characteristics of the SGT: reduced kink effect, low saturation voltage and high output impedance in saturation. The reverse biased barrier at the source prevents bipolar amplification of carriers generated in the high-field regions near the drain, thus reducing the kink effect [75-77]. Due to the SGT's construction (Figure 6.21), when the drain voltage is increased, the current saturates as the semiconductor area under the source is depleted of free carriers at a voltage $\mathbf{V_{SAT1}}=(\mathbf{V_{GS}} - \mathbf{V_T})\cdot\mathbf{C_i}/(\mathbf{C_i}+\mathbf{C_s})$, where $\mathbf{V_T}$ is the threshold voltage and $\mathbf{C_i}$ and $\mathbf{C_s}$ are the insulator and semiconductor capacitances, respectively [3]. At $\mathbf{V_{SAT2}}=\mathbf{V_{GS}} - \mathbf{V_T}$, the channel between the source and the drain pinches off at the drain, similar to a standard FET, and saturation becomes stronger. Since the current is controlled by the reverse biased source barrier, the drain current in saturation is independent of source-drain separation [105] and the output impedance ($\mathbf{Z_O} = \partial I_D/\partial V_{DS}$) in saturation can be very high, especially for $\mathbf{V_{DS}} > \mathbf{V_{SAT2}}$.

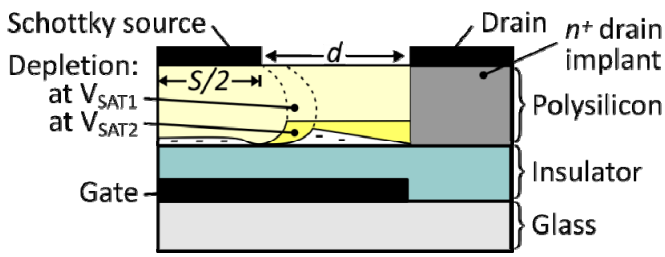


Figure 6.21. Schematic cross-section of the self-aligned polysilicon SGT, showing source length (S), source-drain separation (d) and depletion region when the channel pinches off at the source ($V_{DS}=V_{SAT1}$) and at both the source and the drain ($V_{DS}=V_{SAT2}$), as explained in the text.

Typical output characteristics measured on an excimer laser crystallized polysilicon SGT are shown in Figure 6.22a. The thick insulator (300nm equivalent oxide thickness) ensures that $\mathbf{V_{SAT1}}$ is very small, at the expense of a low transconductance. Figure 6.22b shows that the output impedance $\mathbf{Z_O}$ is very high over a wide range of drain voltage, which is not the case for a typical FET design. By swapping the source and drain terminals, the Schottky barrier is forward biased and the device operates as a FET. Figures 6.22c and 6.22d show the measurement results for the same device in the FET configuration: saturation occurs at high voltages and output impedance is comparatively low.

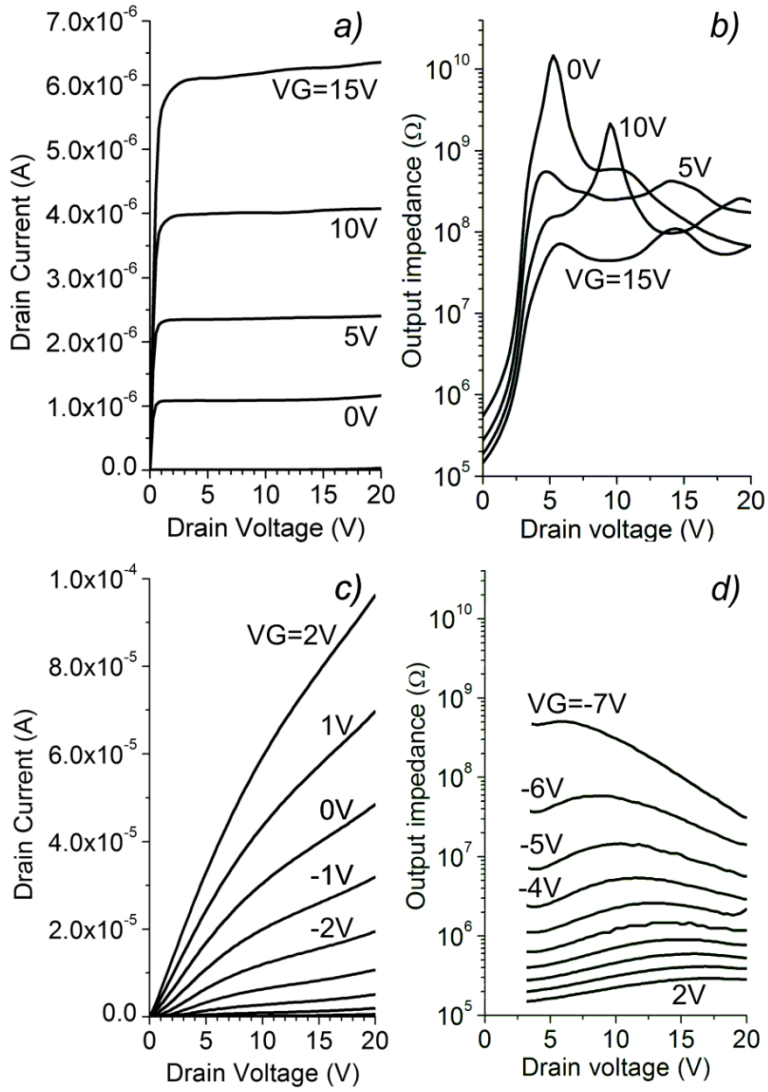


Figure 6.22. a) Output characteristic and b) output impedance measurements at several gate voltages for a self-aligned polysilicon SGT with W=50μm, S=8μm, d=10μm, $3.5\cdot10^{12}/cm^2$ n-type doping in the polysilicon and $1\cdot10^{13}/cm^2$ p-type barrier modification implant; c) output characteristic and d) output impedance measurements for the same device operated as a standard FET by swapping the source and drain terminals.

The region under the Schottky barrier is usually doped in order to modify the barrier profile and this may be a disadvantage for operation in the FET mode, as the drain of the FET may be highly resistive as a result. However, careful design can minimize this effect and it is conceivable that the same device can be used either as a SGT or as a FET by changing the direction of the current through the semiconductor. This would allow circuits to be designed with both FET and SGT devices on the same substrate by using a single technology platform.

As a result of the source barrier controlling the current, the SGT has lower current than the FET for a given gate bias. Despite their lower transconductance [110], SGTs can operate at high frequency [108] if the source-drain gap (**d**) and source length (**S**) (Figure 6.21) are optimized. **d** can be made very small without the need for precise dimensional control, ensuring that frequency behaviour is not compromised by the conductance of the parasitic FET channel. **S** should be set as a process parameter to obtain the highest current density through the source.

These properties of the SGT suggest that this type of device is well suited to circuit applications in which low operation voltage or high output impedance is required. The basic circuit blocks used to accurately replicate *d.c.* currents, called current mirrors, require high output impedance to copy currents precisely in analog bias schemes. Similarly, as high-impedance active loads for high gain amplifier circuits, such current mirror circuits are essential constituents for future mixed-signal system-on-panel configurations.

Using numerical simulations, we have compared the performance of standard current mirrors built with polysilicon FETs and SGTs respectively (Figure 6.23). Simulations have been performed using the Silvaco mixed-mode environment. For FETs, we have used commercial polysilicon SPICE, free from the limitations described in relation to Figures 6.22c and 6.22d, thus ensuring a fair comparison. Since no accurate SPICE model is available for the SGT, these devices were simulated using numerical device modelling and were embedded in the mixed-mode circuit simulation flow.

For this initial investigation we neglect geometry and threshold mismatch with all transistors being identical. Transistor **M1** is connected in the diode configuration (Figure 6.23a), with the gate tied to the drain. A current $\mathbf{I_{REF}}$ =500nA is injected into the drain of **M1** and, by virtue of the common gate bias of **M1** and **M2**, is copied to the drain of **M2** ($\mathbf{I_L}$). Non-idealities such as short channel and kink effects, lead to a mismatch between $\mathbf{I_{REF}}$ and $\mathbf{I_L}$ which is dependent on the drain-to-source voltage ($\mathbf{V_{DS}}$) of **M2**. A cascode configuration (Figure 6.23b) minimizes these effects by dropping the variable output voltage across **M4** and keeping $\mathbf{V_{DS}}$ of **M2** relatively constant regardless of $\mathbf{V_L}$, and close to that of **M1**.

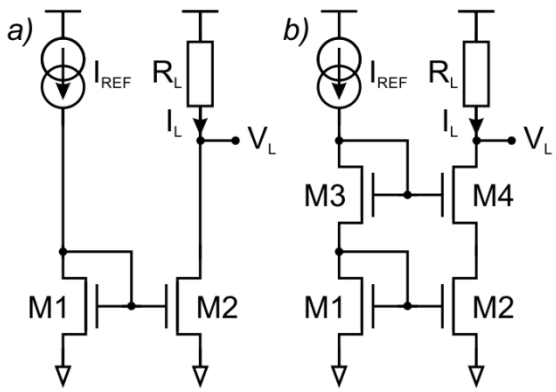


Figure 6.23. Schematic of the a) simple and b) cascoded n-type current mirror.

FET current mirror performance was assessed based on the output voltage swing (i.e. range of $\mathbf{V_L}$) for which $\mathbf{I_L}$ matches $\mathbf{I_{REF}}$ to a given accuracy (0.5% and 10% were considered). The results are shown in Figure 6.24 (considered geometries were: **W**=50μm, $\mathbf{L_{FET}}$=10μm and $\mathbf{W_{FET}}$=50μm, $\mathbf{L_{FET}}$=100μm). As expected, a longer channel FET needs a higher gate bias in order to sink the same current. Accurate current copying starts from a higher voltage but has less dependence on $\mathbf{V_{DS}}$ and slightly better performance can be achieved, as indicated by the overall longer bars. The cascode configuration performs substantially better, but requires higher supply and load voltages to account for the additional threshold voltages of **M3** and **M4**. It is apparent, however, that all FET configurations have a very small range of $\mathbf{V_L}$ (several 100mV to ≈ 2V) over which $\mathbf{I_L}$ is within 0.5% of $\mathbf{I_{REF}}$.

For comparison, simulations were performed on SGT the current mirror comprised of devices with **d**=1μm and **W**=35μm, which are supported by measurements on self-aligned polysilicon SGT structures (Figure 6.22). Despite the value of $\mathbf{d_{SGT}}$ being an order of magnitude less than $\mathbf{L_{FET}}$, the simple SGT current mirror begins operating at a much lower voltage and has a greatly improved output voltage swing, in the range of 10-20V for an accuracy of 0.5% (Figure 6.24). The drain current of the SGT is controlled by the source barrier, and is thus independent of the source-drain separation and, as a consequence, **d** can be made very small, resulting in area savings and potential of being operated at a higher frequency. A cascode configuration is not necessary for the SGT mirror circuit and 10% accuracy can be achieved from below $\mathbf{V_{SAT1}}$ up to the supply voltage. Repeating the simulation for a device with **d**=1μm and **W**=10μm results in an even larger output voltage range. Just as in the FET implementation, the narrower devices require a higher gate bias to be able to sink the same current. This increases the minimum operating voltage of the mirror, but at the same time allows **M2** to function in a regime in which the kink effect [75-77] is diminished. Choosing the right geometry for the transistors allows the operation of the current mirror either over a large range of output voltage, in the case of wider devices, or starting at a lower $\mathbf{V_L}$, for narrower ones

(Figure 6.24). As far as process variability is concerned, the mirror is immune to mismatch in **d** and **S** (Figure 6.22) and alignment errors, as seen in Section 6.2, leading to accurate current copying over a large range of $\mathbf{V_L}$.

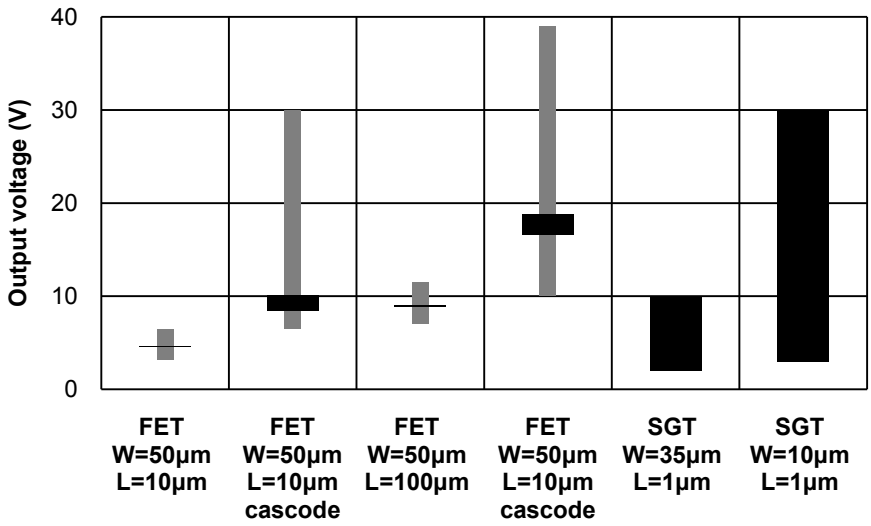


Figure 6.24. Simulation results of output voltage range for 10% (grey) and 0.5% (black) current copying accuracy. Cascode versions of the FET current mirror have significantly better performance than simple mirrors. Similarly, increasing the FET channel length improves the current copying accuracy. However, the performance of the SGT mirror is far superior for a much shorter source-drain separation: 10% accuracy can be achieved throughout the saturation region but, more importantly, 0.5% accuracy is realized over a much larger output voltage range than the equivalent FET circuit; cascoding is not required to achieve good performance. Narrower SGTs need a higher gate voltage to sink the same current and raises the minimum operating voltage, but this higher bias allows operation in a region of reduced kink effect compared to the wider devices.

This analysis has outlined the applicability of the SGT to current mirror circuits in polysilicon. Simulation results show that current mirrors using SGTs can copy current with an accuracy of 0.5% over a range of output voltages which is one to two orders of magnitude higher than can be obtained with a similar FET design. Minimum output voltage is also significantly lower. In an SGT, as the drain bias is increased, the semiconductor pinches off first at the source and then at the drain, leading to low saturation voltages and kink-free, high $\mathbf{Z_O}$ characteristics to high $\mathbf{V_{DS}}$. Simulation results are supported by experimental data.

The SGT can function as an FET by swapping the source and drain terminals (a desirable property with for incorporating both types of device in the same circuit design). Furthermore, the SGT can easily be integrated in the majority of thin-film technologies

and can be used alongside regular FETs on the same panel. Therefore, it is suitable for high performance analog applications made with a variety of semiconductors [116].

Based on our findings, the current mirror circuit using SGTs is proved to be an essential building block for bias circuits or as active loads for high-gain amplifiers as part of future system-on-panel applications made in large-area semiconductors.

6.4.2. SGT gain stage

Section 5.7 described the intrinsic gain performance of the SGT. With values reaching several orders of magnitude more than the standard FET in some cases, the SGT seems to be a very good device with which to build gain stages in large-area electronic technologies.

In order to show the suitability of the SGT for such applications, we will analyse a simple common-source gain stage [56]. The device which acts as an amplifier is an SGT and the load can be either a resistor, a FET or another SGT, as illustrated in Figure 6.25. The common-source configuration is inverting, however we are interested in the absolute value of the gain.

High gain common-source amplification stage

The SGT is used as the amplifying device because of its lower output conductance than that of the FET (see Figures 5.1 and 6.22). At currents in the μA range, $\mathbf{g_d}$ is smaller by around three orders of magnitude for the SGT when $\mathbf{V_D} > \mathbf{V_{SAT2}}$, while $\mathbf{g_m}$ is no more than two orders lower than the FET's. In this range, the SGT can have a gain of several thousand.

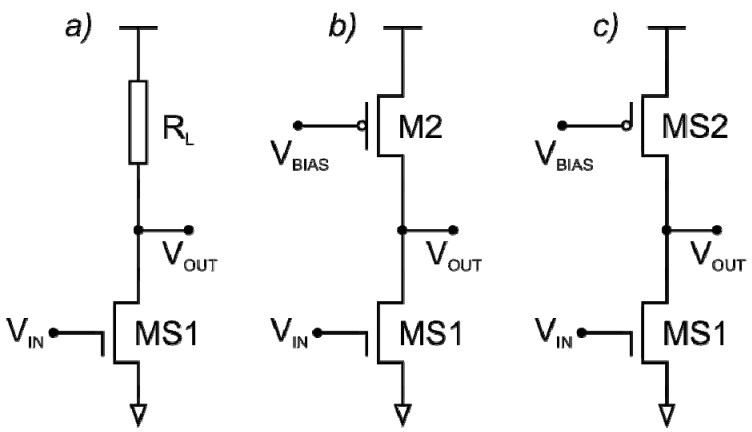


Figure 6.25. Common-source amplifier topology having a SGT as active device and a resistor (a); a FET (b) or another SGT as the load.

From Section 2.4.4, the gain of the amplifying transistor, **MS1** is:

$$A_{V(intrinsic)} = \frac{g_m}{g_d}, \tag{7.1}$$

then the absolute value of the gain of the entire stage is:

$$A_V = \left|\frac{V_{IN}}{V_{OUT}}\right| = \frac{g_m}{g_d + g_L}. \tag{7.2}$$

Here, $\mathbf{g_L}$ is the small-signal output conductance of the load, be that the resistor, FET or SGT and $\mathbf{g_d}$ is the output conductance of the SGT.

For practical reasons, the value of $\mathbf{R_L}$ in Figure 6.25a is in the range 10kΩ-1MΩ. At microampere currents, the small signal output resistance of the **M2** (Figure 6.25b) is in the hundreds of kΩ (see measurement results in Figure 6.22). At the same time, the SGT, **MS1**, has much higher output impedance, approaching 1GΩ. In these cases, $\mathbf{g_d} + \mathbf{g_L}$ approximates to $\mathbf{g_L}$ and

$$A_V = \left|\frac{V_{IN}}{V_{OUT}}\right| = \frac{g_m}{g_L}. \tag{7.3}$$

If a SGT is used as a loading device instead (**MS2** in Figure 6.25c), $\mathbf{g_L}$ and $\mathbf{g_d}$ become comparable, and the gain of the amplifier is on the order of:

$$A_V = \left|\frac{V_{IN}}{V_{OUT}}\right| \approx \frac{g_m}{2g_L}. \tag{7.4}$$

Increased output voltage swing common-source gain stage

In the $\mathbf{V_{SAT1}} < \mathbf{V_D} < \mathbf{V_{SAT2}}$ region, the SGT's gain can be significantly lower, in the 10-500 range. This range of voltages is, however, completely inaccessible to a FET amplifier, due to the fact that the device would be operating in the linear regime in which no useful amplification can be obtained. An increased output swing amplifier using SGTs for both the gain device and the load is able to operate between $\mathbf{V_{OUT}} = \mathbf{V_{SAT1}}$ and $\mathbf{V_{DD}} - \mathbf{V_{SAT1}}$. If the SGT is designed for low saturation voltage, the increase in output voltage range over a FET amplifier, which only operates from what would be $\mathbf{V_{SAT2}}$ and $\mathbf{V_{DD}} - \mathbf{V_{SAT2}}$, can be sizeable.

Since the gain of the SGT in this region is low compared to that obtained for $\mathbf{V_D} > \mathbf{V_{SAT2}}$, a large output swing amplifier would use a load with a relatively high $\mathbf{g_L}$ which would be dominant when the SGT is operating both above $\mathbf{V_{SAT2}}$ (when output conductance is extremely low) and between $\mathbf{V_{SAT1}}$ and $\mathbf{V_{SAT2}}$ (where $\mathbf{g_d}$ is substantially higher).

Temperature effects in SGT common-source gain stages

Some SGT device architectures result in very high temperature coefficients of the drain current (Section 5.6), which can be a concern for amplifiers. This is mostly true in schemes where the load is a SGT, since it has been shown that the intrinsic gain of the SGT which is the active amplifying device does not vary significantly with temperature (Section 5.7.4).

Figure 6.26a proposes a simple solution. By using the current mirror MS2-MS3 and effectively biasing the SGT MS2 with another SGT rather than a FET, the current through the amplifying transistor, MS1, is kept constant despite temperature variations. Should there arise a need for the current through MS1 to be temperature dependent, the schematic can be modified so that the current mirror comprises a diode-connected FET (M3) and a SGT (MS2), as shown in Figure 6.26b.

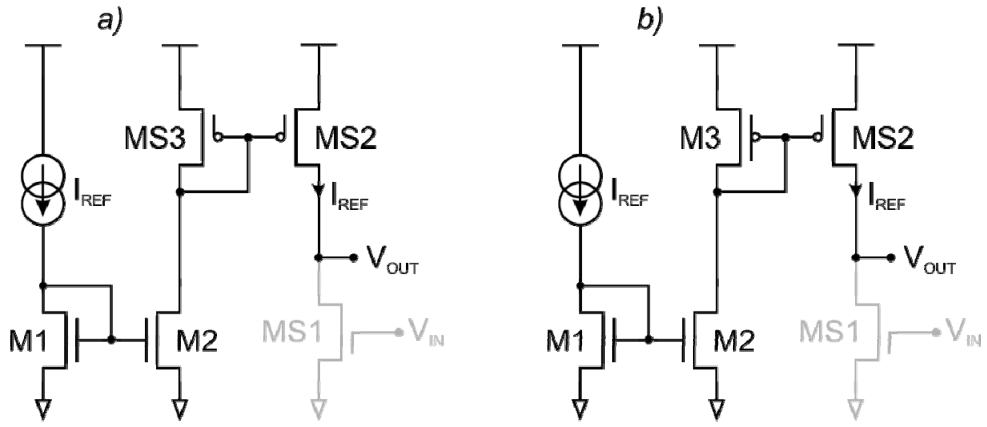


Figure 6.26. a) A quasi-constant current can be maintained through the gain device (MS1) irrespective of temperature by using a SGT current mirror. b) If the current through MS1 needs to be temperature dependent, then the p-type current mirror is formed of a FET and a SGT.

6.4.3. Self heating effects in current mirrors and gain stages

Seeing as the drain current of the SGT is temperature activated, self heating effects need to be assessed and understood in order to minimize their impact in circuit scenarios. The temperature coefficient of the drain current can be very high, especially in devices with barrier "raising" implants (see Section 5.6). Any local temperature changes may lead to deviations from the designed circuit performance.

The worst case scenario occurs when matching currents are generated on devices with different geometries and implicitly different current densities through the source. In current mirrors, however, self heating is not, in principle, a grave problem, because current copying and multiplication usually happens by changing the aspect ratio of the device. (When designing with FETs, one has access to both W and L as parameters for current multiplication in "1:M" mirrors. By construction, in SGTs the source-drain

separation, **d**, is not a design parameter, so the designer can only change the width, **W**, or the number of identical devices connected in parallel, **M**, to create "1:M" current ratios when copying currents.) For "1:M" mirrors built with SGTs the current density stays roughly the same as one of the devices is made M times wider. For even better heat distribution, the perimeter effects can be negated if M identical devices are connected in parallel.

Applying common analog design rules and running the devices at low current density ensures predictable behaviour even when self-heating plays a significant role. Nevertheless, low current density may prove detrimental to high frequency performance (See Section 5.8), therefore application-specific trade-offs need to be made.

6.5. Power dissipation in SGT devices

A key improvement in the performance of the SGT over that of an equivalent FET is the very low saturation voltage. Apart from improving output voltage swing in gain stages, this allows for significantly lower *d.c.* power dissipation in saturation. At the saturation voltage, $\mathbf{V_{SAT}}$, the *d.c.* power dissipation is:

$$P = V_{SAT} \cdot I_D . \tag{7.5}$$

To illustrate the scale of the power saving, a device was operated in SGT and FET mode, by swapping the source and drain. The characteristics are shown in Figure 5.1. Figure 6.27 illustrates the ratio of the power dissipation in the SGT at $\mathbf{V_{SAT1}}$ to that in the FET at $\mathbf{V_{SAT}} = \mathbf{V_G} - \mathbf{V_T}$.

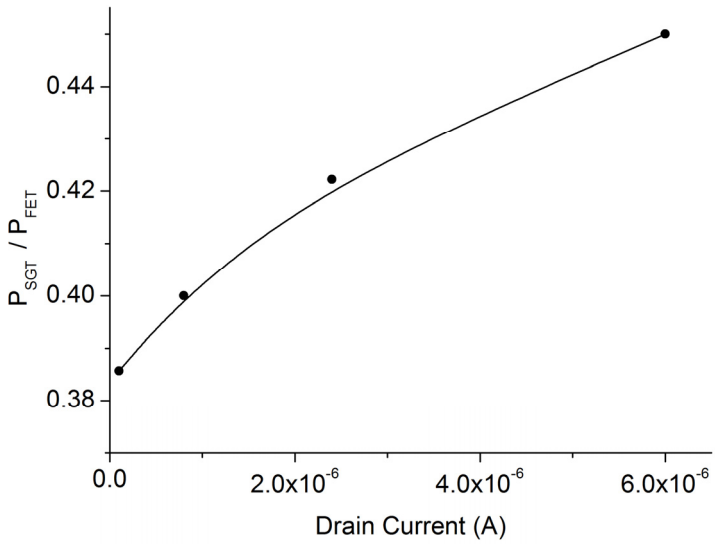


Figure 6.27. The ratio of power dissipation at saturation for the SGT and FET devices in Figure 5.1.

It can be seen from the above that power savings of over 50% are possible when using SGTs, in addition to the high output impedance which is also a desirable attribute of this type of device.

The effective value of $\mathbf{V_{SAT1}}$ will depend, of course, on a number of factors such as doping in the semiconductor, barrier changing implant concentration, conductance of the parasitic FET and temperature (see Sections 5.2.2 and 5.7) and that will influence the power consumption, however, with careful optimization, power reductions of over 75% should be possible.

6.6. Conclusions

Computer simulations have been performed in order to highlight the tolerance to process variability of the drain current in Schottky Barrier Source-Gated Transistor. The results show that the current is immune to source-drain separation (**d**) variations and has reduced source length sensitivity, but good control of insulator thickness and Schottky barrier height is needed. Current uniformity can be optimized further by choosing suitable biasing, adapted to the technology used, which partly negates the effects of semiconductor thickness variations.

The potentially high temperature coefficient of the drain current, which is undesirable in most circuit applications, can be turned to an advantage when designing precision temperature sensors in thin-film circuits. In a limited temperature range and for constant bias current, the gate voltage of the SGT will change fairly linearly with temperature. By varying the gate bias or the concentration in the barrier changing implant, the temperature coefficient can be tuned. Sensors with high precision can be fabricated using cost-effective electronic technologies and integrated at critical points of large-area circuits. It should be noted, however, that low temperature coefficients can be obtained together with high on-currents for devices in which the source barrier has a low value.

SGT characteristics such as low saturation voltage and high output impedance make it an ideal device for analog circuits, an area which historically has been out of the reach of standard FETs in cost-conscious thin-film technologies. Simple current mirrors and gain stages have been investigated in order to highlight the comparative strengths of SGT circuits: larger output voltage swings, better amplification and accurate current copying can be obtained.

Chapter 7. Conclusions and future work

7.1. Summary and conclusions

Polysilicon source-gated transistors (SGTs) have been fabricated on glass and their performance evaluated against that of the standard thin-film field-effect transistor (TFT FET). These structures have a Schottky source and an ohmic contact. By changing the polarity of the current, the characteristics of an SGT and those of a FET can be evaluated on a single device platform.

The polysilicon SGTs show all the characteristics of this type of electronic device: low saturation voltage, high output impedance in saturation, absence of kink effect and a saturated drain current which is independent of source-drain separation and very weakly dependent on source length. The value of the barrier lowering constant, α, is in the range of 2-3nm and agrees well with the theory. By connecting both drains at the same time, the current exactly doubles, proving that for source lengths in excess of 2μm, there is no current sharing between the two halves of the device. This allows for high current density devices to be fabricated and the SGT design to be optimised with drains on either side of the source.

The threshold voltage of these devices can be changed using bulk implants. Using barrier modification implants, the activation energy of the current can be controlled, allowing fabrication of high current, weakly temperature-sensitive devices. Conversely, high temperature coefficients of the current are obtained if a barrier raising implant is used, a feature which could be used in temperature sensors. The barrier changing implants also impact the frequency characteristic of these SGTs. It should be possible to operate the high current devices in a double-drain configuration at well over 200MHz.

Due to the very high output impedance in saturation, the intrinsic gain of these devices can be very large (up to 10,000). It was found that the gain characteristic is insensitive to temperature variations and is highest around the voltage at which the semiconductor is pinched off at both ends ($\mathbf{V_{SAT2}}$).

The frequency, gain and temperature characteristics of the polysilicon SGTs suggest that these devices are suitable for use in analog and mixed signal large area electronic circuits which are very hard to realise with conventional FETs.

A novel structure called the bulk-unipolar source-gated transistor (BUSGT) has been described and simulated using Silvaco Atlas. The barrier is formed by ion implantation underneath an ohmic metal-semiconductor contact. This form of barrier is much easier to pull down using the gate field, so devices can be designed to have a high barrier (to limit off-current) which is very soft (leading to high current output in the on-state). When the barrier is decreased to low values by the gate action, a low temperature coefficient of the drain current is obtained.

The utility of source-gated transistors to analog thin-film transistor circuits has been assessed using several basic circuit blocks. Highly sensitive temperature sensors can be designed using the SGT as the sensing element. SGT gain stages and active loads benefit from the high output impedance that the device shows when compared to the standard FET. The SGT architecture was also found to be very robust and tolerant to process variations. Insulator thickness and source barrier height, however, need to be well controlled.

Overall, the SGT has been proven to be a very versatile device. Its performance is easily tuned during processing to produce high current and high speed, high temperature coefficients or high gain. Its relevance to analog and mixed signal is evident due to several factors.

Firstly, the technological process required for SGTs requires minimal changes from the standard thin-film transistor technology. Indeed, with adequate design, both SGTs and TFT FETs can be created on the same substrate and integrated in the same circuit, and SGT devices can be made to operate both as SGTs and FETs depending on current polarity.

Moreover, applications such as precision operational amplifiers along with other analog functions are difficult to implement in polysilicon and other technologies specific to large area electronics, due to variations during processing, poor quality of the semiconducting material and TFT device physics. The SGT allows fast operation at high gain, with repeatability and robustness. It opens up the possibility of integrating high performance analog blocks into the panel of advanced large area electronic circuits.

7.2. Outlook and future work

In the near future, extensive frequency and transient measurements will be undertaken on the polysilicon structure, aimed mainly at assessing the correlation between the theoretical cut-off frequency and what can be achieved in practice. This study is particularly interesting, as misalignments could introduce deleterious overlap capacitances.

The study on the polysilicon SGTs will continue with comparisons between different geometries. At present, the width of the polysilicon island seems to affect the threshold of the device and the design of the source window (specifically if it overlaps the semiconductor or not) yields different results, particularly in terms of barrier lowering constant and threshold. The next batch of devices will feature a thinner oxide which should increase transconductance and subthreshold slope and reduce gate voltage magnitude. A deeper investigation of the SGT off-state is planned as well.

Also of interest is the fabrication of demonstrator circuits for temperature sensors, current mode logic and signal amplification using SGTs in polysilicon, amorphous silicon and organic materials and the comparison with equivalent FET circuits.

The project will continue with further studies into the technology and performance of SGTs with bulk unipolar barriers and field-emission sources for zero-temperature coefficient of the drain current.

Finally, creating design rules and SPICE models for every type of device would allow easy integration into the circuit design flow. This is seen as a key step in getting this device accepted by the Electronics Industry.

Appendix 1. Definition of a disordered material in Silvaco Atlas

In a polysilicon-FET example, Silvaco write [91]:

```
material region=2 material=silicon mun=300 mup=30
defects nta=1.12e21 ntd=4.e20 wta=0.025 wtd=0.05 \
  nga=1.e18 ngd=3.e18 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16
```

The first line defines the material as crystalline silicon. The subsequent statement is one of two ways of defining the density of defect states, and describes the maximum and the characteristic decay, for Gaussian and exponential tail distributions. The `sig***` parameters represent the capture cross-sections for Gaussian or exponential tail distributions, acceptor or donor states for electrons or holes, respectively.

The resulting density of states is represented in Figure A.1.

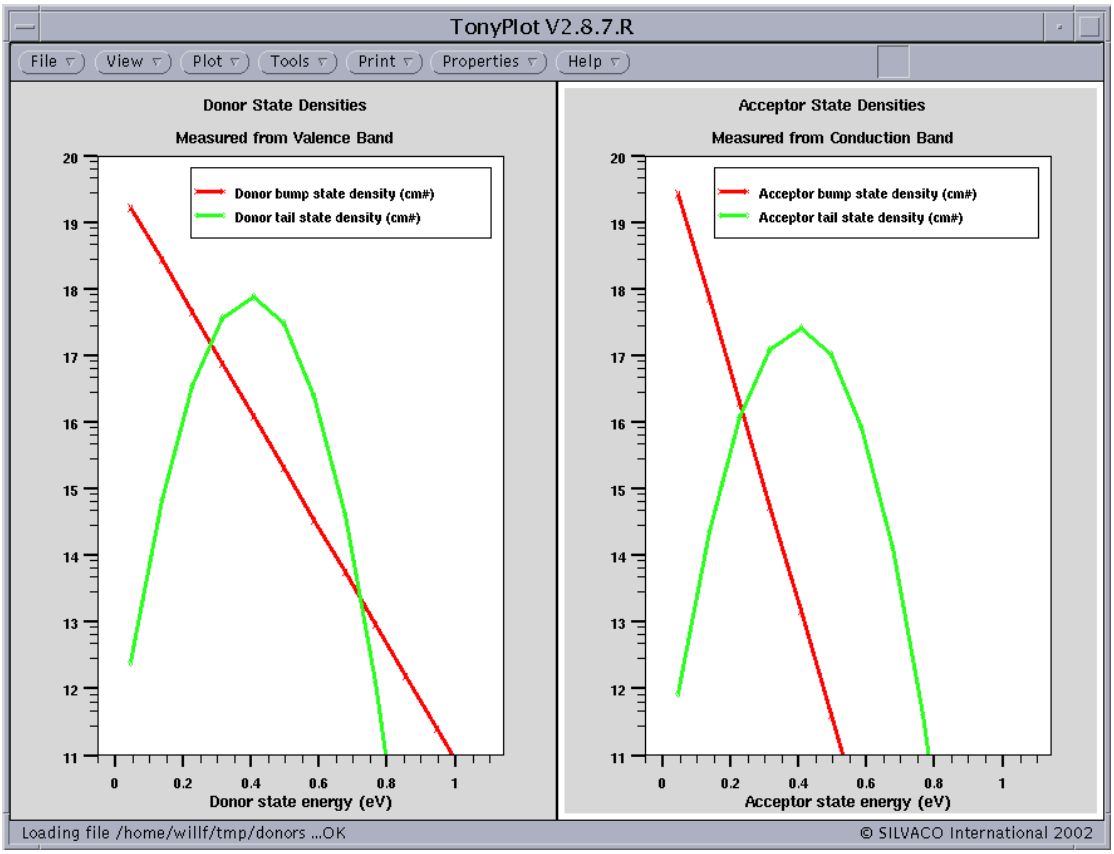


Figure A.1. Syntax guide to define two tail states and two gaussian distributions. NGA and NDG are the integrated values of the Gaussian distributions. Gaussians are entered on energies EGA and EGD respectively, reproduced from [91].

Appendix 2. Silvaco Atlas code example

```
################# Atlas device description ###################

    #  **************** parameter definition ****************

    go internal

    # Set up 7 Device Specifications
    #
    set SLength=10
    set SDgap=0.5
    set DevStart=0
    set DLength=0.5
    set GLength=$"SLength"+$"SDgap"
    set StepWidth=0.1
    set tsi=0.03
    set toxide=0.050
    set tglass=0.05
    set tdope=0.01

    # Material bandgap
    set EpsSi=2.5
    set EgSi=2.5
    set PhiS=0.35
    set GWfun=5
```

```
set Vsupply=8
set Vss=0
set Vinput=5.5
set Rload1=34350
set Rload2=$"Rload1"
set Vref=4
set Wsgt1=3700
set Wsgt2=$"Wsgt1"
set Wsgt=7200
set Vdelta=0.5
set Vhigh=$"Vinput"+$"Vdelta"
set Vlow=$"Vinput"-$"Vdelta"
set Ccoup=6e-14


#  **************** SGT simualation ***************

go atlas

# define models

mesh
#
x.m         l=0   spac=0.15
x.m         l=1   spac=0.05
x.m         l=1.3 spac=0.01
x.m         l=2   spac=0.15

#
#
y.m         l=-0.1     spac=0.05
y.m         l=0   spac=0.005
y.m         l=0.03     spac=0.01
y.m         l=0.08     spac=0.01
y.m         l=0.15     spac=0.05
y.m         l=0.25     spac=0.05

#
#
#  **************** regions ****************
#             1=oxide  2=silicon 3-oxide
```

```
#
region       num=1  y.max=0.    oxide
region       num=2  y.min=0.    y.max=0.02   silicon
region       num=3  y.min=0.02   oxide

#  **************** electrodes ****************
#    1=gate  2=substrate  3=source  4=drain
#
elec  num=1  x.min=0    x.max=1.3  y.min=0.08 y.max=0.08 \
name=gate
elec  num=2  substrate              name=substrate
elec  num=3  x.min=0.   x.max=1.    y.min=0.   y.max=0.  \
name=source
elec  num=4  x.min=1.3 x.max=2 y.min=0.   y.max=0.   \
name=drain
#
#  **************** doping profiles  ****************

doping     reg=2  uniform conc=1.e14 p.type
#doping     reg=2  uniform conc=1.e20 p.type x.right=1 \
char=0.3
doping     reg=2  uniform conc=1.e18 p.type x.left=1.3 \
char=0.3
#
#
#     Set parameters for polysilicon
#
material material=silicon mun=0 mup=0.0033 vsatp=5e9 \
vsatn=5e9 nc300=1e19 affinity=2.5  nv300=1e19 eg300=2.5 \
taun0=1e-8 taup0=1e-8 PERMITTIVITY=4.0

mobility material=silicon vsatp=5e8 vsatn=5e8 PFMOB.P \
EOP.PFMOB=3e5

#
defects nta=1.12e21 ntd=4.e20 wta=0.025 wtd=0.05 \
  nga=1.e18 ngd=3.e18 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 \
  sigtdh=1.e-16 siggae=1.e-16 siggah=1.e-14 \
  siggde=1.e-14 siggdh=1.e-16

contact name=source SURF.REC BARRIER ALPHA=4e-7 \
workfunction=4.5
```

```
contact name=drain workfunction=5
contact name=gate workfunction=5

#  **************Atlas analysis parameters  *************

models  temp=300

method  newton
#trap
# method for transient analysis
#method  newton 2ND TAUTO AUTONR trap
solve init
output E.FIELD BAND.PARAM E.MOBILITY E.VELOCITY \
CON.BAND VAL.BAND QFN
save outf=sgt.str
log outf=sgtft.log


################# SPICE circuit description ##################

go atlas
.begin

Vdd Vdd 0 0 pulse 0 12 5u 5u 2000u 5045u 51m

vin1 in1 0 0 pwl 0 0 5u 0 100u 6 120u 6 120.01u 6.1 \
121u 6.1 121.01u 5.9 122u 5.9 122.01u 6.1 123u 6.1 \
123.01u 5.9 124u 5.9 124.01u 6.1 125u 6.1 125.01u 5.9

vin2 vdd in2 0 pwl 0 0 5u 0 100u 6 120u 6 120.01u 6.1 \
121u 6.1 121.01u 5.9 122u 5.9 122.01u 6.1 123u 6.1 \
123.01u 5.9 124u 5.9 124.01u 6.1 125u 6.1 125.01u 5.9

R1 out1 0 0.12meg
R2 out2 0 0.12meg

I1 Vdd tail 0 pulse 0 100u 5u 5u 2000u 5045u 51m

### Integration of Atlas Device in SPICE Circuit - part 1 ###

atft1 out1=drain in1=gate tail=source infile=sgt.str \
width=345
```

```
    atft2 out2=drain in2=gate tail=source infile=sgt.str \
    width=345

    #     End of circuit description
    #

################## SPICE circuit analysis ##################

    .numeric lte=0.05
    .options print noshift
    #
    #.load infile=sgtdc1
    .log outfile=sgttran
    .save outfile=sgttran
    #
    .tran  .01u .13m
    .print tran

    .end

### Integration of Atlas Device in SPICE Circuit - part 2 ###

    material device=atft1 material=silicon mun=0 mup=0.0033 \
    nc300=1e19 affinity=2.5 nv300=1e19 eg300=2.5 taun0=1e-8 \
    taup0=1e-8 PERMITTIVITY=4.0

    material device=atft2 material=silicon mun=0 mup=0.0033 \
    nc300=1e19 affinity=2.5  nv300=1e19 eg300=2.5 taun0=1e-8 \
    taup0=1e-8 PERMITTIVITY=4.0

    contact     device=atft1 name=source  \
    workfunction=$"EpsSi"+$"EgSi"-$"PhiS" SURF.REC \
    BARRIER ALPHA=4e-7
    contact     device=atft1 name=drain  \
    workfunction=$"EpsSi"+$"EgSi"
    contact device=atft1 name=gate workfunction=$"GWFun"

    contact     device=atft2 name=source \
    workfunction=$"EpsSi"+$"EgSi"-$"PhiS" SURF.REC \
    BARRIER ALPHA=4e-7
    contact     device=atft2 name=drain \
    workfunction=$"EpsSi"+$"EgSi"
```

```
contact device=atft2 name=gate workfunction=$"GWFun"

models device=atft1 fermi srh temp=300 print
mobility device=atft1 PFMOB.P EOP.PFMOB=3e5

models device=atft2 fermi srh temp=300 print
mobility device=atft2 PFMOB.P EOP.PFMOB=3e5

quit
```

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