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First Order Bragg Grating Filters in Silicon on Insulator Waveguides

By

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A Thesis presented to the Faculty of Engineering and Physical Sciences, University of Surrey, for the award of Doctor of Philosophy (PhD.)

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Abstract

The subject of this thesis is the design; analysis, fabrication and characterisation of first order Bragg Grating optical filters in Silicon-on-Insulator (SOI) planar waveguides. It is envisaged that this work will result in the possibility of Bragg Grating filters for use in Silicon Photonics. It is the purpose of the work to create as far as is possible flat surface waveguides so as to facilitate Thermo-Optic tuning and also the incorporation into rib-waveguide Silicon Photonics.

The spectral response of the shallow Bragg Gratings was modelled using Coupled Mode Theory (CMT) by way of RSoft Gratingmod ™. Also the effect of having a Bragg Grating with alternate layers of refractive index 1.5 and 3.5 was simulated in order to verify that Silica and Silicon layered Bragg Gratings could be viable.

A series of Bragg Gratings were patterned on 1.5 micron SOI at Philips in Eindhoven to investigate the variation of grating parameters with a) the period of the gratings b) the duty cycle (or mark to space ratio) of the gratings and c) the length of the region converted to Bragg Gratings (i.e. the number of grating period repetitions).

One set of gratings were thermally oxidised at Philips in Eindhoven (this was to simulate the effects of oxidising Porous Silicon) and another set were ion implanted with Oxygen ions at the Ion Beam Facility, University of Surrey. The gratings were tested and found to give transmission minima at approximately 1540 nanometres and both methods of creating flat surfaces were found to give similar minima. Atomic Force Microscopy was applied to the grating area of the Ion as Implanted samples in the ATI, University of Surrey, which were found to have surface undulations in the order of 60 nanometres.

Key words: Silicon-on-Insulator (SOI), Bragg Grating filter, Coupled Mode Theory (CMT), Thermo-Optic (TO).

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1 Introduction

Primitive means of communication included torches, semaphore, and photo phone [1] and had low communication capacity. Analogue electrical and microwave communications are improvements but carry considerable loss and come somewhat expensive in the usage of copper wiring.

In the modern world there is an increasing need for high speed, high bandwidth communication. This is to address the demand for voice, music, video and digital communication not just between countries but also continents as globalisation progresses and the number of consumers increases. Transmission rates over the last 100 years have improved due to the invention of (1860) telegraph, (1900) telephone, (1940) coaxial cable, (1960) microwave and (1990) optical amplifiers (erbium doped fibre amplifiers [1].

The invention of the laser in 1960 (Maiman: Ruby Laser [2]) provided a radiation source with potential for use as an information carrier. Also the increasing usefulness of fibre optic cable through the seventies with reducing loss over long distances led to the realisation of intercontinental fibre optic communications. Present day optical fibres have a transmission rate capacity in excess of terabits per second and as they have the lowest attenuation in the 1.5 micron wavelength window, such wavelengths are used as long distance carriers. Wavelength Division Multiplexing (WDM) increases the carrying potential of a single fibre and is thus used in modern telecommunications systems.

Copper wiring as well as being expensive, suffers from technical disadvantages: for example at high frequency or bit rate the wires tend to radiate electro-magnetic radiation which causes a loss of energy from the wire. This loss can lead to the possibility of electronic eavesdropping. Glass fibres for fibre optics on the other hand are derived from Silica a commonplace and cheap material. Also they tend to be secure as optical tapping is easily detectable. Thus for some time communication across the Atlantic, for example, has been via optical cable. A contribution to making the situation more optically ergonomic was the development of the Erbium Doped Fibre Amplifier (EDFA) in the early 1990's which meant that optical signals could be

amplified without electronic conversion [3]. Erbium doping creates intermediate energy level transitions which make amplification possible. Figure 1 shows the energy states in an EDFA: the optical pump transfers the electrons to the highest state I11/2 from this they rapidly decay to the intermediate metastable state I13/2. The passage of a photon of just the right energy stimulates return to the ground state I15/2 and photonic amplification occurs [4].

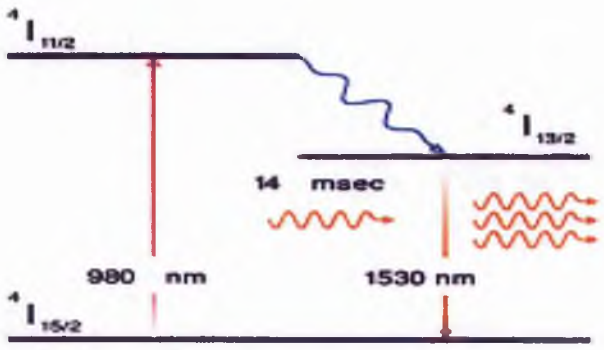


Figure 1 Energy level diagram of EDFA [4].

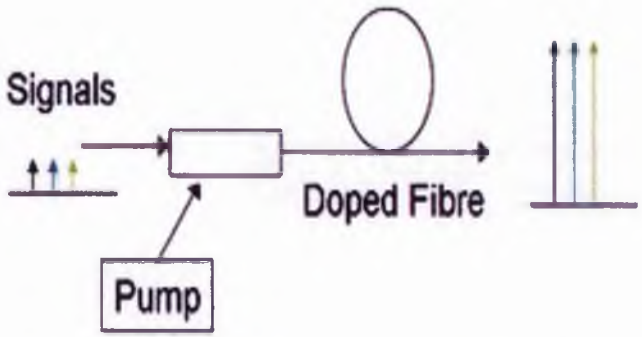


Figure 2 Schematic of an optical fibre amplifier [3].

Figure 2 shows the schematic of an optical amplifier: the three signals are combined with a pump signal and passed into a doped fibre loop where the amplification occurs and the three signals pass on down the fibre in the same direction but larger in amplitude. Electronic level broadening occurs with doping Rare Earth ions into glass and this causes the range of amplifiable wavelengths to be broadened and thus a single amplifier can be used to amplify all signals carried on a fibre [3, 5]. There is a limit to what can reasonably be achieved with fibres due to cost both for installation

and extraneous components and this tends to limit its use to intercontinental or long distance applications. Researchers have been considering for several decades the possibility of all optical networks whereby expensive and time consuming conversions from photonic to electronic signals could be avoided or at least kept to a minimum. The possibility of integrating all the necessary components (from the telecommunications point of view) onto one single chip has for some time been the goal of much of opto-electronics.

However, the means of gaining optical integration was an enigma for optical researchers. For some time it was thought that Lithium Niobate would provide the key since its optical properties were very convenient in terms of rotating the plane of polarisation of laser light under applied electrical voltage. Unfortunately it proved initially difficult to machine and provide wafers similar to Silicon and also gave complicated circuits for manufacturing and so this has caused a reduction in interest.

Silicon would initially seem an unlikely candidate since it has no linear electro-optic effect for modulation and cannot provide a conventional semiconducting light emitter in the manner of III-V or II-VI compounds (e.g. Gallium Arsenide or Zinc Selenide). However, Silicon does have noticeable second order optical characteristics and this has led to the recent development of Raman amplification and lasing [6-16].

A Raman amplifier is an optical amplifier based on Raman gain [11]. The Raman active medium is usually an optical fibre, although it can also be a bulk crystal, for example. An input signal can be amplified while co or counter propagating with a pump beam, the wavelength of which is typically a few tens of nanometres shorter. For Silica fibres, maximum gain is obtained for a frequency offset of about 10 to 15 THz between pump and signal, depending on the core composition.

Compared with Erbium Doped Fibre Amplifiers, a Raman amplifier's typical features are [12]:

- Potential for generating gain in very different wavelength regions provided that a suitable pump source is available.
- Tailoring of the gain spectrum by using different pump wavelengths simultaneously.
- Requires high pump power (possibly raising laser safety issues) and high pump brightness, but can also generate high output powers.

- Requires longer fibre lengths (but transmission fibre in a telecom system may be used).
- Potentially lower noise.
- Fast reaction to changes of the pump power (particularly for co-propagating pump).

As well as these developments in optics developments in electronics are of interest at this stage. Silicon-on Insulator (SOI) has long been a matter of interest to the electronics trade since it produces high quality radiation hardened components which have lower leakage and stray capacitance than their bulk Silicon counterparts and thus considerable money and research have combined to yield the present Ultra Large Scale Integration (ULSI) that we increasingly have today.

Problems facing this ULSI are speed and power dissipation and the solution to this may well be strained Silicon on SOI (for a discussion of this, please see **The Present and The Future** in Chapter Two) in which case the SOI share of the market for ULSI may well increase dramatically from its present few per cent.

Once this has occurred some optical integration may well be necessary in terms of optically induced Wavelength Division Multiplexing both at the inter-chip level and ultimately at the intra-chip level to avoid information bottlenecks.

To further hybridise optics with this ULSI will not be easy but as long as the optics researchers can produce an easy 'bolt-on' for what the electronics engineers are already making, the possibility of 'doing business' between the two groups must exist, and this is an exciting prospect especially with the eventual prospect of all optical hardware somewhere in the overview.

One of the great advantages of SOI from the point of view of Silicon Photonics is the large difference in refractive index between the Buried oxide (BOX) layer of Silica and the surrounding Silicon. This means that with a waveguide above the BOX a very high degree of optical confinement may be achieved. This gives rise to the possibility of considerable miniaturisation compared with other forms of guiding and this can improve device performance and cost efficiency [17].

Wavelength Division Multiplexing (WDM) has long been recognised as being useful in terms of addressing the need for increasing bandwidth in the telecommunications

sector since it means that several signals can be sent down the same optical fibre. One way of providing the multiplexing and demultiplexing that is required for WDM is to use Bragg Gratings at each end, whether it be of a fibre or a waveguide connection. More attention is being placed on systems where WDM takes its place as a part of an all optical network since it was to be expected that this would result in speed and bandwidth benefits.

Bragg Gratings

Some of the above WDM components such as add-drop filters, wavelength routers, Fabry-Perot cavities and tuneable filters can be achieved using Bragg Gratings and it is the purpose of this project to design, fabricate, test and characterise flat surfaced Bragg Gratings in SOI. Two different techniques have been chosen for this and an attempt at comparison will be made.

Project Overview

I started my project by examining the propagation of light down a rib waveguide using Beamprop ™ by way of simulation. Also using simulation, modality was checked for a 1.5 micron rib waveguide with Beamprop ™ and thirdly the expected reflectivity/transmission from a shallow grating was modelled with Gratingmod ™. Beamprop can analyse TM/TE optical propagation down rib waveguides and Gratingmod can analyse optical reflection and transmission down waveguide structures with applied gratings. Both are based upon the principles of coupled mode theory. It became apparent that 75nm of grating depth approximately was required to produce 90% reflectivity and this was modelled using Suspre. Suspre is effectively a graphic representation of skew Gaussian implantation tables derived for various types of ions implanted into different elements or compounds based on the work of Lindhard et al and Dearnalay et al [42 and 43 respectively]. Srim ™ was also used as a check and this is based upon a Monte Carlo analysis of ion bombardment.

Ordinary Silicon wafers were implanted with Oxygen at Nodus at Surrey University and as-implanted and annealed samples were investigated using ellipsometry which gave evidence of Oxide creation. Two 1.5 micron (1 micron BOX) SOI wafers were obtained and masked, using Silicon Nitride, with a suitable grating pattern at Philips in Eindhoven in Holland. Of these one was ion implanted at Surrey and one was thermally oxidised at Philips to simulate the formation of a flat surface grating by way

of porous silicon techniques. This was to try and make a comparison of the two possibilities of fabricating flat gratings in SOI. The wafers were cleaved at Philips to provide planar surface gratings which were then investigated at Surrey.

Chapter Layout

This thesis is organised into the following chapters describing the design, fabrication and measurement of first order gratings on 1.5 micron SOI.

Chapter 2 will provide a review of differing Bragg Grating filters especially implemented on waveguide structures, as well as reviewing situations in WDM, Ion Implantation and Electronics.

Chapter 3 will describe the theory of Bragg Gratings.
Chapter 4 will detail the design and analysis of Bragg Gratings.
Chapter 5 will discuss the different fabrication techniques.
Chapter 6 contains techniques for optimising the results from the grating samples.
Chapter 7 contains the results achieved.
Chapter 8 contains the conclusions from the work relating to the various techniques and recommendations for the future based on the current work.

Chapter 9 contains the suggestions for future work.

Finally Chapter 10 contains the index to all the references in the text and literature review.

2 Literature Review

2.1 Silicon on Insulator

Silicon on Insulator (SOI) is a layered structure consisting of a thin layer of Silicon which is created on an insulating substrate which is usually Sapphire or Silicon Dioxide. Thus SOI circuits differ from generic CMOS (Complementary Metal Oxide Semiconductor) circuits in that their Silicon junction is above an electrical insulator. This process reduces the amount of electrical charge that the transistor has to move during a switching operation: increasing speed (up to 15%) and reducing switching energy (up to 30%) over CMOS based chips and hence power consumption.

SOI devices are usually latch up (where both complementary output transistors conduct causing either malfunction or destruction of the device) resistant and there is a reduction in leakage current: very useful for low power circuit design. SOI chips also reduce the soft error rate, which is data corruption caused by cosmic rays and natural radioactive background signals. Finally CMOS chips have impurities: called dopants added to allow for charge storage via capacitance, SOI chips are not doped which reduces the capacitance allowing for faster and cooler operation. (In semiconductor production, doping refers to the process of intentionally introducing impurities into an extremely pure (also referred to as intrinsic) semiconductor in order to change its electrical properties. For the group IV semiconductors such as silicon, germanium, and silicon carbide, the most common dopants are acceptors from group III or donors from group V elements (Group number refers to the Roman numerals of the columns in the periodic table of the elements). Boron, arsenic, phosphorus and occasionally gallium are used to dope silicon. Boron is the p-type dopant of choice for silicon integrated circuit production, since it diffuses at a rate which makes junction depths easily controllable. By doping pure silicon with group V elements such as phosphorus, extra valence electrons are added which become unbonded from individual atoms and allow the compound to be electrically conductive, n-type semiconductor. Doping with group III elements, such as boron, which are missing the fourth valence electron creates "broken bonds", or holes, in the silicon lattice that are free to move. This is electrically conductive, p-type semiconductor.)

Silicon on Insulator dates back to the early 1960's with the first development of **Silicon on Sapphire (SOS)** [18, 19].

Silicon on Sapphire is a hetero-epitaxial wafer that consists of a thin layer of Silicon grown on a Sapphire wafer using Chemical Vapour Deposition (CVD) epitaxial method where the Silicon atoms are assembled one by one on the surface of the Sapphire wafer. Because the crystal structure of Silicon is similar to Sapphire (non-conformity between the crystal lattice of silicon and sapphire being circa 12.5 % [18, 19]) the SOS structure appears to be one crystal with a strong molecular bond between the two materials.

SOS is a part of the Silicon on Insulator (SOI) family of CMOS (Complementary Metal-Oxide Semiconductor) technologies. Initially the SOS technology was developed for use in military and space applications requiring high temperature and 'radiation hardened' chips. But commercial use of them started from when the first CMOS circuits were formed. A typical manufacture of SOS would involve the growth of high purity artificial Sapphire crystals. The Silicon is then deposited by the decomposition of Silane gas (SiH_4) on heated Sapphire substrates. Silicon on Sapphire is popular with radiation hard applications in the military and aerospace industries. Apart from the expense, the electrical properties of SOS have a tendency to degrade as a result of the high dislocation density due to the lattice mismatch between the Silicon and the Sapphire hence SOI designers looked to alternatives for the top end market.

Today bulk silicon CMOS technology is the dominant semiconductor technology for microprocessors, memories and Application Specific Integrated Circuits (ASICS). The main advantage of CMOS over other technologies (e.g. Gallium Arsenide and bipolar technology) is the much smaller power dissipation and especially when static: power is only used during switching and this allows for more gate integration on a single I.C. and thus better performance.

Wafer Bonding

Silicon wafers can be bonded together. This provides a route to fabricating SOI structures. The wafer which will ultimately become the substrate is oxidised, creating

the desired BOX thickness. A second (donor) wafer which will ultimately become the site for active devices is pressed into close contact with the first wafer and the sandwich is heated in a furnace. Bond strength generally increases with temperature. Finally the second wafer is thinned to leave a final Silicon layer of the desired thickness. This thinning can be done in several ways. A major amount of Silicon from the donor wafer can be removed by etching or grinding. Etching may be rendered selective by implanting an etch stop prior to bonding.

BESOI (bond and etch back SOI)

Besoi was introduced in the early 1970s and involves the oxidation of the surface of two silicon wafers, the formation of a chemical bond between the matching oxide faces and the etching and polishing of the top wafer to give the SOI [20]. Wafer bonding is the preferred means of producing thick SOI: where the BOX and Silicon over layer are thicker than 1 micron [20].

Smartcut

The favoured manner to create SOI material through wafer bonding makes use of mechanical stress to cleave the undesired portion of the donor wafer.

A silicon wafer is taken and thermally oxidised. Next hydrogen is implanted at high density (c. 10^{17} cm^{-2}) at a depth beneath the oxide layer. Finally the wafer is bonded to a second wafer and thermal processing is undertaken at 600 and 1100 degrees C to split the first wafer at the hydrogen implanted depth and improve the bonding between the two wafers [20]. Polishing may be necessary after cleaving to restore flatness.

Simox

Silica was inexpensive but difficult to bond to Silicon due to crystalline differences until the development of **Simox** (Separation by IMplantation of OXygen). Oxygen can be implanted at high energy into a Silicon substrate at a high enough dose that subsequent high temperature annealing forms an Oxide layer underneath the surface

layer of Silicon with both layers forming a molecular bond. The Oxide is an insulator thus producing the Silicon on Insulator structure. This is especially of use for thin SOI material (where BOX and Silicon over layer thickness is less than 1 micron). Ion implantation of Oxygen or Nitrogen into Silicon at doses high enough to produce stoichiometric Silicon Dioxide and Silicon Nitride has been reported since the 1960's (Watanabe and Tooi 1966 and Pavlov and Shitova 1967 [21, 22]).

Such implants require extremely high doses compared to implanting dopants. For example to dope Silicon heavily requires a volume concentration of 10^{18} ions cm^{-3}, which substitutes one dopant atom for roughly 1000 Silicon atoms. For typical I.C. dimensions this requires a dose per area of 10^{15} ions cm^{-2}. In contrast a stoichiometric Oxide dose would be 1000 times greater [23, 24].

The structure resulting from such a high dose implant of Oxygen depends strongly upon the dose and energy of the implant and the temperature of the wafer during implantation. As the dose increases Oxygen builds up to the solubility limit. Further increases result in the formation of disconnected islands of Silica [23, 24]. These islands may form at the surface (lower implant energy) or below the surface (higher energy).

In conventional ion implantation the ions damage the Silicon crystal structure, typically heavy doping is capable of creating a crystalline to amorphous transition. As a result, following implantation the wafer is annealed at temperatures of 900 to 1100 degrees and the crystal structure is re-established by a process called Solid Phase Epitaxy (SPE). This process is driven by the lower free energy of the crystalline state compared to the amorphous, and depends on the presence of a crystal template (the deeper bulk Silicon) in intimate contact with the by now amorphous surface layer. However with Simox the BOX prevents SPE and so the damage caused by the implant must be healed (at least in part) during the implantation. This is achieved by performing the implant at about 500 degrees. The over layer contains significant damage but this can be corrected by subsequent annealing.

In 1978 Izumi, Doken and Ariyoshi of NTT fabricated a CMOS ring oscillator on SOI material prepared by implanting O^+ ions into Silicon [25]. They named the SOI material Simox. By 1982 NTT had demonstrated a 1k SRAM on Simox. A high current implanter was developed also in the late 1970's making Simox development

easier. This was followed by an improvement in annealing techniques. Also a gradual take-up by some of the famous names in electronics occurred as well as interest in terms of integrated optics [24]. Annealing at 1300 degrees was found to result in a flatter interface to the BOX. Also the structure of the Silicon over layer is improved [23, 25].

Optical annealing at 1405 degrees [26] improves these features further. Both the mobility and the solubility of Oxygen in Silicon increase with temperature. Small Oxide precipitates dissolve as the annealing temperature increases: tending to condense on the larger precipitates, an example of a process called Ostwald ripening [27]. At sufficiently high temperatures the only precipitate surviving is the BOX. To minimise the free surface energy the interface between buried Oxide and Silicon becomes planar and smooth.

The reason such a structure is of value in fabricating integrated circuits is that individual transistors can easily be isolated from each other and from the bulk substrate. Without the Buried Oxide (BOX) each transistor is connected to its neighbours and to the substrate electrically. While this electrical coupling can be minimised by careful doping to minimise electrical leakage currents, nevertheless there remain a variety of parasitic loss mechanisms. Replacing these back biased junctions with an insulator improves the isolation very significantly and several benefits accrue. First, it becomes easier to reduce transistor size and increase packing density since junction isolation requires wasting space. Furthermore with the most common transistor configuration CMOS latch up can occur; with close packing SOI makes this impossible. Second, once the transistors are well insulated from the substrate soft errors resulting from the adsorption of ionising radiation are reduced by many orders of magnitude. The reason is that the active Silicon surface is typically 0.2 micron thick compared to the 600 micron thickness of the substrate. In circuits constructed on bulk Silicon the carriers created by adsorption of ionising radiation anywhere in the substrate may diffuse into the active circuit. In circuits constructed on SOI only those carriers which are generated in the top active layer affect the circuit and a thin active layer minimises the problem. Thus SOI found an early market in military and aerospace applications. Third, because the transistors are better isolated from the substrate parasitic losses are reduced. This enables higher speed operation at lower power consumption. This speed/power consumption advantage opens three very

high volume consumer applications. One is communications equipment where the SOI speed advantage can substitute for some more expensive alternatives such as Silicon/Germanium or Gallium Arsenide for high frequency applications. A second is microprocessors for portable battery operated applications such as lap top computers where the reduced power consumption is critical. A third is in high end microprocessor applications such as network servers because of the speed advantage. Fourth, higher temperature IC operation is possible as a direct consequence of the isolation of the active device area by the BOX from electron and holes thermally generated in the substrate: once again only those created in the thin active region of Silicon affect the circuit.

SOI can be made hybrid with bulk Silicon by local implantation, for example CMOS logic on SOI with power switching on bulk i.e. providing yet further hardware modularisation and integration. Quite apart from electronic applications where the isolation of individual transistors from each other and from the substrate is the primary advantage, SOI technology has found applications in other fields. Since it is possible to etch Silicon and Silica with high selectivity, the presence of a buried Oxide permits one to fabricate complex microscopic three dimensional structures. Two applications for such structures are sensors and integrated optics [28, 29].

The Present and the Future

With technologies such as strained Silicon on SiGe on insulator and also sSOI (strained Silicon on Insulator, whereby the process of straining the Silicon increases carrier mobility and therefore improves the high frequency response) currently established as viable present/future options in SOI [30, 31] the future is looking good for SOI. Its increased speed compared with generic CMOS (Complementary Metal Oxide Semiconductor) and lower power dissipation and the other advantages outlined above should ensure increased take-up by industry in the run up to meeting the demands posed by ULSI (Ultra Large Scale Integration).

Strained silicon on insulator is the resultant of combining strained silicon with SOI thus combining the isolation, lower power dissipation and radiation hardening of SOI with the extra speed associated with improved carrier mobility that comes with strained silicon. The imposition of a SiGe layer and with a much thinner silicon layer underneath causes the strain and increases the speed by as much as 30%.

Strained Silicon on SOI provides high frequency benefits up to 30% increase in speed and lowers the output resistance, increasing the drive capability along with the usual SOI benefit of lower power dissipation.

Problems exist with straining such as the fact that holes under strain move at one third the speed of electrons and that Germanium's presence in the strained substrate is undesirable since it causes electrical degradation, however these seem to have been surmounted by the process of local epitaxial straining and the removal of the Germanium in the case of sSOI to leave strained Silicon on Silica. To date it is possible to retain the strain in the strained Silicon over layer to 70nm depth but no further and this will present logistical problems in terms of hybridising with Silicon Photonics but these are likely to be less significant than with other alternatives (e.g. problems with fine machining Lithium Niobate) [32, 33].

Companies of the calibre of IBM, AMD and Intel [34, 35, and 36] are pursuing an interest in sSOI and it cannot be long before market developments in consumer electronics occur and ensure its take up and have the predictable effect on SOI's section of the semiconductor wafer market with the knock-on reduction in SOI wafer unit cost. Attempts at updating SOS have been made [19] but these will still have the disadvantage of poorer integration possibilities and Sapphire degradation and SOS's high speed advantage has been all but wiped out by sSOI etc. The majority of the market is affected by companies of the order of Intel and TI but with modern integration requiring speeds of 4GHz and up, as well as the advent of 65nm process technology sSOI can provide the hardware whilst reducing problems with on-chip power dissipation and heat due to its low capacitance format. It is the author's contention that it is only a matter of time before SOI's (in one form or another) market share is considerably boosted due to the need for further/higher levels of integration and speed and the low power dissipation in SOI. Inter chip and intra chip communications can be achieved using WDM and two Bragg Gratings. From the author's perspective developments in electronics and research in Silicon Photonics are at an interesting stage and the coincidental breakthroughs in both areas of research could well see an early turning to hybrid Electronic/Silicon-Photonic devices to assist with speed/integration problems.

2.2 Surface and Buried Layers in Silicon by means of Ion Implantation.

2.2.1 Surface Layers

The formation of Silicon Dioxide by ion beam implantation into Silicon surfaces goes back to the 1960s.

Watanabe and Tooi [21] reported the creation of a surface layer of Silicon Dioxide after implantation of low energy reactive oxygen ions. They used p-type Silicon wafers with resistivity of 100 ohm-cm. The ion beam was accelerated to 60 keV. This gave a penetration depth of approximately 0.12 micron after irradiation with a current density of $20\mu A/cm^2$ for 200 minutes at sample temperatures ranging from room temperature to 300 degrees Celsius. They further proposed that if the ion energy was increased it would be possible to create a buried Oxide layer. The significance of this work is mainly the initiation of SiO_2 synthesis by ion implantation. Table 1 shows their comparison of IR absorption peak, Dielectric strength and constant and resistivity at 300 degrees K between their 150nm ion implanted film and thermally grown oxide and shows that with the exception of dielectric strength their oxide formed by ion bombardment was of similar quality to thermally grown oxide generally accepted at that time to be the best available silica.

Table 1 shows a comparison of thermally grown and implanted films [21].

	Ion Implanted Oxide	**Thermal Oxide**
IR Absorption Peak (μ)	**9.4**	**9.3**
Dielectric Strength (10^6 V/cm)	**7**	**8.5**
Dielectric Constant (300 degrees Absolute at 1 kHz)	**3.9**	**3.2**
Resistivity at 300 degrees Absolute (Ohm-cm)	**10^17**	**10^15~10^17**

Pavlov and Shitova performed similar work [22]; implanting into the (111) surface of n-type Silicon with a resistivity of 1 ohm cm. However, they gave no details on implantation dosage or energy. They reported on the formation of a surface Silica layer with the possible presence of Silicon and Silicon Monoxide.

Dylewski and Joshi created stoichiometric Silica by high dose O_2^+ implantation into Silicon wafers [37] and found that Infra Red (IR) transmission spectra consistent with SiO and SiO_2 were obtained depending on the ion dose (the latter at a dose of 10^{18} ions per cm^2 at 30keV). Post implantation annealing was found to release a substantial amount of bond strain and also rendered the Silica layers impervious to water attack. This was thought to be due to polymerisation of the SiO_4 tetrahedra, therefore reducing the porosity. In some previous papers there had been some ambiguity over what existed in the surface implant i.e. Silicon, Silicon Monoxide and/or Silica. This paper suggested that this may have been due to ion implantation dose variations.

The authors demonstrated the quality of their work by carefully defining their implantation parameters, which may well not have been well defined in earlier low dose ($<<10^{18}$ ions/cm.^{2}) surface layers created by implantation and by demonstrating that Silicon Monoxide and Silicon Dioxide were obtained in the surface layer dependant on the dose of Oxygen implantation ions and obtaining results consistent with their theory by both infra red transmission techniques and electron microscope reflection diffraction studies on their samples [38].

The same authors [39] implanted O_2 ions at 30keV and ion beam current density about 15 microampere/cm^2 and 10^{18} ions/cm^2 found that the dielectric breakdown properties of Silica films formed by implantation were similar to those created by thermal oxidation of Silicon but found a time dependence of the breakdown process and attributed this to Sodium ion contamination in the formed Silica films, unfortunately they gave no indication as to how the contamination had occurred.

At low current to voltage values the characteristics were ohmic (resistive) and at higher values the characteristics followed a power law consistent with space charge limitation. Annealing increased the resistivity of the films and moved the knee of the ohmic/space charge I-V characteristic to lower values and increased the slope of the space charge curve. Annealing also reduced the dielectric breakdown resistance and reduced polarity dependence of breakdown, possibly due to shrinkage reducing overall breakdown levels and Sodium ion dispersion within the crystalline structure, respectively.

Badawi and Anand [40] formed stoichiometric Silica in Silicon using $^{32}O_2^+$ ion implantation (i.e. implanting molecular, positively charged Oxygen at an atomic mass

unit of 16 since e.g. 18 can be used to create an Oxide marker layer). After annealing they found that the high dose implant produced a surface layer of Silica whereas the medium and low doses produced buried layers (high being 7, medium being 4 and low being $2.5x10^{22}$ ions/cm^3: peak volumetric concentrations of ions, the area dose being approximately 10^{17} O_2 ions/cm^2). The thickness of the films was found to be greater than that predicted by the theory derived by Lindhard, Scharff and Schiott [41] and tables provided by Dearnalay et al [42]. This was attributed to enhanced diffusion during subsequent annealing and also preferential diffusion to the surface. Surface state effects were reduced to a similar level as observed in thermally grown Oxide by two stages of annealing at 750 degrees C and 900 degrees C for one hour.

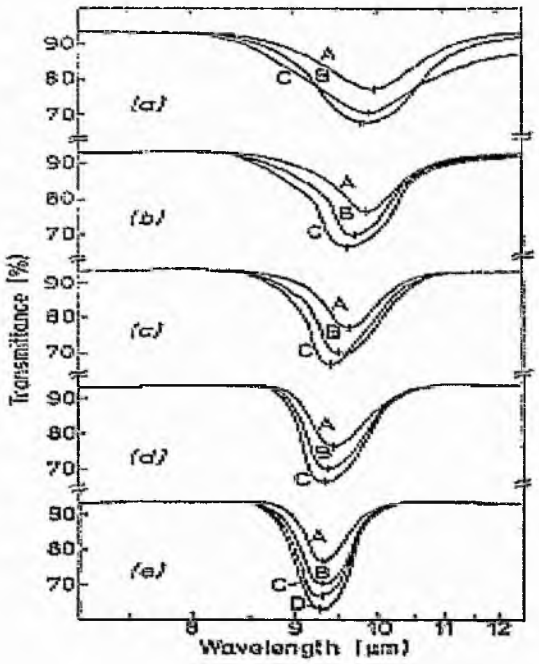


Figure 3 Transmission IR spectra for Badawi and Anand's 50 keV implants for the low dose curves A-High dose curves C, a) as-implanted, b) annealed at 450 degrees , c) 600, d) 750 and e) annealed at 900 degrees and finally the curve marked D in e) for a thermally grown Oxide of thickness 200nm [40].

The infra red transmission is shown in figure 3 and shows a progressive improvement in comparison with thermally grown oxide curve D in section (e) of figure 3 as the annealing temperature is raised. Oxide thickness was confirmed with ellipsometry and quality from C-V measurement.

Gill and Wilson [43] observed using Rutherford Back Scattering (RBS) that mono-crystalline Silicon implanted with Oxygen at 40 and 60 keV penetrated to a similar depth for the same energy for varying ion doses but that at about 0.75×10^{18} ions/cm.^{2} and above the RBS spectra demonstrated a saturation situation similar to that obtained with thermally derived Oxide RBS spectra. They determined this saturation occurred when $n_o/n_{si} = 2$ (where n_o is the number of Oxygen atoms present and n_{si} is the number of Silicon atoms present). The Oxygen then appears to undergo radiation enhanced diffusion which would explain, for example, the fact that the region between the peak and the surface was fully oxidised.

2.2.2 Buried Layers By Oxygen Implantation:

Izumi at al [25] formed buried layers of Silica by atomic ion implantation since this was more energy efficient in terms of buried layer formation than molecular Oxygen (using 150 keV and a dose of 1.2×10^{18} ions/cm.^{2}) to give a Buried Oxide (BOX) layer at a depth of 370nm, and sufficient Oxygen to form stoichiometric silica after annealing. Oxygen and Carbon were seen at the surface of the specimen but unfortunately no reasons for the contamination were given and Carbon contamination is not reported by subsequent authors with respect to buried layers. The layer was 210nm thick. Dislocation and stacking faults were formed at the surface of the Silicon top layer when Oxygen and Carbon contamination was high and for this reason the substrate surface was removed before growing a layer of epitaxial Silicon. The authors' intention in this work was to create a material system which allowed electrical isolation for electronic components fabricated at the surface. To demonstrate this, they created a CMOS/SIMOX (Complementary Metal Oxide Semiconductor/Separation by IMplantation of OXygen) ring oscillator benefiting from total dielectric isolation, which in turn exhibited twice the speed of bulk Silicon devices of the same size. Hence this work became the benchmark for future SIMOX work.

Hemment et al [45] produced buried Oxide layers by implanting doses in excess of 1.4×10^{18} O^+ ions/cm^2. They found that an implantation temperature of 400-500 °C and a furnace anneal at 1150 °C for 2-4 hours were necessary to reduce implantation damage and create mono-crystalline Silicon at the surface. However, the 1150 °C

anneal still left some Silica grain boundaries and this resulted in higher leakage currents at +/- 10 volts DC.

Jaussaud et al [46] reported the creation of buried Oxide layers in Silicon by implanting O^+ ions at 3 x 10^{18} ions/cm^2. They observed threading dislocations at a concentration of 10^{10} per cm^2 in the top layer of Silicon, as well as Silica precipitates. The latter were mainly removed by annealing at 1150 °C for two hours, this increasing the size of the Silica layer and the authors concluded that a much lower dose would have sufficed.

Celler et al [27] reported a 1405 °C irradiative anneal which almost took the Silicon back to its melt temperature of 1412 °C, which removed both defects and Silica precipitates untouched by lower temperature anneals. This resulted in a single crystalline homogeneous Silicon layer with sharp interfaces.

Van Ommen et al [47] and [48] and Stoemenos et al [49] had worked on Silica precipitates in buried Oxide layers and concluded that there was an effective method of Silicon interstitial migration during implantation which must be athermal.

Also Van Ommen et al [47] observed the creation of a Silica super-lattice with time invariant beam current as this had the virtue of almost zero threading dislocations (as observed by transverse electron microscopy) in most of the Silicon over-layer with some remaining near to the buried Oxide layer surface, obviously this would be a matter of interest if the utmost purity were required in the mono-crystalline over layer. Performing the same experiment but with a time variant beam current did not result in the formation of a super-lattice.

Olego et al [26], using Raman spectroscopy (by shining 413.1 nm laser light into the uppermost Silicon over layer of Silicon on Silica structures and observing the varying red Stokes shifts in the Raman spectra), found tensile strains between the various layers in re-crystallised Silicon layers (annealed after implantation), which they attributed to the Silica precipitates. The degree of strain varied from maximum in the as-implanted state decreasing with anneals at 1100, 1200, 1300 and 1405 °C (lamp annealed) with the Silicon annealed at the latter temperature being virtually indistinguishable from virgin Silicon. From the Stokes red shifts, strains of 11.3 kbar were found in the sample annealed at 1100 degrees, 3.3 kbar at 1200 degrees and 1.5 kbar at 1300 degrees, with zero in the lamp annealed sample (1405 degrees).

Duncan et al [50] studied Silicon on Insulator (SOI) using photoluminescence (PL), and found that etch pit counts and defect concentrations decreased with increasing anneal temperature up to 1275 °C. Photo Luminescent defects in SOI are similar to those in Czochralski grown, and plastically deformed Silicon.

Narayan et al [51] found that by implanting at optimum substrate temperature (475-540 °C) and subsequently annealing at 1300 °C for 3-6 hours, dislocation densities in the top Silicon layer could be minimised to about $10^5/cm^2$.

Reeson [52] found that Oxygen implanted into Silicon above a critical value which can be defined as that for which the maximum concentration of implanted species achieves a volume concentration appropriate to the stoichiometric compound and forms Silicon Dioxide. The value required depends on the ion species and target material and for 200keV atomic Oxygen implants into Silicon is 1.4×10^{18} ions/cm^3 and forms stoichiometric Silica whereas Nitrogen implantation results in the formation of a non stoichiometric impurity rich layer. Redistribution occurs after annealing to give stoichiometric end products, but different rates of redistribution apply for Nitrogen or Oxygen. The crystallinity of the silicon over layer is restored by annealing for both Nitrogen and Oxygen implanted buried layers. With Oxygen this is caused by precipitate dissolution whereas with Nitrogen it is caused by defect annealing and re-crystallisation.

Bussmann et al [23] confirmed the implantation and annealing parameters i.e. Oxygen doses at 0.4, 1.8 or 2.2×10^{18} atomic Oxygen ions/cm^2 with an implantation temperature of 500 degrees C. and annealing at 1300 degrees C. for up to 5 hours or 1350 for 4 hours. Also they achieved total dielectric isolation of the top Silicon layer by enclosing it in Silicon Dioxide and they demonstrated very well the progressive absorption of the lower Silica islands with progressive annealing temperature and time to give a smooth and linear lower Silicon Dioxide surface.

Blake [24] pointed out that the structure resulting from a high dose Oxygen (10^{18} ions/cm^2) implant depends strongly on the dose and energy of the implant and the temperature of the wafer during implantation. His report gave a good historical overview of oxygen implantation into silicon as well as annealing and a good account of optical annealing. Figure 4 shows a transmission electron microscope image of a

cross section of a Simox wafer showing from the top the silicon over layer, the buried oxide layer and the silicon substrate.

Figure 4: Shows a Simox XTEM cross section with the silicon over layer on top and BOX (buried oxide layer) in the middle and substrate underneath [24].

As Oxygen is implanted the dose builds up to the solubility limit, and any further increases result in the formation of islands of Silica which are initially disconnected. These islands may form at the surface (lower implant energy – at about 30-40 keV) or below the surface (higher implant energy e.g. about 200keV for buried layer). Indeed implantation was initially envisaged for replacing thermal Oxidation of Silicon since implantation gives far greater control of doping. Performing the implant at 500 °C gives heating during implantation, and with a surface implant it is possible that solid phase epitaxy will help restore the original silicon crystallinity, which is not possible in buried Oxide formation in a process such as the formation of SIMOX. A good discussion of optical annealing is provided in this paper, demonstrating that it is superior to furnace annealing at 1300 °C if it is available. The author also reports that Silicon tubing was implemented in the first commercial implanters to reduce metal contamination, that threading dislocations could be reduced by several implant and annealing steps, and that channelling (in this case in SIMOX) was reduced by the use of a chopper wheel to minimise beam waggle. Ion selectivity is very important in the implantation apparatus as, for example, two layers could be formed with Oxygen: one for atomic Oxygen ions and a separate layer for molecular Oxygen ions since they would have different penetration depths for the same energy, one being twice as massive as the other.

Summary and Conclusion

Oxygen implantation into Silicon is a well established means of forming SiO_2 layers in silicon. The majority of the work has been carried out for buried layers to develop SOI substrates such as SIMOX.

However, significant work also exists related to surface implants. Initial work with surface layers was dogged by problems with dosage, implantation temperature and beam current variation. However, later work produced good quality layers if these parameters were carefully monitored and kept at the right level. Buried Oxide layers always have a problem with threading dislocations and even the best work [26, 27] still gave a level of 10^5 /cm^2 in the bottom third of the Silicon over layer, which may not be a problem for Mosfet designers but would conceivably cause problems for Silicon Photonics for example increasing absorption/scattering problems in rib waveguides and affecting the refractive index. This would be at least one of the reasons for the prevalence of Smartcut in Silicon Photonics [20].

Surface layers of Silica can readily be created in Silicon using, for example, a dose of 1.6 x 10^{17} ions of O^+ per cm^2 to give a layer depth of 75 nm at 20 keV energy as shown in the Suspre ™ simulation in figure 5 [53, 54].

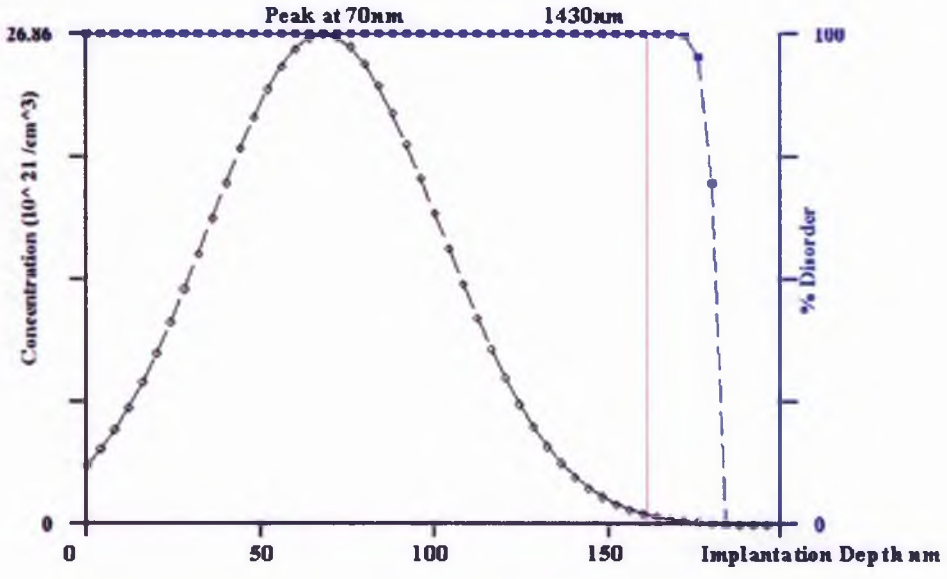


Figure 5 shows a plot of oxygen implantation into silicon (20 keV and 1.6 x 10^{17} ions/cm^2 Suspre ™ simulation.

2.3 DEVICES IN INTEGRATED OPTICS WITH RELEVANCE TO BRAGG GRATINGS IN SILICON ON INSULATOR TECHNOLOGY.

2.3.1 BRAGG GRATINGS.

Bragg Gratings were first described by Sir William Lawrence Bragg approximately one hundred years ago. Periodic structures of the order of the wavelength of the diffracting electromagnetic radiation cause changes in the amplitude and phase of an incident beam in accordance with Bragg's Law. Bragg's Law refers to the simple equation:

$$N\lambda=2d\sin(\theta) \qquad (1)$$

Where λ is the wavelength of the light, which is incident at an angle θ on crystal lattice planes of spacing d. This was derived by the English physicists H.Bragg and his son Sir W.L.Bragg in 1913 to explain why the cleavage faces of crystals appear to reflect X-ray beams at certain angles of incidence, and brought together much thinking about the nature of crystals and lattice planes and the effects thereof on incident electro-magnetic radiation.

Bragg's law is used to determine the structure of a crystal by the angles of the beams of light refracted from it. This observation is an example of X-ray wave interference, commonly known as X-Ray Diffraction (XRD), and was direct evidence for the periodic atomic structure of crystals which had been postulated for centuries. The Braggs were awarded the Nobel Prize in physics in 1915 for their work in determining crystal structures beginning with Sodium Chloride, Zinc Sulphide and Diamond. Although Bragg's law was used to explain the interference pattern of X-rays scattered by crystals, diffraction has been developed to study the structure of all states of matter with any beam, e.g., ions, electrons, neutrons, and protons, with a wavelength similar to the distance between the atomic or molecular structures of interest. Various diffraction orders are created by the constructive interference and these are given by the value of N in Bragg's Law.

2.3.2: Wavelength Division Multiplexing (WDM) Systems.

One way of increasing the bandwidth of an existing optical link without modifying the fibre is to employ the technique of wavelength division multiplexing. In this technique (see figure 6) several different signals are transmitted simultaneously down the fibre on carriers of different wavelength: the signals coming from laser diodes of different frequency then fed into different modulators (whether amplitude, frequency or code modulation). The modulated signals are then combined in the multiplexer before sending down the optical fibre. At the receiving end the signals are then separated into the different frequency components by the de-multiplexer.

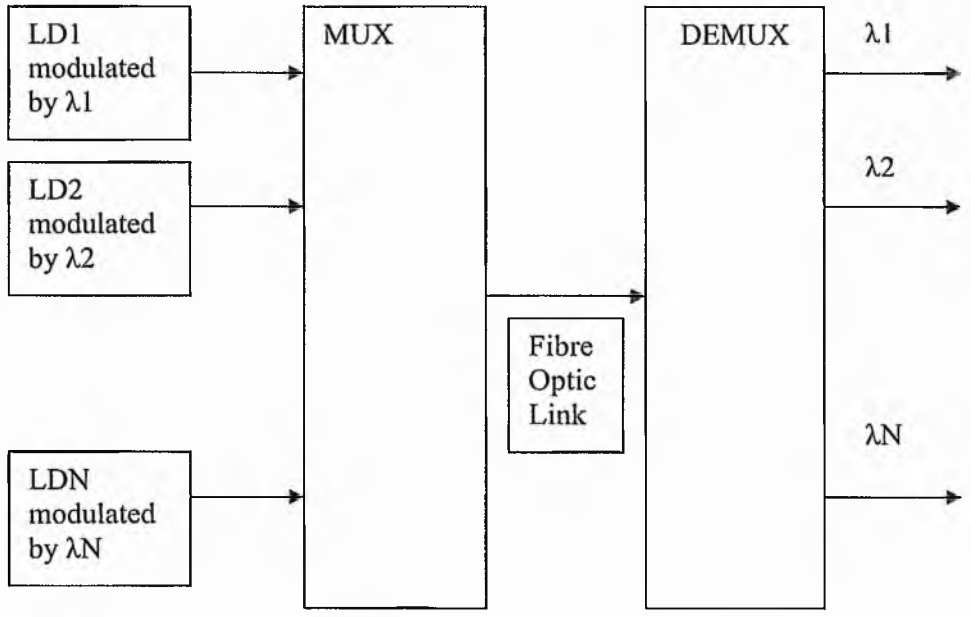


Figure 6 Block diagram of wavelength division multiplexing system.

The main difficulty is in separating the signals at the detector; inevitably, both signal loss and a certain amount of cross talk between the signals are experienced. Several possible methods of signal separation have been proposed [55] such as the use of a prisms or Arrayed Waveguide gratings. Another possibility is to use a diffraction grating to produce the same effect. Kintaka et al [57] have fabricated an optical waveguide demultiplexer for two-wavelength channels from guided waves to free space waves. The waveguide demultiplexer consisted of two types of gratings, i.e. Guided Mode Selected Focussing Grating Couplers and Different Guided Mode-Coupling Distributed Bragg Reflectors (GMS-FGCs and DGM-DBRs). The

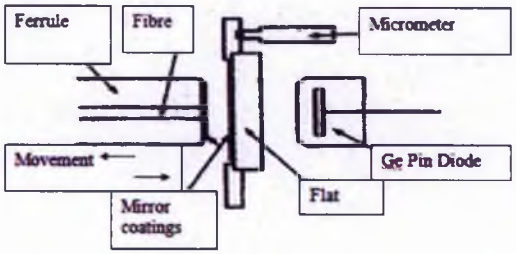
wavelength demultiplexing with 5nm spacing was experimentally demonstrated. Experimental work is being continued to improve device performances such as output efficiency, wavelength selectivity and propagation loss. An add-drop multiplexing device is also under study [57]. This work is not done in SOI and could not easily be transferred to SOI without the provision of high quality relevant Bragg Gratings but nonetheless proves how extremely useful this technology is and especially at a time when on chip WDM technology is becoming necessary to avoid information pile-up between information processing and storage "nodes". It is exactly this sort of application that makes the provision of quality Bragg diffraction gratings a matter of interest to optics designers. Wavelength Division Multiplexing (WDM) operates on the principle of combining different optical wavelengths of light and sending these down an optical fibre. Obviously if N (c.f. figure 6) different wavelengths are combined (multiplexed) at the sending end and de-multiplexed at the receiving end the bandwidth is increased by a factor of N [58]. Dense Wavelength Division Multiplexing (DWDM) was developed with a capacity of 64 to 160 parallel channels at 50 or even 25 GHz intervals and spacing of the order of nanometres. Coarse Wavelength Division Multiplexing (CWDM) comprises up to 18 wavelengths in the range 1270 to 1610 nm spaced by 20 nm [59].

2.3.3 FABRY-PEROT EFFECT AND APPLICATIONS

The Fabry-Perot phenomenon is based around the provision of two planar mirrors with a transparent medium between for example the Helium Neon laser with the gas in a container, and external optical excitation and a silvered/semi silvered mirror to provide the 633nm output. (What is a matter of considerable interest to silicon photonics engineers is the development of a silicon laser. The usage of a 100% reflecting Bragg grating at one end of a rib waveguide and the partial reflecting Bragg grating at the other end provides a part of the solution, but the rest is the stuff of Nobel prizes). This creates a situation where only light which has a wavelength which is an integral dividend of the spacing between the mirrors resonates: all other wavelengths decay in the cavity. In SOI (Silicon on Insulator) these mirrors may be replaced by Bragg Gratings since a Bragg grating is a filter/reflector and can be used in a Fabry-Perot and hence many of the following devices may be replicated in SOI.

Over the last 40 years or so a number of devices have been proposed using this technique: not just in terms of lasing but also in terms of interferometers and filtering where only the correct wavelength of light constructively combines in the interferometer or only the correct wavelength of light traverses the filter. These devices are a matter of interest in terms of SOI since like the Distributed Bragg Reflector (DBR: [60]) they may possibly be analogized by Bragg Gratings in the place of the mirrors and semiconductor material in the place of the cavity filling. Also if the Bragg Gratings could be tuned in terms of frequency response then the laser, interferometer or filter could be of a variable nature yet further increasing its usefulness. Bragg Gratings in SOI are a plausible solution to this technological challenge. Two possible techniques exist for the tuning of variable Bragg filters one is to thermally control the gratings in which case a flat surface would be helpful in terms of heat transfer and the second is electrical as proposed by Cutolo et al [61]. Although the latter is only a theoretical treatment simulated in Medici ™ and could do with experimental verification. Some interferometric applications are described in the following although it should be said that the fundamental effect of the Fabry-Perot is to act as a filter and again the Bragg Grating has the same function so many analogues should be possible.

(a)



(b)

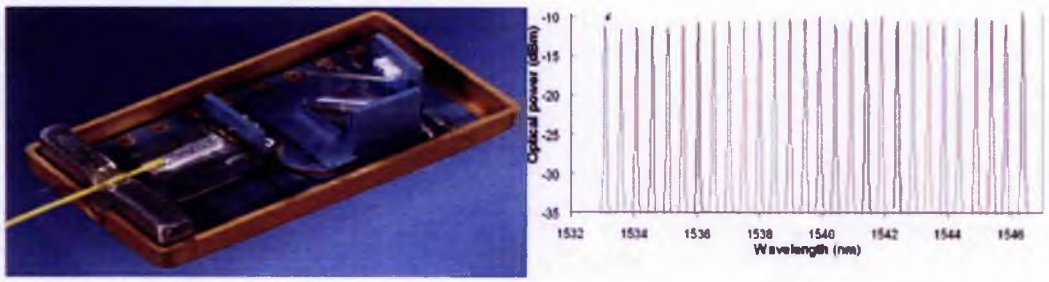


Figure 7 (a) Fibre coupled Fabry-Perot interferometer [62] and (b) industrial usage thereof by way of VTT ELECTRONICS [62]

The Fibre coupled Fabry-Perot interferometer (FCFPI) shown in figure 7a) consists of a single mode fibre mounted within a connector ferrule [62]. The end face is polished and a broadband multilayer dielectric reflection coating deposited by vacuum evaporation. The cavity is tuned by moving the fibre end axially using a piezoelectric electromechanical transducer. A cavity gap of 6 micron produced a FWHM line-width of 5nm, a FSR (free spectral range) of 180nm at 1.5 micron and etalon finesse of 37. To tune the pass band over the FSR, the cavity gap is changed by only half a wavelength. Its main limitation is the degradation in performance produced by the divergence of the beam in the optical cavity. An example of industrial use is given in figure 7b) showing a tunable laser module, and single mode tuning from 1533nm to 1547nm by changing the piezo-electric voltage from 60 volts to 24 volts respectively.

To enable investigation of cascaded FPI, micro-optic bulk FPI devices have been developed [63] and these offer many advantages over the single stage FPI such as improvement in cross talk performance, lower insertion loss and higher finesse.

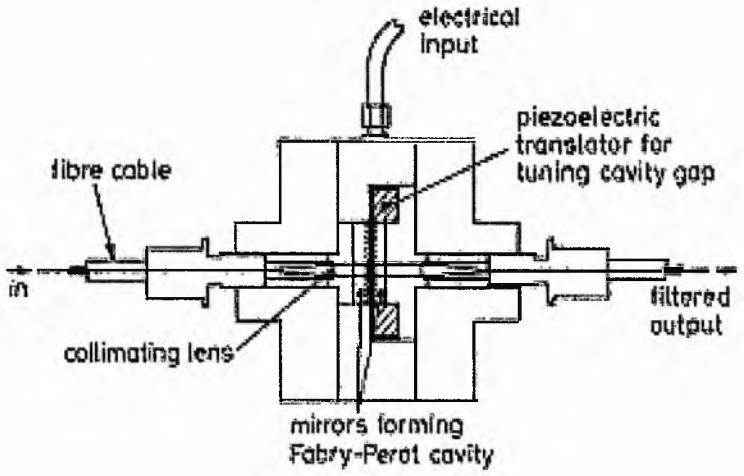


Figure 8 Micro-optic Fabry-Perot interferometer [64].

Figure 8 shows a micro optic Fabry-Perot interferometer (FPI): the incoming fibre is terminated by connector components and coupled to a collimated optimised rod lens [64, 65]. The light then passes through the FPI and is coupled to the outgoing fibre by means of a second rod lens with a piezoelectric actuator controlling the F-P gap.

This device offers a tuning range between 1.25 and 1.53 micron with FWHM line width of 4.7nm. SOI alternatives offer cheaper, more reliable solutions.

2.3.4 BRAGG GRATING TUNEABLE FILTERS

(a) Fibre Bragg Gratings

For more than ten years Fibre Bragg Gratings have found increasing applications in Wavelength Division Multiplexing (WDM) communications systems [66, 67]. They help stabilise diode lasers and provide channel filtering for add-drop modules [67]. An optical Fibre Bragg Grating can be made by producing periodic variations in the fibre refractive index along a short section in the core of an optical fibre (often this is done by the usage of photo resist and exposure to a high output laser e.g. the excimer) [66]. This phase grating acts as a band rejection filter, reflecting wavelengths that satisfy the Bragg condition. The first demonstration of fabrication of narrowband high reflecting Bragg Gratings by Hill et al in 1978 [68] with the writing of gratings within fibres has attracted considerable interest. By utilising the sensitivity of the grating wavelength to strain and thermal changes, it can be used to realise sensors and narrowband tuneable optical filters [69-72]. However, the low temperature sensitivity of 0.0125nm/°C [71] severely limits the tuning range. Compressive Bragg grating tuneable filters [73] actuated with a linear motor have been realised by taking into account the good stress and strain properties of Silica optical fibres and the fact that Silica is 23 times stronger under compression than under tension. Tuning ranges of up to 32nm have been reported but the tuning speed was limited to a few seconds [75]. In 1997, Iocco et al [74] improved the tuning speed into the millisecond region by compressing the Bragg grating with a piezoelectric stack actuator. A tuning range of 15nm and a settling time of less than 2ms were obtained at a wavelength of 1550nm. Such a device is of potential use in wavelength multiplexing or as a wavelength selective filter where tuning speed is crucial. High finesse fibre Fabry-Perot interferometers, (FFP) provide ultra high selectivity but their spectra are periodic in frequency, so the number of supported channels in a WDM line is proportional to the Free Spectral Range (FSR). Fibre gratings provide a true band pass filter but their band pass selectivity is generally lower than that attainable with FFPs. These limitations can be solved using a structure that combines the selectivity of the FFP and the band pass nature of a fibre grating as was theoretically described in [75] by Capmany et al. The first experimental demonstration of the filter operation is

presented [76] and a range of tuning of several hundreds of Gigahertz can be achieved by using a combination of coarse and fine tuning stages, achieving a maximum tuning range limited only by the thermal stability of the grating. Betts et al demonstrated a variable finesse Fabry-Perot Interferometer using Bragg gratings. This was a very sensitive instrument although this is only viable for fibre optics [77].

(b) Bragg Gratings in SOI.

An alternative implementation of Bragg gratings is their incorporation into Silicon waveguide structures. In the published literature relating to Silicon, Bragg Gratings are either configured as high reflectivity periodic structures used to improve Fabry-Perot cavity finesse [76] or as part of a hybrid p-i-n modulator which is used to vary the Bragg wavelength and hence the intensity of the propagating light [73].

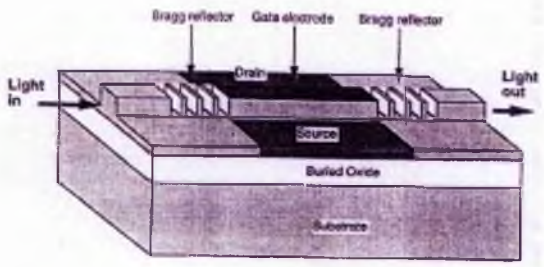


Figure 9 schematic view of the fabry-perot grating waveguide modulator [78].

In figure 9 is shown the classic Fabry-Perot cavity but with Bragg reflectors in the place of conventional mirrors. The application of potentials to the source, gate and drain electrodes will change the cavity characteristics and cause modulation. The authors found that cascading several modulators improved the reflectivity.

As demonstrated by Liu and Chou [78], twelve trenches of Bragg reflectors showed almost unity reflectivity over a 120nm range, centred on 1300nm, for a cavity length of 18.3 micron. The usage of Bragg reflectors to increase the finesse of a Fabry-Perot cavity greatly reduces the modulator size, leading to faster modulator operation. The proposed modulator can also be used as a tuneable spectral filter with a much narrower resonance peak and larger intensity modulation.

Cutolo et al [61] have proposed and modelled a pin diode Bragg reflector integrated into a SOI (Silicon on Insulator) waveguide, with a response time of 12 ns and operating power of 4mW for a 50% modulation depth. Amplitude modulation is achieved by carrier injection changing the refractive index of the guiding layer.

The design of a tuneable filter with the integration of Bragg gratings on a SOI wave guide is very flexible as the reflectivities of the Bragg reflectors can be easily controlled by the number of etch trenches and trench depth [61]. This offers significant advantages over competing technologies such as fibre: facilitating the possibility of mass production and utilising established Silicon technology and has the potential for subsystem integration.

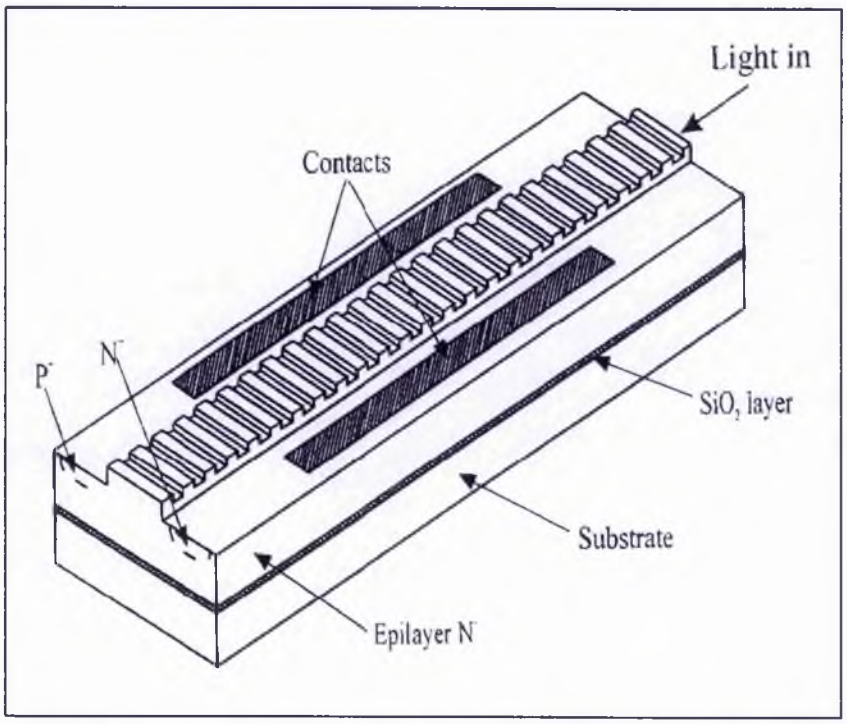


Figure 10 schematic view of Bragg waveguide modulator in SOI [61].

In figure 10 we see the schematic of a Bragg waveguide modulator: when potential is applied to the p and n contacts the refractive index of the guiding layer is changed by way of carrier injection. This then shifts the peak reflectivity of the Bragg mirror to a different wavelength. The longitudinal and transverse sections are shown in figures 11 and 12 and the simulation was run in Medici ™.

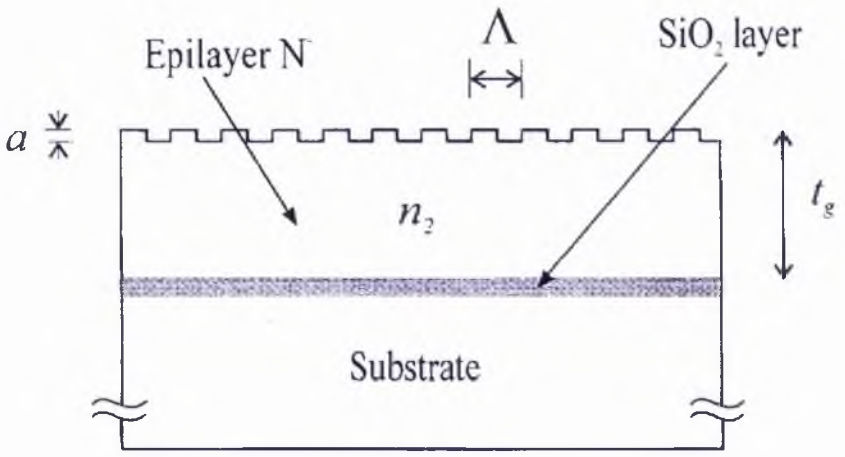


Figure 11 Longitudinal section of figure 11 [61].

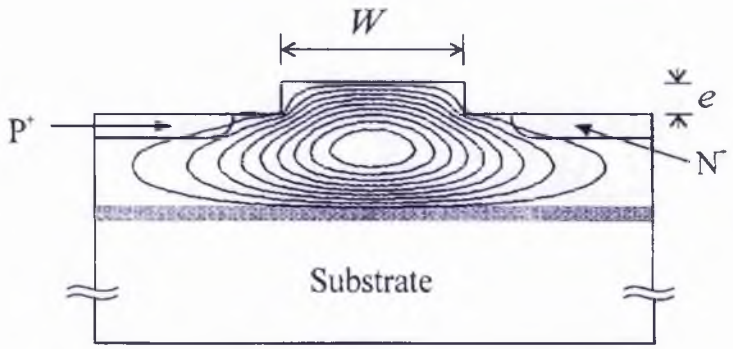


Figure 12 Transverse section showing contour lines of equal optical field strength [61].

ARRAYED WAVEGUIDE GRATING TUNEABLE FILTERS

In 1999, Toyoda et al [79] developed a tuneable filter using polymer-Arrayed Waveguide Grating (AWG) demultiplexers with a tuning range of 10nm around 1550nm. Unfortunately the wavelength tuning range is limited and the response is slow due to the slow response time of the Peltier type heater that was used. The same authors improved the tuning range to 20nm and response time of 2-60ms, a cross talk of <-30dB by implementing two different heating structures that allow forward and backward tuning [80]. The structure that they came up with is shown in figure 13.

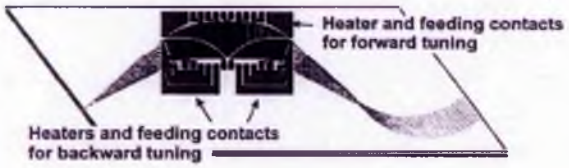


Figure 13 layout of optical phased array with the heaters on the top [80].

A Thermo-Optic wavelength tuneable filter in Silica on Silicon has been demonstrated using a similar phase shifter [80]. The tuning range was about 6nm because the inherent thermo-optic coefficient of Silica (4.5×10^{-6}/K) [81, 82] is smaller than that of polymer (-1.6×10^{-4}/K) [79]. Trinh et al [83] had demonstrated AWG multi / demultiplexers in SOI. This device has successfully demultiplexed 4 wavelengths centred 1.9nm apart at 1550nm, cross-talk to neighbouring channels was less than -22dB, insertion loss was below 6dB for all channels and a TE-TM shift of less than 0.04nm was demonstrated. Recently, Pearson et al [84] have presented theoretical and experimental results detailing the design and performance of AWG demultiplexers fabricated in SOI. The authors have emphasised that polarisation birefringence can be removed by an appropriate choice of the SOI ridge waveguide width to height ratio [84]. Reactive Ion Etching (RIE) is more a favourable fabrication technique compared to chemical etches because it can produce the precise geometry profiles required for producing a waveguide with zero birefringence. However, ridge waveguides fabricated by RIE may suffer from sidewall roughness if care is not taken. As reported in previous work [85], this sidewall roughness can cause very high losses in small cross section waveguides.

ELECTRONICALLY SWITCHABLE BRAGG GRATINGS

A recent development in the field of Bragg gratings is the Electronically Switchable Bragg Grating [86] this depends on the configuration of a Bragg grating in Holographic Polymer Dispersed Liquid Crystal. A composite electro-optical [87] medium of this nature is called a Holographic Polymer Dispersed Liquid Crystal (H-PDLC). Since H-PDLCs contain liquid crystals exhibiting an electro-optic effect, their periodic structure can be altered or turned on or off by the application of an electrical field. Under these conditions H-PDLCs are generally referred to as Electronically

Switchable Bragg Gratings (ESBGs). A schematic of ESBG operation is shown in figure 14 and shows the core, cladding, H-PDLC layer, switchable Bragg gratings, diffracted photon beams and the electrodes used for control.

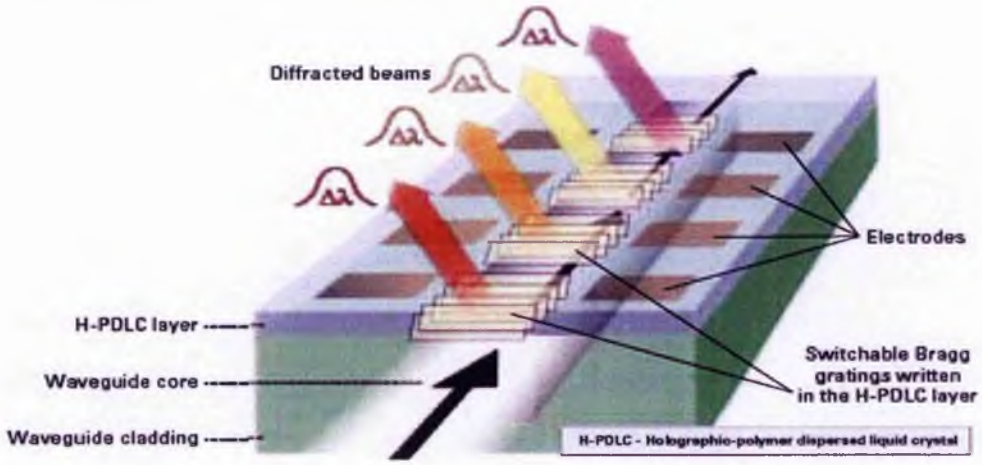


Figure 14 ESBGs can provide a platform for various WDM functions [86].

ESBGs can be used in grating assisted planar waveguide Mach Zehnder coupled optical add/drop [86] multiplexers / demultiplexers (OADMs). If one has a Mach Zehnder interferometer with ESBGs in both arms then the resonant frequency can be tuned to drop just one channel, if the gratings are electronically erased then the system reverts to an all pass. Due to the symmetry of the device it is correspondingly possible to add as well as drop simultaneously by adding in one arm and dropping in the other providing the full OADM functionality. The placing of additional matched pairs of gratings with different resonant wavelengths would permit the OADM to drop or add several different wavelength channels at once. Channel cross-connecting (i.e. routing signals from individual input ports to one or more selected output ports) is a required function in communication systems. ESBGs allow this function to be implemented in the optical rather than electronic domain, eliminating substantial cost associated with electronic to optical conversion. Optical space switching can be implemented using ESBGs to generate phase delays in phased array planar waveguide structures to build a number of simple switching elements. In summary, liquid crystal replaces fibre cladding, a Bragg grating is recorded on the liquid crystal for each wavelength and the gratings can be switched on and off.

Despite these benefits ESBGs are basically slow, the settling time of 50 microseconds is likely to preclude faster WDM applications and the application is unlikely to be easily compatible with waveguide based integrated optics (a matter of constant concern with optically based SOI is that it should be physically compatible with what the electronics SOI designers are already producing) and this may well limit its usefulness to sensor applications and other fixed device applications where settling time and compatibility were not a matter of the essence. Thus although these devices are very versatile and configurable there must still be a need for fast response variable Bragg Gratings and it would seem as if flat ion implanted Bragg Gratings were becoming one of the major contenders for the solutions to the vacant positions in integrated optics.

RECENT DEVELOPMENTS IN BRAGG GRATINGS

Aalto et al [88] fabricated a corrugated Bragg Grating on a SOI rib and enhanced reflectance by extending the grating to the shoulder of the rib (wide grating structure). Their e-beam writing technique produced some flaws with first order but none with second order gratings and their calculation gave extra reflectance peaks due to higher order propagating modes (see figure 17).

Although they had problems with first order e-beam the technique is promising for higher order gratings in SOI as great quality of documented period is required and quality of maintained periodicity also.

However the gratings are corrugated which limits their application and no experimental results are given. In figure 15 we see the first and second order grating profiles and in figure 16 a schematic of the fabrication.

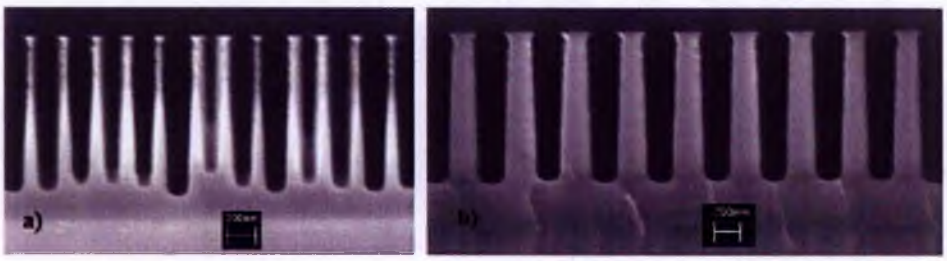


Figure 15 a) first and b) second order gratings [88].

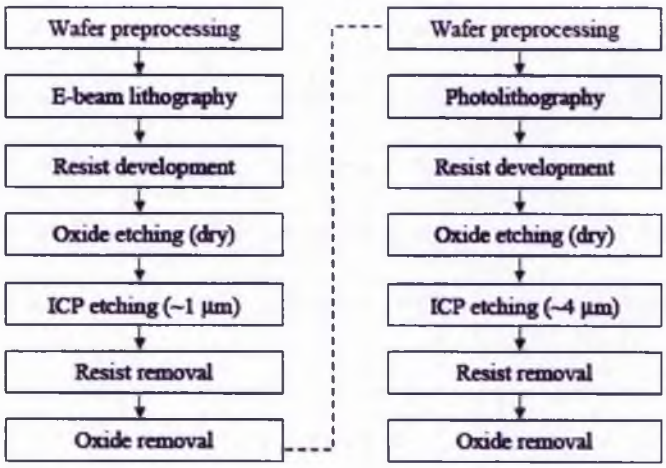


Figure 16 processing steps in the grating fabrication and the waveguide [88].

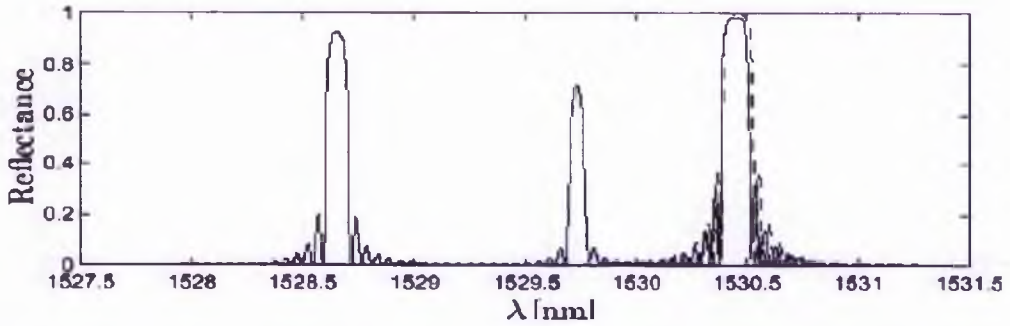


Figure 17 Aalto's calculation demonstrated higher order propagating modes i.e. single modality had been lost [88].

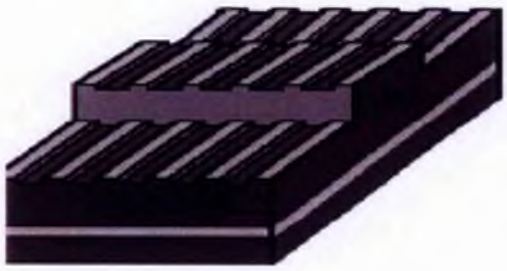


Figure 18 wide grating structure [88].

In figure 18 we see the structure of the gratings with the grating extending beyond the top of the rib waveguide and in the simulation (figure17) we see the presence of higher order modes caused by putting a grating on the top of a rib waveguide.

Banyasz et al [89] produced gratings in glass by ion implantation of Helium and Nitrogen. Photo resist was deposited on the glass surface and used as a mask for the implantation as shown in figure 19 in schematic.

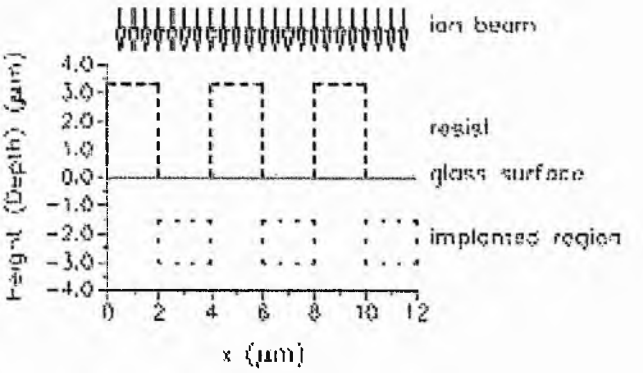


Figure 19 schematic of the implantation [89].

Various dose and ion energies were applied and the effective optical path modulation is shown in table 2.

Table 2 the modulation of the optical path produced by the implantation [89].

Number of experiment	Implanted ion	Energy (keV)	Dose (x 10^15 ions/cm^2)	D (nm)
1	Helium	500,650,800	100	120
2	Nitrogen	500,800,1160	15	220
3	Nitrogen	1600	40	240
4	Nitrogen	1160	10	180

These contained gratings caused by index change and by surface relief. The surface relief was estimated from figure 20 to be 300nm for a 2 micron line width. The surface relief was thought to be caused by volumetric changes in the silica or sputtering. The gratings could not be used in SOI firstly as silica would be difficult to transfer to SOI and secondly a 4 micron periodicity implies function outside the telecommunications wavelength range.

Figure 20 scanning electron microscopy of the grating edge [89].

The gratings were not very shallow due to the small changes in refractive index caused by implanting nitrogen into glass. Incorporating into SOI must be a problem since glass was used as the basis for the implantation. Ion implantation into Silicon is better as this can be done straight into SOI and the change in refractive index is about 2 for Silica creation from a Silicon start. Boehme et al [90] presented laser etching of wet Silica to create gratings, again although the fabrication is novel, transfer to SOI is difficult and the gratings are in relief. Ferguson et al [91] present use of Focussed Ion Beam milling to create gratings in fibres; this technique could be modified to create relief gratings in SOI. Florea et al [92] present the interferometric technique using photo-resist for grating manufacture: if this was conjoined with ion implantation rather than etching it could create flat gratings in SOI. Li et al [93] by a two step exposure process created surface gratings in photo-resist obviously this technique could be used to create SOI relief gratings. Moreau et al [94] report the formation of Sol-Gel gratings by holographic interferometry as shown in the schematic of figure 21 where the fringes are caused by recombining the light from an Argon laser onto the sample.

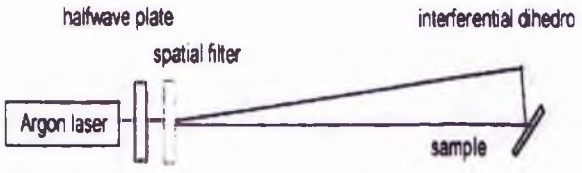


Figure 21 schematic of holographic setup [94].

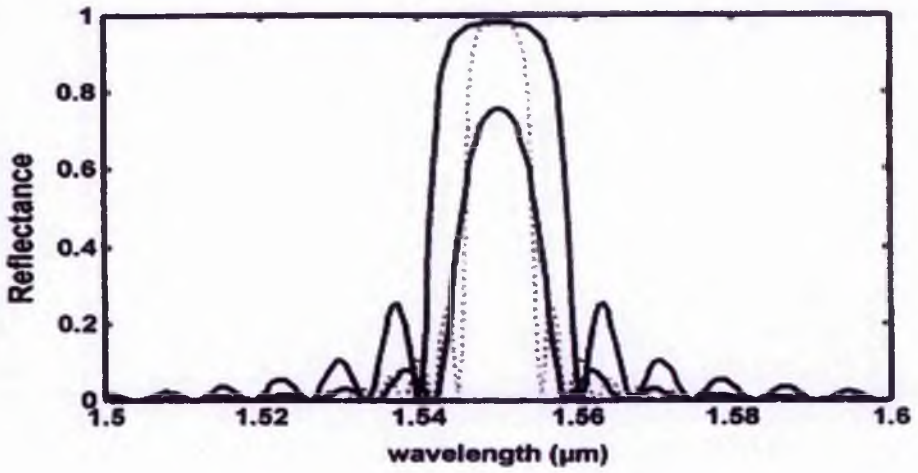


Figure 22 the influence of the refractive index change on the bandwidth. The bandwidth is halved when the index change is halved but the reflectance is reduced: this is compensated for by the grating repeats (dotted lines) [94].

The gratings give good quality telecommunication band gratings by a matter of balancing the bandwidth change with the number of grating repeats as shown in figure 22. Sol-Gel is subject to a poor take up in Europe possibly due to wet-chemistry fabrication difficulties also unfortunately it is difficult to envisage an easy hybridisation with rib waveguide SOI.

Mouroulis et al [95] presented a scheme for creating surface relief gratings by X ray lithography.

By definition X-ray lithography can only create surface relief gratings and so from the perspective of this project is inadequate see figure 23.

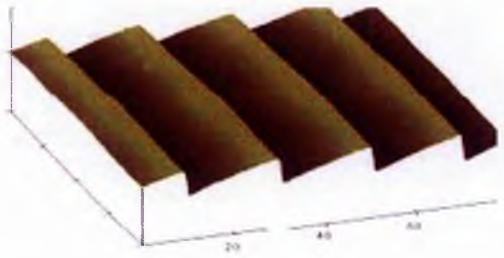


Figure 23 atomic force measurement scan of grating with 20 micron period [95].

The authors demonstrated gratings of up to 80 per cent efficiency but their results only went as far as 1100nm avoiding 1300 and 1550 nm which are the wavelengths of significance in terms of telecommunications, also Silicon is opaque below 1200nm so on the basis of the present set of results it would be impossible to transfer to modern Electronics/Silicon Photonics.

Wiesmann et al [96] designed apodised surface gratings and reported 99.9% reflectivity at 1537nm. The apodisation was achieved by varying the grating duty cycle and resulted in 20 dB of side lobe suppression outside of 1.36nm. The gratings were constructed of a 2 micron thick SiON (Silicon Oxy-Nitride) layer grown by Plasma Enhanced Chemical Vapour Deposition (PECVD) on a thermally oxidised Silicon wafer. The gratings were defined by electron beam lithography. Although these results are impressive it is not easy to see how the gratings can be transferred to usage in all optical networks or in SOI since obviously implantation into a masked SOI rib waveguide must be more ergonomic, easier for industry to 'tool' up to and therefore more likely to receive industrial take-up and therefore more likely to happen in the real world.

Lim et al [97] produced a Bragg grating in Indium Phosphide (InP) with two stages of masking: one for the 1 micron waveguide and one for the grating itself. The grating was formed out of Reactive Ion Etching (RIE) and they claimed good mark-space ratio and periodicity (important for the maintenance of wavelength reflection characteristics).

Intriguingly despite claims for the quality of the grating they gave no optical measurements or results in their paper, also there was no estimation of the overall expense and ease of production of the gratings. This lack of results precludes informed comment but the usage of Indium Phosphide again must be a problem with SOI compatibility: as always the bigger picture is vitally important when discussing research viability.

Murphy et al [98] reported creating a Bragg reflection filter (by Reactive Ion Etching) in SOI by etching an 800 nm ridge in 3 micron Silicon layer to ensure mono-modality and further etching a Bragg grating on the surface of the ridge to a depth of 150 nm, with a duty cycle close to 50%. Their results gave extra dips in the TE (Transverse Electric) transmission spectrum caused by coupling to leaky modes with a

fundamental mode at 1543 nm for a periodicity of 223 nm. So like a FBG with coupling to cladding modes, the coupling to leaky modes for a nominally single mode rib situation gives a noticeably loss-prone guide. However, this is one of the first successful (and quite recent) attempts to create a narrowband grating in SOI. The process itself uses three stages of etching and this may make manufacture somewhat difficult and loss-prone and less convenient than a planar surface as is the process undertaken in this project.

In figure 24 we see the fabrication process used to pattern the fine-period Bragg Gratings on top of the SOI ridge waveguides. Two masking layers are first patterned, one on top of the other, to define the gratings and the waveguides.

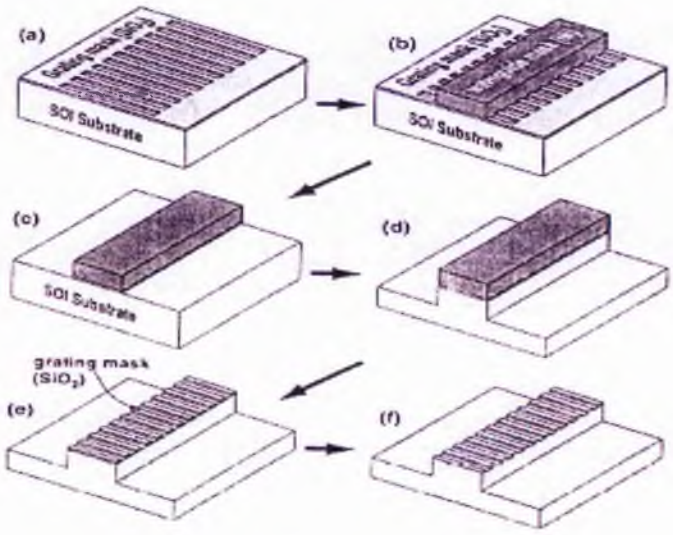


Figure 24 Murphy's fabrication process [98].

Fabrication of the grating was as follows (cf. figure 24): two masking layers were first patterned one on top of the other, figure 24 (a) grating mask and in figure 24 (b) waveguide mask, to define gratings and guides and the device was then formed through a series of etching steps [98] c, d and e etching steps and then cleaned and polished.

Nishiyama et al [99] reported the creation of Bragg Gratings by exposing Ge-B-SiO_2 (Germanium-Boron-Silica) glass films from an excimer laser and subsequently annealing at 600 degrees for one hour. The annealing reversed the photo-induced refractive index pattern and enhanced its thermal stability. The stabilised channel waveguide with a Bragg Grating showed diffraction efficiency of 18.0 dB and 18.7

dB for TE and TM like modes respectively. The manufacture is simpler than conventional dry etching and may be of use in the area of FBGs but transferring the technique to SOI would be difficult.

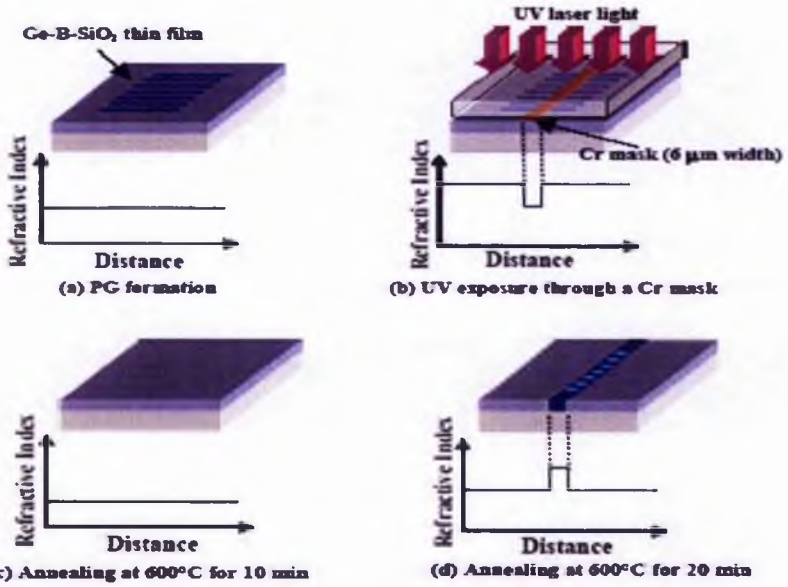


Figure 25 Nishiyama's annealing of germanium boron silica glass [99].

Figure 25 shows this process with the creation of a photo-induced grating (PG) in (a) and ultra violet light exposure from an excimer laser in (b) and two stage (c and d) thermal annealing. The refractive index in the non irradiated region became higher than that of the irradiated one after annealing for longer than 10 minutes in contrast with the case before annealing.

Lin Zhu et al applied direct electron beam writing to fabricate corrugated sidewall Bragg Gratings in polymer waveguides and demonstrate multichannel pass band filters based on a phase-shifted design. They successfully used electron beam direct writing to fabricate and then tested and compared with theoretical predictions a multiple channel pass band filter in a polymer waveguide with phase-shifted corrugated sidewall Bragg Gratings. Although the gratings are not flat and are in polymer rather than Silicon this is still a successful implementation of gratings in a rib waveguide. The lack of flatness could be a problem and some manufacturing difficulties would arise with transferring the design to SOI. Also with a grating period of 500nm these are not working at telecommunications frequencies. Figure 26 confirms the quality of the fabrication [100].

Figure 26 scanning electron micrograph of Lin Zhu's grating device [100].

Ta'eed et al [101] reported Bragg Gratings in SOI created by way of Focussed Ion Beam milling. In figure 27 we can clearly see the ridge waveguide and the Silicon shoulder underneath with the buried Oxide layer and substrate layers respectively.

Figure 27 shows a SEM of the rib waveguide used in Taeed's work [101].

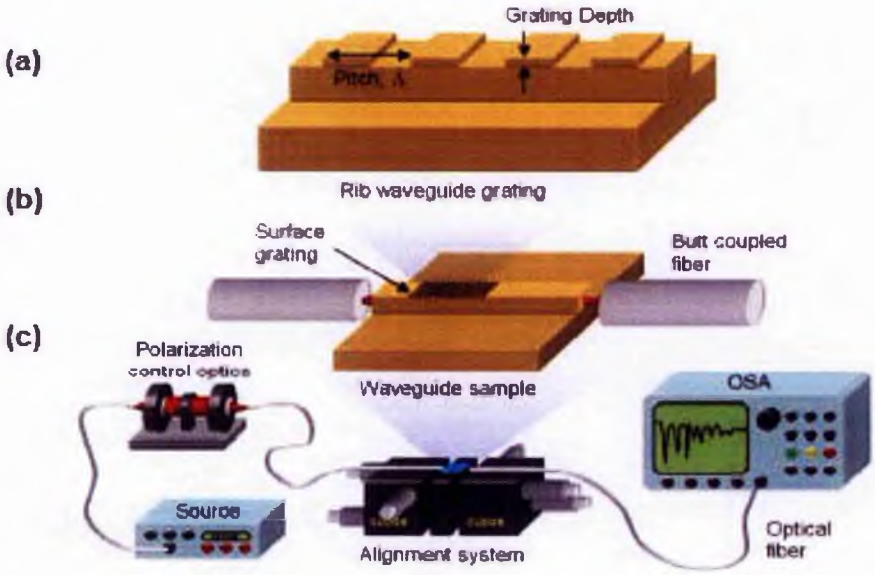


Figure 28 setup a) the focused ion beam milled grating structure b) coupling to the grating waveguide and c) measuring the optical grating system [101].

In figure 28 we see the experimental set up for Taeed's work.

In section (a) we see the corrugated grating on top of the SOI waveguide.

In section (b) we see the grating butt coupled to optical fibre.

Finally in section (c) we see the measurement system with a source variable polarizer, thumbwheel control alignment system and Optical Spectrum Analyzer.

They provided useful data on mode conversion but their method is likely to be expensive, the gratings are not flat and not well suited for mass production.

Jones et al [102] constructed a rib waveguide in Silicon Oxy-Nitride SiON which was transplanted into a rib waveguide and tested. The purpose was to see if this gave improved thermal resistance as SiON has 8 times less thermo-optic coefficient than Silicon and compare grating response.

Their result was successful as the purpose of this project is to explore possible applications of Silicon's noticeable thermo-optic effect, however, the extra complexity and presumably expense of the manufacture precludes all but the most temperature sensitive SOI applications (e.g. precision temperature sensors and temperature stabilisation).

A schematic for the fabrication is shown in figure 29.

Figure 29 schematic of silicon oxy nitride waveguide integrated into SOI [102].

Canning et al [103] report the creation of 34 dB gratings using direct UV writing in optical guides. These were formed in Plasma Enhanced Chemical Vapour Deposition (PECVD) grown Germanium doped Silica tri-layers. The results were at the telecommunications significant wavelength of 1553 nm. The lack of follow-up on their work may be due to expense and fabrication difficulty and inability to transfer to areas of technology currently under industrial scrutiny/exploitation.

Subramanian provides an interesting account of grating creation in the sides of a SOI rib waveguide by optical lithography to create the guide and e-beam (fig. 30) to form

the grating followed by reactive ion etching to create the finished article [104]. The simulation results and SEM photographs seem impressive but as they say 4 nm deviation in the grating periodicity destroys its reflectivity. No results for grating reflectivity were provided due to the non availability of an e-beam system that was free of vibration. The lack of flatness in the gratings limits grating variability and control and although the fabrication is novel it could conceivably prove difficult and expensive in mass production.

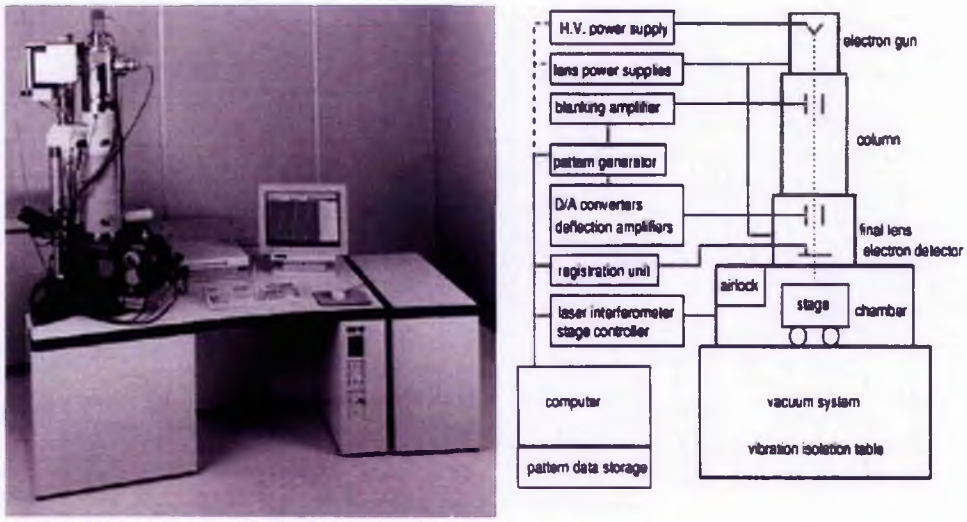


Figure 30 shows the e-beam lithography system used [104].

One conclusion from the work of both Lim and Murphy is that Bragg gratings are not easy to make in SOI by way of etching due to the need for accurate masking and etching over a distance of several hundred microns, and the same accuracy requirement applies to Focussed Ion Beam milling [101].

Photonic Crystals

Over the past ten years or so, much attention has been focussed on the development of Photonic Crystals (PCs).

Yablonovitch [105] had demonstrated the phenomenon by fabricating holes in a crystal structure which came to be known as Yablonovite and also had demonstrated that the full vector application of Maxwell's equations gave results that were accurate in terms of modelling these devices. Photonic Crystals have two or more likely three dimensional arrays of varying refractive index and the combination gives rise to a photonic band gap that forbids propagation of a certain frequency range of light [106]. This forbidden band gap helps control light and produces unconventional optical

effects. For example 100% transmission waveguide bends can be made in Photonic Crystals as can waveguide crossings and channel drop filters.

Gadot et al [107] had realised a photonic band gap in graphite and used it to manipulate electromagnetic radiation at microwave frequencies. [108] Photonic Crystals working in the infra red telecommunications section have only been realised in the past few years because of the need for suitable materials and nano-technological processing techniques. [109] Narrow line width lasers are very important in DWDM (Dense Wavelength Division Multiplexing) communications and can be fabricated using Photonic Crystals formed from the III-V semiconductors or rare earth doped glass and need less threshold current than surface emitting lasers.

Loncar et al [110] had designed and made a Silicon Photonic Crystal optical waveguide which is of interest since it may be incorporated in SOI and is functional at telecommunications frequencies and exhibits no loss.

Maystre [111] had created a Photonic Crystal diffraction grating with efficiencies approaching 100%. The curves of grating efficiency for the s polarisation show a shape that is comparable to classical gratings; however, the curves for the p polarisation are inferior. These results are not at telecommunications frequencies and it is hard to see how the work could be harmonised with SOI at the relevant frequency.

Yokoi et al had succeeded in reducing the off centre peaks in a waveguide based Photonic Crystal diffraction grating by means of apodisation [112]. However, the same comments with respect to ease of manufacture at telecommunications frequencies apply (see below). Their work nonetheless represents an attempt albeit initial to harmonise PC applications with SOI and is of interest for this alone.

At first sight of the PC literature it might seem that Photonic Crystals could sweep the board in optical electronics but this is questionable due to the cost and difficulty of manufacture since nanotechnology is required to construct components at infra red telecommunications frequencies. A second problem would be the seeming difficulty of integration of Photonic Crystal elements compared with SOI. Also III-V and Rare Earth doped glass can be difficult to machine making production of components that use these compounds both difficult and expensive. Since initial tooling, setup and investment funding are very important considerations for industry and the future

success of Silicon Photonics is assumed to rest on cooperation between academia and industry these are very important matters. A further problem is the need to hybridise with SOI for future research and development. However, if this need is addressed things like 90 degree bends with no loss could begin to appear in the SOI world. Finally and of some relevance to this project it is unlikely in the foreseeable future that Photonic Crystals will be able to supply an alternative to Bragg Gratings in SOI.

Summary and Conclusion

It has been my purpose to show in this part of the report the usefulness of Bragg Gratings not only from the perspective of current applications but also the possibility of further applications with respect to achievements with Fabry-Perot technology (i.e. in terms of lasers, interferometers and filters: the provision of a Bragg reflector in the place of a plane mirror and the provision of a semiconductor filling for the Fabry-Perot cavity). Alternatives to Bragg Gratings in SOI have been considered with critical comment to the present state of the art. The future of SOI looks good: not only is it used in modern radiation hardened, low leakage and stray capacitance CMOS electronics but also its low power dissipation under high integration may well mean a bigger share of the overall consumer market especially with new techniques such as sSOI becoming more commercially applicable. The use in photonics makes the possibility of hybrid optical electronics systems more feasible. Also recent developments in stimulated Raman emission bode well for optical amplification and lasing and with the very recent emergence of narrow band Bragg Gratings in SOI making the future of All Optical Networks based on SOI seem that much more possible.

Thus the current conclusions on Bragg gratings are:

(1) Bragg Gratings are well established as Wavelength Division Multiplexing components.

(2) Bragg Gratings are relatively difficult to make in Silicon on Insulator due to the need for very accurate etching over a very short grating period.

(3) If it is possible to create a more or less planar grating surface on the top of the rib of a SOI rib waveguide variable thermal tuning could be accomplished with the use of a control feedback heater to give a variable frequency Fabry-Perot effect.

3 THEORY

3.1 Bragg Gratings

The original diffraction gratings were hairs strung between two finely threaded screws, later in the nineteenth century diffraction gratings were formed by the fine ruling (to the order of the wavelength of light) of glass using a diamond cutter. White light hitting the diffraction grating is split into its component colours by diffraction through the grating: different wavelengths combining constructively at different angles to create a multi-coloured effect as the observer moves.

Bragg Gratings are formed by the different layers in a crystalline structure reflecting incident light and the angles of constructive reflection will give information about the crystal lattice planes.

Other areas where gratings are used are in telecommunications in wavelength division multiplexing where their ability to split and recombine the different optical wavelengths can be used to send several optical signals down one fibre optic link.

Bragg's Law can easily be derived by considering the conditions necessary to make the phases of the beams coincide when the incident angle equals the reflecting angle (following the approach of Stonybrook [113]).

The rays of the incident beam are always in phase and parallel up to the point at which the top beam strikes the top layer (see figure 31 overleaf). The second beam continues to the next layer where it is reflected. The second beam must travel the extra distance AB+BC if the two beams are to continue travelling adjacent and parallel. This extra distance must be an integral (N) multiple of the wavelength (λ) for the phases of the two beams to be the same:

$$N\lambda = AB+BC \qquad (2)$$

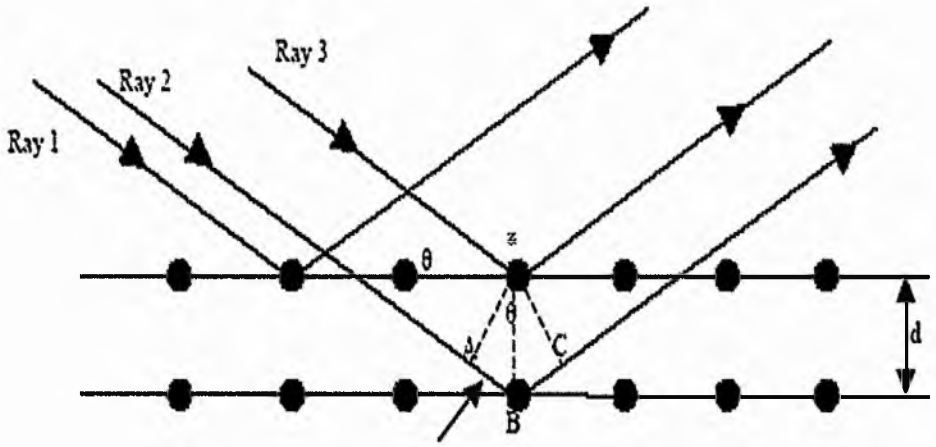


Figure 31 deriving Bragg's law using reflection geometry [113].

The lower beam must travel the extra distance (AB+BC) to continue travelling parallel and adjacent to the top beam.

Recognizing d the interplanar spacing as the hypotenuse of the right angle triangle formed by BAz, we can use trigonometry to relate d and θ to the distance (AB+BC). The distance AB is opposite θ so,

$$AB=d\sin(\theta) \tag{3}$$

Because AB=BC equation {2} becomes,

$$N\lambda = 2AB \tag{4}$$

Substituting equation {2} in equation {4} we have,

$N\lambda = 2d\sin(\theta)$,

And Bragg's law has been derived.

By a similar argument the Bragg wavelength λ_B can be expressed as $2n_{eff}S$, where S is the periodicity of the Bragg Grating and n_{eff} is the effective Refractive Index of the propagating wave.

Bragg Gratings are already in use, written in photosensitive fibres as a periodic Refractive Index variation. All fibre devices have low insertion losses but if cost efficiency, size reduction or separation of several wavelength channels is important then Bragg Gratings in SOI offer an attractive alternative.

As Silicon has a high Refractive Index (about 3.5) it makes for the possibility of creating smaller grating components than is possible with Fibre Bragg Gratings.

The propagation of optical modes in periodic corrugated or implanted waveguides can be analysed accurately by using the Floquet-Bloch Theory [114, 115]. If the depth of the corrugations is much less than the waveguide thickness (in this case approximately 50nm in a 1.5 micron waveguide), Coupled-Mode Theory (CMT) is widely used for the analysis of waveguide gratings. The derivation of Coupled Mode Theory equation follows the work of Erdogan [116-118] and Othonos et al [67]. We start by writing the transverse component of the electric field in the ideal mode approximation to Coupled Mode Theory as a superposition of the ideal modes (the modes in an ideal waveguide where no grating perturbations exist).

$$E^T(x,y.z,t)= \Sigma_m[A_m(z)\exp(jz\beta_m)+B_m(z)\exp(-jz\beta_m)]E_m^T(x,y)\exp(-j\omega t) \quad (5)$$

Where the coefficients $A_m(z)$ and $B_m(z)$ are slowly varying amplitudes of the mth mode travelling in the -z and +z directions, β is the propagation constant and $E_m^T(x,y)$ the transverse mode field.

$$dA_m/dz=j\Sigma_q A_q(C^T_{qm}+C^L_{qm})\exp[j(\beta_q-\beta_m)z]+\Sigma_q B_q(C^T_{qm}-C^L_{qm})\exp[-j(\beta_q+\beta_m)z] \quad (6)$$

$$dB_m/dz=-j\Sigma_q A_q(C^T_{qm}-C^L_{qm})\exp[j(b_q+b_m)z]-\Sigma_q B_q(C^T_{qm}-C^L_{qm})\exp[-j(\beta_q-\beta_m)z] \quad (7)$$

The transverse coupling coefficient C^T_{qm} between the m and q modes in the above equations is given by the following integral:

$$C^T_{qm}(z)=w/4\iint\{(\Delta \epsilon)(x,y,z)e_m^T(x,y)dxdy \quad (8)$$

Where $\Delta \epsilon(x,y,z)$ is the permittivity perturbation. The longitudinal coupling coefficient C^L_{qm} is defined in a similar way to the above transverse coupling coefficient C^T_{qm}. The Bragg Grating will create a coupling between optical waveguide modes and grating regions wherever the difference between their propagation constant is equal to:

$$\beta_q-\beta_m=2n\pi/\Lambda \quad (9)$$

Equation (9) is a well known phase matching condition, when this condition (9) is satisfied, the qth and mth mode will be resonantly coupled via the nth Fourier component of the periodic perturbation $\Delta \epsilon(x,y,z)$ [118]. Let us assume that the period Λ of the perturbation is chosen that $n\pi/\Lambda$= approximately $2\beta_q$ for some integer n. The phase matching condition can thus be satisfied by the coupling between the mode β_q and its reflected mode which has a propagation constant of $-\beta_q$.

Since

$$\beta_q-(-\beta_q) =2\beta_q=2n\pi/\Lambda \quad (10)$$

Let us consider a waveguide with grating section of length L. A wave with an amplitude A(0) is incident from the left on the grating section. The boundary conditions are A(z)=A(0) at z=0 and B(z)=0 at z=L, we obtain the following expressions for mode amplitudes [118]

$$A(z)=A(0)e^{j(\Delta\beta z)/2}[\text{scoshs}(L-z)+j1/2\Delta b\text{sinhs}(L-z)]/[\text{scoshs}L+j1/2\text{sinhs}L] \quad (11)$$

$$B(z)=A(0)e^{-j(\Delta\beta z)/2}[-jk^*\text{sinhs}(L-z)/(\text{scoshs}L+j/2\text{sinhs}L)] \quad (12)$$

Where s and $\Delta\beta$ are given by

$$s = \{k^*k-(\Delta\beta/2)^2\}^{1/2} \quad (13)$$

$$\Delta\beta=2\beta_q-n2\pi/\Lambda \quad (14)$$

By substituting equation 14 into equation 13, we get

$$s= \{k^*k-(\beta_q-l\pi/\Lambda)^2\}^{1/2} \quad (15)$$

$$s= \{k^2-\delta_d^2\}^{1/2} \quad (16)$$

With δ_d being the tuning from the resonant coupling and k is the grating coupling strength.

$$\delta_d =\beta_q-n\pi/\Lambda \quad (17)$$

$$=2\pi n_{eff}[1/\lambda-1/\lambda_d] \quad (18)$$

This gives the Bragg Condition for the gratings

$$\lambda_d=\lambda_{Bragg}=2n_{eff}\Lambda \quad (19)$$

Where n=1 represents a first order grating.

The fraction of power coupled to the backward propagating mode ($-\beta_q$) is called the mode reflectivity is defined as

$$R=|B(0)/A(0)|^2 \quad (20)$$

And is given by

$$R=k^{*}k\sinh^{2}sL/\{s^{2}\cosh^{2}sL+(\Delta\beta/2)^{2}\sinh^{2}sL\} \qquad (21)$$

Under phase matching conditions $\Delta\beta=0$, the reflectivity R reaches its maximum value according to equation 21

$$R_{max}=\tanh^{2}|kL| \qquad (22)$$

Such device structures have been realised (cf chapter 2).

In this particular application RSoft Gratingmod ™ was used to provide the simulation based on the principles of Coupled Mode Theory.

Firstly the simulator was run in order to provide information about the length of grating that would be required for both first order and third order Bragg Gratings and it is clear from figures 32 and 33 that the length of grating required for the first order is much shorter than the third.

Third order gratings would make problems like masking much simpler, but at the time of the project inception all sub micron masking needed to be done via Southampton University and so the choice would have had no effect on the project management. It is clear that to achieve a first order Bragg grating at 1550nm a period of 228nm is required (e.g. via Gratingmod ™) it is possible to create a third order grating with a period of 684nm.

However, the Bragg reflectors become less efficient at third order and hence a longer grating length is required to increase the reflectivity. Thus from figures 32 and 33 a length of approximately 4000 micron is required for first order and 100,000 micron is required for third order.

In order to make e-beam writing time of an achievable economic nature and in order to minimise the chance of errors in periodicity, a very conservative top length of 1000 micron was chosen and the gratings required being first order with a nominal period of 228nm.

The other attraction of choosing the first order gratings is that the diffraction efficiency would be optimal ensuring the best quality gratings.

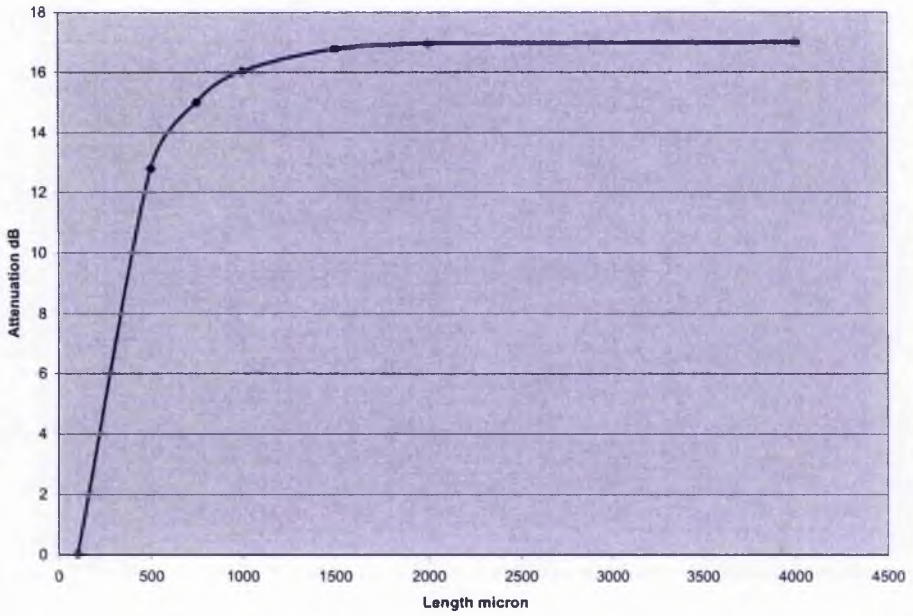


Figure 32 first order grating length simulation, depth=100nm [121]

In figure 32 above we see that the (supposed) ogive curve for first order Bragg gratings reaches a plateau at about 4000 microns. Whereas in figure 33 below we see that the plateau is only reached at about 100000 microns. In terms of the present project such a length would have proved prohibitively expensive in terms of e-beam writing cost.

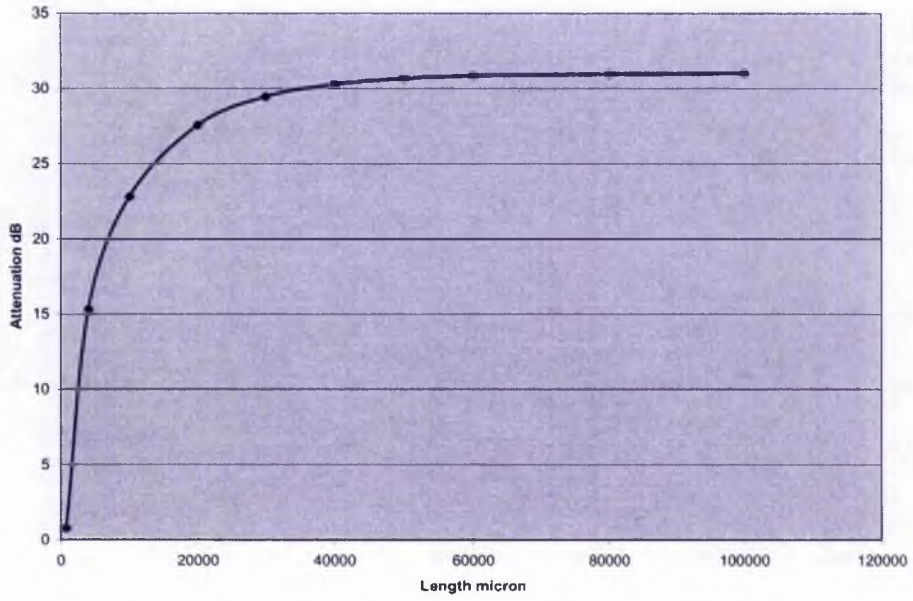


Figure 33 third order grating length simulation, depth=100nm [121]

3.2 Wave guides in SOI

Single mode optical confinement can be achieved in Silicon on Insulator by the provision of a ridge in the top of the Silicon and a buried oxide layer (BOX) in the body of the Silicon and a substrate layer underneath. This is because the change in refractive index between the Silicon and Silicon Dioxide is large enough to trap the fundamental mode between the ridge or rib and the BOX.

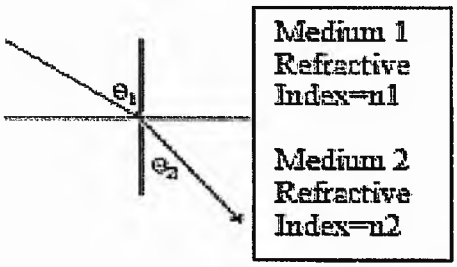


Figure 34 diagram of Snell's law.

According to Snell's Law, (as shown in figure 34)

$$n_1\sin(\theta_1)=n_2\sin(\theta_2) \tag{23}$$

Where n_1 and n_2 are the indices of refraction for refraction for two different materials in contact with each other and θ_1 and θ_2 are the angles an incident and refracted ray of light make to the normal, respectively.

If $\theta_2=90^\circ$ and $n_1>n_2$ then light incident in the medium will be totally internally reflected for any angle greater than the critical angle, θ_c where:

$$\theta_c = \sin^{-1}(n_2/n_1) \tag{24}$$

Thus for a Silicon ($n_1=3.5$) and Silica ($n_2=1.5$) interface, the critical angle is 24.5°. This means that Silicon has strong optical confinement when surrounded by a material of a much lower index of refraction such as Silica or air. Hence, the over layer of an SOI structure is a very desirable material for making waveguides with strong optical confinement. However, an SOI wafer only intrinsically has confinement in the vertical direction, but not in the horizontal, and therefore is not very useful for creating optical devices.

A two dimensional waveguide, also known as a strip waveguide, can be created simply by etching away two closely spaced parallel trenches in the over layer. This

type of waveguide has a serious drawback in that in order to make the waveguide single mode; the waveguide's cross-sectional dimensions need to be of the order of several hundred nanometres. This would make coupling light to the waveguide a very difficult task.

A solution to this issue is to create what is known as a rib waveguide. A rib waveguide, pictured in figure 35 (a), is created by only etching partial trenches in the Silicon instead of etching down to the Oxide as in the case of a strip.

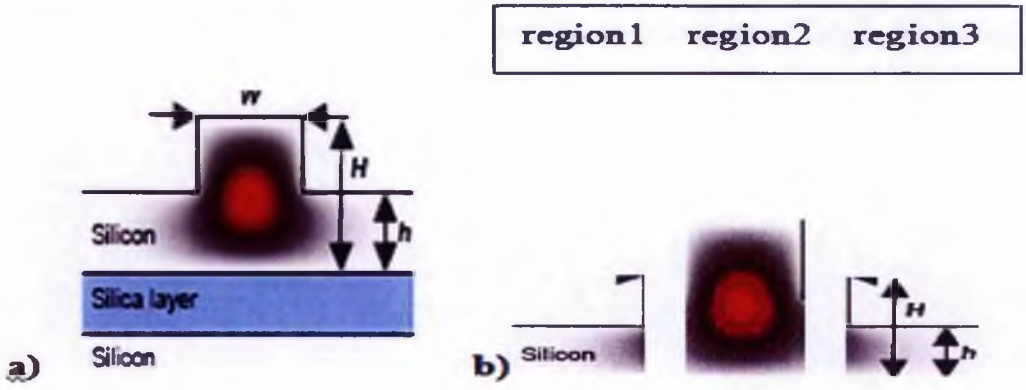


Figure 35 cross sectional view of a rib waveguide.

The result is a waveguide whose cross-sectional area can be much larger than that of a strip waveguide and yet maintain the desired characteristic of allowing only one optical mode to propagate within it (the single mode condition) [119].

A simple analysis technique known as the Effective Index Method (EIM) can be used to treat rib waveguides [120].

In figure 35(b) the rib is broken up into three regions. Investigating region 1 first, the lower portion is broken up into three regions. Investigating region 1 first, the lower portion is Silicon while the upper portion is air.

The Effective Index Method takes the indices of refraction of the Silicon and air regions and in effect averages them together. This effect is identical for region 3. The result is an effective index of refraction that is lower than the index in region two.

Thus confinement is achieved in the horizontal direction but less so than in the situation with the strip waveguide. The mode is less tightly confined and hence the waveguide supports fewer modes than a strip of similar dimensions.

3.3 The Theory of Ellipsometry

Ellipsometry is a non-contacting, non-destructive technique for the measurement of surfaces and very thin films on surfaces using polarised light. No other measuring technique is as direct or inherently as precise as ellipsometry: a good quality ellipsometer can detect film conditions of under an Angstrom thick [122, 123].

Ellipsometry is superior to alternate methods of thin film measurement such as reflectometry (which relies on measurements of absolute light intensity) as it rests upon the independent determination of two independent parameters, Delta (phase difference between the two beams) and Psi (the amplitude ratio of the two beams). This then enables the discovery of not only the Refractive Index of the film but also its thickness. Also the ratio technique is insensitive to temperature fluctuations as well as absolute source intensity variations providing accurate results under varying experimental conditions.

Light reflected from a uniform surface is characterised by two reflection amplitudes r_p and r_s, the first for light polarised in the p direction, which is in the plane of incidence, and the second for light polarised in the s direction which is perpendicular to the plane of incidence.

The ellipsometry method compares the p reflected field with the s reflected field, thus eliminating the necessity of measuring separately the incident intensity and the reflected intensity (as is the case with reflectometry). In ellipsometry the comparison is made by polarising the incident beam so that it has two coherent s and p waves, whose amplitude and phase are then altered by reflection. The reflected light becomes elliptically polarised. Formally what is measured is the complex ratio of amplitude reflectivities for p and s polarised electromagnetic waves

$$R=r_p/r_s=\mathrm{Re}(R)+j\,\mathrm{Im}(R) \qquad (25)$$

As equation 25 suggests the general solution for the measurement of the ratio is complex and this implies the necessity of computer iteration to obtain the solution.

Fresnel's equations, usually written in terms of the angles of incidence and propagation, can be written

$$R_s=(q_1-q_2)/(q_1+q_2),\ R_p=-(Q_1-Q_2)/(Q_1+Q_2) \qquad (26)$$

Where R is the fraction of the intensity of the incident light that is reflected from an interface of two different refractive indices and the subscript s denotes that the electric field of the light is oscillating perpendicular to the plane of propagation, similarly p denotes that the electric field is parallel to the plane of propagation.

Let q_1 be defined as the normal component of the wave-vector in the incident medium labelled 1. A similar definition applies for medium 2. Also:

$$Q_1=q_1/n_1^2 \tag{27}$$

An alternative notation is often used wherein

$$R=r_p/r_s=\rho=\tan(\psi)\exp(j\Delta) \tag{28}$$

Where ρ is the length of the vector joining the origin and the point r in the complex plane, and Δ is the phase angle, measured from the positive real axis. Thus ellipsometry measures a phase quantity Δ as well as an amplitude ratio ψ. These can be directly inverted into the optical constants of the material and this transform is given in equation (29) below.

$$\epsilon=\epsilon_1+j\epsilon_2=n^2=\{n+jk\}^2=\sin(\varphi)^2[1+\tan(\varphi)^2\{(1-\rho)/(1+\rho)\}^2] \tag{29}$$

Where φ is the angle of incidence and ρ is as equation 9, ϵ is the dielectric permittivity of the film layer and k the complex component of n the refractive index.

If we define

$$\eta=\int[dz(\epsilon-\epsilon_1)(\epsilon-\epsilon_2)/\epsilon] \tag{30}$$

Where η is the first order change in the reflection properties, then the Im(R) at the Brewster angle is given by

$$\mathrm{Im}(R)=\pi/\lambda\eta(\epsilon_1+\epsilon_2)^{1/2}/(\epsilon_1-\epsilon_2) \tag{31}$$

For non-absorbing media η is real and gives a measure of the film thickness. Ellipsometry does not directly measure film thickness or optical constants, it measures ψ and Δ. To extract useful information about a sample, it is necessary to perform a model dependent analysis of this data.

This is done in the VASE (Variable Angle Spectroscopic Ellipsometry) programme [122].

First, data are acquired covering the desired spectral range and angles of incidence. A model for the optical structure of the sample is then constructed. For example, this may include a substrate and a single film on top or multilayer structures.

Second, the Fresnel equations along with the assumed model are used to predict the expected ψ and Δ data for the wavelength and angles of incidence chosen.

As an example consider a Silica film on a substrate. To model the dispersion in index of refraction, a Cauchy formula [122, 123] is used to calculate the Silica refractive index as a function of wavelength.

$$n = A+B/\lambda^2+C/\lambda^4,\ k\ (l) =0\ (\lambda=\text{wavelength}) \qquad (32)$$

Once the Psi and Delta information is received from the ellipsometry the programme iterates around values of A and B (and if required C) and the thickness of the Silica layer to give a dynamic indication (via the Cauchy formula [122, 123]) of the Silica's refractive index with respect to frequency and the best fit thickness.

3.4 How the Ellipsometer Works

The ellipsometer has several different designs governing its operation. The University of Surrey Ellipsometer [124] worked on the principle of light derived from an incandescent lamp. This light is selected in the region of 400nm to 1000nm wavelength, by means of a prism and a collimator. It is then directed through a polarising analyser (basically a polarizer) and then reflected off the sample. Linearly polarised light, when reflected from a surface, will change its state to elliptically polarised because of the presence of the thin layer of the boundary surface between the two media. By means of the Fresnel formulae the optical constants of the layer can be determined. The reflected light then passes through another polarizer and is then detected via a variable slit and a multi-element diode array detector. Changing the orientation of the polarizer and analyzer it is possible to view all states of the sample, positive, negative and intermediate and values for Psi and Delta are obtained for 400 to 1000nm. Psi and Delta derive from equation (9) where the ratio of the complex reflectance for the perpendicular and parallel polarisations is defined as the product of tan (psi) and exp (jdelta), thus Psi is the ratio of their magnitudes and Delta is the

difference in their phase. Once these sets of results are obtained the WVASE32™ (Variable Angle Spectroscopic Ellipsometry for windows copyright J.A.Woollam Co. Inc. [122]) programme provides a computer fit for the Psi and Delta to give an amount for the refractive index and thickness of the film.

3.5 Ion Implantation

Introduction

For performing ion implantation atoms or molecules are ionised (commonly by the application of an alternating radio frequency field which has the effect of stripping the electrons from the molecules creating a plasma and the positively charged ions are accelerated in an electric field out of the ion source). They are then accelerated in an electric field (extraction grid see the schematic figure 36) and purified by a mass filter and energy filter (basically only the ions of the correct mass perform the correct circular motion under a magnetic field and these are the ones selected at the aperture) and implanted into the target material. A wide variety of combinations of target material and implanted ions are possible. The energy of the implanted ions can vary between several keV and several hundred keV. The range of the implanted ions in the substrate depends on the mass of the implanted ions, their energy and the mass of the substrate atoms, crystal structure and the direction of incidence [136].

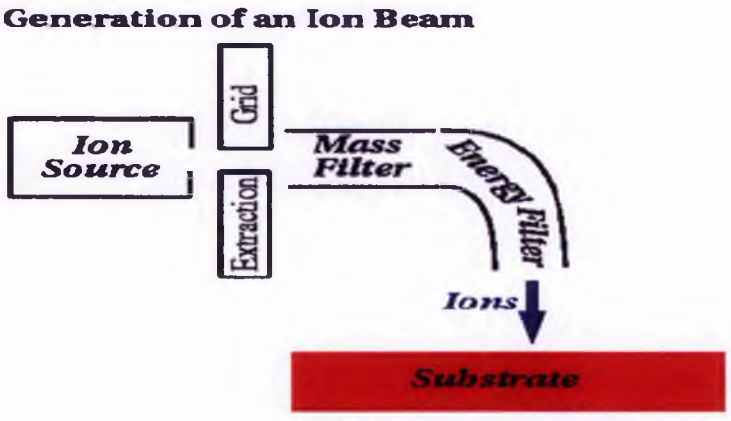


Figure 36 the Ion Implanter [142]

This section is an attempt to display and describe the major components of a high current ion implanter. The ion beam implanter is used to alter the near surface properties of semiconductor materials. Typical machines used in the manufacture of electronic devices use beam energies from 2 keV up to 2 MeV. The implanter described here has an energy range from 0.5 keV to 50 keV. The ion source is a Radio Frequency (RF) multi cusp ion source to produce the desired ion species. The beam then passes through a pre-acceleration section. The bias voltage gives the beam sufficient energy to allow selection of the desired species required for implantation by a 90 degree dipole analysing magnet.

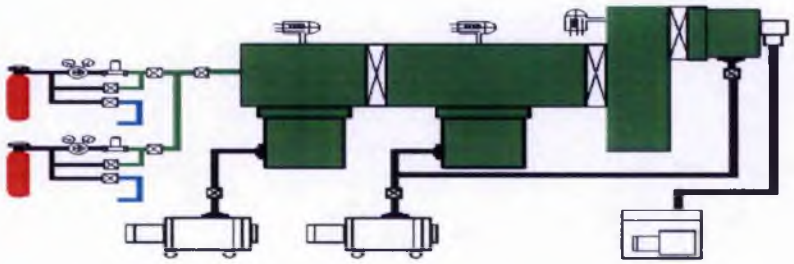


Figure 37 shows the Vacuum System [142]

The ion implanter requires a high vacuum system in order to generate plasma and transport an ion beam from the ion source through the analyser magnet to the process chamber in figure 37 this is shown using three different pumping stages.

The **Ion Source** has arrays of permanent magnets to produce a multi-cusp magnetic field in regions remote from the plasma grid and the RF antenna, for largely confining the plasma by lengthening the path of ionising electrons and reducing their drift to the walls. The ion source has a chamber which is short in length, relative to its transverse dimensions, and the RF antenna is at an even shorter distance from the plasma grid which contains one or more extraction apertures. RF electric field coupled into the plasma chamber maintains a low pressure (10^{-2} --- 10^{-3} Torr) discharge. Positive ions are expelled from the discharge by a negatively biased extraction electrode.

The **Magnetic Filter** in an ion source reduces the production of undesired ion species and improves the ion beam quality. High energy ionising electrons are confined by the magnetic filter to an ion source region where the high energy electrons ionise gas molecules. One embodiment of the magnetic filter uses permanent magnets oriented

to establish a magnetic field transverse to the direction of ions from the ion source region to the ion extraction region. In another embodiment low energy 16 keV electrons are injected into the ion source to dissociate gas molecules and undesired ion species from desired ion species. The mass analysing magnet positioned along the beam path between the source and the process chamber deflects ions through controlled arcuate paths to filter ions from the beam while allowing certain other ions to enter the ion process chamber. The magnet includes multiple magnet pole pieces constructed from a ferromagnetic material and having inwardly facing pole surfaces that bound at least a portion of an ion deflection region. One or more current carrying coils set up dipole magnetic fields in the deflection region near the pole pieces. Additional coils help set up a Quadra Pole field in the deflection region. A controller electrically coupled to the coils controls current throughput to create the magnetic field in the deflection region near the pole pieces. The analyser magnet is used to select the desired ion species. As the ions travel through the magnetic field the magnetic force serves to move the particles in a circular path in accordance with the Right Hand Rule.

Here's how it works: The magneto-static field cannot change the kinetic energy (K.E.) of the particles only the direction of their velocity. K.E. = $1/2mv^2$, the radius R of the circular path is proportional to the velocity of the particle.

$$R=m\,v\,/\,q\,B \qquad (33)$$

Thus the greater the mass of the ion the greater the radius of curvature and only ions of the required mass are allowed through.

Measuring Ion Beam Current: The Faraday Cup [142]

A Faraday cup, figure 38 [142] is a device for measuring the current in a beam of charged particles. In its simplest form it consists of a conducting metallic chamber or cup which intercepts a particle beam. An electrical lead is attached which conducts the current to a measuring instrument. Detection can be as simple as an ammeter in the conducting lead to ground or a voltmeter or oscilloscope displaying the voltage developed across a resistor from the conducting lead to ground. A bias voltage applied either to the cup itself or a repelling grid preceding the cup or a magnetic field is usually used to prevent secondary emission from distorting the reading. The design can be significantly more complicated when it is necessary to make measurements of

very short pulses or very high energy beams which may not be fully stopped in the thickness of the detector.

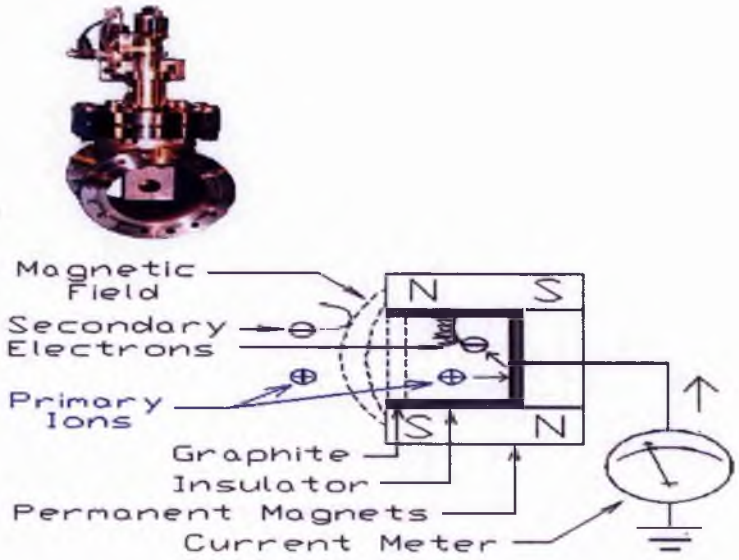


Figure 38 Faraday cup and electrical schematic [142]

Figure 38 shows a Faraday cup and the schematic of the current measuring system. The name of the device is intended to honour Michael Faraday the discoverer of electro-magnetic induction, electro-magnetic rotations, the magneto-optic effect, diamagnetism. The Faraday cup is arranged in the process chamber and beam line corresponding to an ion beam shooting position. For each positive ion that enters the Faraday cup an electron is drawn from ground through the current meter to neutralise the charge of the ion. The magnetic field stops outside secondary electrons from entering and secondary electrons produced inside from leaving.

Charge Neutralisation

As the ion beam is directed into contact with the wafer the wafer charges positively. The charging is often non uniform and can create large electric fields at the wafer surface (e.g. as much as several hundred volts) and damage the wafer causing it to become unsuitable for use as a semiconductor material. In order to neutralise the charge an apparatus is provided in which electric charge of opposite polarity to that of the charged beam is generated near the wafer surface to neutralise the charged beam or build up of electrostatic charge on the surface. There are several different methods of accomplishing this.

RF Plasma Cell Charging Control:

This is an apparatus for maintaining an ion beam along a beam path from an ion source to an ion implantation station where work pieces are treated with the ion beam.

An ion beam neutraliser is positioned upstream from the ion treatment station and includes confinement structure which bounds the ion beam path. An electron source positioned within the confinement structure emits electrons into the ion beam. An array of magnets supported by the confinement structure creates a magnetic field which tends to confine the electrons moving within the confinement structure. An interior magnetic filter field is created inside the confinement structure by a plurality of axially elongated filter rods having encapsulated magnets bounding the ion beam and oriented generally parallel to the ion beam path.

This interior magnetic field confines higher energy electrons from leaving the ion beam path and permits lower energy electrons to drift along the ion beam.

An Ion beam neutraliser

High energy electrons are directed through an ion beam neutralising zone or region containing an ionisable gas. As the high energy electrons collide with the gas molecules they ionise the gas molecules and produce low energy electrons which are trapped by a positively charged ion beam. As high energy electrons pass out of the neutralising zone they are deflected back to the neutralising zone by a cylindrical conductor biased to deflect the high energy electrons and an accelerating grid for accelerating the electrons back through the beam neutralising zone.

Electron-beam charge neutralising system

The apparatus includes an electron source for generating an electron beam and a magnetic assembly for generating a magnetic field for guiding the electron beam to the work piece. The electron beam path preferably includes a first section between the electron source and the ion beam and a second section which is coincident with the ion beam.

The magnetic assembly generates an axial component of magnetic field along the electron beam path. The magnetic assembly also generates a transverse component of the magnetic field in an elbow region between the first and second sections of the electron beam path. The electron source preferably includes a large area Lanthanum

Hexaboride cathode and an extraction grid positioned in close proximity to the cathode [137].

The apparatus provides a high current, low energy electron beam for neutralising charge build-up on the work piece.

4 DEVICE DESIGN

This section will describe the design of a single mode Silicon on Insulator waveguide and also the simulation and design of SOI Bragg gratings. Simulation using RSoft BeamProp ™ [121] is described and the ideal waveguide dimensions will be established.

4.1 Single Mode Operation

Work done by Thomas Murphy [98] was used as the basis for the design parameters in 1.5 micron SOI. An etch depth of 800nm was chosen to minimise birefringence and the graph in Figure 39 was obtained by running RSoft Beamprop™ [121] and checking for the computed mode spectrum. A series of simulations were run and modality found to be minimum at y=1.33 microns vertical height from the top of the waveguide.

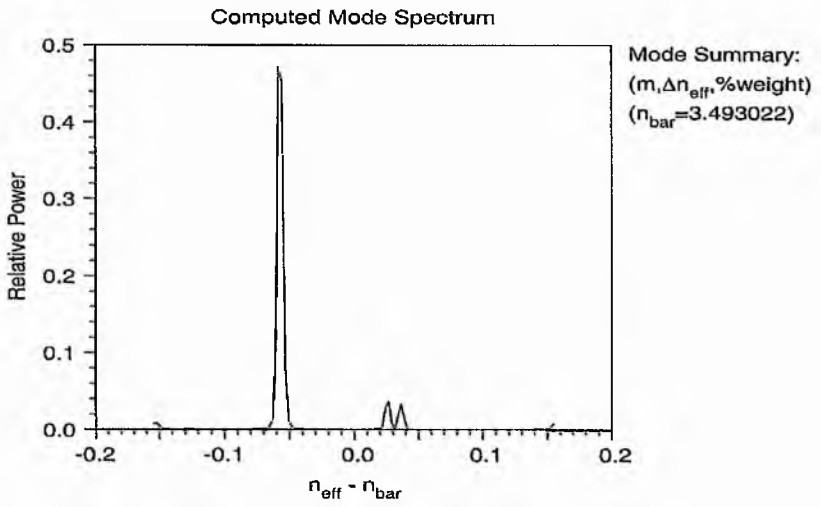


Figure 39 Beamprop ™ computed mode spectrum on a 1.5 micron ridge waveguide [121].

4.2 WAVEGUIDE DESIGN

Integrated optics in Silicon has been investigated throughout the last two decades [119, 120]. Several main components of integrated optics include optical waveguides, waveguide couplers, optical filters, optical switches and optical modulators. The main

advantage of integrated optics in Silicon is that the cost of processing the wafers is far cheaper than other materials such as III-V semiconductors and Lithium Niobate. Moreover, Silicon is a well studied material; its processing techniques are mature and widely used in the electronics industry. Optical waveguides in Silicon are possible for wavelengths greater than 1.2 micron at which Silicon is transparent.

4.3 BRAGG GRATING DESIGN

All the work presented here is based on first order Bragg Diffraction Gratings using Coupled Mode Theory. Depending on design parameters such as the grating length and the magnitude of refractive index perturbation (depth of the grating), the Bragg Grating can function as a narrowband transmission or reflection filter or a broadband mirror.

4.3.1 UNIFORM BRAGG GRATINGS

The spectrum in Figure 40 was obtained by running Gratingmod: RSoft ™ simulation software for a grating period of 228nm and a grating depth of 50nm. As well as these parameters the waveguide was chosen as 1.5 micron Silicon above a Buried Oxide layer of 1 micron and the assumed change in refractive index between the mark and space regions of the grating was chosen as from 1.0 to 3.5 i.e. from air to silicon. A series of curves were obtained for different grating depths and for example 30 nm gave relative reflected power of 0.6 to 0.7 whereas 100nm gave reflected power at about 0.99.

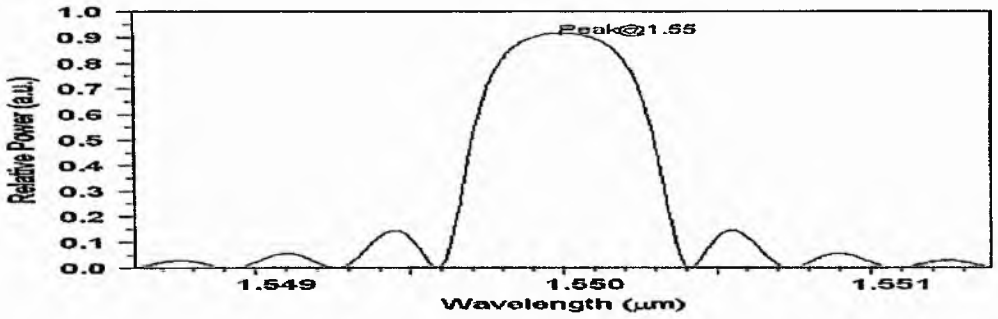


Figure 40 Gratingmod simulation of reflected power for a 1.5 micron rib waveguide with 50nm of grating with refractive index change from 3.5 to 1.5 [121].

4.3.2 Simulation

By way of introducing the method it would be helpful to explain that Suspre ™ is a simulator providing a graphic representation of implantation damage, depths etc. based on stored tables of skew Gaussian implantation results.

It can be downloaded from the implantation section of the University of Surrey website. Once downloaded and installed click on the desktop icon and the title page opens and with one left mouse click moves to the selection screen.

Select the ion in the case of the surface implant oxygen and the target in this case silicon by dragging the elemental symbol to the appropriate position on the selector chart. Next select ion flux in the case of the surface implant 10^{17} ions per square centimetre and the required ionic energy expressed as kilo electron volts again in the case of the surface implant this would be 10.

All that is required now is to press the 'new' button on the panel and a plot of various parameters including implantation range will be displayed, select the parameters you want to display by way of the selector boxes under the plot area and simply store the curves for future report/reference.

The selection screen also has selector boxes for non elemental targets such as glass, perspex or silicon nitride.

Simulation Results

In figures 41 to 44 we see the reasons for selecting Silicon Nitride as the bulk implant masking material: at 10 keV it gave little difference in terms of Suspre concentration with depth plots by comparison with Gold (which would have required a sacrificial layer).

Also Nitrogen is shown to implant slightly deeper than Oxygen because the ion is less massive and tends to implant further into the target for a given energy, see figure 45 (as Nitrogen could also be used for the implantation), and from figure 41 the Oxygen implantation would yield a surface layer at 10 keV of between 20 and 40 nm. Annealing would push this layer nearer the surface due to diffusion and surface tension effects on the lower part of the oxide layer [23, 24].

30×10^{21} ions/cc

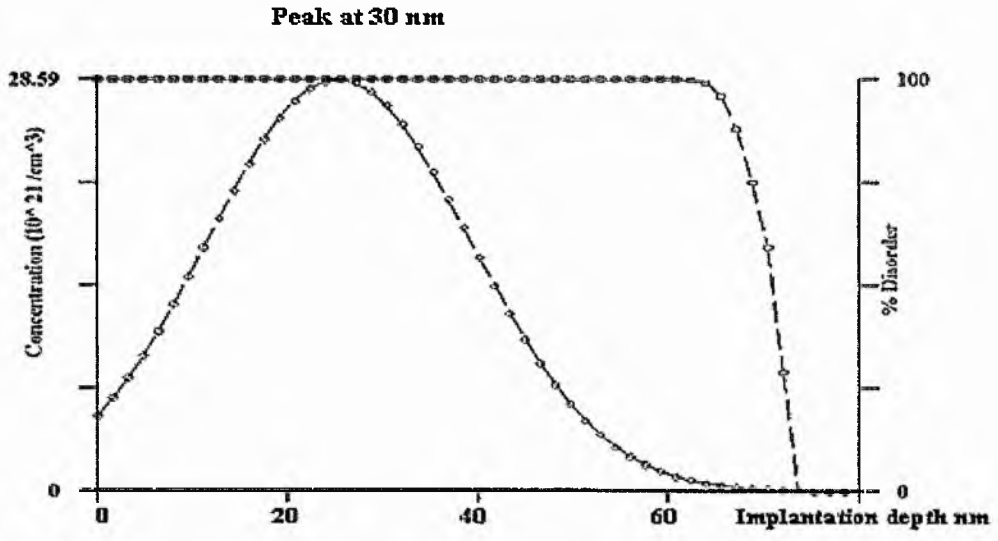


Figure 41 oxygen implanted into silicon @ 10keV and 10^{17} ions/cm^2 [54]

In figure 41 we see the peak of the implant at about 30nm. The depth of the implant after annealing might well shrink to 30 to 40nm after allowing for surface tension effects that is to say that the lower edge of the oxide layer contracts to leave the minimum surface area, also the oxygen tends to diffuse preferentially to the surface [23, 24]. In figure 42 we see the implant peak at about 70nm which would provide a good depth of grating for investigation.

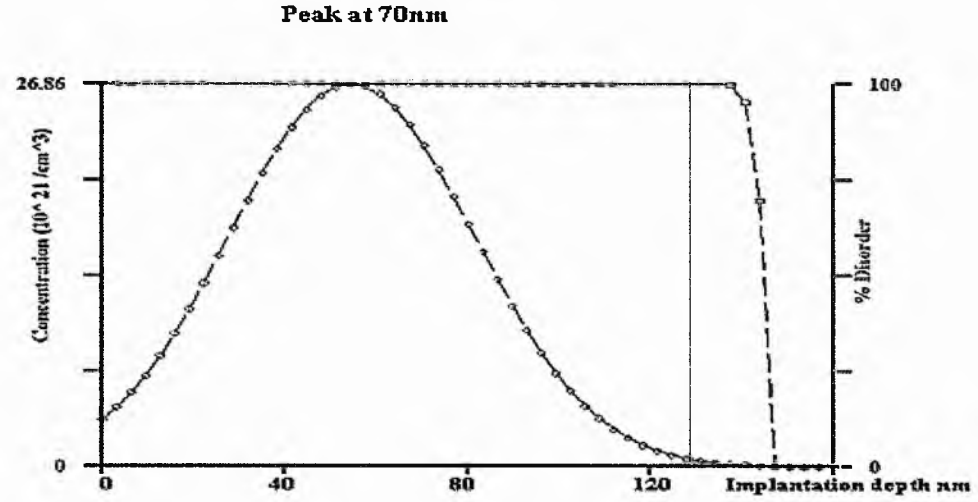


Figure 42 Implantation of oxygen into silicon @ 20keV / $1.6.10^{17}$ ions/cm^2 [54]

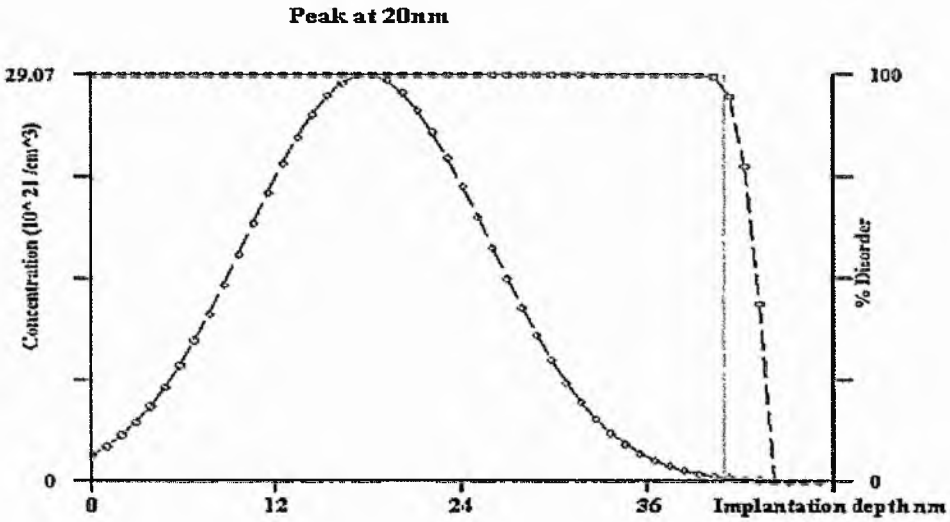


Figure 43a) Oxygen implanted into silicon nitride@ 10keV and 10^{17} ions/cm^2 [54]

In figure 43 a) and b) we see 10/20 keV oxygen implantation into Silicon Nitride with the upper limit for the implantation depth at 86nm and the disorder limit set at 80nm in 43 b).

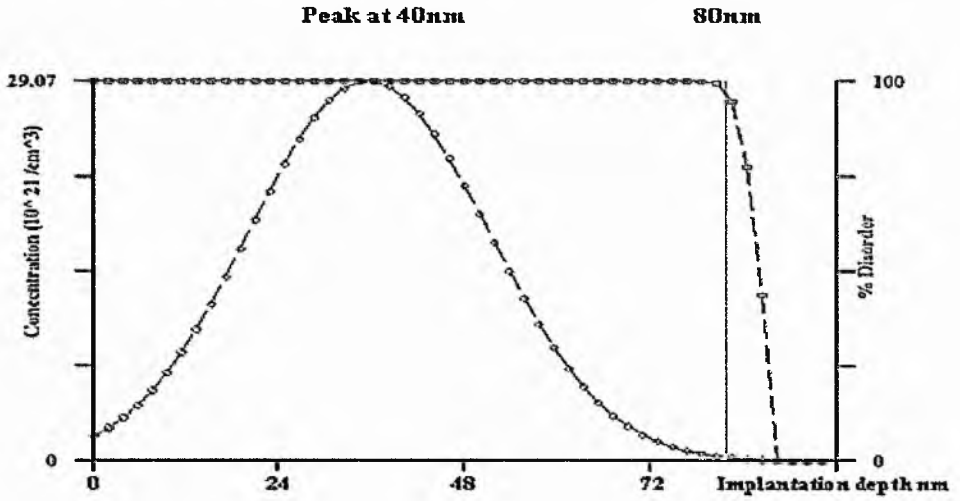


Figure 43 b) Oxygen implanted in Silicon Nitride at 20keV and 10^{17} ions/cm^2 [54]

Thus it would seem from the simulation that a 100nm layer of Silicon Nitride would suffice as a masking material for Oxygen implantation into Silicon.

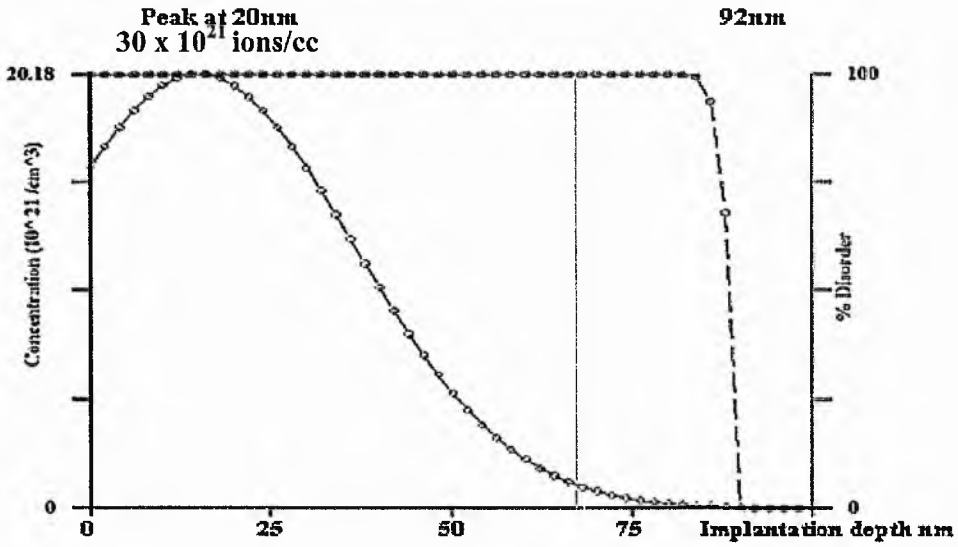


Figure 44 Oxygen in Gold @ 20keV and 10^{17} ions/cm^2 [54]

In figure 44 we see the upper limit for Oxygen implantation into Gold at 92nm from the x axis limit, however, the usage of Gold would require a Silica sacrificial layer and for this reason Silicon Nitride was considered superior as it greatly reduced manufacturing difficulties.

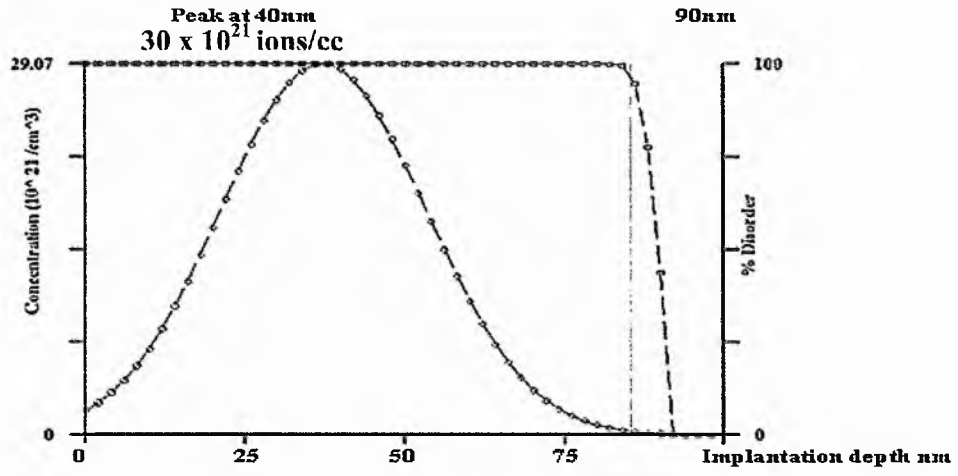


Figure 45 Nitrogen in Silicon @ 10keV and 10^{17} ions/cm^2 [54]

In Figure 45 we see the greater mobility of Nitrogen (as its atomic weight is less than Oxygen and therefore for the same kinetic energy must have a higher ionic velocity and would require more 'stopping' than oxygen ions which is accomplished by means of interaction with the silicon atom's valence band electrons) expressing itself by way

of greater implantation depth into Silicon. In Figures 46 to 50 we see a progression of simulation results (via Gratingmod [121]) for a 1.5 micron waveguide with a succession of grating depths from 30 nm to 100 nm, please note that the green plot represents transmitted power and blue reflected power.

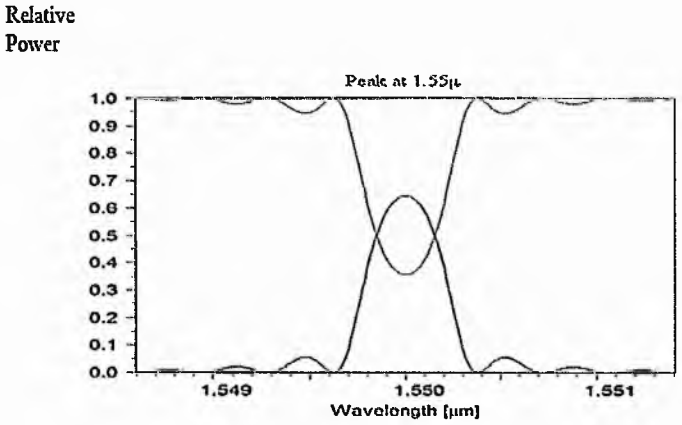


Figure 46 simulation of 30nm silica into silicon grating @ period 228nm [121]

Note that in figure 46 the peak transmittivity/reflectivity occurs at telecommunications wavelength 1.55 micron: its value being less than 70% and the small effect of the side lobes of the reflectivity spectrum.

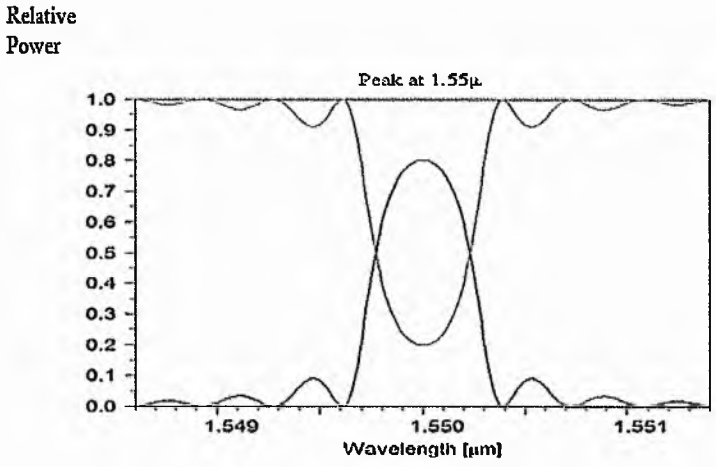


Figure 47 simulation of 40nm depth silica silicon grating @ period 228nm [121]

At 40nm grating depth in figure 47 the side lobes are still small but the peak at 1.55 micron has elevated to more than 80%.

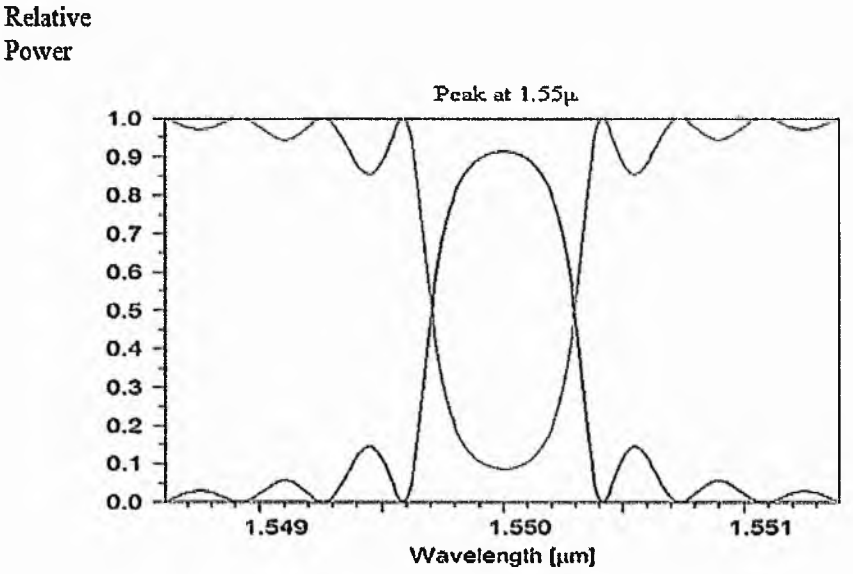


Figure 48 simulation of 50nm depth silica into silicon grating [121]

At 50nm grating depth in figure 48 the peak at 1.55 micron is now in excess of 90% and the side lobes at 15% transmittivity/reflectivity are still small.

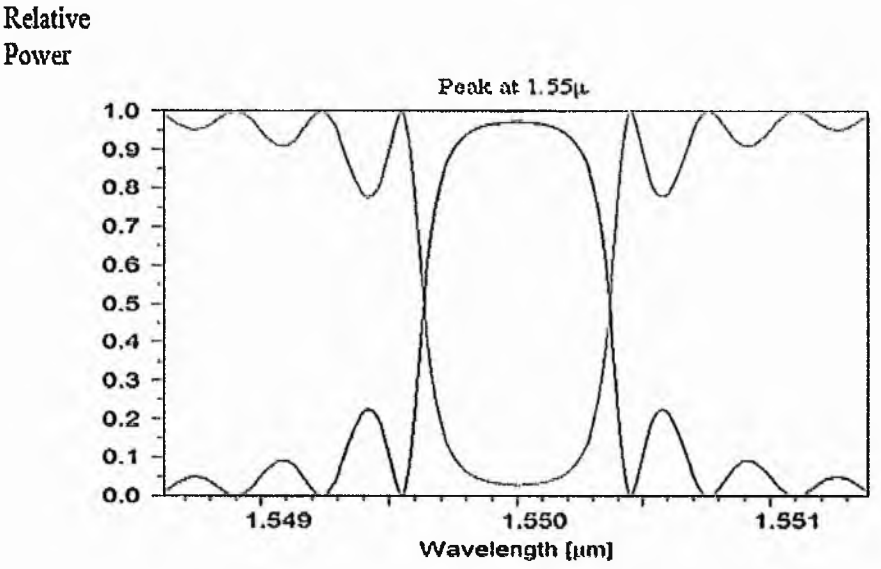


Figure 49 simulation of 80nm depth silica into silicon grating [121]

At 80nm grating depth in figure 49 the side lobes are now at 25% transmittivity/reflectivity and the peak has noticeably flattened.

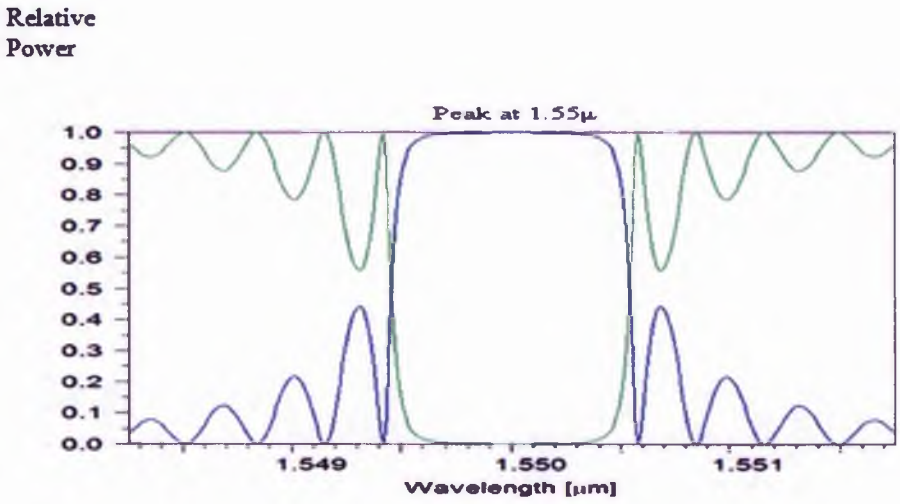


Figure 50 simulation of 100nm depth silica into silicon grating [121]

At 100nm grating depth in figure 50 the peak is much flattened and the side lobes have climbed in reflectivity to over 40%. From these curves (i.e. figures 46 to 50) the choice of a 75nm grating for a 1.5 micron waveguide would seem desirable since not only is 90% reflectivity achieved but also the need for apodisation to reduce the effect of the side lobes is reduced and this simplifies the grating design. Finally figures 51 and 52 were taken from Beamprop ™ [124] and shows negligible the power transmission down a 1.5 micron rib waveguide over 1000 micron length.

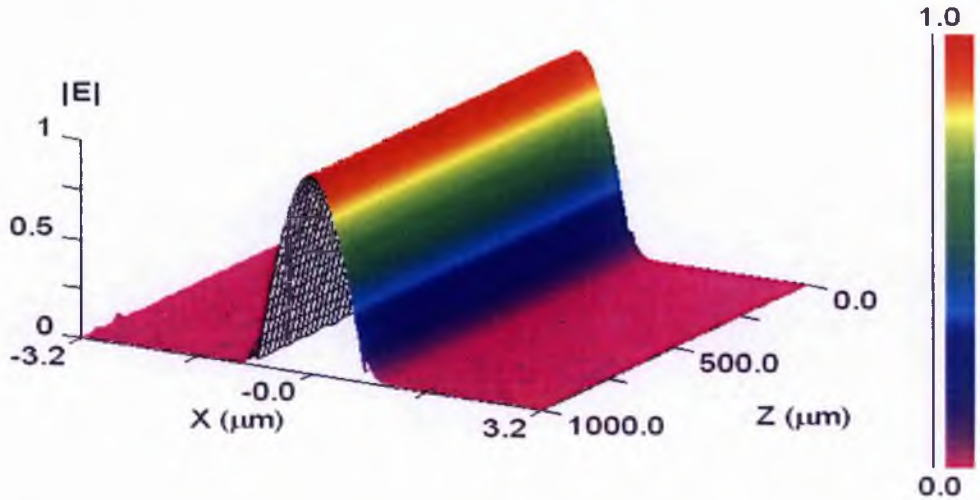


Figure 51 shows a 3D representation of power versus direction down a 1.5 micron rib waveguide [121]

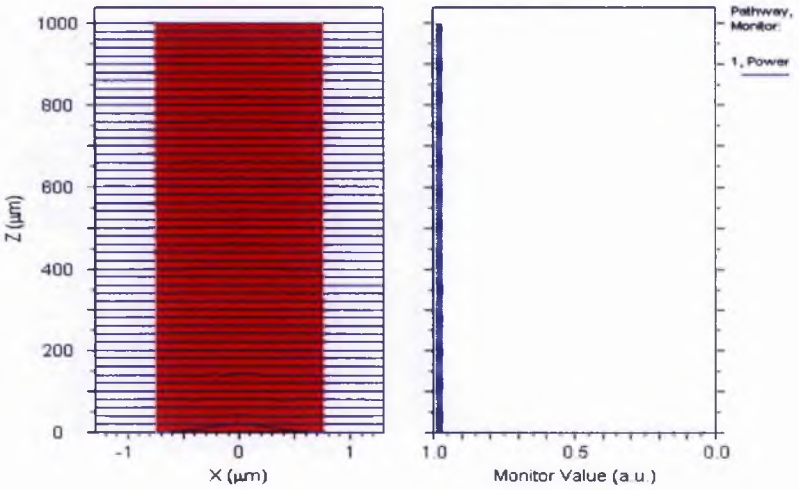


Figure 52 shows power versus Z direction for a 1.5 micron rib waveguide [121]

Figures 51 and 52 confirm that there will be negligible power loss down a z distance of 1000 micron for a 1.5 micron rib wave guide. The implantation range was modelled using Suspre simulator with a dose of $1.6x10^{17}$ O ions/cm^2 and energy of 20keV. There was a further surface implant simulated of $0.8x10^{17}$ions/cm^2 and an energy of 10keV (it was also assumed that the substrate would be at an elevated temperature of 500 degrees during implantation to minimise damage to the Silicon). The ion implantation was to be performed at Nodus, Surrey University. The simulated overall effect is shown in figure 53.

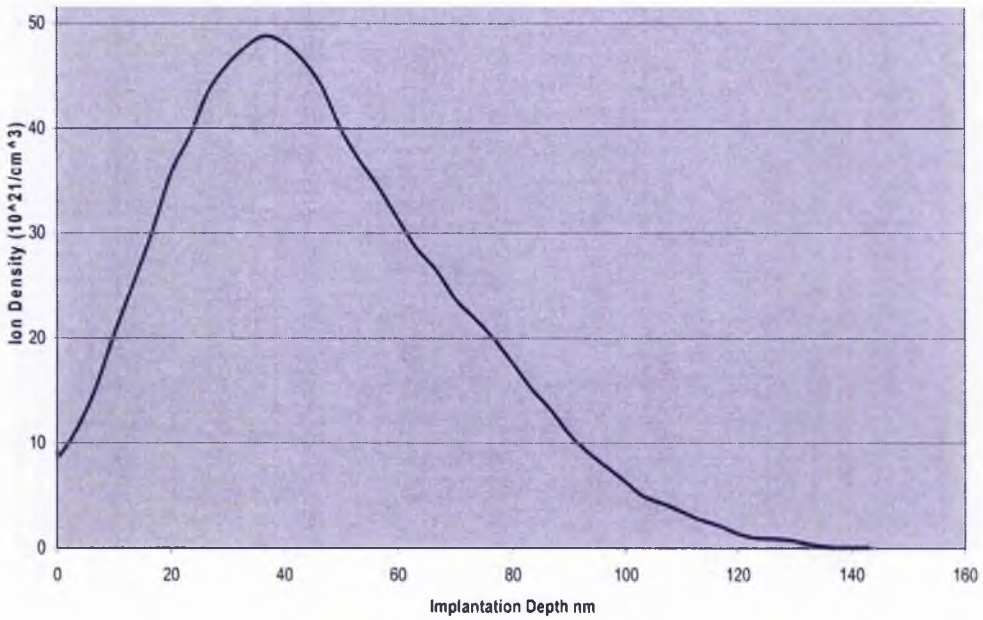


Figure 53 the simulation results for the implantation at 10 and 20 keV were added together to give a combined implant curve [54]

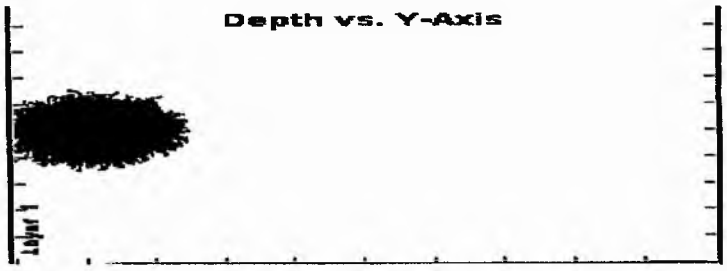


Figure 54 Srim calculation of range for 60 keV energy and straggle considerations [53]

Srim was run to check the Suspre results with a Monte Carlo type simulation see figure 54.

4.4 ELLIPSOMETRY

Ellipsometry [123] measures the change in polarization state of light reflected from the surface of a sample. For thin film sample analysis, the optical system under analysis is simply the reflection of light from the sample. The measured values can be expressed as ψ and Δ, and these are related to the ratio of the Fresnel reflection coefficients, R_p and R_s for p and s polarised light, respectively:

$$P=R_p/R_s=\tan(\psi)e^{i\Delta}. \quad (28)$$

Because ellipsometry measures the ratio of two values it can be highly accurate and very reproducible. Because the ratio is complex, it also contains 'phase' information (Δ), which makes the measurement very sensitive.

The ellipsometer used was at Surrey University and was a M-44 made by J.A.Woollam & Co. Inc. and used WVASE32 software for the computer fitting to the derived Delta and Psi curves.

The M-44 was mounted atop a Newport optical bench and the device overall was controlled via a Computer and a VB-200 (stepper) motor controller. The device took light from an incandescent lamp made it monochromatic, collimated it, and directed it

through a polariser onto the samples and examined the reflected beams via a second polariser and diode detector matrix.

The angle of incidence of the beam to the sample as well as other parameters such as the number of iterations were all set by the Computer by way of the VASE (Variable Angle Spectroscopic Ellipsometry [122]) programme incorporated into the Computer.

The first stage in determining whether an ion implantation Bragg grating was a viable solution was to perform a bulk implant on Silicon wafers and determine whether the required refractive index changes had occurred. The stages of this section of the work are listed below.

4.5 Bulk Implant

Three Silicon wafers were masked off into approximately 50 by 2mm squares at Southampton University with 100nm thick Silicon Nitride. These were ion implanted with Oxygen at Surrey University with densities of 0.3, 0.8 and 1.6 x 10^{17} ions per cc. The implantation was performed at energy of 10 keV since only a surface layer was required. The orientation of the sample was set as normal to the implantation as would be the case with a rib waveguide and the implantation temperature was set to 500°C as was customary with SIMOX. The temperature, beam current and beam size are allowed to stabilise before implantation. The ion beam is energised, collimated and filtered (to remove impurities e.g. spurious Boron from the beam). The ion beam must be set to the correct temperature and this may take several hours from cold. The temperature and energy of the beam are very important with this kind of implantation since it determines the mobility of the ions after implantation and hence the degree of approach to stoichiometry and has an effect on the annealing requirement. Some of the samples were then cleaved and annealed at 1300°C for four hours so as to give a comparison between the annealed and the as-implanted state. These samples were then investigated with scanning electron microscopy and ellipsometry to see if a surface layer of Silicon Dioxide could be detected and if so what change in refractive index had occurred because of the implantation. In terms of the experiments the ellipsometer was calibrated via a mirror surface and then the VASE ™ (Variable Angle Spectroscopic Ellipsometry [122]) windows were opened. The sample was

placed on the ellipsometer base to reflect the vertical light beam back upwards and the acquire data button was pressed on the top pull-down menus and align sample was selected to initiate the setting up of the sample and finally spectroscopic scan to run the tests at two different angles. There are two tilt screws to adjust the supporting plane and two micrometer screws to adjust the x-y position. Escape exits the programme and then follows the final set-up screen to adjust the iris and the beam on the detector to maximise the light to the detector (the latter does not vary too much once initially set up and merely needs checking to verify each time the sample is changed). The ellipsometer was then run through the spectrum from 400 to 1000 nm and six sets of results were obtained from the wafers at 0.3, 0.8 and 1.6 x 10^{17} ions/cc. These were then computer fitted to predictions based on the assumption of a Silica layer of between 20 and 30 nm and a possible fit was observed: in order to resolve the ambiguity it would be necessary to perform electron microscopy on the samples and/or to rerun the experiments with the samples in an annealed state. Once some of the cleaved samples had been annealed, both annealed and as-implanted samples were taken for examination with the scanning electron microscope. The samples were placed individually in the observation chamber of the Scanning Electron Microscope (SEM) and the chamber was closed and evacuated by way of the mechanical air pump. Then the heater was allowed to warm up and the samples were investigated initially under low magnification set by the control panel to determine the portion of the sample being observed on the monitor. Finally the magnification was increased to the uppermost limit to try and find any evidence of nanometre sized layers of Silicon Dioxide on the top of the Silicon.

Ellipsometry and SEM Results

All three implantation densities gave approximately the same depth of surface Silica 20nm for the as-implanted and 30nm for the annealed specimens (which for a 10 keV implantation energy was roughly in accord with the Suspre simulation: see the simulation section). Two differing computer models described above gave similar results although some preference must be given to the single layer model as the diminution in the interstitial layer was more in accord with the published literature [23, 24] than for the graded model. The authors reported the increasing absorption of interstitial Silica islands into the top layer with increasing severity of annealing. In this respect it might be wise to increase the annealing temperature to 1350 degrees for

the product annealing in order to virtually completely remove the interstitial layer. A refractive index lowering was reported of the same order as used in the simulation programme provided in Appendix 1 and which had given favourable reflectivity figures for Silica in Silicon gratings (i.e. 90% for 75nm implanted gratings). The usage of the highest implantation density with a 100nm Silicon Nitride mask is not to be recommended as the sputtering caused by such a high level of bombardment is liable to remove most or the entire mask: this is not the case at the lower densities. Annealed and as-implanted samples were loaded into the Scanning Electron Microscope (SEM) the chamber was evacuated using the pump and the scan was started via the amplifiers and the switch panel. The Scanning Electron Microscopy performed on the samples was inconclusive as several nanometres of electro-phosphorescence occurred at the top of the sample layers: this was repeated at different positions on different samples. The electrical charging, however, does indicate the presence of an insulator such as Silica.

Conclusions

In the case of the current project, a reduction in the dose may be necessary to reduce spreading at the edges of an implantation mask especially in terms of constructing a grating where 50/50 mark space ratio between Silicon marks to Silica spaces is desirable. A general methodology would be to reduce the dose to the critical level required for stoichiometry (i.e. 1.4×10^{18} ions /cc. or in this case 0.75×10^{18} ions/cm^2 at 15-30 keV; a surface implant might be unnecessary due to Oxygen diffusion to the surface) and, if necessary, to adjust the mark space ratio of the grating mask to provide the correct grating mark/space ratio. The table for SRIM ™ Outputs/Oxygen in Silicon, see Appendix 1 gives a worst case straggle for 20 keV Oxygen at 26 nm. It was decided to vary the mark space ratio and check its effect and therefore to proceed without further MSR consideration. Annealing at 1350 degrees C for four hours would seem to be adequate to absorb the lower Silica islands. The usage of Gold as a masking material in the grating manufacture would presumably require the presence of a Silica sacrificial layer to prevent the gold sputtering onto the exposed implanted surface. The Gold mask dimensions also need careful consideration because a high aspect ratio mask may be difficult to achieve. From figure 42 the projected range of Oxygen in Gold is given as 92 nm at 20 keV so a Gold grating mask could be achieved with a depth of 100 nm and a width of the order of 100 nm to achieve a first

order grating at a period of 228 nm. However, from figure 41 it is clear that a 100 nm mask of Silicon Nitride would suffice for 10/20 keV applications and since this would not involve the necessity of sacrificial layers this was chosen. For a 1.5 micron SOI wave guide only 75 nm of implanted Silica is required for approximately 90 % reflectivity in the grating so that the expedient of using a 1.5 micron wave guide required approximately 75 nm of Silica depth and about 15 keV of implantation energy. Since this made the masking situation simpler this was the expedient that was initially chosen. It was decided to create Bragg Gratings with variable length of grating to determine effect of length of grating with respect to attenuation. Also mark to space ratio would be varied to determine the effect on Bragg Wavelength. Gratings up to 1000 micron would be constructed thereby minimising the risk of change in periodicity which would endanger grating performance, but should nonetheless provide good attenuation cf. figure 34. First order gratings were to be made as they would provide optimal performance. Also gratings would be made using thermal oxidation as a check and also as a possible alternative means of creating flat gratings.

Footnote

N.B.

Oxygen (or for that matter nitrogen) implantation into silicon could not be simulated using Silvaco ™ simulator as it cannot cope with (these) gaseous elements.

5 Fabrication

5.1 Introduction

Two 1.5 micron SOI wafers (with a Buried Oxide layer 1 micron in thickness) were set aside for the purpose of this project. Originally the work was to have been achieved in Southampton but due to the fire at the university was redirected to Philips in Eindhoven, Holland.

Mask Design

Masks were both designed and drawn here at the University of Surrey using a programme called L-Edit ™ made by Tanner Research, Inc. [126] (see figure 55). This programme was originally designed for creating masks used to fabricate Ultra Large Scale Integration (ULSI) electronics. It allows the user to draw many different shapes with nanometre resolution. This programme is more than adequate for defining gratings as the smallest dimension used in any part of the device design is of the order of a hundred nanometres. During the photolithographic process a positive photo resist is used. This means that whatever part of the photo resist is exposed, that photo resist, and subsequently a controlled amount of Silicon under the exposed photo resist, will be coated with 100 nm of Silicon Nitride during the fabrication process. The mask therefore defines those areas that are to be exposed by light and those to be protected from it. A layout is created by drawing a series of grating structures in a predetermined area. A test chip is defined by the two gratings contained in this area plus the central non-grating area left blank for test purposes.

Figure 55 L-edit design with repetition of grating line [125].

Stages in Masking:

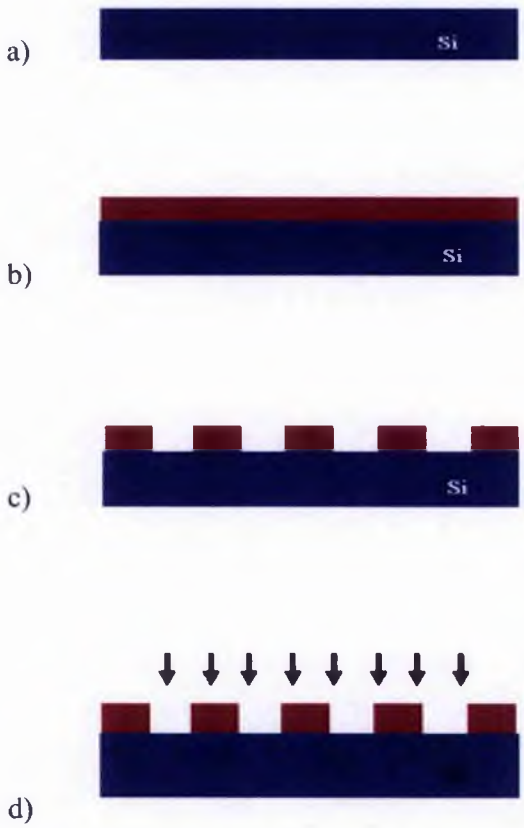


Figure 56 schematic of fabrication: Starting with SOI (a) a positive photo resist is applied (b) and the mask for the grating is e-beam written thereto (c), the exposed resist is removed and silicon nitride grown to a depth of 100nm by LPCVD and finally the Ion Implantation (d) occurs normal to the wafer at 500 degrees substrate temperature and with 1.6 x 10^{17} ions per cm squared at 20 keV.

In figure 56 we see that: An electron beam mask was prepared for both wafers from the L-Edit programme. The wafers were cleaned with fuming Nitric acid. The mask was imprinted on the wafers by exposing a 2.2 micron positive photo resist. This was then e-beam written. This was then hard baked in order to prepare for the dry etching. After this the exposed resist was stripped and the wafers cleaned again. 100nm of Silicon Nitride was deposited at 740 degrees by LPCVD (Low Pressure Chemical Vapour Deposition). The wafers were treated by electron beam lithography and then hard baked to prepare for dry etching. The unexposed areas were etched and checked visually and by Scanning Electron Microscopy to confirm adequate etching. The photo resist was then stripped. One wafer was returned via Innos to Philips at Eindhoven whilst the other was retained for implantation at Nodus.

Figure 57 shows the masking done at Philips in Eindhoven e-beam writing was used for the identification, alignment and grating masking.

Figure 57 scanning electron microscope images of the masking a) chip identification b) alignment marks C) Grating Masking and d) Grating Edge [126].

The purpose of the thermal oxidation was to simulate the oxidation of porous Silicon and thereby simulate the creation of a completely flat grating.

With this in mind the first wafer was subjected to cleaning with fuming Nitric acid. It was then wet oxidised to deposit 180+/- 5 nm of Oxide cleaned and checked. The Oxidation for the wafer from batch k4008s was done in a furnace with wet O_2 at 1000C for 20 minutes and 15 seconds.

The actual procedure from start involves:

i) Loading the wafer into the furnace at an idle temperature of 400 degrees with nitrogen flowing in the tube.

ii) Switching to dry oxygen and taking the temperature up in a ramp to 1000 degrees (ramp rate 10 degrees/minute giving a ramp up time of 60 minutes).

iii) Switching to wet oxygen for the calculated oxidation time (dry oxygen was fed through a bubbler containing de-ionised water heated to 80 degrees).

iv) Unloading in nitrogen.

A Silicon check wafer was Oxidized with the work wafer and Nanospec measurements on the check gave a thickness of 1906A (flat) 1808A (middle) 1841A (curve).

Once the work at Nodus was completed both wafers were returned to Philips where they were cleaved along the chip lines and coated with photo resist before returning to Surrey.

5.2 Thermal Oxidation

Under exposure to Oxygen, a Silicon surface Oxidizes to form Silicon Dioxide [127-129] (SiO_2). Native Silicon Dioxide is a high-quality electrical insulator and can be used as a barrier material during impurity implants or diffusion, for electrical isolation of semiconductor devices, as a component in MOS transistors, or as an interlayer dielectric in multilevel metallization structures such as multi-chip modules. The ability to form a native Oxide was one of the primary processing considerations which

led to Silicon becoming the dominant semiconductor material used in integrated circuits today.

The Oxide of Silicon, or Silicon Dioxide (SiO_2), is one of the most important ingredients in semiconductor manufacturing [127], having played a crucial role in the development of semiconductor planar processing. The formation of SiO_2 on a Silicon surface is quite often accomplished through a process called thermal oxidation. Thermal oxidation, as its name implies, is a technique that uses extremely high temperatures (usually between 700-1300 degrees C) to promote the growth rate of Oxide layers.

The thermal oxidation of SiO_2 consists of exposing the Silicon substrate to an oxidizing environment of O_2 (so called **dry oxidation**) or H_2O (**wet oxidation**) at elevated temperature, producing Oxide films whose thicknesses range from 60 to 10,000 angstroms. Oxidation of Silicon is not difficult, since Silicon has a natural inclination to form a stable Oxide even at room temperature, as long as an oxidizing ambient is present. The elevated temperature used in thermal oxidation therefore serves primarily as an accelerator of the oxidation process, resulting in thicker Oxide layers per unit of time. Thermal oxidation is accomplished using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system for moving process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes. The heating system usually consists of several heating coils that control the temperature around the furnace tubes. The wafers are placed in quartz glassware, known as boats, which are supported by fused Silica paddles inside the process tube. A boat can contain many wafers, typically 50 or more. The oxidizing agent (Oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafers where the oxidation occurs [130-133].

During **dry oxidation**, the Silicon wafer reacts with the ambient Oxygen, forming a layer of Silicon Dioxide on its surface. The reaction is as follows:

$Si + O_2 = SiO_2$

In **wet oxidation**, Hydrogen and Oxygen gases are introduced into a torch chamber where they react to form water molecules, which are then made to enter the reactor where they diffuse toward the wafers. The water molecules react with the Silicon to produce the Oxide and Hydrogen gas as a by-product:

$Si + 2\ H_2O = SiO_2 + 2H_2$

These oxidation reactions occur at the $Si\text{-}SiO_2$ interface, i.e., Silicon at the interface is consumed as oxidation takes place. As the oxide grows the $Si\text{-}SiO_2$ interface moves into the Silicon substrate. As a result, the $Si\text{-}SiO_2$ interface will always be below the original Si wafer surface. The SiO_2 surface, on the other hand, is always above the original Si surface. SiO_2 formation therefore proceeds in two directions relative to the original wafer surface.

The amount of Silicon consumed by the formation of Silicon Dioxide is also fairly predictable from the relative densities of Si and SiO_2, i.e., the thickness of Silicon consumed is 46% of the final thickness of the Oxide formed. Thus an Oxide that is 1000 Angstroms thick will consume about 460 Angstroms of Silicon from the substrate.

Wet oxidation is preferred to dry oxidation for growing thick oxides, because of the higher growth rate. However, fast oxidation leaves more dangling bonds at the silicon interface, which produce quantum states for electrons and allow current to leak along the interface. (This is called a dirty interface) Wet oxidation also yields a lower density oxide, with lower dielectric strength.

The long time required to grow a thick oxide (100nm or more) in dry oxidation makes this process impractical. Thick oxides are usually grown with a long wet oxidation bracketed by short dry ones (a dry-wet-dry cycle). The beginning and ending dry oxidations produce films of high-quality oxide at the outer and inner surfaces of the oxide layer, respectively.

Mobile metal ions can degrade performance of MOSFETS (sodium is of particular concern). However, chlorine can immobilize sodium by forming sodium chloride. Chlorine is often introduced by adding hydrogen chloride or trichloroethylene to the oxidizing medium. Its presence also increases the rate of oxidation.

Thermal oxidation can be performed on selected areas of a wafer, and blocked on others. Areas which are not to be oxidized are covered with a film of silicon nitride, which blocks diffusion of oxygen and water vapour. The nitride is removed after oxidation is complete. This process cannot produce sharp features, because lateral

(parallel to the surface) diffusion of oxidant molecules under the nitride mask causes the oxide to protrude into the masked area [151]. In figure 58 we see the silicon wafers stored in a vertical rack during the reaction the entrance aperture cap and the inlet for water vapour or dry oxygen.

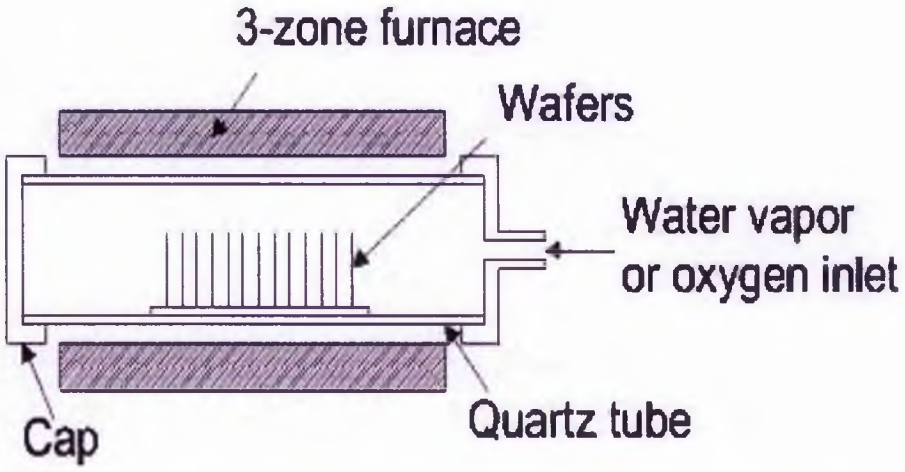


Figure 58 shows a schematic of a thermal oxide furnace with the wafers held vertically during reaction [151]

Deal and Grove performed the initial investigation into the theory of thermal oxidation [128,129]. Based on a simple model of oxidation which takes into account the reactions occurring at the two boundaries of the Oxide layer as well as the diffusion process, the general relationship in equation 34 was derived.

$$x_0^2+Ax_0=B(t+\tau) \qquad (34)$$

This relationship was shown to be in excellent agreement with oxidation data obtained over a wide range of temperature (700°–1300°C), partial pressure (0.1–1.0 atmospheres) and Oxide thickness (300–20 000 Å) for both Oxygen and water oxidants. The parameters A, B, and τ were shown to be related to the physico-chemical constants of the oxidation reaction in the predicted manner. Such detailed analysis also led to further information regarding the nature of the transported species as well as space-charge effects on the initial phase of oxidation. Kageshima et al [134] have been studying Silicon Thermal Oxidation in the atomic world by solving quantum dynamics (motion law in the atomic world) with a supercomputer. When crystalline Silicon is exposed to Oxygen gas at temperatures around 1000 degrees, the surface Silicon reacts with the Oxygen to become Silicon Oxide. Since this phenomenon (Silicon Thermal Oxidation) has various useful properties, it plays

quite an important role in the fabrication of semiconductor devices as ULSI chips which are the heart of today's electronic information and communication hardware such as cellular phones, fax machines, electronic communication switching systems, and personal computers. For similar reasons, the Silicon Thermal Oxidation will no doubt play an essential role in the fabrication of new generation semiconductor devices (e. g. Silicon Single-Electron-Transistors), as part of the future of an highly advanced information and communication society. The fabrication of these new-generation devices inevitably requires atomic control. This control is also necessary in thermal oxidation, but is quite difficult to achieve. Observations on the atomic scale reveal mysterious phenomena in thermal oxidation, such as "initial enhanced oxidation" and "pattern dependent oxidation", which cannot be explained by the conventional thermal oxidation theory. Kageshima et al [134, 135] found that in Silicon Thermal Oxidation, in addition to Oxygen sinking into the Silicon to form surface Oxide, a lot of Silicon also sinks into the surface Oxide. This Silicon penetration into the Oxide enables us to explain the "initial enhanced oxidation" naturally and consistently. Furthermore, the Silicon penetration can be expected to enable us to predict and control the "pattern dependent oxidation" with atomic precision, as well as predict and control the physical and electrical properties of the formed Oxide. However, perhaps it should be said that their research cannot entirely be fulfilled without certain situations occurring with SETs (Single Electron Transistors) etc. [134]. Nonetheless, the pre-eminence of ion implantation due to cost effectiveness and constructability in the nano-world might be replaced by a return to thermal oxidation in the world of single electron transistors (SETs).

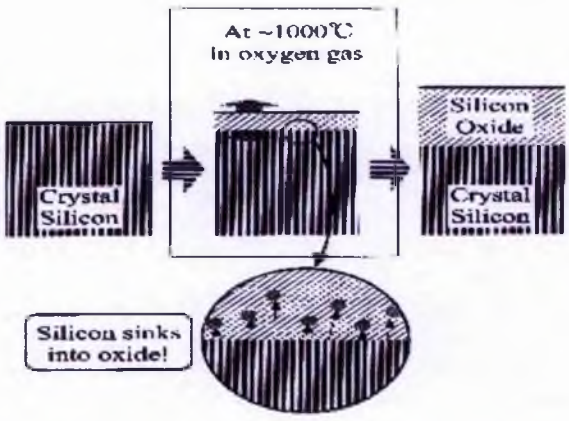


Figure 59 schematic view of thermal oxidation of silicon (Kageshima) [135].

In figure 59's schematic we see the silicon 'sinking' into the grown oxide as predicted by Kageshima's simulation and this gave better agreement with experiment over a wider range of parameters than classical theory. In figure 60 we see the superior agreement with experimental result provided by Kageshima's work.

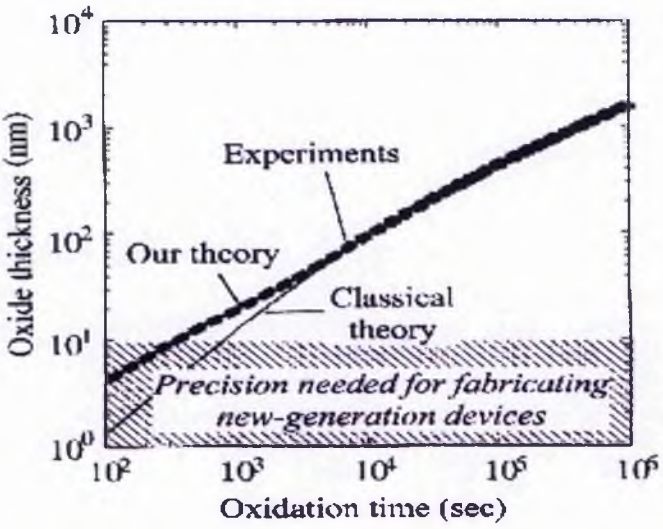


Figure 60 comparison of experimental results, new theory (Kageshima) and classical theory [135].

5.3 Ion Implantation:

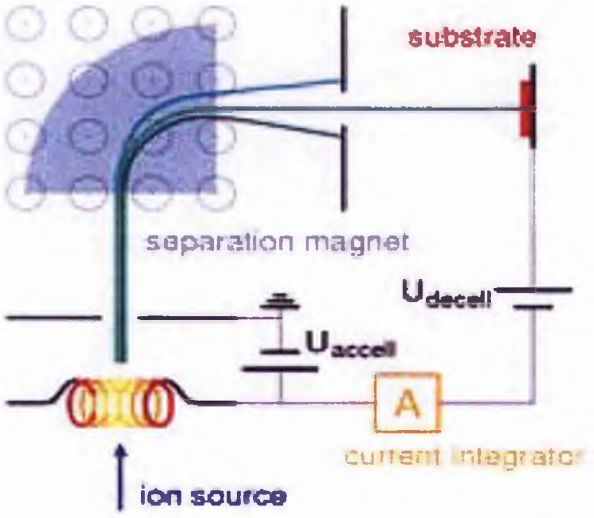


Figure 61 schematic of implanter [136].

Introduction

Ion implantation is shown in schematic in figure 61. For performing ion implantation atoms or molecules are ionised (commonly by the application of an alternating radio frequency field which has the effect of stripping the electrons from the molecules creating a plasma [137] and the positively charged ions are accelerated in an electric field out of the ionisation chamber). They are then accelerated in an electric field and purified by a mass separator (basically only the ions of the correct mass perform the correct circular motion under a magnetic field and these are the ones selected at the aperture) and implanted into the target material. A wide variety of combinations of target material and implanted ions are possible. The energy of the implanted ions can vary between several keV and several hundred keV. The range of the implanted ions in the substrate depends on the mass of the implanted ions, their energy and the mass of the substrate atoms, crystal structure and the direction of incidence [136].

The main advantages of ion implantation (in comparison to diffusion) for the doping of semiconductors are:

Short process times, good homogeneity and reproducibility of the profiles. It provides exact control of the amount of implanted ions by integrating the current. This is of particular importance for low concentrations, e.g. for adjusting the threshold voltage of MOS transistors. A relatively low temperature is required during the process. Different materials can be used for the masking, e.g. Oxide, Nitride, metals, and resist. Implantation through thin layers is possible (e.g. Silicon Dioxide or Silicon Nitride). Low penetration depth of the implanted ions. This allows modification of thin areas near the surface with high concentration gradients. Sequences of implantation steps (with different energies and doses) allow optimisation of the dopant profiles.

There are also some disadvantages such as:

Damage of the substrate is caused by the implanted ions. The change of material properties is restricted to the substrate domains close to the surface. Additional effects during or after implantation (such as channelling or diffusion see below) make it difficult to achieve very shallow profiles and to theoretically predict the exact profile shapes.

Method

Ions are created from a gaseous form of the compound which is converted into plasma by means of the electrons being stripped from the parent atoms: thus e.g. oxygen O_2 is converted into O^+ ions.

Ion implantation equipment typically consists of an ion source, where ions of the desired element are produced, an accelerator, where the ions are electro-statically accelerated to a higher energy, and a target chamber, where the ions impinge on a target, which is the material to be implanted. Each ion is typically a single atom, and thus the actual amount of material implanted in the target is the integral over time of the ion current. This amount is called the dose. The currents supplied by the implanters are typically small (microamperes) and thus the dose which can be implanted in a reasonable amount of time is small. Thus ion implantation finds application in cases where the amount of chemical change required is small.

Typical ion energies are in the range of 10 to 500 keV. Energies in the range 1 to 10 keV can be used but result in a penetration of only a few nanometres or less.

Energies below this result in very little damage to the target and fall under the designation of ion beam deposition. However, there is often great structural damage to the target and because the depth distribution is broad the net composition change at any point in the target will be small. The energy of the ions as well as the ion species and the composition of the target determine the depth of penetration of the ions in the solid: a mono-energetic ion beam will generally have a broad depth distribution. The average penetration depth is called the range of the ions. Under typical circumstances ion ranges will be between 10 nanometres and 1 micron. Thus ion implantation is especially useful in cases where the chemical or structural change is desired to be near the surface of the target. Ions gradually lose their energy as they travel through the solid both from occasional collisions with target atoms (which cause abrupt energy transfers) and from a mild drag from the overlap of any electron orbital in proximity which is a continuous process. The loss of ion energy in the target is called stopping.

The introduction of dopants in a semiconductor is the most common application of ion implantation. In semiconductor production doping refers to the process of intentionally introducing impurities into an extremely pure (also referred to as intrinsic) semiconductor in order to change its electrical properties. The impurities are

dependant upon the type of semiconductor. Lightly and moderately doped semiconductor is referred to as extrinsic. A semiconductor which is doped to such high levels that it acts more like a conductor is called degenerate. Some dopants are generally added as the (usually Silicon) boule is grown giving each wafer an almost uniform initial doping. To define circuit elements selected areas (typically controlled by photolithography) are further doped by such processes as diffusion and ion implantation, the latter method being more popular in large production runs due to its better controllability. The number of dopant atoms needed to create a difference in the availability of a semiconductor to conduct is very small. Where a comparatively small number of dopant atoms are added (of the order of 1 every 100,000,000 atoms) then the doping is said to be low or light. Where many more are added (of the order of 1 in 10,000) then the doping is referred to as heavy or high. This is often shown as n^+ for n-type dopant or p^+ for p-type doping. Dopant ions such as Boron, Phosphorus or Arsenic are generally created from a gas source so that the purity of the source can be very high. These gases tend to be very hazardous. When implanted in a semiconductor each dopant atom creates a charge carrier in the semiconductor (hole or electron depending on if it is a p-type or n-type dopant) thus modifying the conductivity of the semiconductor in its vicinity.

Silicon-on-Insulator

SOI wafers are produced by one of two main methods both of which rely on ion implantation:

Simox: Separation by Implantation of Oxygen: Oxygen can be implanted at high energy into a Silicon substrate at a high enough dose that subsequent high temperature annealing forms an Oxide layer underneath the surface layer of Silicon. The Oxide is an insulator thus producing the Silicon-on-Insulator structure.

Smart Cut ™:

First Oxidised surfaces are grown on two wafers and then bonded together. Most of the top wafer is then cleaved away along a band of Hydrogen bubbles which form from implanted ions. The thin layer of Silicon that is left behind is isolated from the substrate by what were originally the surface Oxide layers [20].

Crystallographic damage

Each individual ion produces many point defects in the target crystal on impact such as vacancies and interstitials. Vacancies are crystal lattice points unoccupied by an atom: in this case the ion collides with a target atom resulting in transfer of a significant amount of energy to the target atom such that it leaves its crystal site. This target atom then itself becomes a projectile in the solid and can cause successive collision events. Interstitials result when such atoms (or the original ion itself) come to rest in the solid but find no vacant space in the lattice to reside. These point defects can migrate and cluster with each other resulting in dislocation loops and other defects.

Damage recovery

Because ion implantation causes damage to the crystal structure of the target which is often unwanted ion implantation processing is often followed by thermal annealing. This can be referred to as damage recovery.

Sputtering is a physical process whereby atoms in a solid target material are ejected into the gas phase due to bombardment of the material by energetic ions. Sputtering is largely driven by momentum exchange between the ions and atoms in the material due to collisions. The process can be thought of as atomic billiards with the ion (cue ball) striking a large cluster of close-packed atoms (billiard balls). Although the first collision pushes atoms deeper into the cluster subsequent collisions between the atoms can result in some of the atoms near the surface being ejected away from the cluster. The number of atoms ejected from the surface per incident ion is called the sputter yield and is an important measure of the efficiency of the sputtering process. Other things the sputter yield depends on are the energy of the incident ions, the masses of the ions and target atoms and the binding energy of atoms in the solid. The ions for the sputtering process are supplied by plasma that is induced in the sputtering equipment (plasma is typically an ionised gas and is usually considered to be a distinct phase of matter in contrast to solids, liquids and gases. Ionised means that at least one electron has been dissociated from a proportion of the atoms or molecules. The free electric charges make the plasma electrically conductive so that it responds strongly to electromagnetic fields). In practice a variety of techniques are used to modify the plasma properties, especially ion density, to achieve the optimum sputtering conditions, including usage of RF (Radio Frequency) alternating current,

utilisation of magnetic fields, and application of a bias voltage to the target. Sputtered atoms ejected into the gas phase are not in their thermodynamic equilibrium state. Deposition of the sputtered material tends to occur on all surfaces inside the vacuum chamber. Sputtering is used extensively in the semiconductor industry to deposit thin films of various materials in integrated circuit processing. Thin antireflection coatings on glass for optical applications are also deposited by sputtering. Perhaps the most familiar products of sputtering are low emissive coatings on glass used in double glazing. The coating is a multi-layer containing silver and metal oxides such as Zinc Oxide, Tin Oxide or Titanium Oxide. Some of the collision events result in atoms being ejected from the surface and thus ion implantation will slowly etch away a surface. The effect is only appreciable for very large doses.

Ion channelling If there is a crystallographic structure to the target and especially in semiconductor substrates where the crystal structure is more open, particular crystallographic directions offer much lower stopping than other directions. The result is that the range of an ion can be much longer if the ion travels exactly along a particular direction, for example the <110> direction in Silicon and other diamond cubic materials. This effect is called ion channelling and like all the channelling effects is highly non-linear, with small variations from perfect orientation resulting in extreme differences in implantation depth. For this reason most implantation is carried out a few degrees off-axis where tiny alignment errors will have more predictable effects. Ion channelling can be used directly in Rutherford backscattering and related techniques as an analytical method to determine the amount and depth profile of damage in crystalline thin film materials.

Diffusion

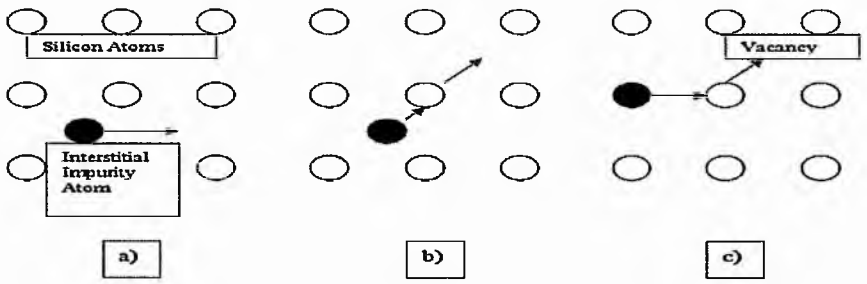


Figure 62 shows the three possibilities for impurity take up in silicon [139].

In figure 62 we see the three possibilities for 2D diffusion (a) where the impurity ion moves amongst vacancies in the Silicon lattice (b) where the impurity ion replaces a Silicon atom in the lattice and the Silicon ion is displaced to an interstitial site and (c) where the impurity ions do not replace Silicon atoms in the crystal lattice but remain in the interstices. This makes exact implantation profiles more difficult to predict [139] since it is not possible to whether implanted ions will displace lattice atoms or remain interstitial.

RBS or Rutherford Backscattering Spectrometry [140] is an analytical technique in materials science. It is named after Ernest Rutherford who in 1911 first explained Geiger and Marsden's experimental results for alpha particle scattering from a very thin Gold foil in a backward direction by using the Coulomb electrostatic force between the positively charged nucleus and the positively charged alpha particle. A detector is placed such that particles which scatter from the sample at close to a 180 degree angle will be collected. The energy of these ions will depend on their incident energy and on the mass of the sample atom which they hit, because the amount of energy transferred to the sample atom in the collision depends on the ratio of masses between the ion and the sample atom. Thus measuring the energy of scattered ions indicates the chemical composition of the sample. Additionally in the case that the incident ion doesn't hit any of the atoms near the surface of the sample but instead hits an atom deeper in the incident ion loses energy gradually as it passes through the solid and again as it leaves the solid. This means that RBS can be used as a means to perform a depth profile of the composition of the sample. This is especially useful in analysis of thin-film materials. For example films about half a micron in thickness can be profiled using a 2 MeV Helium beam, or films up to about 1 micron thick can be profiled with a 2 MeV Hydrogen beam. RBS is now a very widely used analytical technique which has the great advantage that it is absolute: requiring no standards for quantification. It is one of a family of techniques collectively known as ion beam analysis.

Ion beams are used extensively to both process and characterise materials. In the keV to MeV energy range, for example, ion beams are used to implant dopant atoms into the interior of a semi-conducting wafer to alter its electronic properties. A p-n junction, for example, can be produced by implanting Boron into n-type Silicon substrate, see figure 63.

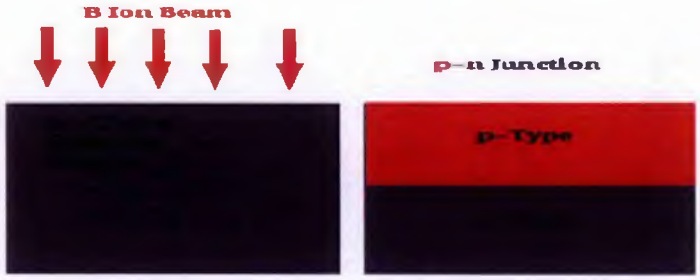


Figure 63 creation of a p-n junction by implanting boron into n-type [141]

Two other examples of the use of ion beams as a materials fabrication tool are ion-beam synthesis and ion-assisted growth. Rather than implant ions into a substrate ion-beam synthesis deposits atoms at or near the surface of a substrate. Because the ions are deposited at relatively high energies this technique can be used to produce materials with metastable structures. In ion-beam assisted deposition an ion beam is used to locally deposit energy at the surface of a substrate. Inert ions like Argon can be used to add extra kinetic energy at a substrate while other low energy gas phase species are simultaneously deposited both techniques are shown in figure 64.

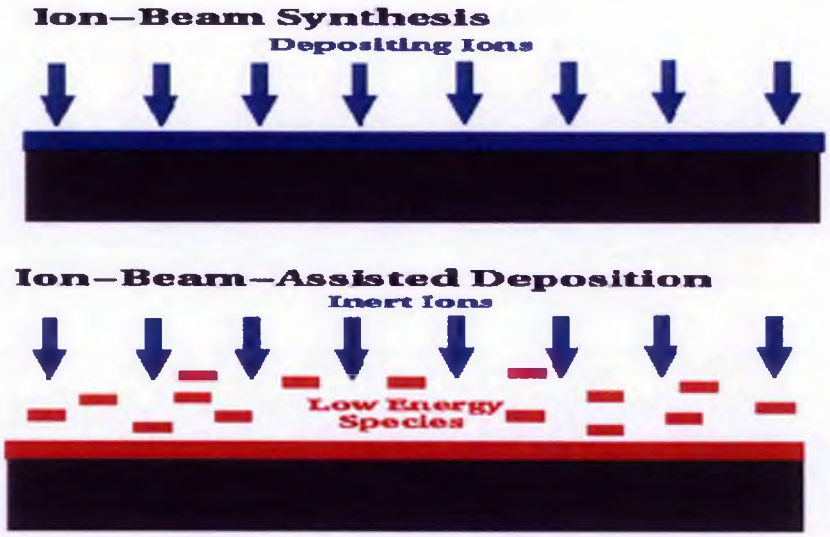


Figure 64 shows Ion Beam Synthesis/Deposition [141]

Both ion-beam synthesis and ion-assisted growth can also be used to 'densify' materials by knocking atoms into voids and other defects that may occur during the vapour deposition of materials, the process is shown in figure 65.

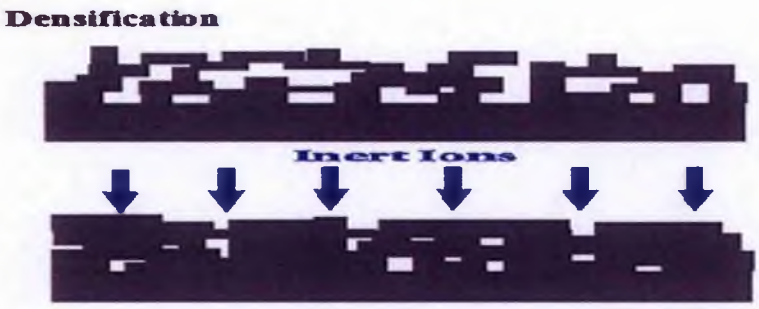


Figure 65 shows the principle of Densification [141]

Ion beams can also be used as a fabrication tool. Focussed Ion Beams, for example, have been used to produce micron-scale (and sometimes smaller) features on solid substrates. Ion beams have also been used to machine scanning-probe microscopy tips into well defined shapes. These are needed to accurately measure surface topologies using Atomic-Force Microscopy. By measuring the mass of ions sputtered from a substrate the composition of a solid as a function of depth can be determined.

Ion Implantation on the Second Wafer

The second 1.5 micron SOI wafer was implanted at Nodus, Surrey University on the second of June 2006. Oxygen ions in the form O_2^+ were used for the implant. Initially ions were implanted at 20 keV and at a dose of 1.6×10^{17} ions/cm^2 and a second implant was performed at 10 keV with a dose of 5×10^{16} ions/cm^2. The implantation was performed at a temperature of 500 degrees by virtue of an optical lamp heater assembly. After this the wafer was reunited with its partner in batch k4800s and returned to Philips in Eindhoven where both were sawed to provide individual chips for investigation.

5.4 Polishing

Polishing is required before the chip can be tested as its edges will be rough after sawing.

The tool consists of a variable speed rotating 8 inch platen (figure 68) onto which is mounted a grinding/polishing disc which is held in place by a metal retaining ring. In order to 'lubricate' the polishing disc and wash away polished off debris and a water jet is turned on for the duration of the polishing.

A dedicated sample holder was designed for use with this polisher and the chips are held onto it by clear wax. The sample holder is shown in figure 67 and consists of several parts a grooved mount and height adjusting strips (figure 66) as well as the

holder itself. The holder and mount and strips if required are positioned on the top of the hotplate so that on reaching about 150 degrees melted wax can be put onto the sides of the holder so as to hold the chips in place by capillary action until the wax has hardened on removal from the plate and cooling.

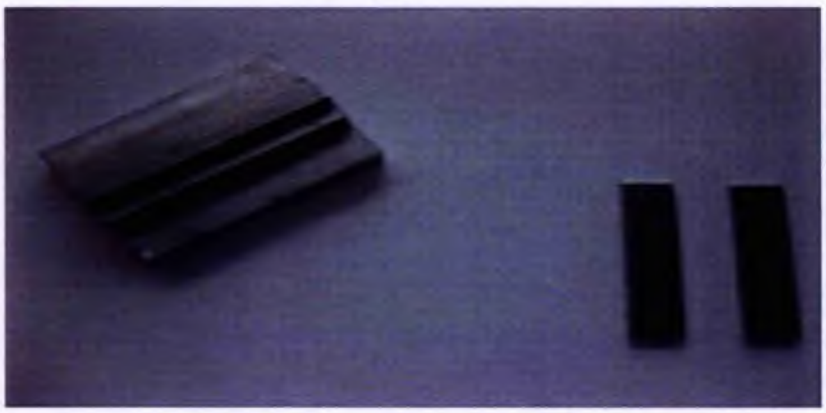


Figure 66 the Sample Holder Carrier (and two height adjusting strips for small chips).

The sample holder itself (figure 67) is an Aluminium block with two holes drilled through it and a groove machined underneath. The holes are intended as tweezers gripping points to assist with locating the holder prior to polishing and its removal after polishing.

The machined groove is intended to help locate the sample holder in its mount which will be used to locate and fix the chips with wax and it can be used to view the top faces of the chips under the microscopes as well as the removal of the chips once polishing is complete.

The sample holder mount comprises a block of Aluminium into which a ridge has been milled for locating the sample holder to stop it moving when the test chips are being located. Strips of Aluminium are placed onto the mount to act as wedges to locate the chips higher or lower according to chip size (see figure 66). The sample holder is held in place above the platen by a retaining ring which is in turn connected to a cantilever arm [143]. To ensure contact between the samples and the polishing pad, a spring loaded sample holder clamp is used (see figure 68).

The actual procedure for mounting the chips is as follows: The sample holder, mount and height adjustment strips, are placed on a thermostatically controlled hot plate and

allowed to heat up to a temperature greater than about 150 degrees such as is sufficient to melt the wax used for holding the chip to the sample holder.

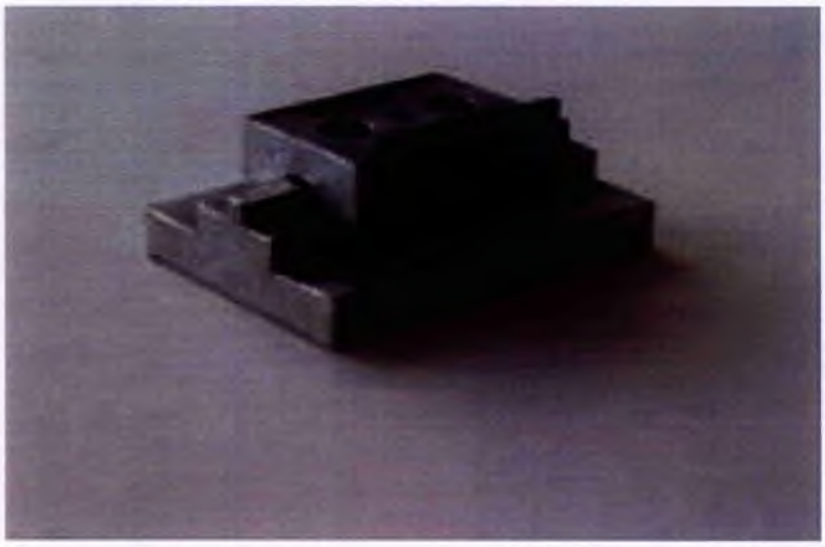


Figure 67 Sample, Sample Holder and Mount

Around this temperature [143] the clear wax begins to melt. Wax is touched to a separate Aluminium block on the top of the heater plate and a small amount is allowed to melt onto it. Some of this is then applied to the long sides of the sample mount: care must be taken at this stage as too much will cause the sample mount and sample mount holder to stick together on cooling. Using plastic tweezers the chips are then located on the top of the sample holder and gently pushed into a vertical position using a Q-tip cotton bud: it is good to note at this point that the chip is held in place by the surface tension of the melted wax since if this is so then the mount and holder may be gently removed from the hotplate and allowed to cool without any movement on the part of the chip. This method is repeated for both sides of the holder: it is important to note that the holder must be balanced so if the user has only one sample then a dummy chip must be used on the second side of the holder. When the mount and holder are cool, the sample holder can be removed from the mount. If the sample holder is sticking to the mount, small force may be applied between the holder and the mount with a small screwdriver or similar. If this method is unsuccessful, the mount/holder will have to be reheated, the test chips removed, and then the mount and holder can be separated. The individual pieces should then be allowed to cool down and subsequently cleaned with acetone before attempting to mount the test chips

again. Prior to placing the sample holder on the polisher, a polishing film is placed on the plate and locked down with the polishing pad retaining ring. It is important to check the surface of the plate for debris prior to adding the film as even the smallest contaminants can push up on the film causing scratching on the facet surface. Thus the plate surface is usually rinsed with the water nozzle prior to adding the film. The film is then placed at the edge of the plate and slid on to not only displace any debris and water, but also to remove any air bubbles trapped between the plate and film. In figure 68 is shown the outer metal retaining ring, glass platen, sample holder and retaining clamp. In order to mount the silicon carbide or alumina paper it is first necessary to remove the outer metal retaining ring and clean the platen with a wet tissue and locate the grinding paper and replace the outer ring. The chip and its holder are place in one of the holes in the sample holder and the retaining clamp is applied. Depending on the nature of the work two to one half rings of extra pressure are applied from the spring prodder: one half for finer work.

Figure 68 Outer Metal Retaining Ring Glass platen, Sample Holder and Retaining Clamp.

The metal retaining ring is then pushed down along the rim of the plate, holding the film in place. The sample holder is placed in one of the holes in the sample holder retaining ring as shown in Figure 68. The spring loaded pressure arm prod is then lowered onto the top of the sample holder. The arm has evenly spaced lines scribed around it. These lines act as a qualitative measure of the applied pressure. Typically the prod is pushed one line lower than its free locating position. The clamp is pushed down to this level and locked into place using the Allen head screw on the side of the

upper ring. To remove the sample holder, the above steps are carried out in reverse. The water nozzle is then turned on and aligned so that it sprays toward the centre of the plate through the hole diametrically opposite the one containing the sample. The plate rotation is then turned on, starting the polishing sequence with the desired grit size film placed on the plate. Because there are so many factors that affect the polishing quality, sample preparation is far from an exact science. Regardless, the following recipe is given as it has been found to be repeatable and has provided good facet quality. For fine polishing Aluminium Oxide (AlO_2) film was used due to availability and cost and for the initial coarse polishing Silicon Carbide paper was used. For initial polishing and for uses where large amounts of material removal are necessary a 2400 Silicon Carbide sheet is used in the right hand Metaserv polisher (if the surface is very rough then 1200 Silicon Carbide can be used for two minutes on each facet but for most sawing applications this should not be necessary). The sample holder is placed in the polisher and the water nozzle is turned on as discussed above. The plate rotation is then turned on and set to a speed of approximately 100rpm. As the initial polish sets the stage for the future polishing steps, care should be taken to ensure that the sample holder is seated properly in the sample holder retaining ring and that the pressure arm is centred in the middle of the sample holder. After ten minutes of polishing, the samples are removed and observed under a microscope. The front face of each of the test chips should be observed to see if the necessary amount of removal has occurred and that a significant angle is not being formed across the chip. An angle can be observed by visually comparing the chip and carrier edge. If a considerable tilt should be observed across the test chip, the test chip can be put back into the polisher and the pressure arm can be pulled slightly to the side of the test chip that requires the removal of more material. Polishing with this first coarse film should also be continued until any chips caused by the dicing saw are removed. Once the desired material removal is achieved, the sample holder is removed from the polisher and turned over to polish the opposite facets. Even if very little or no material is required to be removed (such as the inner edges of a die cut in half) it is still a good idea to begin with the 2400. It quickly removes chips and scratches that may have occurred during the dicing and also helps to remove any tilts in the chip with respect to each other that may have occurred when the test chips were attached to the sample holder. With this polishing film, the die edges should have a shiny metallic look when observed under a low magnification (e.g. 40 times magnification) microscope. When

the desired amount of material has been removed from both sides of the test chip, the 2400 film is removed from the polisher and replaced with a 4000 Silicon Carbide paper. Before starting to polish with this pad, the test chip, especially their facets, are cleaned with water and a cotton bud. As the removed material from the previous film is of the order of microns, it can contaminate the 4000 film. It was found that a speed of 75rpm or less gave the best results with this film and it is recommended to touch the top of the push rod and holder sides at the start of polishing to check for any judder and if necessary reseat the holder if all is well a polishing time of ten minutes is recommended. Material removal is no longer as much a concern as it was for the 2400 pad. The focus of the polishing from here forward is to reduce the depth of the scratches on the facets. Therefore when using these films the scratch pattern on the edges of the chips should be observed. The scratches should all lie in the same direction. If they are not then the sample holder should be placed back on the polisher for a longer period of time. When all of the scratches lie in the same direction, it is an indication that the pad has uniformly polished the entire edge of the chip. With this polishing film, the die edges should look mainly black with uniform scratches in the same direction when observed under a low magnification (40 times) microscope. Both edges of each die should be polished with this pad before proceeding to the next pad. Polishing with this pad usually takes about ten minutes but the time is dependent on how long it takes to obtain a uniform scratch pattern on the edges. Both test chips, especially the facets, are cleaned with a damp cotton swab before proceeding to the next polishing step. A 1 micron Aluminium Oxide sheet (yellow) is used next. This is used in the left hand Metaserv as this has a glass plate for the purpose and using a different Metaserv may help to reduce contamination which could cause unwanted scratching during the later stages of fine polishing. The glass plate must be cleaned with a tissue and running water prior to placing the yellow sheet, also the sheet must not be touched and must be slid using tweezers onto the wet glass plate to ensure clean bubble free contact (the same procedure applies to the 0.3 micron sheet discussed later, also in the left hand Metaserv). With this film the speed of the plate is set to 50 rpm, the minimum speed of the wheel. It is important to check for judder with the left hand Metaserv and clean and reseat the sample holder as and if necessary. The amount of material removed with this pad is minimal so longer polishing times are allowed (e.g. ten to twenty minutes). The edges of the chips should be checked every five minutes or so. Under a low magnification (40 times)

microscope the edges should start to take on a blackish appearance with no real observable scratch pattern. Both sides of the chips are polished with this pad before continuing to the final pad. The dies are cleaned one final time before continuing with the final polishing film. A 0.3 micron AlO_2 film is used as the final polishing film (for ultra fine work, for example where reflection measurements were to be taken, a 0.05 micron film could be used but it may be necessary to expand the polishing time to the order of one hour per facet with considerable increase in the risk of contamination. Also if it is considered that a grinding sheet had become worn or damaged during the course of polishing one facet then it is advisable to replace the sheet rather than run the risk of serious scratching on the next facet). The optimal speed for this film was found to be 50 rpm. The time taken on this film is the most variable of the films as it depends on the quality of the facets. After 10 minutes of polishing with this pad the individual facets are checked under a high power microscope (100-200 times) for scratches. A trade-off is ultimately made during this polishing step between time and the chip facet quality. Also, the longer the chips are polished, the higher the risk a contaminant may be introduced during the polishing. If there are an unacceptable number of scratches observed on the facets or if the quality of the facets decreases over time, the film should be replaced with a new one. When an adequate polish has been achieved (probably after about 10-20 minutes per facet), the sample holder is placed back on the sample holder mount. Both are then placed back on the hot plate in order to melt the wax attaching the test chips to the sample holder. The height adjustment strips are not used for this step. After several minutes on the hot plate the test chips will begin to slide downward. At this point a pair of plastic tweezers may be used to slide the test chip horizontally off of the sample holder, taking care not to touch the freshly polished edges. The chips are then placed on a tissue and allowed to cool. The sample holder and mount are then removed from the hot plate and allowed to cool. Acetone soaked cotton swabs are used to remove any residual wax from the back of the test chips. When the backside of the test chip is clean, a fresh Acetone soaked cotton swab is used to wipe down the polished edges. Only one swipe should be made with a single swab to prevent further contamination of the facet area. The sample holder should also be cleaned to prevent the build-up of wax. The AlO_2 films, however, are relatively inexpensive and therefore should be discarded after being used as the likelihood of contamination through multiple handlings is high. The initial test

chips obtained from the processed wafers were prepared using the sample preparation method discussed above.

Footnote

N.B. The ion as-implanted samples are blue due to Silicon Nitride with yellowish grating areas presumably caused by sputtering whereas the thermal-oxide samples are of a purple hue.

6 Experimental Techniques

Introduction

A series of scans were taken of all the samples in transmission, which is passing polarised laser light through the sample and measuring how much the sample grating absorbs at a given wavelength. In figure 69 we see the setup required for transmission testing: a variable laser output is taken to the sample via a single mode fibre and polariser and thence passes to a detector under computer control to record the scans. In b) we see the pens used to setup the optics on the monitor screen, the T metal sample holder, the carbon tipped tweezers used to place the sample on the holder with minimal damage and the IR to visible convertor: invaluable for tracing IR optics.

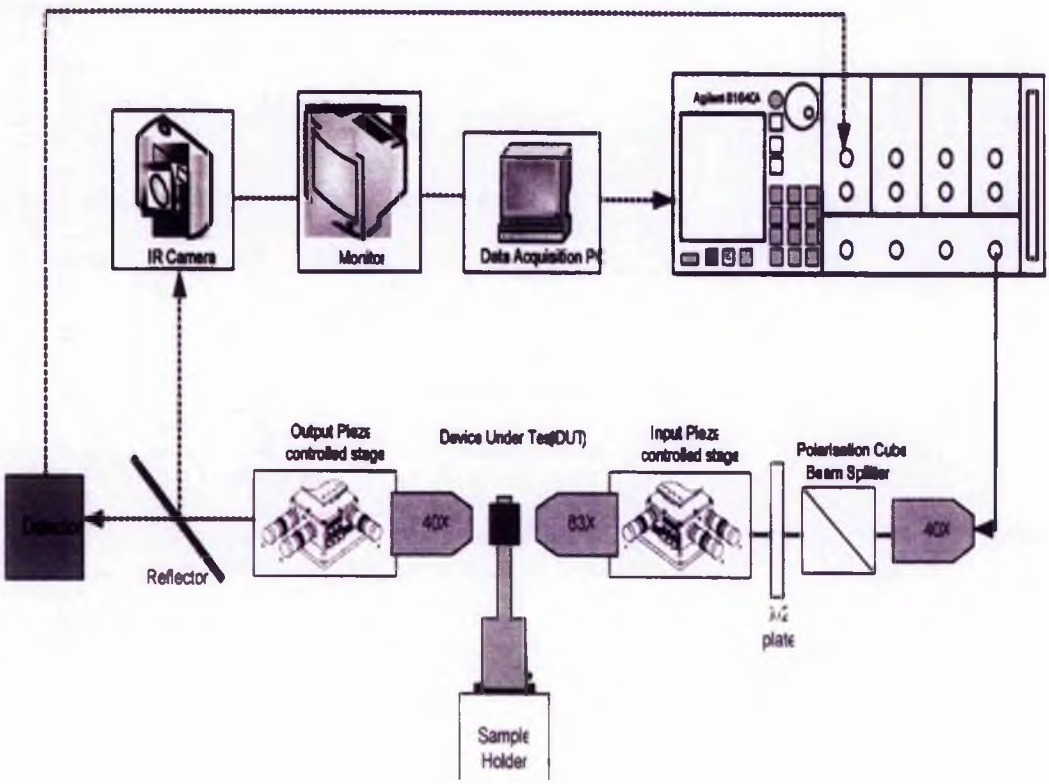


Figure 69 (a) Schematic showing setup for transmission grating characterization

Figure 69 (b) tools of optical setup, 1) Washable markers for monitor marking, 2) T shaped bar for mounting chips, 3) Carbon tipped tweezers for holding chips whilst mounting and 4) IR sensitive light pad for locating laser beam.

Equipment:

1 A tunable laser

2 A Single Mode (SM) fibre to couple light into the waveguide

3 Two micrometer controlled xyz set-ups to ensure optimal coupling into and out of the wave guide

4 A 50 micron diameter Multi-Mode (MM) pick-up fibre to collect light from the other end of the waveguide or just free space coupling to the detector.

5 A power meter to measure the power in the light emerging from the waveguide.

Procedure:

Introduction:

The set-up is obtained by shining light from an incandescent lamp onto the SOI, an image of the top layer is obtained on the monitor and left hand xyz focussing achieved. Thereafter focussing is obtained on the right hand entry side by taking the light from the fibre bundle to the input lens and observing the transfer through the top layer. Next the laser is turned on and the set-up completed to provide the best image of the laser spot on the monitor and the best power at the detector. Once this has occurred a scan is initiated on the National Instruments ™ software and the results recorded. A polarizer is used to separate TE and TM scans.

Detail:

In order to prepare for running a scan the correct size of metal T shaped chip carrier is first located and clamped into place on the micrometer controlled x-z variable assembly located to the front of setup1. When placing the chip on the carrier care must be taken, firstly to avoid getting finger grease or other contamination on the carbon tipped tweezers used to grasp the chip and secondly on removing the chip from its sample box as the chip easily separates with force from its sticky backed location and can easily be sent flying across the room causing woeful damage! Once the chip is located on the chip carrier it is gently and approximately located using the carbon tipped tweezers (on no account should any other kind of tweezers be used as damage to the chip will result). When using the equipment for the first time it is advisable to set the left and right hand micrometers to about 4 on the scale and then to initiate the set-up as this gives the optimum flexibility for later variations. The light cable from the incandescent lamp set to about 2 is taken to the vertical camera input hole to the right of the central column and an image of the chip can be seen on the right hand monitor, to facilitate the left hand optical set-up the camera is moved to the left hand edge of the chip so that the monitor may be marked with the set up point achieved.

Figure 70 the variable lamp and detector and flip-up mirror in the foreground.

The flip-up mirror (figure 70) to the left of the left hand lens and xyz micrometers are to be carefully elevated (thus avoiding damage to its internal spring) and the light from the variable incandescent lamp (set to about 3) taken via the optic cable to the

top hole above the camera aperture: the light is then reflected to illuminate the SOI edge placed on a suitably sized T shaped metal carrier. An unfocussed image will be observed on the left hand monitor. The left hand side z control is adjusted to obtain a clear image of the SOI (if planar the image of the top layer above the box should be visible and if a rib waveguide then the rib should be visible). If necessary the left hand y control is adjusted to obtain a faint spot on the top of the chip. Again, if necessary, the left hand z control is adjusted so that prominent features such as waveguides, if fitted, are central on the monitor screen (figure 74). Once a clear image of the BOX and top layer has been obtained the screen is marked with a washable felt tip and attention transfers to setting the right hand micrometer stage (figure 71).

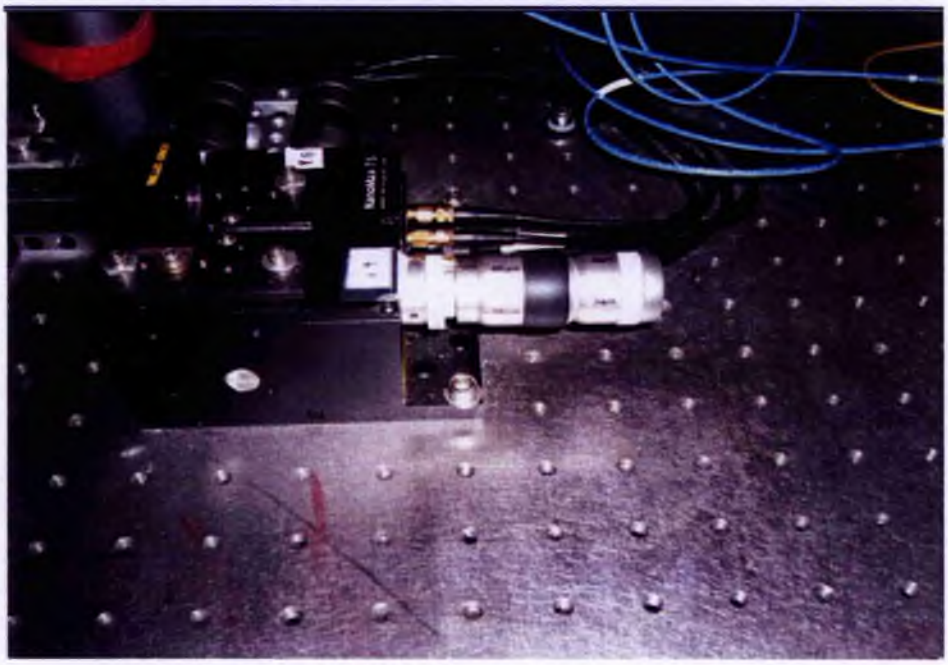


Figure 71 the right hand micrometer controls

So the optical cable from the lamp is taken to the left hand side of the central vertical column holding the camera supplying the right hand monitor and the right hand camera micrometer is turned to transfer imaging to the right hand side of the optical chip. Once the right hand side of the chip has been located and lined up with the monitor marking the light from the optical cable is inserted into the right hand lens (figure 72). The right hand micrometers for x and z are then adjusted to obtain the best optical image, ideally two semicircles of light separated by the central BOX.

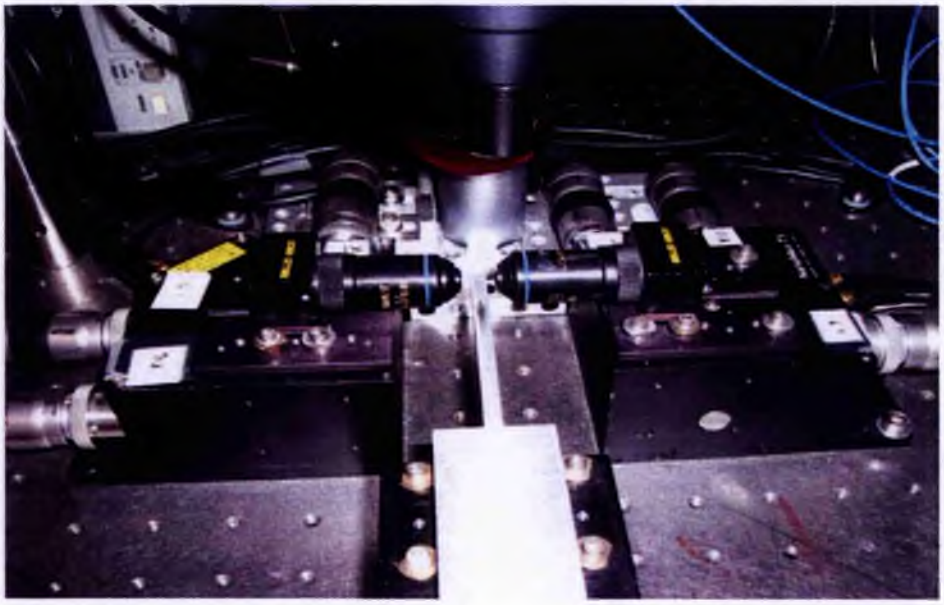


Figure 72 the fibre optic cable is shown inserted into the vertical camera aperture and once this is set to the right hand side of the chip the cable is moved to the right hand aperture and the light focussed onto the chip.

If necessary turn Y slowly clockwise to improve the focus and definition. Switch on the tunable laser (if necessary for difficult set-ups use the boxed, broadband, fixed frequency laser which is much higher power) and observe fringe interferometry from the bulk of the Silicon chip. If necessary flip the detector/camera mirror down and adjust the x and z control on the free space input to the far right of setup1 for maximum power at the detector, as this is a difficult setting it may be best left to the research staff at the start of a series of scans. Return the mirror to the upright position and adjust the right hand x micrometer for maximum fringe brightness. Next adjust the y micrometer such that the top fringe should become more visible and separate from the substrate fringes: the top fringe would be visible at the height in marker on the left hand monitor. Adjust x and y controls so that the light is maximised in the top layer: it is necessary to diminish the light in the substrate fringes to a minimum even if this means that the top fringe is slightly off maximum, if necessary iterate between the left hand monitor and the detector to obtain the best set-up. Iterate y and z micrometer controls to obtain the maximum light on detector and check that the top fringe shape is still as you would expect.

Figure 73 Piezo-electric Controllers.

Finally a piezoelectric controller (figure 73) is located on the shelf above setup1 and the x, y, and z settings on this must be trimmed and iterated to provide the best transmission power reading on the detector: optimisation is very important as this will reduce noise on the scans. The mirror is raised again to check mode shape and lowered for scanning. On the scan GUI (graphic user interface: figure 75 Photonetics scan) the wavelength variation and power are selected and for the first scan initialise is selected, in which case the scan is started once initialisation has occurred.

On completion the scan may be stored electronically and if it is promising a further scan may be taken at reduced variable wavelength range and diminished wavelength step size to increase quality. A polarizer is provided to the right of the free space area and 357 degrees selected for TE scans and 42 degrees selected for TM scans.

In figure 74 we see the output that would be obtained for the case where the gratings were in place on the top of a rib wave guide. In the planar case a series of fringes caused by interferometry of the laser light in the substrate is replaced by the appearance of a top fringe from the active surface Silicon layer; the monitor screen is marked with washable ink during set-up to identify either the position of the output wave guide spot or the height of the planar top fringe.

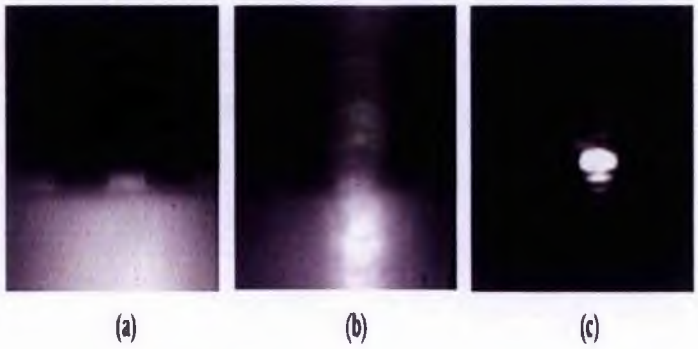


Figure 74 (a) Image of output wave guide showing the top layer and etched rib waveguide, (b) unfocused laser output and (c) focused laser output.

In figure 75 we see the photonetics scan graphic user interface, changes to the scan parameters are set by mouse and keyboard.

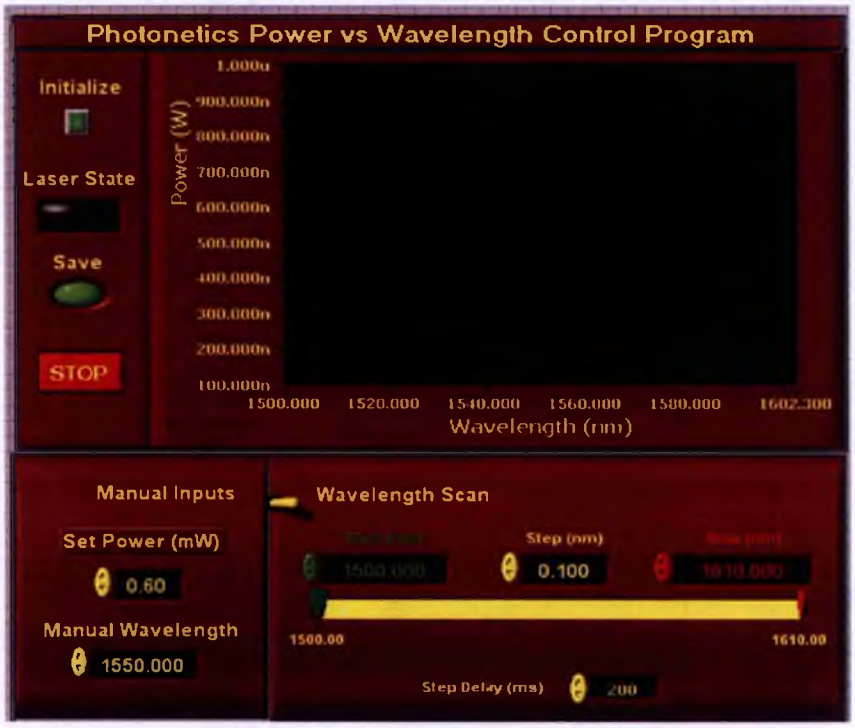


Figure 75 Photonetics Scan Graphic User Interface.

Finally temperature measurements were achieved with a Peltier heat pump, a large copper slab is used to mount the sample providing some thermal stability and a feedback looped controller box is used to set the target temperature, the box and copper slab are shown in figure 76.

Figure 76 (a) Peltier temperature controller, (b) Copper Carrier.

Footnote

Please note that rib waveguides had been etched onto one of the planar samples (D1 Ion as Implanted) by stripping the Silicon Nitride mask from the SOI surface by immersing in boiling 80% Phosphoric Acid for 20 minutes. The ribs were provided by etching to a new rib waveguide mask with Silicon Hexafluoride gas. Triple cleaning then occurred prior to optical investigation. The sample was damaged in the course of external anti-reflection coating and it has not been possible to obtain reflection measurements.

7 RESULTS and DISCUSSION

Introduction

In this chapter we discuss the findings of the transmission tests on the planar gratings and analyse the data with respect to changes in grating length, period and mark to space ratio. In this regard the samples were labelled as follows:

D series

D3 represented a standard sample of standard period 228nm but with a length of only 100 microns, D1 was the same but with a length of 500 microns and D2 was of length 1000 microns: again having the same period.

B series

B1 has a mark to space ratio of 1, B2 has a mark to space ratio of 1.05, B3 has a mark to space ratio of 0.95 and B4 a mark to space ratio of 0.9. Otherwise all samples have a period of 228nm and a length of 250 microns. B5 is the odd one out with a periodicity of 248 nm with a mark to space ratio of one and length of 250 microns.

C Series

C1 has a period of 276 nm, C2 a period of 200 nm and C3 a period of 176 nm. Otherwise C1-3 have a mark to space ratio of unity and grating length of 250 microns. C4 and C5 have the standard period of 228nm and unity mark to space ratio but are 200 and 300 microns long respectively.

As well as investigating the effect of changing the above mentioned parameters a sample D2 as implanted was measured against change of temperature over 15 to 35 degrees Celsius to investigate whether these gratings could form the basis of a viable temperature sensor, or thermally tunable filter.

Furthermore the performance of the ion implanted gratings was contrasted with the thermal oxide gratings in order to compare commercial viability. Also where the ion implanted samples gave gaps in the results matrix the thermal oxide gratings tended to work and vice versa, and this had the beneficial effect of covering most areas of investigation.

In addition an attempt was made at annealing the as-implanted gratings with a view to creating gratings of silicon and stoichiometric silica half periods.

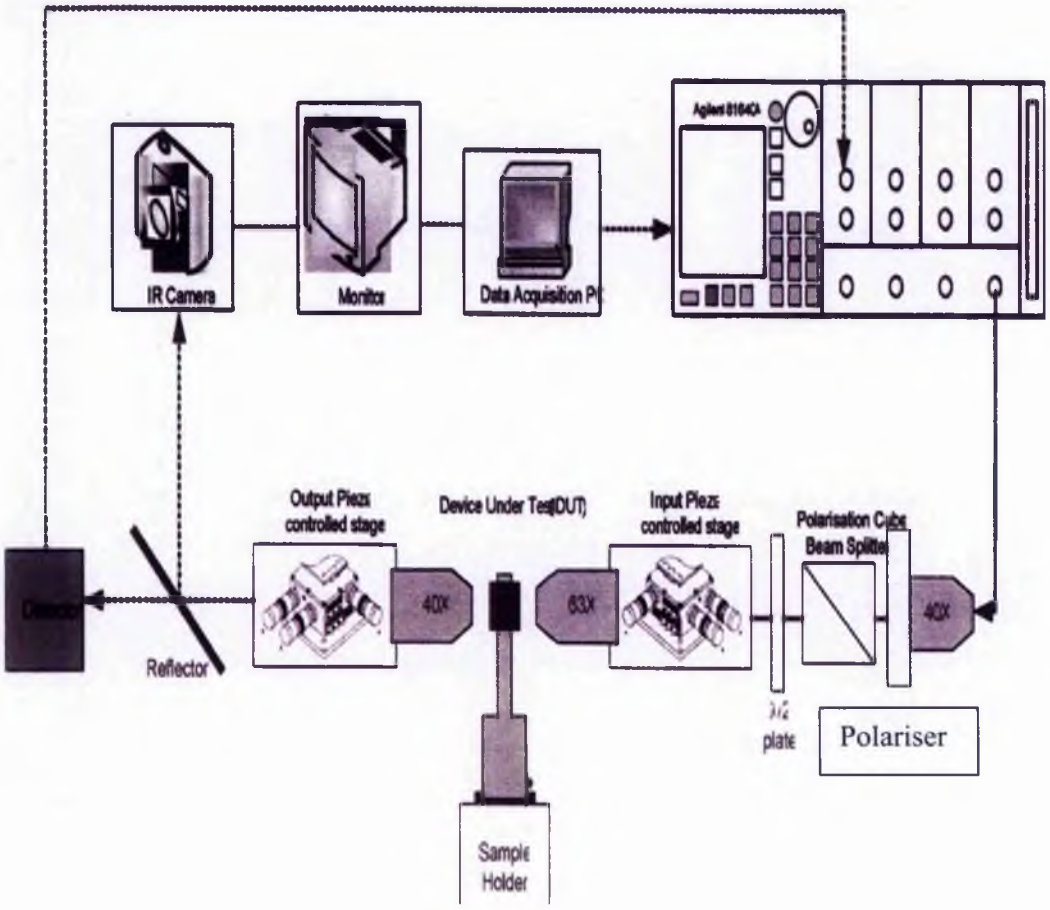


Figure 77 apparatus for measuring the transmission grating characteristics

In figure 77 we see in schematic form the equipment used for the transmission measurement: the output from the tunable laser is taken to the sample by a mono-mode optical fibre, next it is aligned and focused by the right hand (input piezo) x,y,z stage, it then passes through the sample and is re-focused and aligned by the left hand (output piezo) x,y,z stage and finally the output is measured at the detector and saved on the computer.

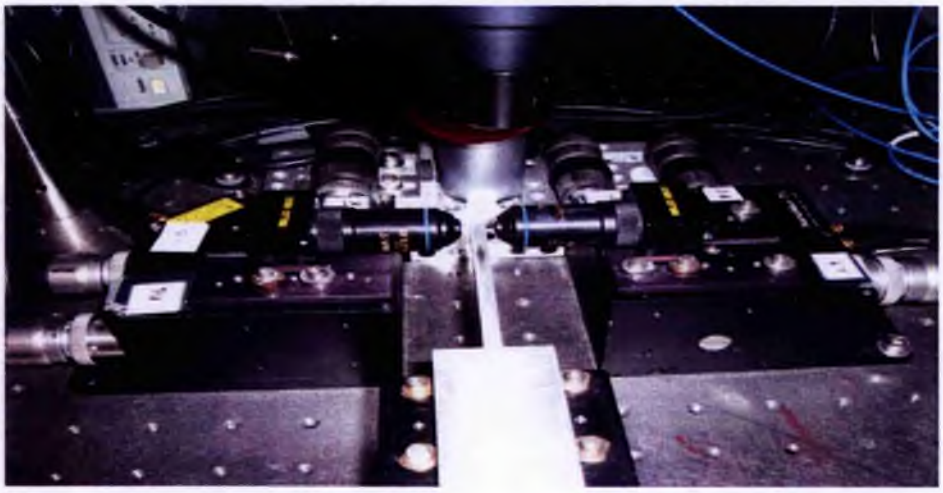


Figure 78 the sample mounted on the T bar and the x,y,z micrometer stages used to align both sets of stages to provide optimum alignment

Figure 78 shows the left and right hand stages for the optical setup. This is obtained by shining light from an incandescent lamp onto the SOI, an image of the top layer is obtained on the monitor and left hand xyz focussing achieved. Thereafter focussing is obtained on the right hand entry side by taking the light from the fibre bundle to the input lens and observing the optical transmission through the top layer. Next the laser is turned on and the set-up completed to provide the best image of the laser spot on the monitor and the best power at the detector. A scan is initiated on the National Instruments graphic user interface and the laser steps through the wavelength range selected. If a functioning grating is present on the sample then the point in the transmission where the grating is functioning will let only a tiny fraction of the light through compared with the areas distant from the Bragg wavelength 'dip' in the transmission spectrum.

As implanted results.

As shown in figure 79 the as implanted gratings consist of a half period of silicon and a half period of oxygen implanted silicon. The implanted area is slightly below the silicon surface due to sputtering during implantation.

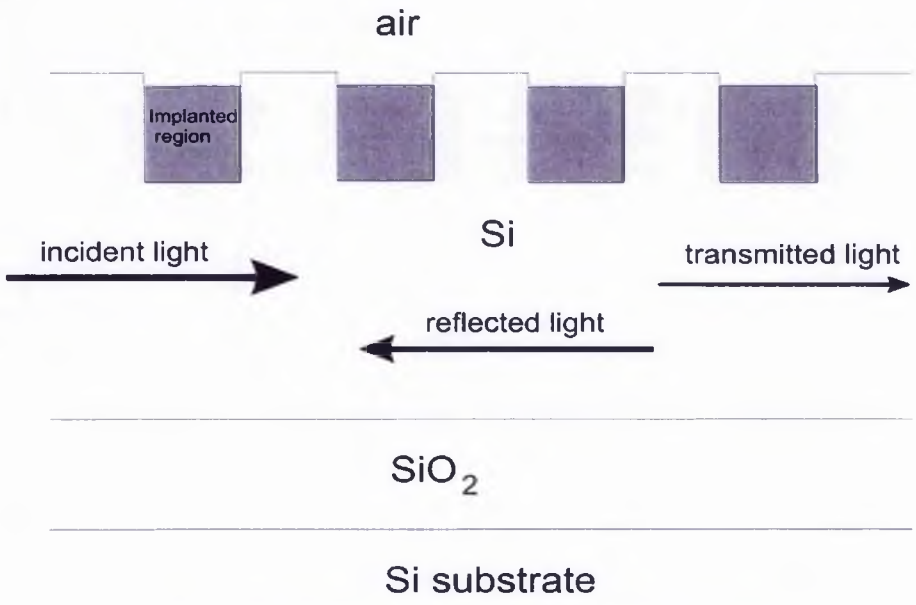


Figure 79 schematic of the as implanted gratings

Figure 42 from section 4.3.2 is reproduced below as figure 80 to show the depth of the gratings: the true depth must be of the order of 140nm as can be derived from the % disorder curve.

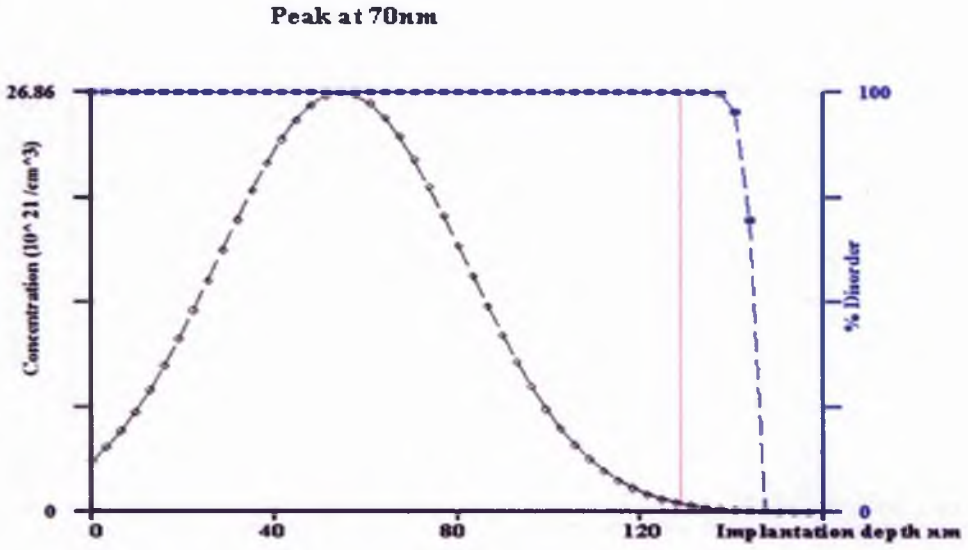


Figure 80 Implantation of oxygen into silicon @ 20keV / 1.6.10^{17} ions/cm^2 [54]

Table 3 results matrix for TE/TM polarization for the as Implanted samples (free space transmission).

TE	Markspace Ratio	Length micron	Period nm	Attenuation dB	FWHM nm	Dip λ nm
B1	1	250	228	3.02	0.9	1543.9
B2	1.05	250	228	3.3	1	1541.9
B3	0.95	250	228	3.1	1.6	1541.9
B4	0.9	250	228	5.7	1.6	1542
B5	1	250	248	10.37	2.6	1557
C1	1	250	276			
C2	1	250	200			
C3	1	250	176			
C4	1	200	228	4.2	1	1540.8
C5	1	300	228	5.4	1.2	1544.2
D1	1	500	228	9.6	0.9	1543.9
D2	1	1000	228	16.8	1	1542.3
D3	1	100	228	3.45	1.6	1541
TM	Markspace Ratio	Length micron	Period nm	Attenuation dB	FWHM nm	Dip λ nm
B1	1	250	228	3	1.3	1535
B2	1.05	250	228	2	1.5	1533.4
B3	0.95	250	228	2.2	0.7	1534.2
B4	0.9	250	228	3.3	1.6	1536.1
B5	1	250	248	1.5	1.2	1551.1
C1	1	250	276			
C2	1	250	200			
C3	1	250	176			
C4	1	200	228	2	1.3	1533.4
C5	1	300	228	3.3	1.2	1536.2
D1	1	500	228	3.45	0.9	1534.8
D2	1	1000	228	11	1	1533.8
D3	1	100	228			

Table 3 summarises the free space transmission results for the as implanted samples. The designed wavelength for 228nm period is 1550nm and the measured wavelength varied between 1540.8 and 1543.9 (samples C4 and D1). Partial explanation for the discrepancy is the fact that Gratingmod is designed for use with Fibre Bragg gratings and can only be considered an approximation with respect to simulation of gratings in

SOI. Further explanation for the differences can be obtained from diurnal temperature change affecting the grating response (caused by the thermo-optic effect in the silicon, cf Cohen [102] who had derived a result of 2.4nm change over 20 degrees for a silicon relief grating) and an error of 4nm in the e-beam writing accuracy associated with the Philips fabrication facility in Eindhoven [144]. In general a Full Width at Half Maximum (FWHM) figure is achieved of the order of 1nm, the only exceptions being at the extremities of the wavelength range i.e. sample B5 at 2.6nm (also 4.9 nm for sample C2 made by thermal oxidation); an explanation could be that at the extremities of the wavelength range (B5/C2) higher order modes were coalescing into the Bragg dip, but rather a lot of work would be needed to substantiate this.

A maximum attenuation figure of about 17dB is achieved which is possibly of the order of the level of attenuation necessary to justify commercial exploitation.

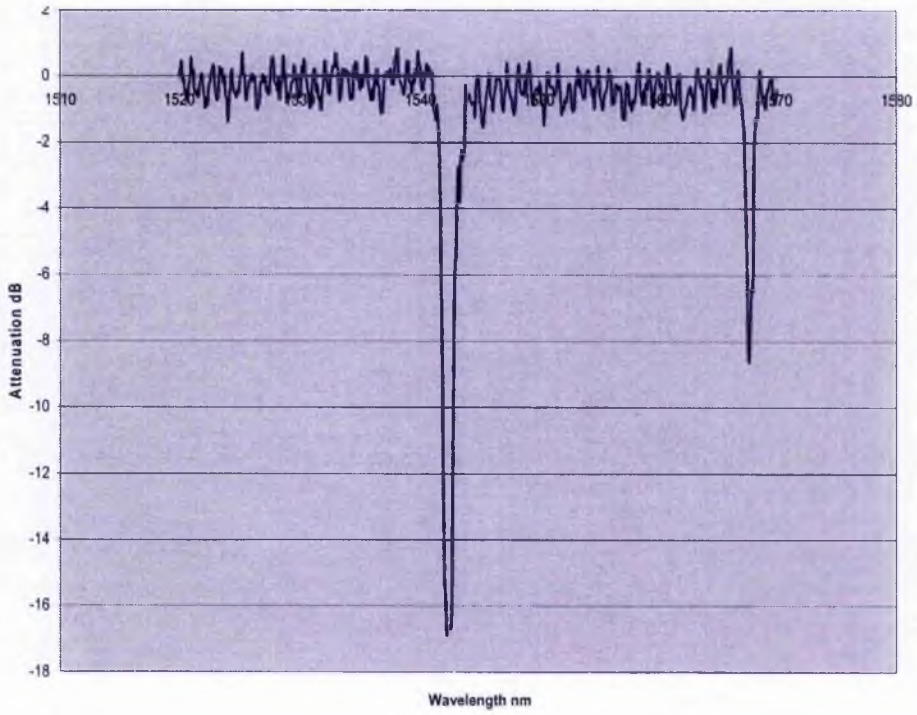


Figure 81 TE transmission spectrum for D2 as Implanted sample.

In figure 81 we see the best ion as implanted TE scan with 17dB attenuation and 1nm FWHM.

TM scans were run as well as TE. In general these had smaller peak values for Bragg dip attenuation than the TE for example D2 as implanted had a Peak TM dip of 10dB

whereas the peak value of TE dip was 17 dB a differential of 7 dB . The dips, if any, were sometimes lost in Fabry-Perot/Fresnel noise. There was typically 5-10 nm difference in grating wavelength dip. A TM scan for D2 ion as-implanted is shown in figure 82.

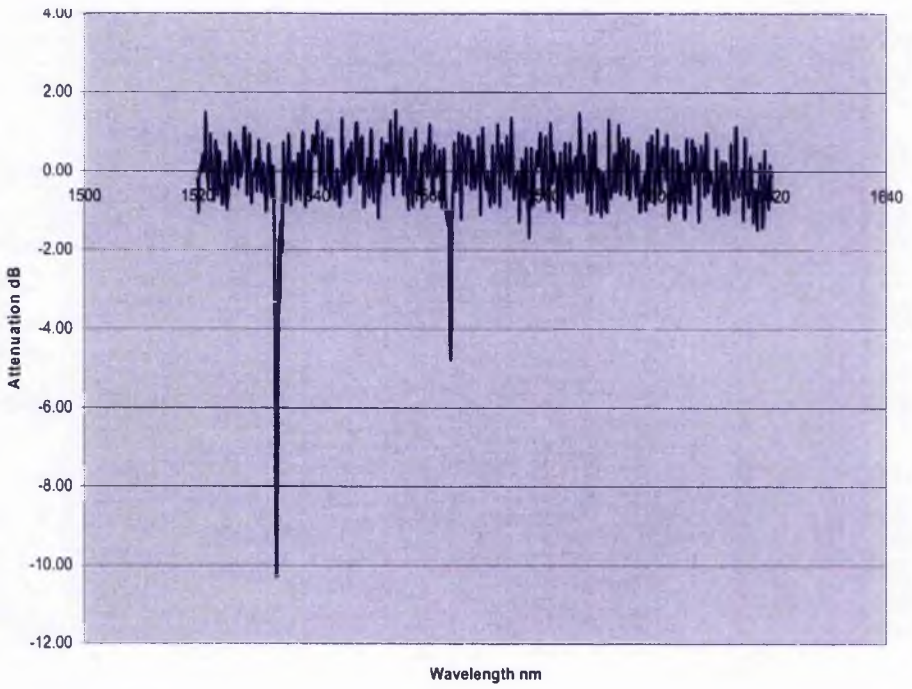


Figure 82 TM transmission spectrum for D2 as Implanted sample.

Figure 82 above reveals a primary dip at 1535nm compared with that of the TE at 1542nm. There is also a secondary dip at 1562 nm compared with 1568 nm for the TE. These dips were not caused by TM/TE breakthrough as the wavelength is not consistent. A sample was damaged during anti-reflection coating (D1 as implanted) but was re-examined and still gave the same second dips even though it only had one grating upon re-polishing and its size was reduced to about 3mm by 4mm. Finally non apodised gratings give leakage through the side lobes (see figure 83) and these are shown in the simulation to be equidistant from the Bragg dip and this is clearly not happening with these samples. Figure 83 is shown below for a 100nm depth of grating and clearly shows 40 % dips in transmission.

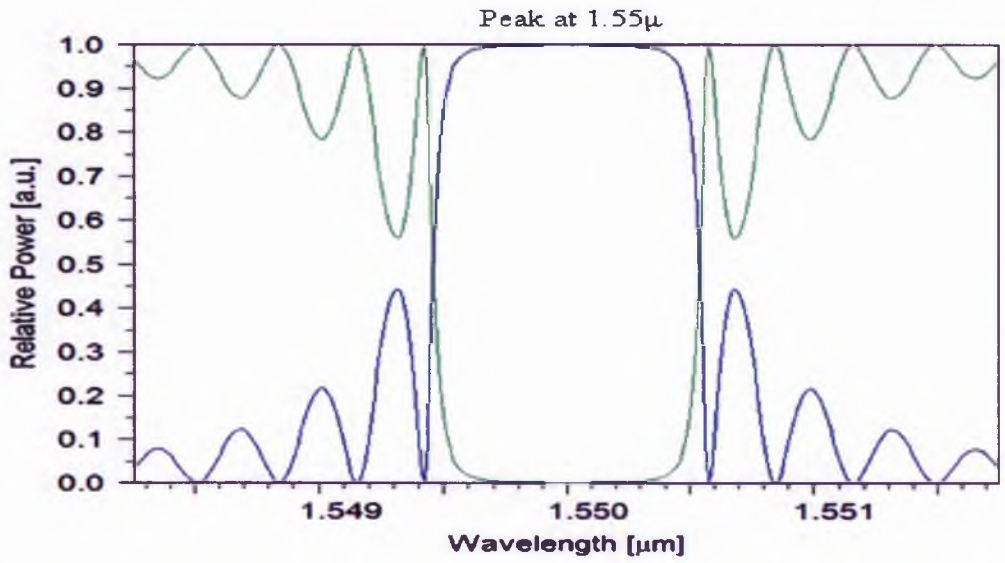


Figure 83 simulation of 100nm depth silica into silicon grating [121]

Thus although higher modality was not conclusively proven to be responsible it was emerging as one of the major potential causes of the second dip.

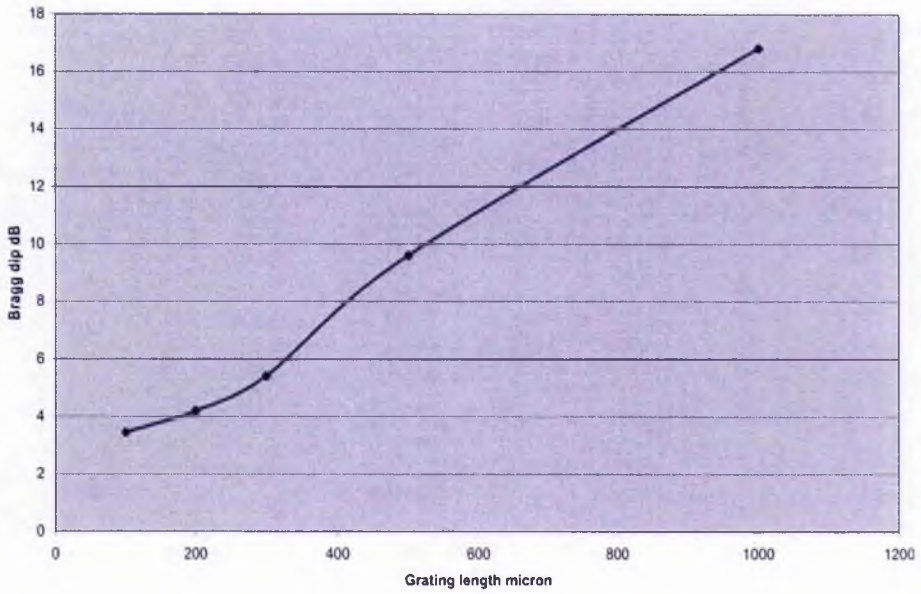


Figure 84 grating dip versus grating length for as Implanted TE

Figure 84 shows the TE variation of Bragg dips against wavelength for the as implanted samples and with minor variations follows the trend set in figure 32: first order simulation reproduced below as figure 86.

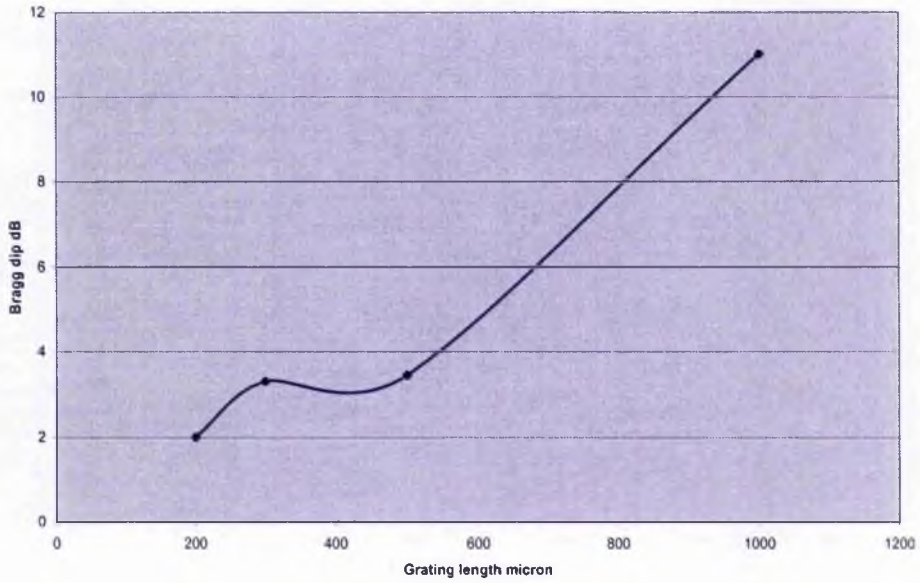


Figure 85 grating dip versus grating length for as Implanted TM

In figure 85 is plotted the curve of grating dip against grating length for TM polarisation for the as implanted samples with period of 228nm. Figures 84 and 85 follow with minor fluctuation the first part of the first order simulation curve, see figure 32 (reproduced as figure 86 below).

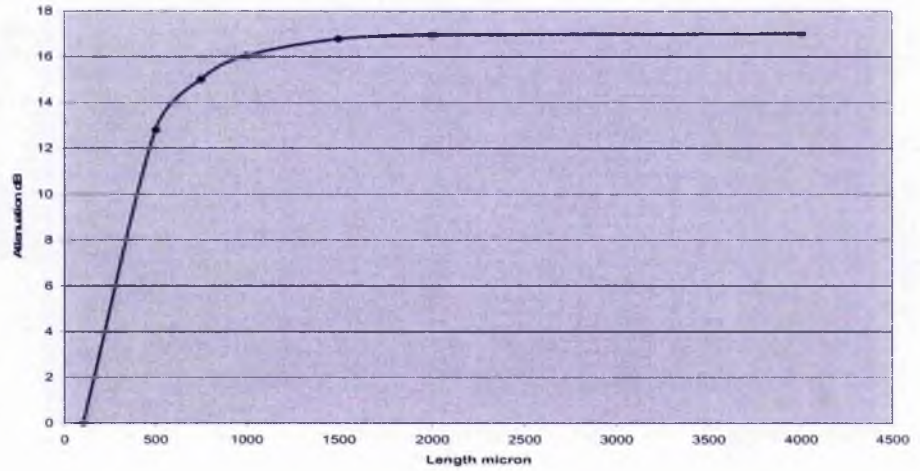


Figure 86 (reproduced fromFigure 32) first order grating length simulation [121]

Figures 87 and 88 below show the variation of dip wavelength with duty cycle changes for TE and TM polarised ion as implanted gratings, and they show slightly less change in Bragg wavelength dip than the simulator figure 89.

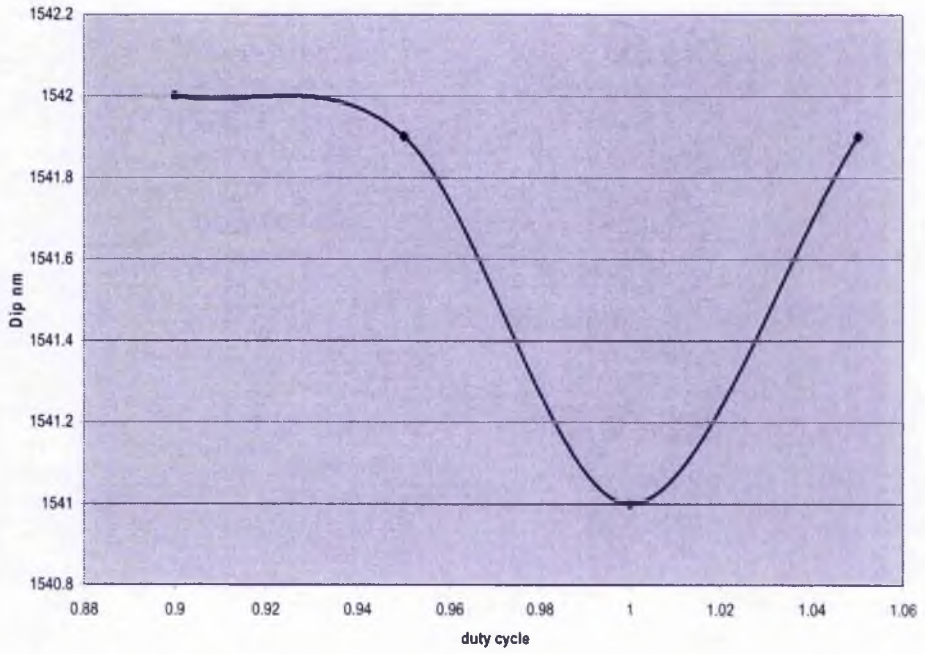


Figure 87 dip versus duty cycle as Implanted TE

Figure 88 shows a slight improvement in the TM ion as implanted scans, plotted against change in duty cycle compared with the simulator figure 89.

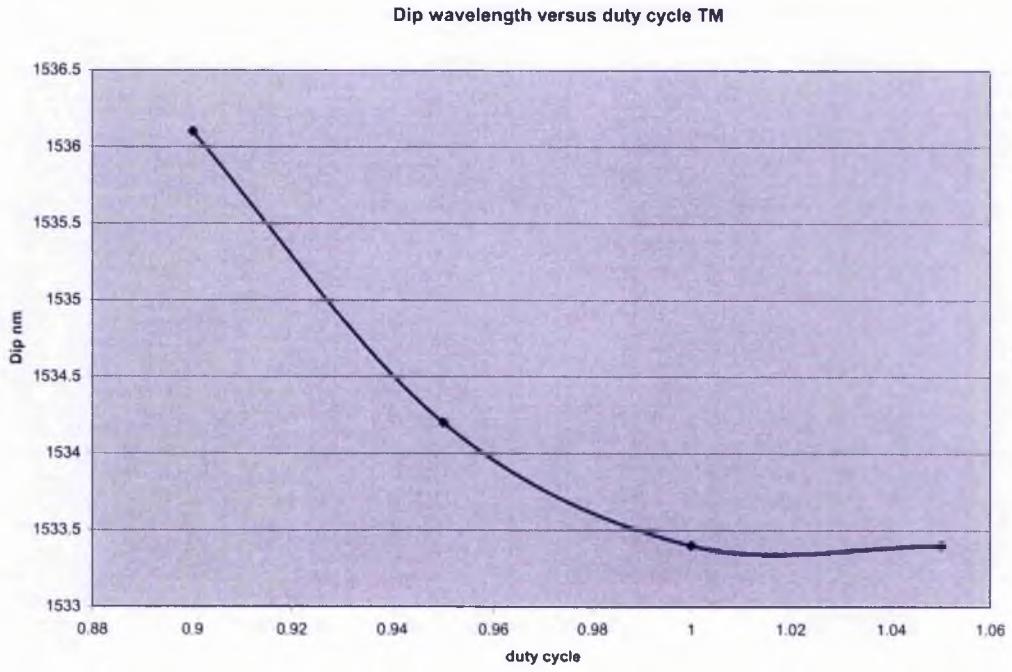


Figure 88 dip versus duty cycle as Implanted TM

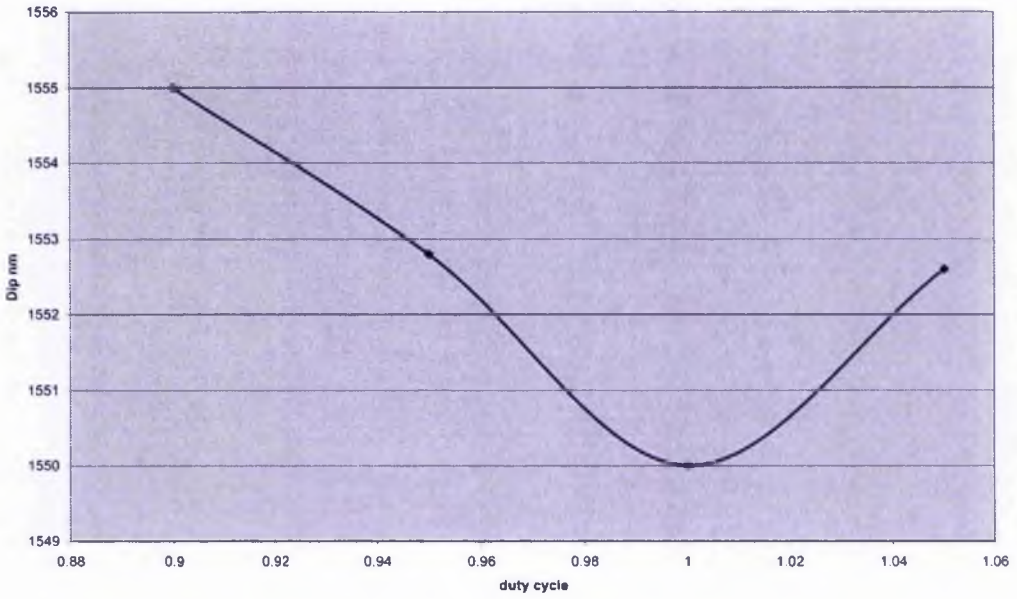


Figure 89 simulated change in Bragg dip with duty cycle

Figure 89 shows the simulated result taken with the latest issue of Gratingmod and shows an increase in Bragg dip with change in duty cycle from unity. The agreement is qualitatively good for both TE and TM polarisations; although the absolute dip wavelength is shifted for both TE and TM, suggesting a shift in the period that could be caused by beam straggle/period errors.

Thermal Oxide results

The labelling of the chips for the thermal oxide samples was the same as that of the ion implanted samples and the chips were tested in the same way as the as implanted samples by placing on the metal T bar and setting the optics as in the previous.

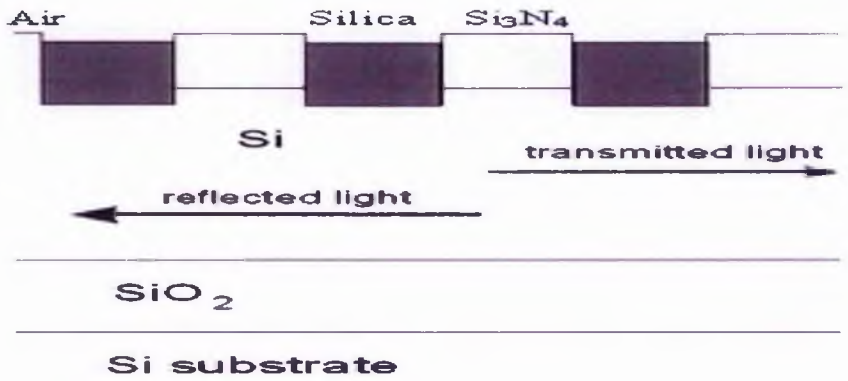


Figure 90 diagram of thermal oxide sample

In figure 90 we see a schematic of the thermal gratings whereby the 100nm of silicon nitride per half period is countered by 140 nm of silica and thus there is a secondary grating of 40nm of silica versus silicon underneath the primary grating (upper) of 100 nm of silica versus silicon nitride.

This is caused by the fact that in order to grow a 100nm layer of silica above a silicon surface about 40nm of silica must be created below the surface (for a discussion of this please see the section on thermal oxidation in the fabrication chapter). The overall simulation is shown in figure 91.

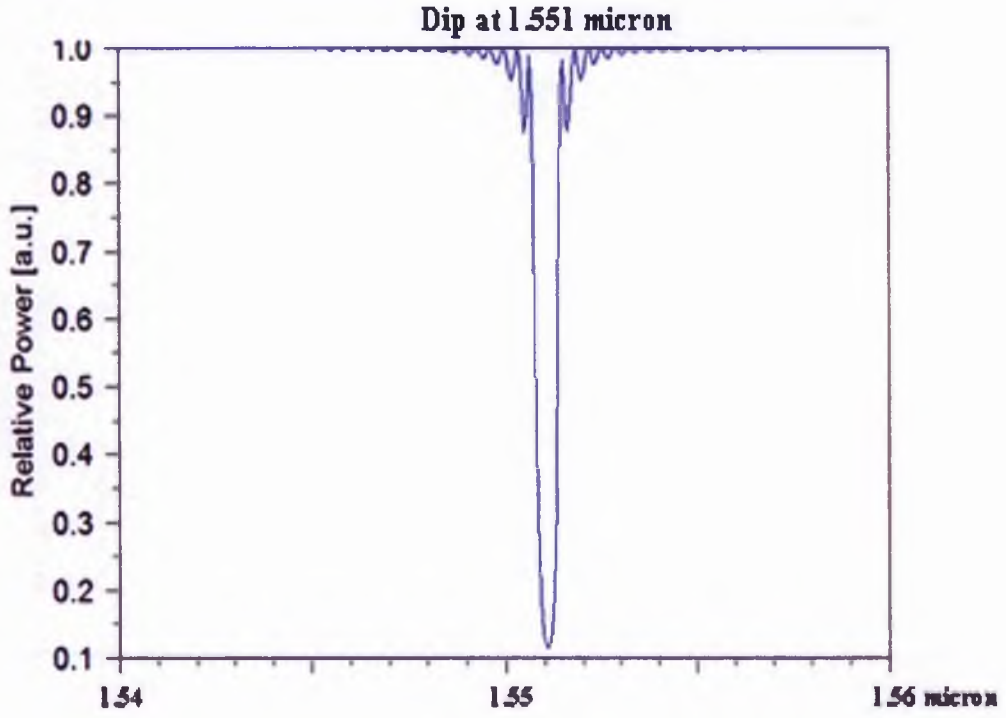


Figure 91 simulation for the thermal oxide grating at 228nm period

Below we see a similar results matrix for the thermal oxide gratings as was prepared for the as implanted gratings and as before it is necessary to bear in mind that D1-3 varies the effect of grating length and B1-4 vary mark to space ratio and B5 and C1-3 vary the periodicity and C4 and C5 provide an extra check on the effect of changing the grating length.

Table 4 Results matrix for TE/TM polarization for the Thermal Oxide samples (free space transmission).

TE	Markspace Ratio	Length micron	Period nm	Dip λ nm	FWHM nm	Attenuation dB
B1	1	250	228	1545.9	4	2
B2	1.05	250	228	1544	1.2	0.5
B3	0.95	250	228	1545.2	1.5	4.15
B4	0.9	250	228	1547.4	1.7	8
B5	1	250	248	1566.8	2.6	13.1
C1	1	250	276			
C2	1	250	200	1519	4.9	17.1
C3	1	250	176			
C4	1	200	228	1545.9	1.5	2.14
C5	1	300	228	1545.9	0.9	3.3
D1	1	500	228	1542.4	0.6	2.85
D2	1	1000	228	1546.3	1	3.7
D3	1	100	228	1544.2	1.2	1.7
TM	Markspace Ratio	Length micron	Period nm	Dip λ nm	FWHM nm	Attenuation dB
B1	1	250	228			
B2	1.05	250	228			
B3	0.95	250	228	1540.3	0.8	1.65
B4	0.9	250	228	1540.5	1.4	0.73
B5	1	250	248	1541.5	1.7	1.5
C1	1	250	276			
C2	1	250	200			
C3	1	250	176			
C4	1	200	228			
C5	1	300	228			
D1	1	500	228			
D2	1	1000	228			
D3	1	100	228			

Table 4 summarises the thermal oxide results achieved. The gratings display a TE dip magnitude of 0.5 to 4.15 dB with the exception of B5 and C2 which are 13.1 and 17.1 dBs respectively. In general a Full Width at Half Maximum figure is achieved of the order of 1nm. The only exceptions being at the extremities of the wavelength range (i.e.1566 nm for sample B5 and 1520 nm for sample C2). Also samples C2 and B5 have only one grating dip that was observable on the current setup. A possible explanation is the avoidance of power division in the existence of higher order modes.

Figure 92 depicts the change in transmission free space attenuation for thermal oxide gratings with respect to grating length.

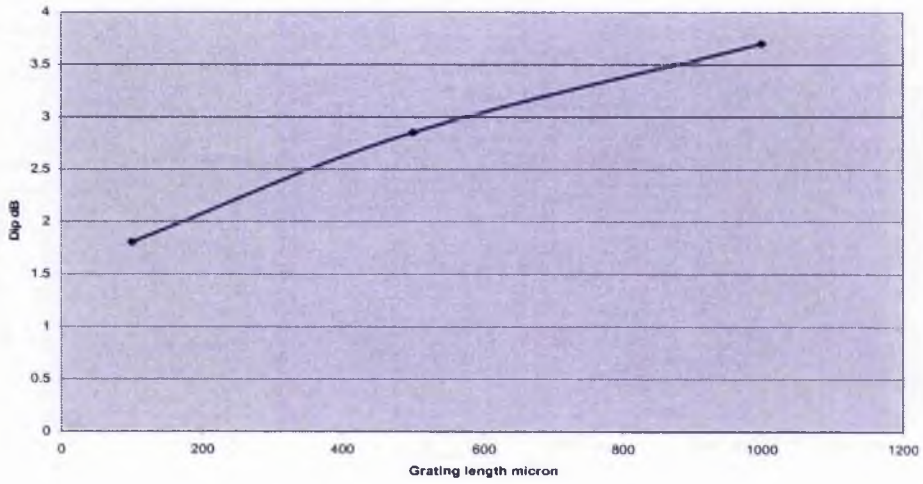


Figure 92 grating dip versus grating length for thermal oxide TE

A comparison with the simulation cf figure 93 (reproduced below from figure 32) reveals some conformity with the lower region of the curve.

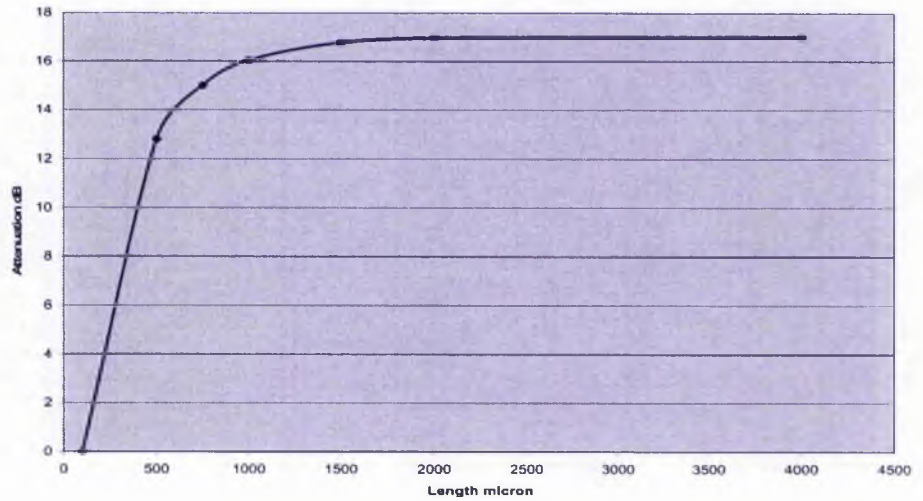


Figure 93 (reproduced from Figure 32) first order grating length simulation [121]

Figure 94 shows the result for B5 TE Thermally Oxidised and shows a large increase in the magnitude of the wavelength of the Bragg Dip due to increasing the grating period to 248 nm and an increase in FWHM, also the magnitude of the attenuation depth is increased possibly due to no observable second peak (up to 1620nm: as observed on the Agilent laser), as before.

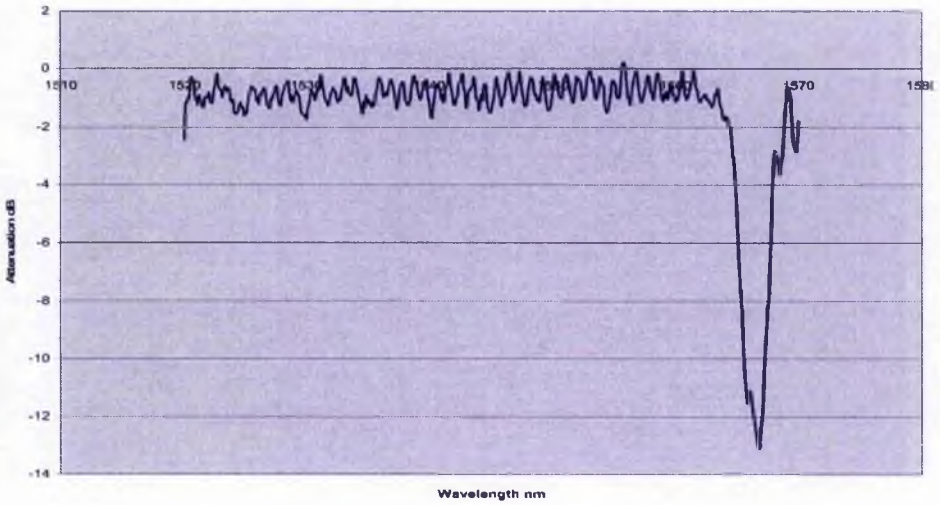


Figure 94 B5 TE thermal oxide scan for free space transmission

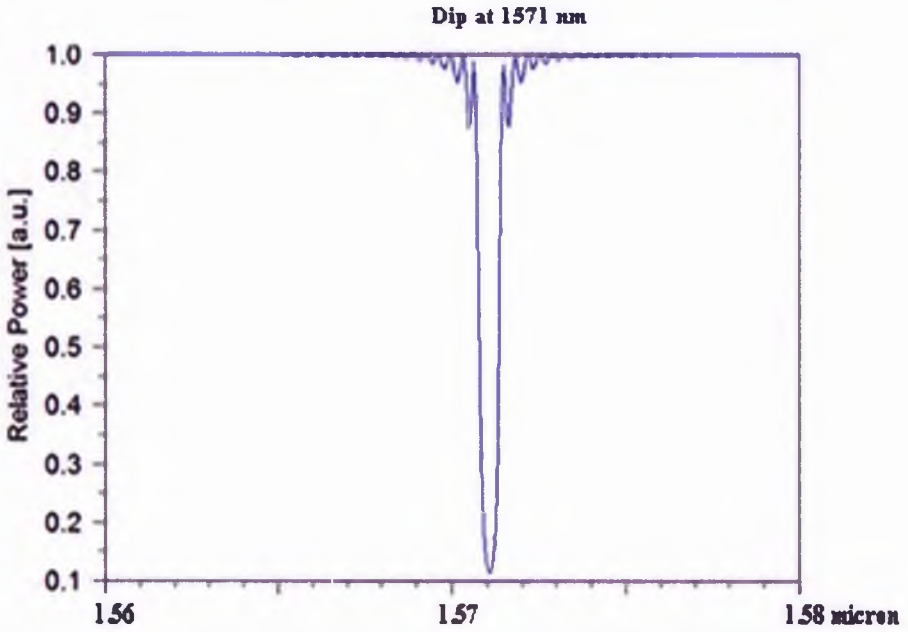


Figure 95 simulation result @ 248nm period (B5 TE)

In figure 95 we see the simulation result for the period change the wavelength difference may be caused by the +/_ 4nm shift in the period.

In figure 96 we see a reduction in the dip wavelength for sample C2 where the period is reduced to 200 nm and also an increase in the dip magnitude and FWHM and there being again no observable second dip.

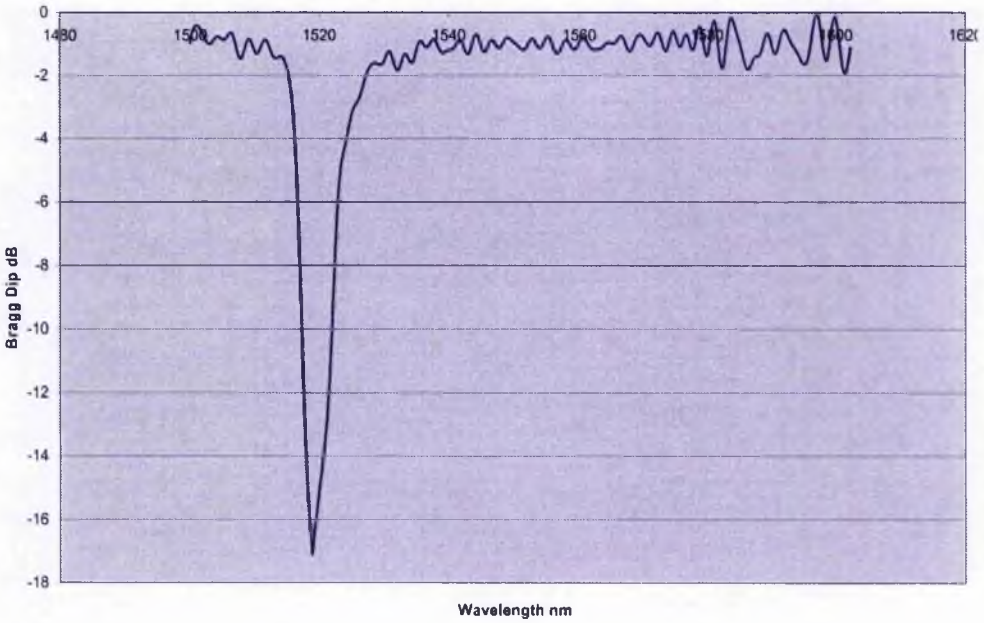


Figure 96 C2TE thermal oxide free space transmission spectral scan

In figure 97 is shown the simulation result and shows good agreement with figure 96.

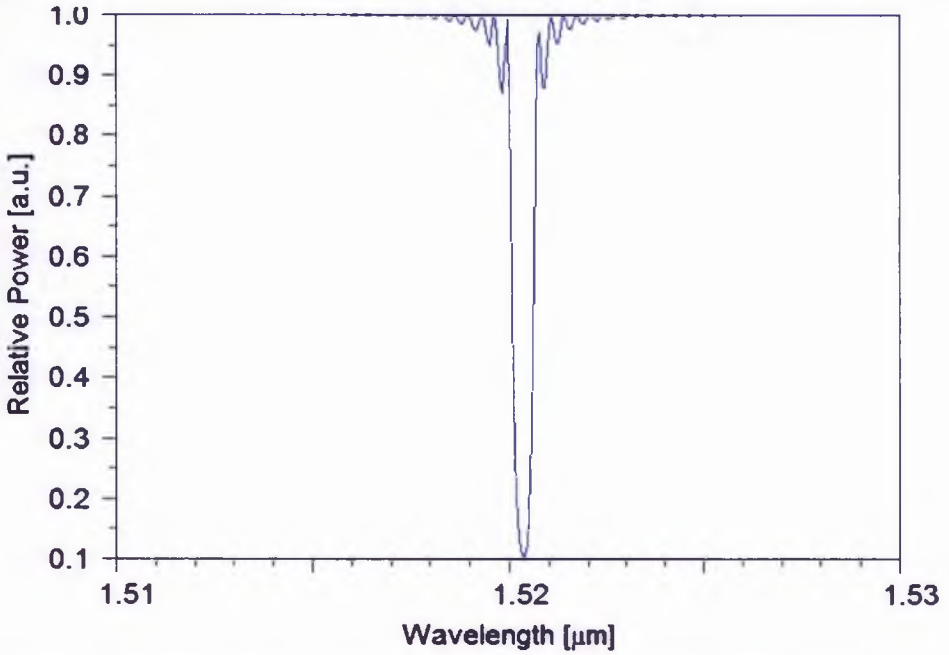


Figure 97 simulation result at 200nm period for C2 TE thermal oxide

In figure 98 we see the variation of the Bragg dip wavelength with the grating period which has but three data points and is only for thermal oxide: again due to sample scarcity. This follows the linear law predicted by theory cf equation 19.

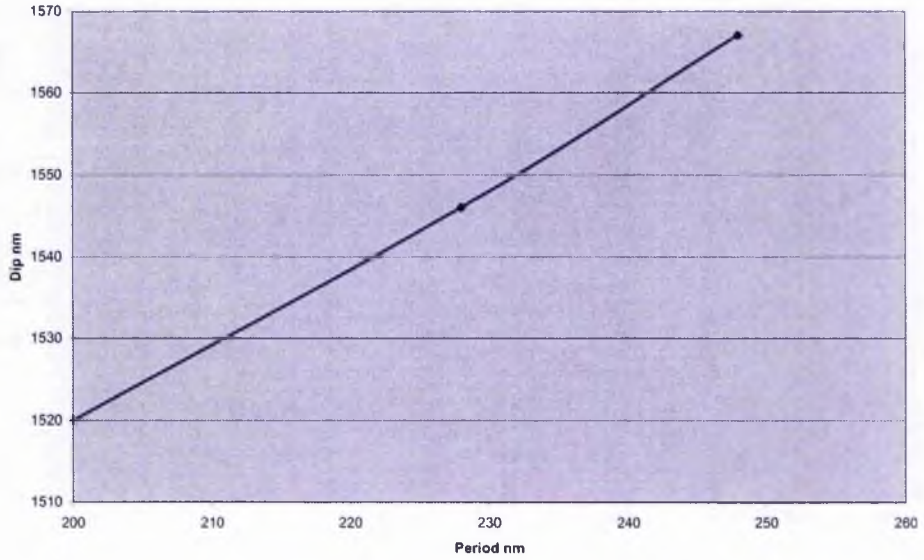


Figure 98 TE polarization dip versus period (thermal oxide only)

In figure 99 we see the result of the simulation for dip versus period and shows good agreement but with only three data points.

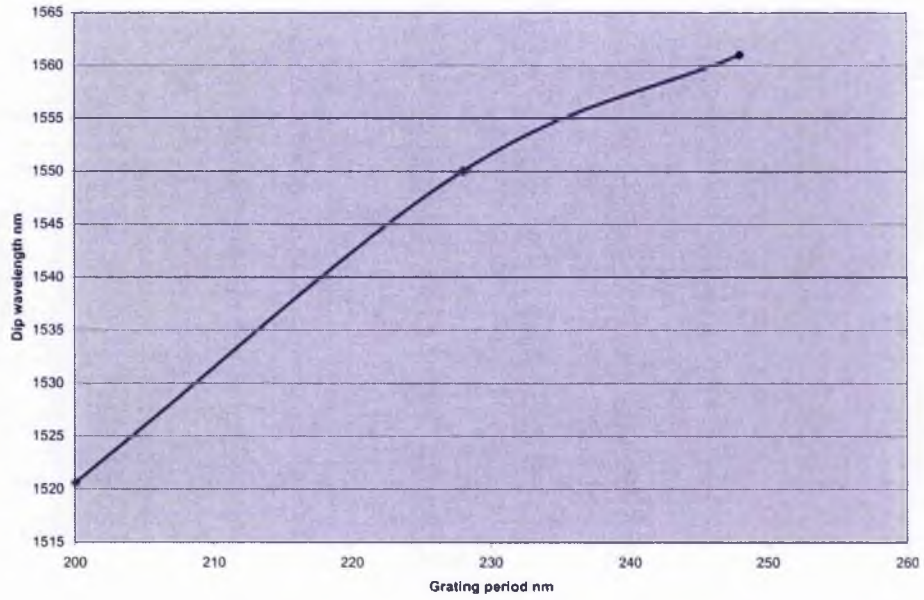


Figure 99 simulation of dip versus period

The curve of mark to space ratio against Bragg dip is plotted in figure 100 but only for the TE polarisation of the thermal oxide gratings as TM did not function.

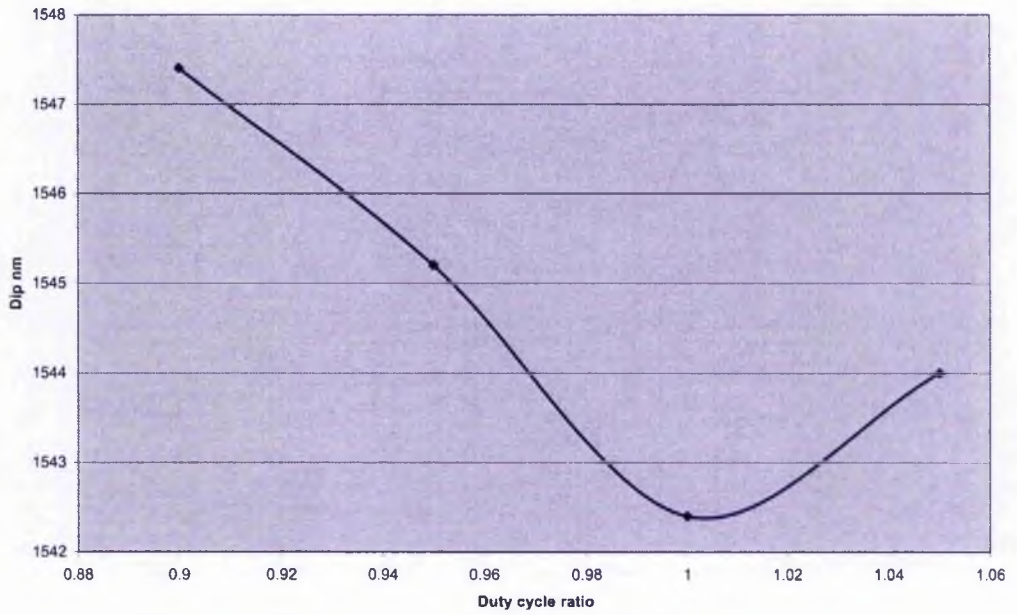


Figure 100 dip versus duty cycle thermal oxide: TE polarisation

Figure 100 shows an increase in the dip wavelength with departure from unity duty cycle.

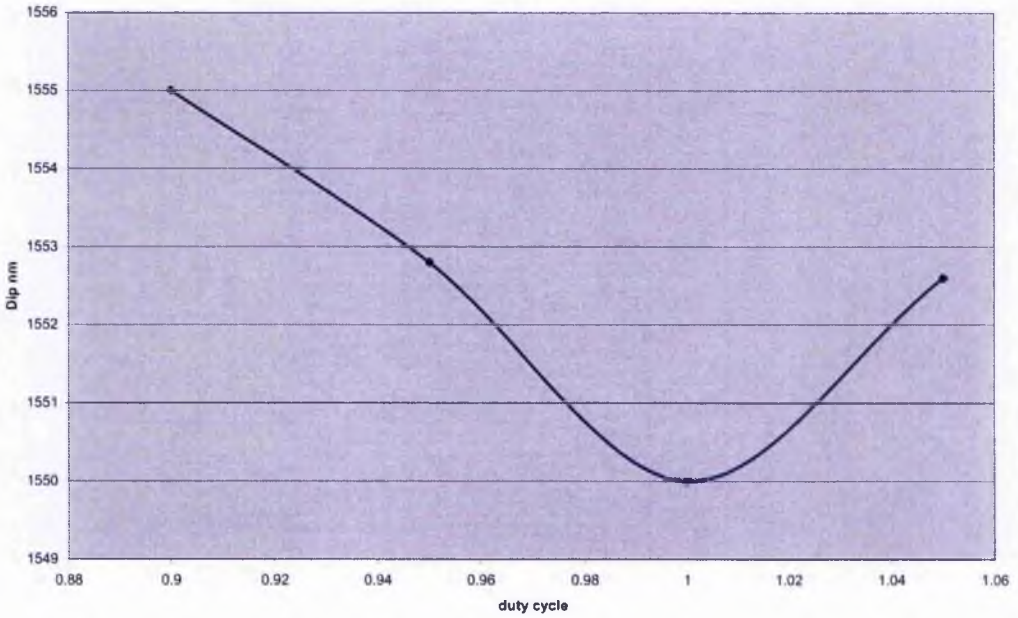


Figure 101 (from Figure 89) simulated change in Bragg dip with duty cycle

Figure 101 (Figure 89, reproduced from before) shows the simulated result taken with the latest issue of Gratingmod and shows an increase in Bragg dip with change in duty cycle from unity and in this respect bears the most similarity to the thermally oxidized

grating result. The thermal oxide gratings have no implantation straggle and this may well be the reason. The absolute agreement is off by less than 10nm which may be due to lateral diffusion of oxide.

Comparison of as implanted and thermal oxide gratings

With regard to length of grating the as implanted gratings gave a better Bragg dip attenuation than the thermal oxide for example D2 as implanted gave 16.8 dB attenuation as opposed to 3.7 dB for D2 thermal oxide. The reason for this is possibly due to the refractive index difference.

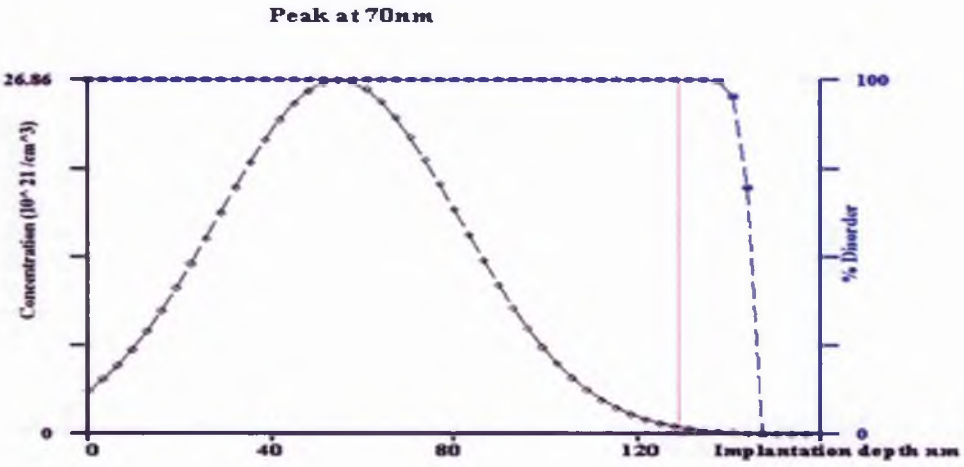


Figure 102 (figure 42) Implantation of oxygen into silicon @ 20keV / $1.6.10^{17}$ ions/cm^2 [54]

As seen in figure 102 (42 reproduced) above the as implanted gratings give about 140 nm of percentage disorder which is the same as the 140 nm of thermal oxide created to level the thermal silica with the 100 nm of deposited silicon nitride mask. Another possibility might be the shape of the gratings since the thermal oxide gratings must be approximately rectangular in profile as opposed to the implanted gratings, which are the product of random collisions and slowing of passing ions with interaction with valence electrons.

Enlarged dips of 13 and 17 dBs were obtained at 1566 and 1520 nm respectively (thermal). This may be caused by power division between modes for the intermediate wavelengths. Sample B5 ion as implanted gave extra attenuation similarly to its

thermal oxide counterparts and also displayed a broadening of the FWHM. This would seem to fit in with the modality theory rather than being caused by the fabrication. Sample C2 as implanted did not work so no possibility of comparison exists. With regard to period versus Bragg dip only two results are available for as implanted so no possibility of comparison exists. With regard to the changes in duty cycle there was some similarity between the thermal oxide experimental result and the simulation and this might be expected from the fact that they had no implantation straggle. The as implanted TE and TM results showed a little increase with change in duty cycle. This probably means that straggle swamped the masking changes (22.8nm maximum) and was caused by ion beam divergence.

Despite the fact that the last two effects were mainly observed in the thermally oxidised gratings, they can be extrapolated for as Implanted and thus a full set of results have effectively been obtained with regard to the two original SOI samples and the masking changes implicit on them.

The temperature response of sample D2 Ion as Implanted was taken over a range of 20 degrees.

Figure 103 temperature response experiment (a) Peltier temperature controller, (b) Copper Carrier.

In figure 103 we see a photograph of the Peltier controller and copper carrier used in the temperature experiment: the sample is placed in a thermal circuit with the Peltier heat pump by virtue of being placed on the copper carrier and this is connected to the power supply and also feedback to the power supply switches off the power supply once the required temperature is achieved.

The purpose of the experiment was to establish the grating's credentials as a potential temperature sensor and to compare the change in Bragg response with theory. The sample was placed on the sample holder above the Peltier heater mounted in the base of the Copper holder. The required temperature was selected on the control and when this was reached the indication of heating/cooling ceased. Once this had occurred the spectral scan was initiated. The results were taken on the same day and completed in a single run starting at 15 degrees and ending at 35 degrees.

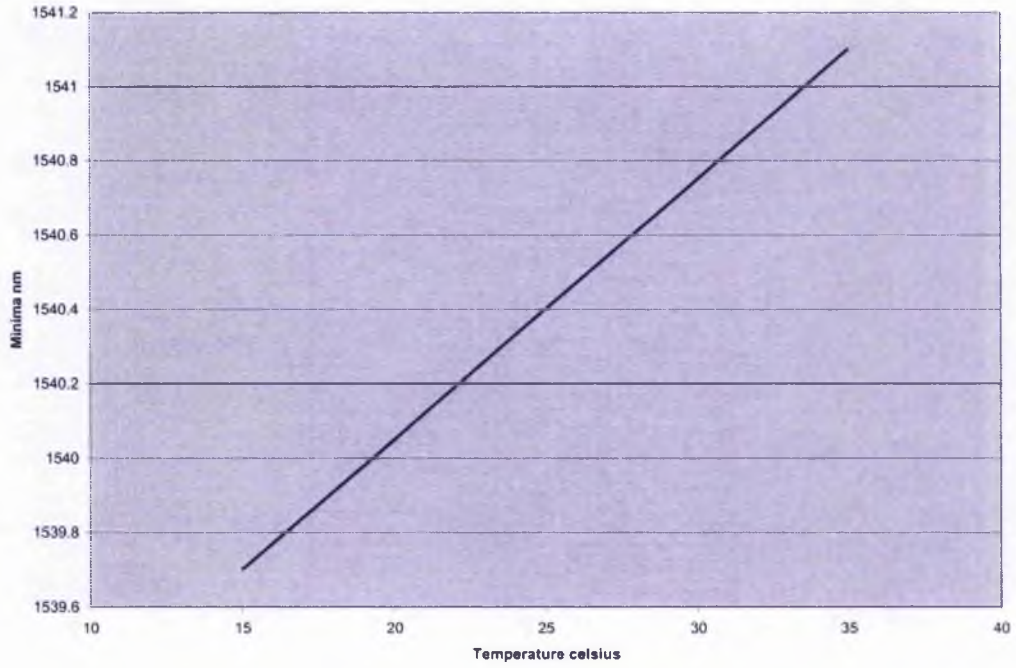


Figure 104 the variation of Bragg Dip versus Temperature.

In figure 104 we see that the relationship between the Bragg dip wavelength and the temperature, this is a fitted linear line to the results in table 5. Table 5 shows the scans were achieved with a shift of 0.3/0.4nm in the Bragg dip for every five degrees change in temperature. The result achieved is a shift of 1.4 nm whereas Cohen [102] obtained a shift of 2.4 nm over a 20 degrees change in temperature for a silicon relief

grating designed for 1537 nm. Cohen attributed its 8x difference to SiON due to the latter having a lower thermo-optic coefficient. In this case the difference between the figures obtained and Cohen's could be caused by either the poor conductivity between the sample and the Peltier or by the difference in thermo-optic effect between silicon/air gratings and silicon/as-implanted (damaged) silicon gratings.

Table 5 experimental results for the measurement of Bragg dip variation with temperature

Temperature	Wavelength nm
15	1539.7
20	1540.1
25	1540.4
30	1540.7
35	1541.1

Figure 105 shows the outer limits on the transmission curves over 15 to 35 degrees. The results obtained confirm that the samples could be used to create a viable temperature sensor for changes in the ambient temperature as well as a tunable filter. The spectrum taken at 15 degrees was run first thing in the morning and the spectrum at 35 degrees was taken about midday it is possible the difference in dip attenuation was caused by a shift in the ambient temperature.

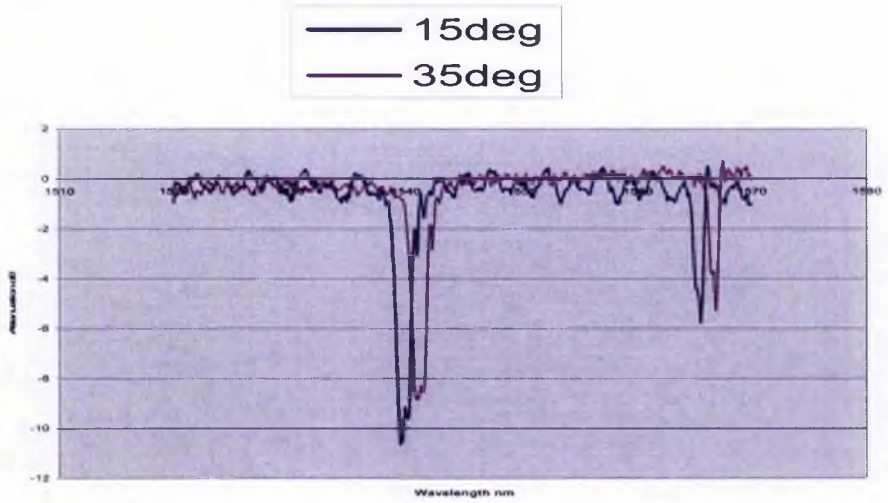


Figure 105 the outer limits of the transmission curves at 15 and 35 degrees (blue=15 and pink=35 degrees, respectively)

Atomic force microscopy (AFM [145, 146] was applied to the as implanted samples and showed the horizontal lines as viewed from the top of the implanted pattern of the gratings figure 106.

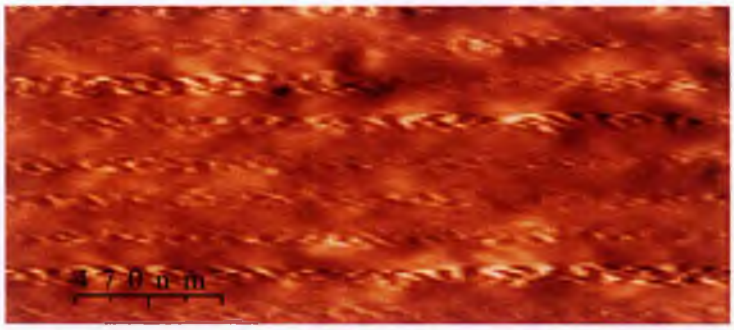


Figure 106 shows AFM (D1) from above and shows the ion implanted grating lines

Atomic force microscopy was applied to the as Implanted samples and revealed ridges 60nm deep as demonstrated in figure 107.

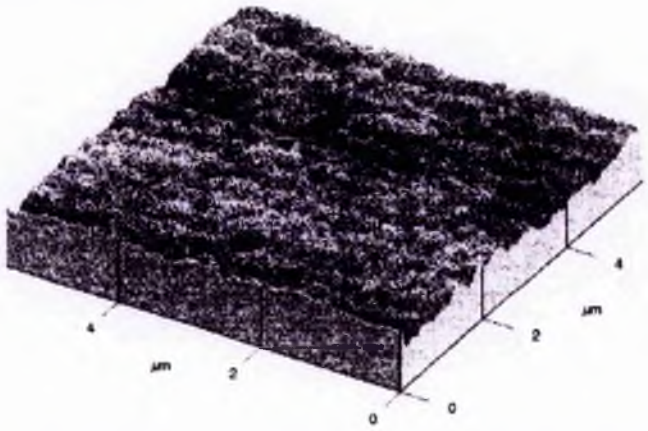


Figure 107 AFM of sample D1 (Ion as Implanted) revealing 60nm peaks

A sixty nm relief grating was simulated see figure 108 and revealed over 90 percent reflection of transmitted spectra at the target wavelength, since this is not revealed in the spectra of D1 as implanted the conclusion that somehow surface roughness had occurred in the sample and was not periodic was unavoidable and this would explain some of the noise in the as implanted spectra.

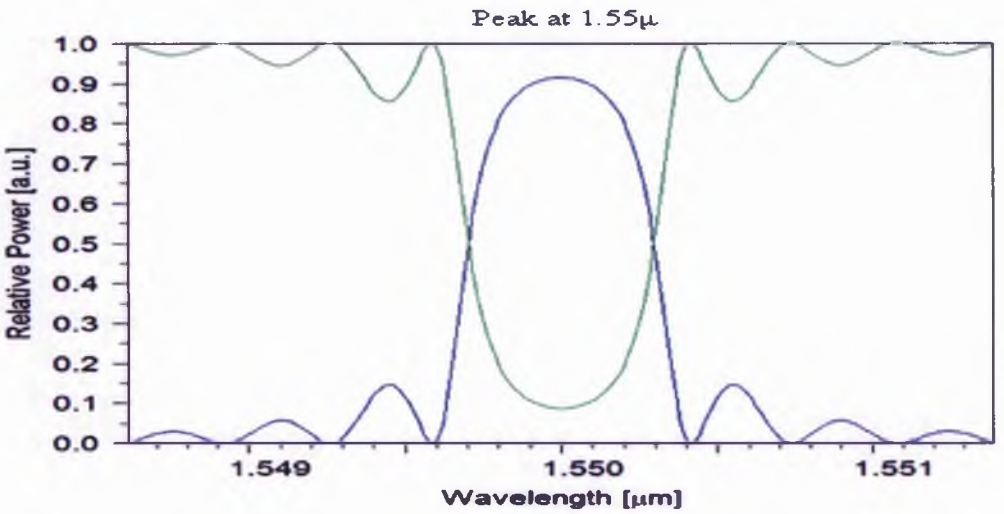


Figure 108 60 nm relief grating simulation: silicon/air

Annealing

The annealing was carried out at the Ion beam centre at Surrey University where the samples were held at the anneal temperature for four hours before cooling. The annealing was carried out in an argon environment.

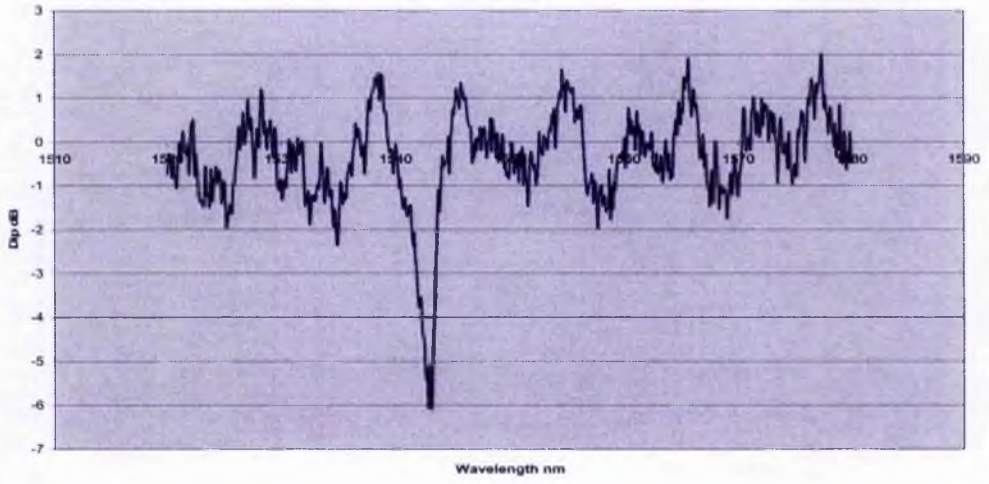


Figure 109 the effect on the TE curve of annealing sample C5 at 1100 degrees

In figure 109 we see the effect on the TE transmission curve of C5 of annealing at 1100 degrees and observe the extra noise compared with figure 110: as-implanted.

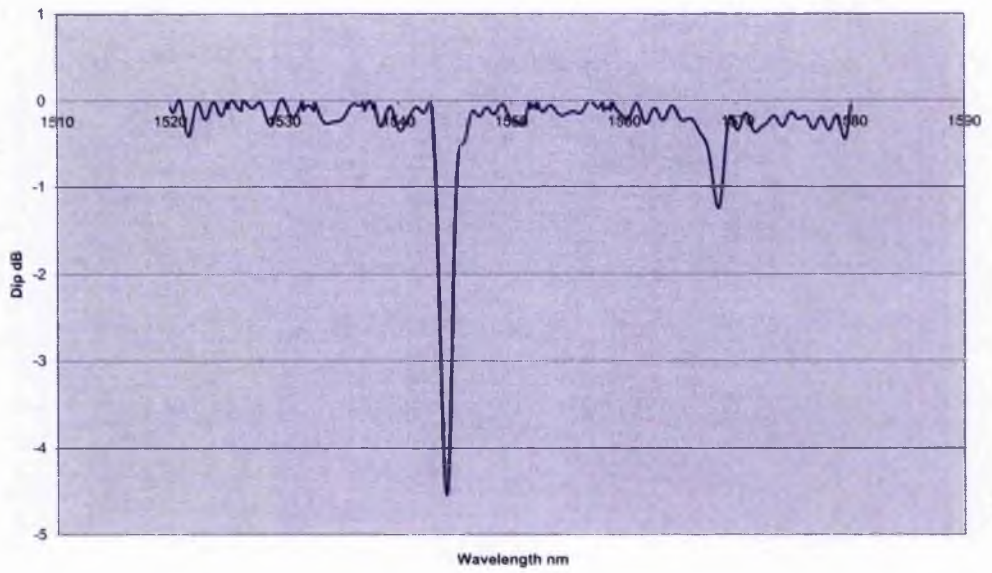


Figure 110 the TE resultant of sample C5 as implanted

In figure 110 we see the dip is slightly less: 4.5 dB as opposed to 6dB and the noise is of a different period, the noise in the as implanted is Fabry-Perot. The noise addition in the annealed sample is possibly caused by the incomplete nature of the anneal, leaving un-aggregated silica islands next to the silica layer and possibly causing diffraction effects [23].

Figure 111 the rounded edge of the damaged grating

In figures 111 and 112 we see the disastrous effects of annealing at 1350 degrees with damage to the grating in 111 and de-lamination in 112.

Figure 112 the damaged grating at the top and delamination below

Sample B4 was annealed to 1350 degrees but experienced de-lamination of the top layer and loss of grating function (see figures 111 and 112).

This was thought to be due to the usage of Smartcut ™ SOI wafers which are considered to be more fragile than Simox or Besoi[see references 147, 148].

With this in mind D3 was chosen as a sacrificial sample and annealed at 1100 degrees. At 1100 degrees the noise on the scan was increased but the transmission dips were still in the same place. Sample D3 gave a better TE grating dip than as-implanted but the noise was considerably enhanced possibly as the annealing was not at the ideal temperature (1350 degrees for four hours [24]).

Sample D3 was further annealed to 1200 degrees but showed delaminating damage at the facet edges and the grating structure was destroyed as with B4: the outlines of the grating were still visible but the grating was reduced to several discontinuous oval shapes and showed no evidence of a grating dip on the transmission setup.

Sample C5 was only taken to 1100 degrees annealing for four hours. C5 gives 6 dB attenuation in the Bragg TE dip after annealing as opposed to 4.5 before. As can be

seen from the scan little change in Bragg Dip wavelength had occurred but the noise had changed giving rise to the suspicion that incomplete annealing had occurred and the islets of silica caused by the implantation had not completely conglomerated and were causing problems with the spectral scans [23] see figures 109 and 110.

Uncertainty

The periodicity caused by the e-beam writing was considered to have an error of 4nm [144] and so, from figure 95, must be causing an error of 4nm on the position and from table 5 the possible variation in ambient temperature in the autumn of about 15 degrees gives an error of about 1nm in dip value (since 20 degrees gave an overall change of 1.4 nm) and so the overall error in Bragg dip reading may be as high as 5nm from one sample to another. D2 thermal oxide gave a dip at 1546 nm this being the highest of that type whereas the simulator gave a result of 1551 nm and thus there is an uncertainty in the simulation of about 5 nm; possibly some of this difference being due to the fact that there is an uncertainty in the simulation as Gratingmod is designed for FBGs.

8 Discussion

Introduction

This project has been beneficial both academically to the author and to the field of silicon photonics. The results obtained from the study of flat Bragg gratings in SOI have produced a better understanding of planar SOI waveguides. It has also been an interesting project from the evolution of the fundamental concepts necessary to design the device, to the experimental considerations for properly investigating the characteristics of the fabricated devices. Also, with the unexpected results such as secondary dips in the transmission spectra, a more fundamental level of understanding of these devices has been obtained by the author. The aim of this chapter is to discuss the key findings of this research and the conclusions that may be drawn from them.

Gratings have been demonstrated functioning at 1540nm (TE mode) a significant telecommunications wavelength and this is sufficiently near to the target of 1550nm bearing in mind the error of 4nm on the periodicity [144] and the rather approximate method of simulation to validate the design process. If these gratings could be inexpensively manufactured then items of use in Wavelength Division Multiplexing such as add drop filters, wavelength routers, Fabry-Perot cavities and tuneable filters could be realised in SOI and mass produced thus reducing cost and increasing market share.

Transmission dips of the order of 17 dB, coupled with a FWHM of 1nm has been obtained at a grating length of 1000 micron with sample D2 as implanted. Attenuation of 17dBs has also been achieved with just one grating dip observed: with sample C2 thermally oxidised which was a quarter of the length of sample D2 as Implanted. Sample C2 thermal oxide seems to imply that greater grating efficiency can be possible.

D1-3 (with 100, 1000 and 500 microns of grating length respectively) as implanted gratings reveal a linear increase in grating attenuation (expressed in dBs see figure

113 reproduced below for the TE polarization plot) as a function of the increase in length.

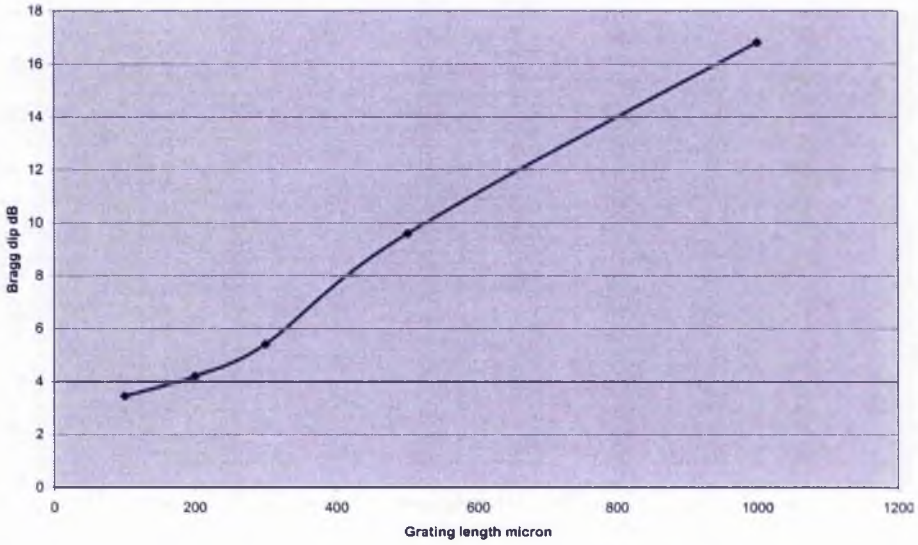


Figure 113 reproduced from Figure 84 grating dip versus grating length for Ion as Implanted TE

This compares with the lower portion of the simulation figure 114 reproduced below.

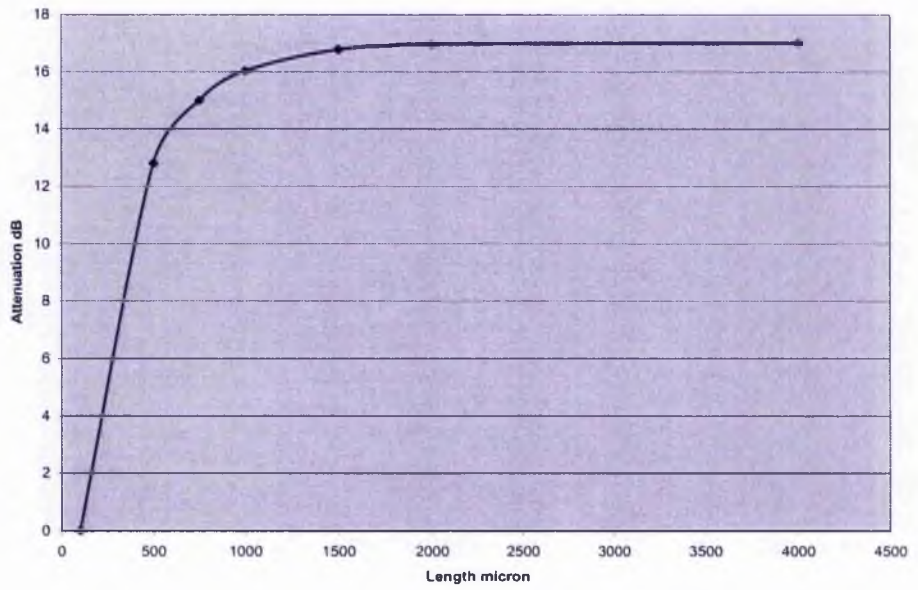


Figure 114 reproduced from Figure 32 first order grating length simulation [121]

Figure 114 reproduced above derived by way of the Gratingmod ™ simulator suggests a region of the grating length versus attenuation curve where the relationship is linear. The primary dip wavelength in as implanted samples of the same nominal

periodicity varies from 1541 to 1543.9nm. The deviation from the nominal design wavelength may be caused by the uncertainty in the periodicity which had a possible maximum variation of 4nm [144]. Figure 115 has a slope of unity for change in Bragg dip wavelength with period and therefore a change in wavelength of 4 nm would be observed.

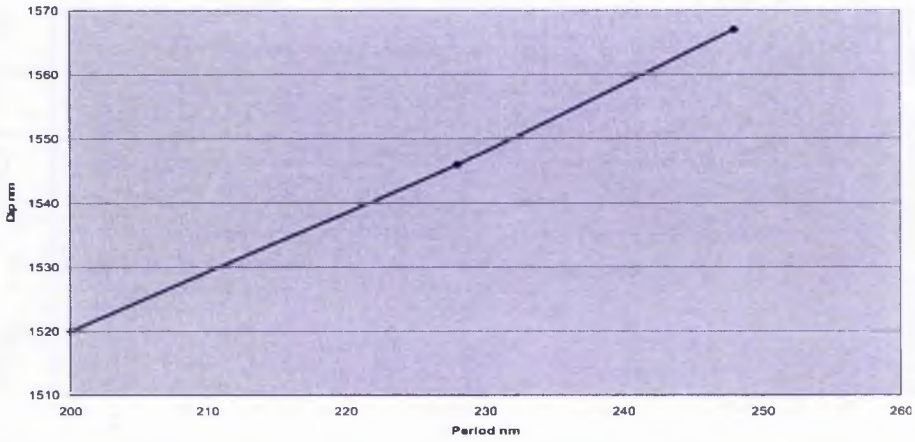


Figure 115 dip versus period (thermal oxide only)

The full width at half maximum (FWHM) was found to be 1nm or less (with the exception of B2/C5 for which see below), this agrees well with the 1nm obtained by simulation see figure 50 reproduced below for a 100 nm depth grating. Samples B1, B2, B3 and B4 (duty cycle 1, 0.9, 0.95 and 1.05) as implanted reveal little change in attenuation, FWHM, and dip wavelength with duty cycle. This may be caused by problems with the ion implantation straggle swamping the changes in duty cycle of the gratings. Since the change in duty cycle is of the order of 10% of the period (228nm) this is consistent with the 22.3nm straggle predicted by SRIM (see Appendix 1). The extra error must have been caused either by the ion beam being divergent. From the present data it is not possible to gain a quantitative estimate of the straggle.

Sample B5 (248nm periodicity and 250nm length) as implanted displays a shifted dip wavelength consistent with its increased periodicity and also shows increased attenuation at the dip wavelength compared to its as implanted counterparts of the same length. Possibly this is caused by the fact that although the sample has a second dip at 1620nm, it is fairly small compared with the others and represents only a small loss of energy to higher order modes. The increased Full Width at Half Maximum is

possibly due to modality. The second dips were not caused by TM/TE breakthrough as the wavelength is inconsistent. The size and the number of gratings per chip were also not a factor. Finally non apodised gratings give leakage through the side lobes (see figure 50) and these are shown in the simulation to be equidistant from the Bragg dip and this is clearly not happening with these samples. Figure 50 is reproduced below as 116.

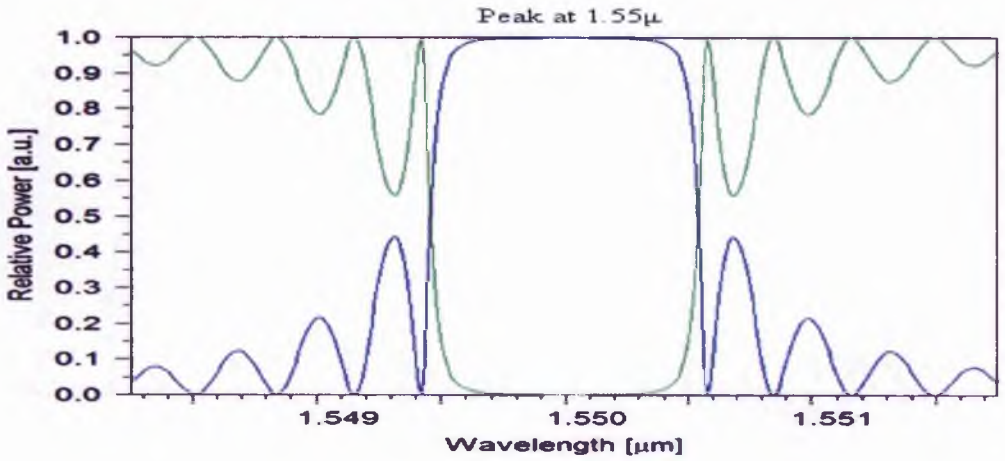


Figure 116 (Figure 50) Transmission (green)/Reflection (blue) spectrum for 60nm depth of grating

Thus higher modality was shown to be one of the more probable causes of the second transmission minima in the free space scans.

The thermal oxide gratings gave a dip of lower attenuation than the ion as implanted, with the exception of B5 and C2 at the edge of the range of wavelengths considered. These two samples also gave increased FWHM compared with the rest. It is not possible to create a definitive conclusion on the basis of the data: no second dips were observed but this is just in the confines of the measurement taken (1500 to 1610 nm) on the then available setup. The possibility that in their case higher order modes were coalescing into the main Bragg dip and increasing its dip attenuation and FWHM exists; however, much work would be needed to substantiate this hypothesis.

The variation of Bragg dip (as implanted) with temperature was monitored and found to be linear see figure 117 reproduced below, in agreement with Cohen et al. [102] and reported to be dependent on the thermo-optic effect of silicon.

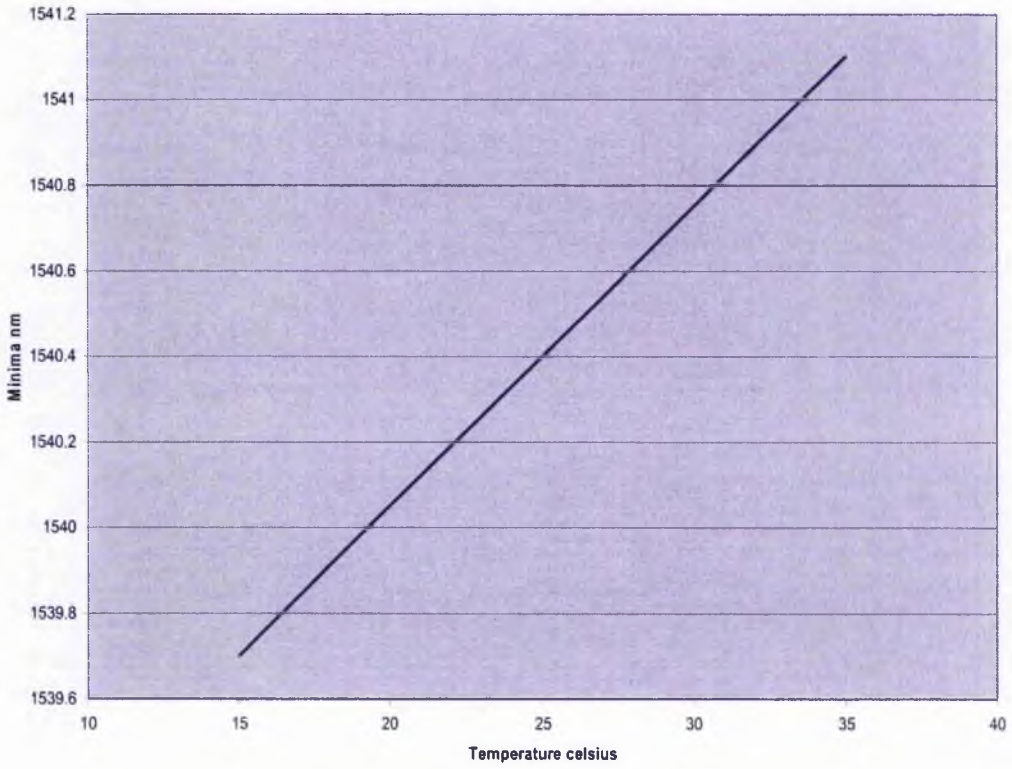


Figure 117 the variation of Bragg Dip versus Temperature.

The gratings made at Surrey University display a change of 1.4 nm over a variation of 20 degrees and Cohen's silicon relief gratings are showing 2.4 nm shifts over a similar range the difference either caused by different thermo-optic effect in the gratings or poor contact with the Peltier. However despite the differences the basis for a temperature sensor (or thermally tunable filter) has been shown.

An increase in Bragg dip wavelength with deviation from unity duty cycle ratio was observed for the thermal oxide gratings (see figure 118).

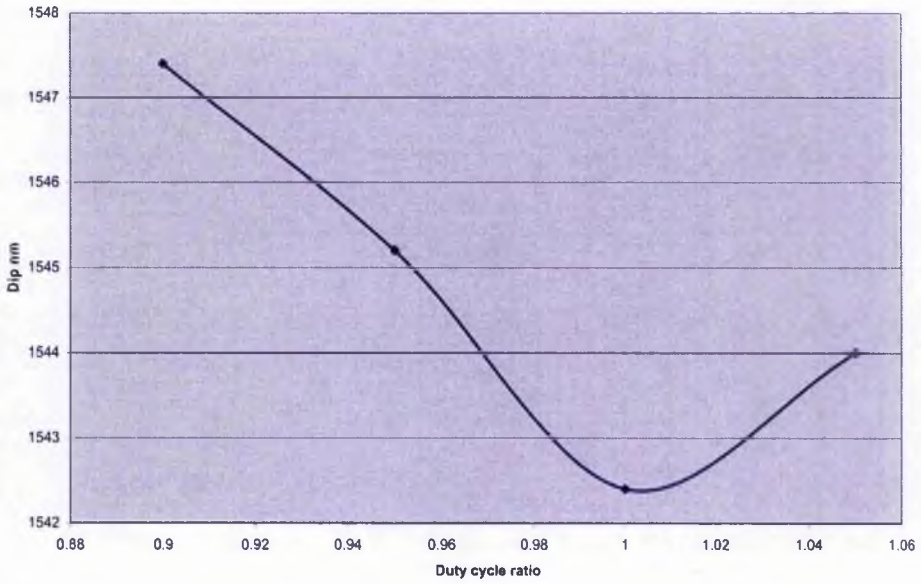


Figure 118 dip versus duty cycle thermal oxide

This compares favourably with the simulation figure 119 shown below.

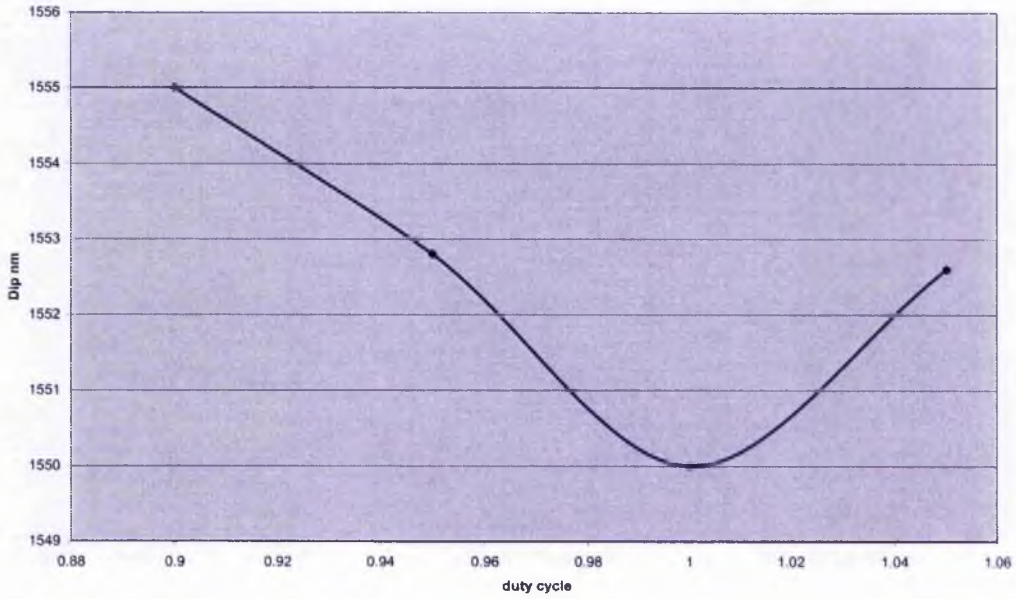


Figure 119 simulated change in Bragg dip with mark to space ratio

The reason for this may be that the thermal oxide gratings have no implantation straggle and thus give a genuine result whereas the ion implanted ones may have sufficient straggle to swamp the experiment. The figure of 22.3nm straggle that had been predicted by Srim (Appendix 1) is of the same order as the variation in the duty

cycle of the grating masks (10% of 228nm being 22.8nm). Quantitative conclusions are difficult to draw but clearly any change in duty cycle according to the simulator causes an increase in dip wavelength, this is confirmed by the thermal oxide result with the difference in absolute wavelength possibly caused by oxide diffusion and the difference between as implanted and thermal oxide due to implantation straggle.

Atomic Force Microscopy (AFM) showed 60nm fluctuations in the surface of the ion as implanted gratings. According to the modelling if this were periodic it should have created a grating with 90% Bragg dip attenuation in transmission since this was not the case the surface roughness must be random and must therefore have made a contribution to the noise in the results. This is shown in figure 120 reproduced below.

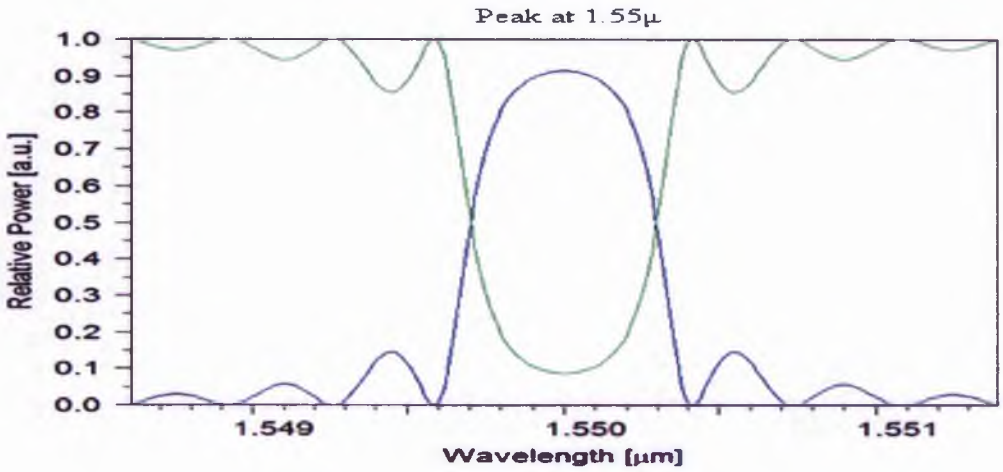


Figure 120 60 nm relief grating simulation: silicon/air

Annealing was only partially successful with grating damage occurring at or above 1200 Celsius. The wafers were Smartcut and could not survive the target temperature of 1350 Celsius for four hours [24]. Smartcut does seem to exhibit fragility compared with other SOI [147, 148]. The results of the annealing were inconclusive but the dip magnitude increased by 1.5 dB and there was more FP noise.

The thermally oxidised gratings at 228 nm periodicity display a variation in dip wavelength from 1542.4 nm to 1546.3 nm as measured on samples D1, D2 and D3.

From the previous discussion of temperature the variation in dip due to ambient changes could be as high as 1nm. The uncertainty in e-beam positioning was given as 4nm maximum [144] thus the 3.9nm differential is easily explained by e-beam plus ambient. The target wavelength was 1551 nm see figure 121: simulation. Thus the maximum difference between the simulation target and the result for sample D2 thermal oxide was 4.7nm; possibly some of this is due to the fact that Gratingmod was designed for FBGs and not SOI.

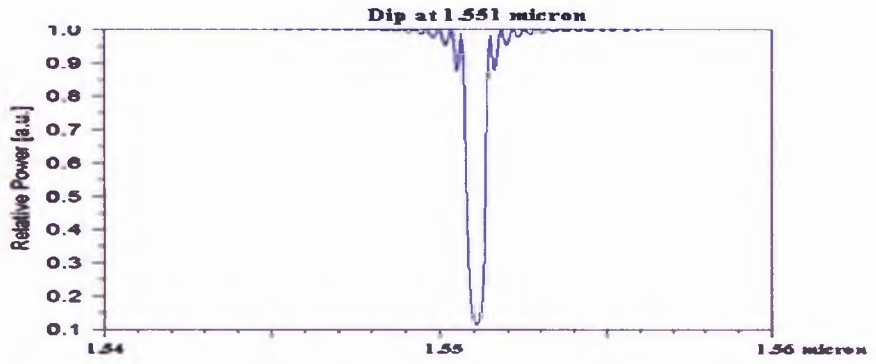


Figure 121 simulation for the thermal oxide grating at 228nm period

Whilst the Thermally Oxidised gratings would provide a better engineered product it is likely that some sort of variation on the implantation approach would involve less production steps and be more commercially viable. The attempt to create stoichiometric Silicon Dioxide is less likely to appeal to industry since it involves the further expensive and time consuming step of annealing and also increased implantation dose. The as implanted samples proved that implantation damage could create good gratings despite the 500 degrees elevated temperature of implantation used to provide first order healing of implantation damage. Thus, if it were viable, masking followed by room temperature implantation, could create gratings using implantation damage and provide a two step and therefore simple and cost effective production sequence.

It is the author's contention that Bragg gratings could be made commercially viable by way of masking and implantation without the annealing step (once the work had been done to establish the viability of room temperature implantation) and that this

would establish a technique which would be in contention with Ring Resonators in Wavelength Division Multiplexing, Silicon on Insulator applications, and that the ease of fabrication of grating related SOI could lead to gratings becoming the method of choice in many applications (much as macro-gratings had become the method of choice as opposed to prisms in the realm of spectrometry etc.). It is admittedly not always easy for an external observer to deduce why a technique had become a method of choice in industry, but in this case the process is ergonomic, needing little initial tooling once the process setup is complete, leads to mass production fairly easily and so the prediction as to what industry might do in terms of ULSI communications bottlenecks is not very risky. For an example of applications in ULSI please see the work of Kintaka et al [57] and their comments with respect to Bragg gratings and Wavelength Division Multiplexing.

9 Conclusion

It should be possible to create gratings with FWHM of 1nm and functioning anywhere in the region of 1520 to 1570nm by varying the periodicity from 200 to 248nm. Also gratings of 17dB attenuation have been demonstrated using a grating repeat length of 250nm. (In order to achieve this it is necessary to investigate the causes of the enlarged FWHM at the extremities of the wavelength range which may well be caused by modality.)

The possibility of creating Bragg gratings by thermal oxidation, ion bombardment damage and to a lesser extent ion bombardment unto stoichiometry via annealing have been investigated and presumably the bombardment damage, especially if it could be achieved at room temperature, would be the most ergonomic and likely to become the method of choice in industry.

10 Future Works

Introduction

A series of additional experiments can be envisaged to further develop the understanding of the work in this project. This work is presented in the list below.

1 One of the issues with the methodology of the project is that it is difficult to simulate planar or rib wave guide photonics and then superimpose a Bragg grating and then move on into fabrication. In the absence of a more rigorous mathematical analysis of the effect of gratings in SOI a more pragmatic approach was adopted using approximate simulation. Placing a Bragg grating on the top of a rib waveguide or a planar waveguide affects the optical field situation and affects modality [88, 98]. The presence of secondary dips in some of the transmission spectra suggests the existence of higher order modes. The 'second dip phenomenon' was unchanged with reducing chip size since one of the gratings obtained after the abortive attempt at anti-reflection coating was left on an area of silicon approximately 4 by 3 mm. and this was polished and tested. Likewise reducing the number of gratings per chip from two to one had no effect. The second dip phenomenon was not related to TM/TE breakthrough as the wavelength was inconsistent but was not observed with thermal oxide samples C2 and B5 dipping 1520 or 1567 nm although they had increased FWHM. This further suggests modal issues in 1.5 micron SOI at or around 1550nm, see figure 122 below.

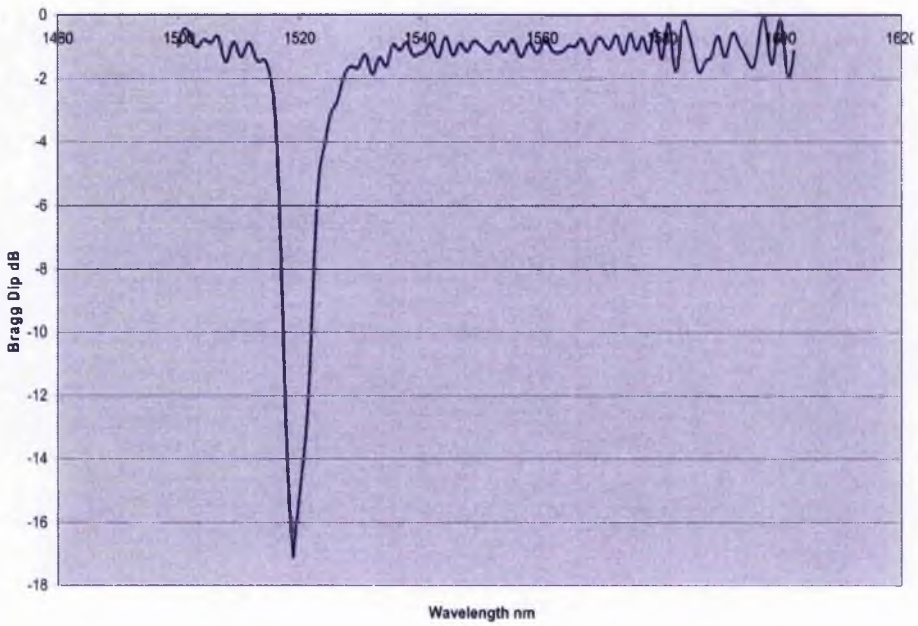


Figure 122 C2TE thermal oxide free space transmission spectral scan

However, in the absence of an accurate theory of gratings in SOI a more definitive conclusion cannot be drawn. Thus there is the need for more theory and experiment.

2 Try implanting Nitrogen into SOI for comparison, since it is reasonable to assume that a commercially viable process for creating gratings involving masking and implantation has been described but no comparison of implantation ions has been attempted. It would also be instructive to see how the extra mobility of the nitrogen ions affect the depth of implantation and thereby grating performance and possibly to compare oxygen and nitrogen based annealing.

3 It would be instructive to compare different implantation temperatures in order to investigate the effects on implantation damage and its healing. From this would come an understanding of the refractive index change on the exposed wafer areas. It may well be that the

gratings could be constructed with room temperature implantation. If this turns out to be the case then it is necessary to optimise the refractive index change with respect to ion flux. Once this work is completed industry could be presented with an inexpensive two step package for creating Bragg gratings en masse.

4 A tuneable optical add-drop multiplexer based on the thermo-optic effect could be demonstrated by incorporating the gratings into a Mach-Zehnder interferometer in the manner of Tao Chu [149] with the exception of utilising rib waveguides rather than his wire waveguides, and this again would be of considerable benefit to WDM SOI research.

5 Reflection tests should be carried out on the gratings. In house rib waveguides had been etched onto one of the samples (D1 as implanted) by stripping the silicon nitride with boiling phosphoric acid and etching with silicon hexafluoride gas. This sample was destroyed in the course of externally contracted anti-reflection coating and so no results have been reported here.

6 It would be good to apodise the gratings and observe the effect on side-lobe suppression also it might help to reduce oscillations in the transmission/reflection spectra which would be a possible contribution to noise. Apodisation could either be by way of varying the amplitude or duty cycle of the gratings.

7 If possible sine and square gratings could be compared with a view to investigating whether they might provide lower loss or better reflection, although fabrication issues might make this difficult.

8 Although the temperature dependence has been determined it would be helpful to demonstrate a fully characterised working temperature sensor and a thermally tunable filter with feedback control.

9 Gas, liquid and proximity sensors could be demonstrated, it should be possible to encapsulate the gratings to protect against hazardous environments.

10 The chips were Smartcut ™ and experienced complete de-lamination on annealing at 1350 degrees [147, 148] which would otherwise be the ideal annealing temperature in the absence of optical annealing [24, 27]: the usage of Besoi or Simox would presumably enable higher annealing temperatures (1100 degrees was used). In general grating transmission attenuation had improved with annealing but more noise was visible. A better approach to stoichiometry would be provided by using other SOI and annealing to 1350 for four hours [24].

11 Silicon Nitride was used as a mask for this project and was invaluable since it not only functioned as a mask for the ion implantation but also for the thermal oxidation as it was impervious to oxygen or water vapour penetration. If however, stoichiometry was to be achieved for shallow gratings then possibly an ion flux of greater than 1.6×10^{17} ions/cm^2 would be considered, in which case the nitride mask would be completely sputtered and become useless. Therefore other masking would need to be considered.

12 In the published literature relating to Silicon on Insulator, Bragg Gratings are either configured as high reflectivity periodic structures used to improve Fabry-Perot cavity finesse (Liu and Chou [78]) or as part of a hybrid p-i-n modulator which is used to vary the Bragg dip

wavelength and hence the intensity of the propagating light (Cutolo et al [61]). Therefore, the idea that every instance of macroscopic gratings could be replicated in SOI had not been completely investigated. There was some talk at the University of Alberta of attempting to realise Cutolo's work with electrical control of Bragg dip, in the real world, since his work was in simulation, but thus far nothing has been published. The gratings created in this project could be used in this respect.

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Appendix 1 SRIM

Srim was run to obtain figures for straggle as well as compare implantation depths. The figures obtained are reproduced below and the row of interest to the project is that commencing 20 keV and giving a longitudinal straggle of 223 angstroms.

SRIM version ---> SRIM-2000.39
Calc. date ---> May 19, 2004

Target = Oxygen in Silicon
Density = 2.3212E+00 g/cm3 = 4.9770E+22 atoms/cm3
======== Target Composition ========

Atom Name	Atom Numb	Atomic Percent	Mass Percent
Si	14	100.00	100.00

Disk File Name = Oxygen in Silicon
Stopping Units = MeV / (mg/cm2)

Ion = Oxygen [8] , Mass = 15.995 amu

Ion Energy	dE/dx Elec.	dE/dx Nuclear	Projected Range	Longitudinal Straggling	Lateral Straggling
10.00 keV	5.688E-01	7.384E-01	248 A	132 A	96 A
11.00 keV	5.894E-01	7.316E-01	270 A	142 A	103 A
12.00 keV	6.090E-01	7.244E-01	292 A	152 A	111 A
13.00 keV	6.276E-01	7.169E-01	314 A	161 A	117 A
14.00 keV	6.452E-01	7.092E-01	336 A	170 A	124 A
15.00 keV	6.622E-01	7.014E-01	358 A	180 A	131 A
16.00 keV	6.784E-01	6.936E-01	380 A	189 A	138 A
17.00 keV	6.940E-01	6.858E-01	402 A	197 A	144 A
18.00 keV	7.090E-01	6.782E-01	424 A	206 A	151 A
20.00 keV	7.376E-01	6.631E-01	469 A	223 A	164 A
22.50 keV	7.709E-01	6.449E-01	524 A	244 A	180 A

Appendix 2: RSoft Gratingmod Software [121]

A: Programme to simulate grating reflectivity at various depths of implantation.

Ave_height = (Max_height+Min_height)/2

L = 1000

Max_height = Min_height+Mod_depth

Min_height = 1.45

Mod_depth = 0.05

Period = 0.228

alpha = 0

background_index = 1.447

boundary_max_y = 1.52

cover_index = 1

delta = 2.031

dimension = 3

domain_max = 5

eim = 0

free_space_wavelength = 1.55

grating_fixlambda = 1

grating_mode_output = 0

grating_scan_option = 4

height = 1.5

index_display_mode = DISPLAY_CONTOURMAPYZ

k0 = (2*pi)/free_space_wavelength

launch_type = LAUNCH_GAUSSIAN

profile_type = PROF_STEPINDEX

sim_tool = ST_GRATINGMOD

slab_height = 0.6

slice_display_mode = DISPLAY_CONTOURMAPXY

structure = STRUCT_RIBRIDGE

width = 1.1

user_taper 1

type = UF_GRATING

gr_profile_type = 1

gr_apodization_type = APOD_UNIFORM

gr_chirp_type = CHIRP_LINEAR

gr_phase = 0

gr_period = Period

gr_apodization_coef = 0

gr_chirp_coef = 0

end user_taper

segment 1

index_taper = TAPER_USER_1

height_taper = TAPER_USER_1

begin.x = 0

begin.z = 0

begin.height = Ave_height

end.x = 0 rel begin segment 1

end.z = L rel begin segment 1

end.height = Min_height

end segment

N.B. Please note that with Gratingmod ™ it is necessary to first run the mode simulator and then run the full simulation with the usage of the pre-determined modal characteristics otherwise modal considerations will cause programme errors.

Appendix B Programme obtained from RSoft to simulate mode change in a complex grating.

Depth = 0.1

Length = 1024

N0 = background_index

N1_average = (N1_min+N1_max)/2

N1_max = Nmat1

N1_min = N0

N2_average = (N2_min+N2_max)/2

N2_max = Nmat2

N2_min = Nmat1

N3 = Nmat1

N4 = Nmat3

Nmat1 = 3.3

Nmat2 = 3.5

Nmat3 = 1.5

Period = 0.228

W1 = 0.1*(5/12)

W2 = 0.2

W3 = 0.3

W4 = 0.4

alpha = 0

background_index = 1

boundary_max = 2

boundary_min = -2

delta = 0.1

domain_min = 0.5*Period

eim = 0

free_space_wavelength = 1.55

grating_scan_option = 7

height = 0

index_display_mode = DISPLAY_CONTOURMAPXZ

k0 = (2*pi)/free_space_wavelength

launch_position = -0.5

launch_type = LAUNCH_GAUSSIAN

launch_width = 0.15

profile_type = PROF_STEPINDEX

sim_tool = ST_GRATINGMOD

slice_step_size = Period/4

step_size = Period/4

width = 5

```
user_taper 1
    type = UF_GRATING
    gr_profile_type = 0
    gr_apodization_type = APOD_UNIFORM
    gr_chirp_type = CHIRP_LINEAR
    gr_phase = 0
    gr_period = Period/2
    gr_apodization_coef = 0
    gr_chirp_coef = 0
end user_taper
user_taper 2
    type = UF_GRATING
    gr_profile_type = 1
    gr_apodization_type = APOD_UNIFORM
    gr_chirp_type = CHIRP_LINEAR
    gr_phase = 0
    gr_period = Period
    gr_apodization_coef = 0
    gr_chirp_coef = 0
end user_taper


segment 1
    color = 9
    begin.x = -W1/2-W2-W3-W4
    begin.z = 0
    begin.width = W1
    begin.delta = N1_max+0*N1_average-N0
    end.x = 0 rel begin segment 1
    end.z = Length rel begin segment 1
    end.width = W1
```

```
    end.delta = N1_max+0*N1_min-N0
end segment

segment 2

    color = 12
    begin.x = width/2
    begin.z = 0
    begin.delta = Nmat3-N0
    end.x = 0 rel begin segment 2
    end.z = Length rel begin segment 2
    end.delta = Nmat3-N0
end segment

segment 3

    color = 10
    begin.x = -W2/2-W3-W4
    begin.z = 0
    begin.width = W2
    begin.delta = N2_average-N0
    end.x = 0 rel begin segment 3
    end.z = Length rel begin segment 3
    end.width = W2
    end.delta = N2_average+0*N2_max-N0
end segment

segment 4

    color = 11
    begin.x = -W3/2-W4
    begin.z = 0
    begin.width = W3
    begin.delta = N3-N0
    end.x = 0 rel begin segment 4
    end.z = Length rel begin segment 4
    end.width = W3
    end.delta = N3-N0
```

```
end segment

segment 5
    color = 13
    begin.x = -W4/2
    begin.z = 0
    begin.width = W4
    begin.delta = N4-N0
    end.x = 0 rel begin segment 5
    end.z = Length rel begin segment 5
    end.width = W4
    end.delta = N4-N0
end segment



launch_field 1
    launch_pathway = 0
    launch_type = LAUNCH_GAUSSIAN
    launch_tilt = 0
    launch_mode = 0
    launch_mode_radial = 1
    launch_width = 0.15
    launch_position = -0.5
end launch_field
```

Appendix C Programme obtained from RSoft to simulate complex grating characteristics.

```
Depth = 0.1
Length = 100
N0 = background_index
N1_average = (N1_min+N1_max)/2
N1_max = Nmat1
```

N1_min = N0

N2_average = (N2_min+N2_max)/2

N2_max = Nmat2

N2_min = Nmat1

N3 = Nmat1

N4 = Nmat3

Nmat1 = 3.3

Nmat2 = 3.5

Nmat3 = 1.5

Period = 0.2456

W1 = 0.1

W2 = 0.2

W3 = 0.3

W4 = 0.4

alpha = 0

background_index = 1

boundary_max = 2

boundary_min = -2

delta = 0.1

domain_max = 1

domain_min = 0.5*Period

eim = 0

free_space_wavelength = 1.55

grating_fixlambda = 1

grating_mode_autocalc = 0

grating_mode_file_back_1 = ff.m00

grating_mode_file_fwd_1 = ff.m00

grating_mode_numback = 1

grating_mode_numfwd = 1

grating_scan_option = 7

height = 0

index_display_mode = DISPLAY_CONTOURMAPXZ

k0 = (2*pi)/free_space_wavelength

launch_position = -0.5

```
launch_type = LAUNCH_GAUSSIAN
launch_width = 0.15
profile_type = PROF_STEPINDEX
sim_tool = ST_GRATINGMOD
slice_step_size = Period/4
step_size = Period/4
width = 5


user_taper 1
    type = UF_GRATING
    gr_profile_type = 0
    gr_apodization_type = APOD_UNIFORM
    gr_chirp_type = CHIRP_LINEAR
    gr_phase = 0
    gr_period = Period/2
    gr_apodization_coef = 0
    gr_chirp_coef = 0
end user_taper
user_taper 2
    type = UF_GRATING
    gr_profile_type = 1
    gr_apodization_type = APOD_UNIFORM
    gr_chirp_type = CHIRP_LINEAR
    gr_phase = 0
    gr_period = Period
    gr_apodization_coef = 0
    gr_chirp_coef = 0
end user_taper


segment 1
    color = 9
```

```
    index_taper = TAPER_USER_2
    begin.x = -W1/2-W2-W3-W4
    begin.z = 0
    begin.width = W1
    begin.delta = N1_average-N0
    end.x = 0 rel begin segment 1
    end.z = Length rel begin segment 1
    end.width = W1
    end.delta = N1_min-N0
end segment

segment 2

    color = 12
    begin.x = width/2
    begin.z = 0
    begin.delta = Nmat1-N0
    end.x = 0 rel begin segment 2
    end.z = Length rel begin segment 2
    end.delta = Nmat1-N0
end segment

segment 3

    color = 10
    index_taper = TAPER_USER_2
    begin.x = -W2/2-W3-W4
    begin.z = 0
    begin.width = W2
    begin.delta = N2_average-N0
    end.x = 0 rel begin segment 3
    end.z = Length rel begin segment 3
    end.width = W2
    end.delta = N2_max-N0
end segment

segment 4
```

```
    color = 11
    begin.x = -W3/2-W4
    begin.z = 0
    begin.width = W3
    begin.delta = N3-N0
    end.x = 0 rel begin segment 4
    end.z = Length rel begin segment 4
    end.width = W3
    end.delta = N3-N0
end segment

segment 5
    color = 13
    begin.x = -W4/2
    begin.z = 0
    begin.width = W4
    begin.delta = N4-N0
    end.x = 0 rel begin segment 5
    end.z = Length rel begin segment 5
    end.width = W4
    end.delta = N4-N0
end segment



launch_field 1
    launch_pathway = 0
    launch_type = LAUNCH_GAUSSIAN
    launch_tilt = 0
    launch_mode = 0
    launch_mode_radial = 1
    launch_width = 0.15
    launch_position = -0.5
```

end launch_field

N.B. Please note it is necessary to run the modal programme first and then store the computed mode so that this may be entered into the height (main: appendix c) programme prior to running the grating analysis.