# CMOS Compatible Integrated Optical Isolator

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## Abstract

Herein we present our efforts to realise a novel integrated optical isolator. Utilising the principles of total internal reflection, the isolator is CMOS compatible and can be realised in a variety of materials.

## Introduction

The recent announcement of an electrically pumped light source on the material system of Silicon On Insulator (SOI) has improved the likelihood of a fully-integrated silicon photonic telecommunications platform [1]. However with the advent of an integrated light source, also comes the instability issues that can occur due to back reflections from subsequent components in the optical path. In discrete component systems, these problems can be avoided through the use of an optical isolator positioned between the light source and the optical circuit to block the reflected light. The optical isolators used in current systems generally work on the premise of Faraday rotation. Although effective in operation these particular isolators are not CMOS compatible as they require materials with strong magneto-optic coefficients, for example garnet. However there may be another way to realise an optical isolator that can be integrated into CMOS compatible devices. In this paper we demonstrate, through the use of modelling and theoretical analysis, the feasibility of an integrated optical isolator based upon total internal reflection.

## Isolator Design

Total Internal Reflection (TIR) is a well-known phenomenon that has been utilized in integrated optics for, among other things, switching [2]. TIR can also be utilised to create an optical isolator. As shown in Figure 1, the input light represented by the solid black line, propagating in the material of lower refractive index (doped region) towards the interception of the three waveguide predominantly undergoes refraction across the interface with the region of higher refractive index (un-doped region). This light will exit the device via the output waveguide. Any back reflected light propagating back towards this interface can undergo total internal reflection providing that the index difference is sufficient. This case is represented in Figure 1 by the grey dashed line. The back reflected light is therefore reflected away from the input port, and thus providing isolation.
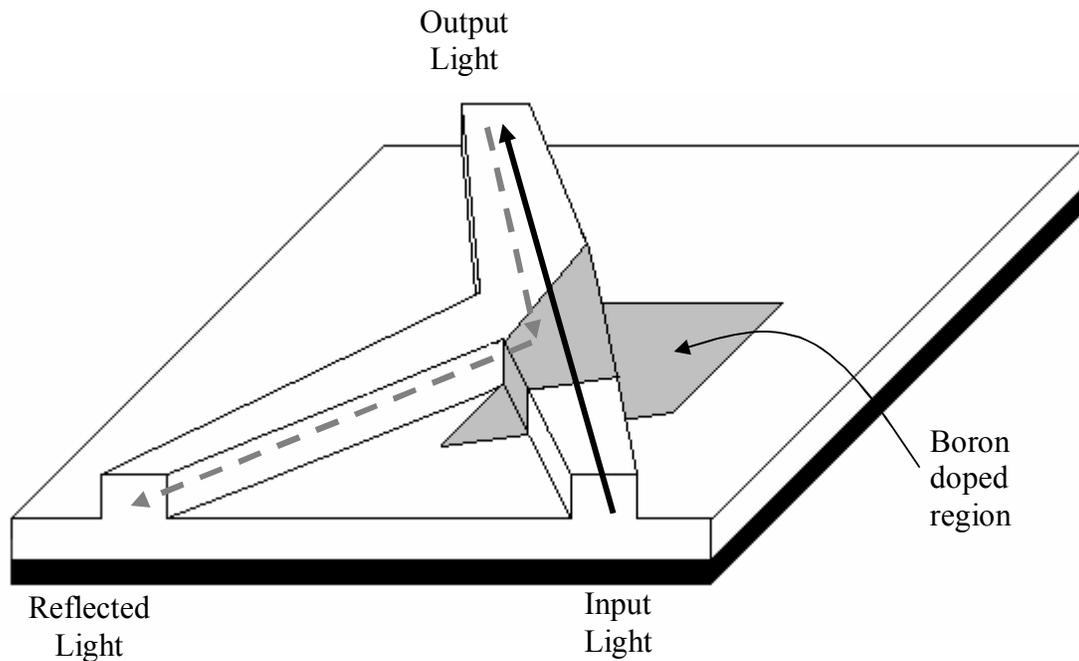
**Output Light**

**Boron doped region**

**Reflected Light**

**Input Light**

*Figure 1 – Diagram showing the layout of the optical isolator.*

### Device Fabrication

As the functionality of the proposed isolator is based upon the principles of TIR, the fabrication process can be tailored to many different material systems and device structures. This makes the proposed design highly advantageous as compared to devices based upon Faraday rotation. In the case of silicon photonic devices, the interface of the two differing refractive indices may be formed using a variety of techniques such as doping or implantation damage. The waveguides meanwhile may be formed by conventional fabrication means such as reactive ion etching or selective doping.

### Modelling

Modelling of a single device has been carried out in 3D BeamProp, a three dimensional BPM method modelling package from Rsoft [3] to predict the device's performance. Specific device dimensions are stated here in order to model the device although these dimensions have yet to be optimised. The waveguides have an initial width of 2.8μm but gradually taper outward over a length of 100μm to a width of 7μm in the centre of the device so as to reduce crosstalk. The interception angle between the waveguide and the material interface plane is varied between 1.5° and 2.5°. The refractive index change in this case is caused by doping the silicon with boron. Figure 2 demonstrates that for a waveguide interception angle of 1.5° and boron doping concentration of $8e18$ cm$^{-3}$ an isolation of approximately 17dB can be achieved with an insertion loss of only 2dB.
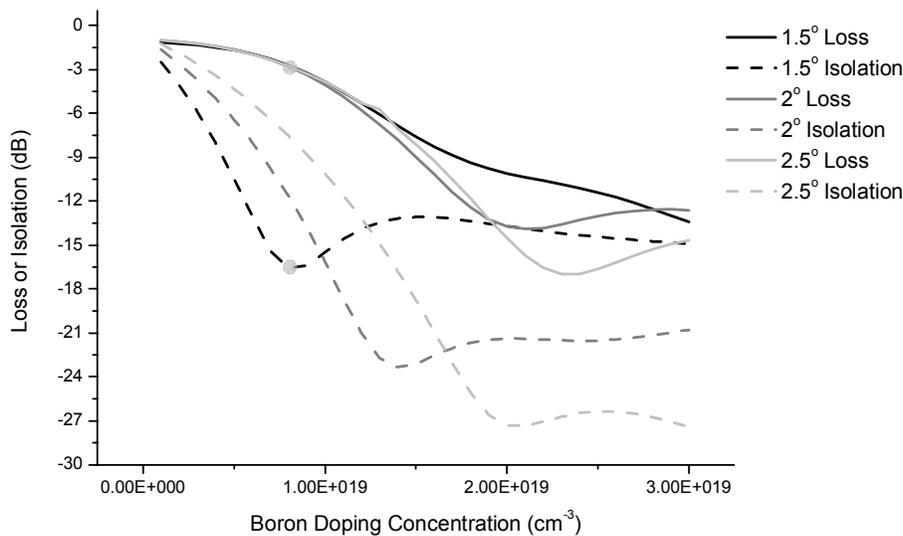
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***Figure 2 – Modelling results showing the level of isolation and associated loss through different doping concentrations and waveguide interception angles.***

As yet the device design has not been optimised and a much improved performance is expected through further optimisation of the device dimensions.

## Conclusion

Herein we have presented a means by which to realise a CMOS compatible isolator that has an insertion loss of approximately 2dB and isolation of 17dB. Furthermore this device can be integrated into plethora of integrated optical device configurations. It is believed that the development of such an isolator in integrated format can have significant benefits for future optical integrated circuits. Furthermore, device optimisation is likely to lead to a reduction in insertion loss.

## References

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