Analytical Models for Delay and Power Analysis of Zero-V_{GS} Load Unipolar Thin-Film Transistor Logic Circuits

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***Abstract*—In thin-film transistor (TFT) logic circuit applications, propagation delay and power dissipation are two key constraints to be considered in optimal circuit design and synthesis. The unipolar zero-V_{GS}-load logic design is widely used for implementation of TFT digital circuits, because of the simple structure, easy processing, and relatively high gain. In this work, the analytical models for delay and power were developed for zero-V_{GS}-load inverters, which clarify the relationships between device and design parameters and the two key design constraints. The proposed models were verified by circuit simulations, and could serve as a guideline for optimal design of unipolar zero-V_{GS}-load logic circuits.**

***Index Terms*—delay, power, thin-film transistor, zero-V_{GS} load inverter**

I. Introduction

With the advances of various semiconductor materials including organic small molecules, polymers and metal oxides, and related processing techniques, the potential applications of thin-film transistors (TFTs) in general signal processing for ubiquitous electronics are attracting more and more attention [1]-[7]. To prompt these advanced TFT applications, circuit-level design and optimization is becoming as crucial as performance improvement at the material and device levels. Propagation delay and power dissipation are two key constraints to be concerned in optimal circuit design and synthesis [8],[9]. To analyze and extract the delay and power of complex circuits, development of analytical models for the basic inverter circuit is the first step [10]-[13]. In silicon, numerous delay and power analytical models have been proposed for the complementary inverter circuit [14]-[16]. However, for most TFT technologies, it is difficult to find n- and p-type semiconductor materials with equivalent performance and compatible processes that would allow the fabrication of high performance complementary logic circuits. Therefore, various unipolar logic designs have been proposed [17]-[19]. At present, noise margin analytical models have been developed for optimal design of TFT circuits for the required robustness and yield [10],[11], however, a study of delay and power trade-offs and development of related models has not yet been undertaken. In this work, transient models for delay and power analysis were developed for the zero-V_{GS} load inverter, which is suitable for depletion-type TFTs to achieve high gain and large noise margin [20],[21]. Based on the models, the influence of the device and design parameters on the propagation delay and average power can be analyzed systematically. Although focusing on the zero-V_{GS} load type circuits, the presented approach in this work would also be a useful reference for developing analytical models for other types of unipolar TFT logic circuits.

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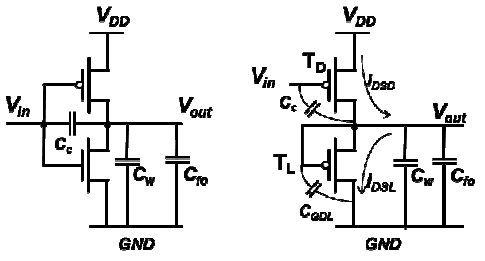
II. Derivation of the Models



(a) (b)

Fig. 1. The schematic of the inverter circuits with capacitance distributions: (a) the complementary type inverter and (b) the zero-V_{GS} load inverter.

Fig. 1(a) shows the circuit schematic of a standard complementary type TFT inverter, which is composed of a p-type TFT and a n-type TFT, while as shown in Fig. 1 (b), the p-type TFT zero-V_{GS} load inverter is composed of a p-type driving TFT (T_D) and a p-type load TFT (T_L). In the following analysis to derive the static and transient behavior models of the inverter, the conventional analytical field effect transistor (FET) current-voltage model was used with the drain-source current (I_{DS}) in the linear regime being described as:

$$I_{DS} = -(W/L)\mu C_{ox}\left(V_{GS} - V_{th} - V_{DS}/2\right)V_{DS} \quad (1)$$

and in the saturation regime being given by:

$$I_{DS} = -\left[W/(2L)\right]\mu C_{ox}\left(V_{GS} - V_{th}\right)^2\left(1 - \lambda\left(V_{DS} - V_{GS} + V_{th}\right)\right) \quad (2)$$

where W is the channel width, L is the channel length, C_{ox} is the gate dielectric capacitance per unit area, V_{th} is the threshold

voltage and λ is the output resistance parameter. In the following, for easy derivation of the explicit analytic transient models, λ is taken to be zero by assuming a large enough output impedance, which is applicable to most of the reported organic and oxide TFTs with relatively long channels.

Based on (1) and (2), the expressions of the transfer curve in different regions can be derived as following with the detailed procedure given in the appendix:

when $V_{in} < V_{in,a}$,

$$V_{out} = V_{in} - V_{th} + \sqrt{(V_{DD} + V_{th} - V_{in})^2 - N \times V_{th}^2} \quad (3)$$

when $V_{in} > V_{in,b}$,

$$V_{out} = V_{th} - \sqrt{V_{th}^2 - (V_{DD} + V_{th} - V_{in})^2 / N} \quad (4)$$

Here, $N = (W_L/L_L)/(W_D/L_D)$ is the relative sizing of T_D to T_L, assuming that all electrical parameters of the two TFTs are identical. W_D and L_D are the channel width and channel length of T_D, and W_L and L_L are the channel width and channel length of T_L. V_{DD}, V_{in} and V_{out} are the power supply voltage, the input and output voltage, respectively. $V_{in,a}$ is the input voltage when T_D transiting from the linear regime to the saturation region; $V_{in,b}$ is the input voltage when T_L transiting from the saturation region to the linear regime. $V_{out,a}$ and $V_{out,b}$ are the output voltages when $V_{in} = V_{in,a}$ and $V_{in} = V_{in,b}$, respectively. When $V_{in,a} \le V_{in} \le V_{in,b}$, V_{out} could be any value between $V_{out,a}$ ($V_{out,a} = V_{in,a} - V_{th} = V_{DD} - \sqrt{N} \times V_{th}$) and $V_{out,b}$ ($V_{out,b} = V_{th}$), since $V_{in,a}$ approximately equals to $V_{in,b}$ [10].

For the unipolar logics, during the whole operation period, V_{out} cannot be completely pulled up to V_{DD} or down to the ground (*GND*). The maximum and minimum V_{out} values, V_{max} and V_{min} can be obtained by taking V_{in} to be 0 and V_{DD} in (3) and (4), respectively, and are given as:

$$V_{max} = \sqrt{(V_{DD} + V_{th})^2 - N \times V_{th}^2} - V_{th} \quad (5)$$

$$V_{min} = V_{th} \times \left(1 - \sqrt{1 - 1/N}\right) \quad (6)$$

To analyze the dynamic behaviors of the inverter, it is important to determine the load capacitance of the circuit. As shown in Fig. 1(a), for the well-studied complementary type inverters, the load capacitance is normally considered to be composed of the wiring capacitance C_w and the fan-out gate capacitance C_{fo}. For more accurate analysis, the Miller effect also needs to be taken into account, resulting in the Miller capacitance as an additional part to the capacitive load. The Miller capacitance can be expressed as γC_C, where C_C is the coupling capacitance between the input and output nodes including the gate-to-drain capacitances of both p-type and n-type transistors, and γ is the Miller factor, with a typical value of 2 [8],[9]. In a p-type zero-V_{GS} load inverter as shown in Fig. 1(b), C_C only consists of the gate-to-drain capacitance of one transistor (T_D), and the gate-to-drain capacitance of T_L(C_{GDL}) becomes part of the load capacitance. Therefore, for the zero-V_{GS} load inverters, the total load capacitance can be expressed as:

$$C_L = C_w + C_{fo} + \gamma C_C + C_{GDL} \quad (7)$$

During transient operation, C_L is charged by the source-to-drain current of T_D (I_{DSD}), and discharged by the source-to-drain current of T_L (I_{DSL}), as shown in Fig. 1 (b). Therefore, the following differential equation can be obtained:

$$C_L (dV_{out}/dt) = I_{DSD} - I_{DSL} \quad (8)$$

Based on (1) and (2), transient equations of the output voltage (V_{out}) can be derived from (8). In the case of low-to-high V_{out} transition, T_D works in the linear regime and T_L starts to go from the linear regime into the saturation regime when $V_{out} = V_{th}$. When $V_{out} > V_{th}$, (8) becomes:

$$C_L (dV_{out}(t)/dt) = K_D (-V_{DD} - V_{th} - 0.5(V_{out} - V_{DD}))(V_{out} - V_{DD}) - 0.5K_L (V_{th})^2 \quad (9)$$

where K_D=(W_D/L_D)μC_{ox}, K_L=(W_L/L_L)μC_{ox},. V_{out} during low-to-high transition can thus be derived as:

$$V_{out}(t) = -V_{th} - M \tan(0.5 K_D M (t/C_L + A)) \quad (10)$$

where M=((K_L/K_D)(V_{th})^2-(V_{DD}+V_{th})^2)$^{0.5}$, and A=-2arctan(2V_{th}/M)/(M·K_D).

In the case of high-to-low V_{out} transition, T_D goes from the linear regime into the saturation regime when $V_{out} = V_{DD}$-V_{th} (if V_{max} is larger than V_{DD}-V_{th}), while T_L goes from the saturation regime into the linear regime when $V_{out} = V_{th}$. Therefore, when $V_{th} < V_{out} < V_0$, (8) becomes:

$$C_L (dV_{out}(t)/dt) = -0.5K_L (V_{th})^2 + 0.5K_L (V_{th})^2 \quad (11)$$

V_{out} during high-to-low transition can thus be derived as:

$$V_{out}(t) = V_0 - (K_L - K_D)(V_{th})^2 / (2C_L) \times t \quad (12)$$

where V_0 is the smaller value of V_{max} and V_{DD}-V_{th}.

The propagation delay (t_p) and power consumption are two key figures of merit for logic circuit design. t_p can be described as $t_p = (t_{pLH} + t_{pHL})/2$, where t_{pLH} is defined as the time it takes V_{out} to charge from V_{min} to (V_{min}+V_{max})/2, and t_{pHL} is defined as the time it takes the V_{out} to discharge from V_{max} to (V_{min}+V_{max})/2. Based on (5), (6), (10) and (12), the expressions for t_{pLH} and t_{pHL} can be derived as:

$$t_{pLH} = 2C_L \arctan\left(-\left(V_{th} + 0.5(V_{min} + V_{max})\right)/M\right)/(K_D M) - 2C_L \arctan\left(-(V_{th} + V_{min})/M\right)/(K_D M) \quad (13)$$

$$t_{pHL} = (V_{max} - V_{min}) \times C_L / \left((K_L - K_D)(V_{th})^2\right) \quad (14)$$

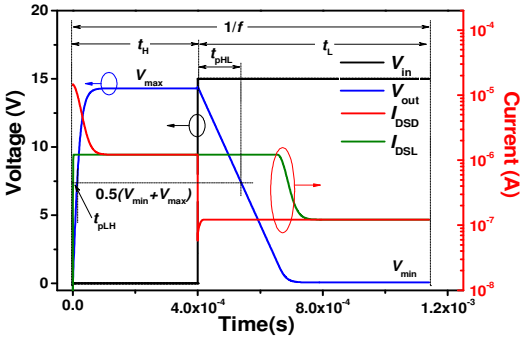


Fig. 2. Illustration of the definitions of t_{pLH}, t_{pHL}, t_H, t_L, and the waveform of the source-to-drain current of T_D (I_{DSD}) during a whole switching period. The waveforms were obtained with W_D=50 μm, W_L=500 μm, C_{fo}=15 pF.

The average power consumption (P_{avg}) during a switching event in a logic circuit is composed of the static part (P_{stat}) and the dynamic part (P_{dyn}). In the p-type unipolar circuit, P_{stat} is mainly contributed by the DC current from V_{DD} to GND when

V_{out} is held high, since when V_{out} is low, T_D is slightly switched off with much lower leakage current as illustrated in Fig. 2. The current can be expressed as $0.5K_L(V_{th})^2$, since T_L is operated in the saturation regime with V_{GS} of 0. Therefore, P_{stat} can thus be derived as:

$$P_{stat} = 0.5K_L\left(V_{th}\right)^2 V_{DD} t_H f \quad (15)$$

P_{dyn} is the power used to charge C_L, and can be described as

$$P_{dyn} = C_L\left(V_{max} - V_{min}\right)V_{DD} f \quad (16)$$

where f is the signal frequency of V_{in}, t_H is the duration of V_{in} being held at the low level, and t_L is the duration of V_{in} being held at high level. t_H and t_L are chosen to allow V_{out} to rise to the V_{max} and fall to V_{min} during the transient operation.

III. Model Verification Method

TABLE I List of the parameters and the values used for the study

Symbol	Quantity	Values
f	signal frequency of V_{in}	50 Hz
t_H	the duration of V_{in} being held at the low level	10 ms
t_L	the duration of V_{in} being held at the high level	10 ms
V_{DD}	power supply voltage	15 V
V_{th}	threshold voltage	1.5 V
μ	mobility of T_D and T_L	1 cm^2/Vs
N	relative sizing of T_D to T_L	5 to 75
L_D,L_L	channel lengths of T_D and T_L	5 μm
W_D	channel widths of T_D	10 μm to 80 μm
W_L	channel widths of T_L	$N \times W_D$
C_{GI}	gate dielectric capacitance per unit area	130 μF/m^2
C_w	wiring capacitance	5 pF
C_{fo}	fan-out capacitance	0 pF to 15 pF
γ	Miller coefficient	2
C_C	input-output coupling capacitance	W_D×3 nF/m
C_{GDL}	gate-to-drain capacitance of T_L	W_L×3 nF/m

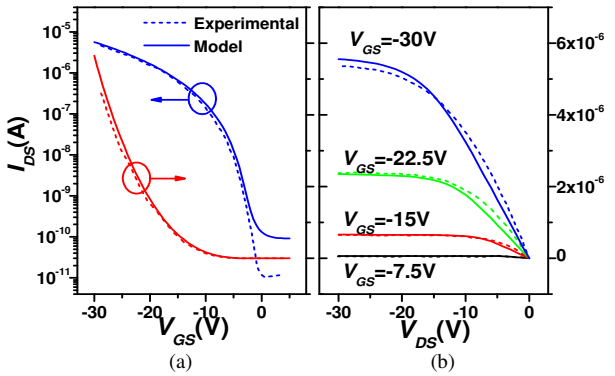


Fig. 3. (a) Transfer and (b) output characteristics of an actual organic TFT [23] fitted with the Level-61 RPI TFT model.

To verify the derived models, circuit simulations were performed using the HSPICE circuit simulator [22]. Since the models were derived based on the conventional analytical FET current-voltage model with a constant mobility, Level-40 HP TFT model was first used to comprehensively verify the derived propagation delay, power dissipation and power-delay-product models. The values of the parameters used for the study are listed in Table I. Then the models were applied to an organic TFT technology, with values of the simulation parameters obtained by fitting the experiment data [23] to Level-61 RPI TFT model to test their applicability for devices of gate voltage dependent mobility [22]. As shown in Fig. 3, the extracted key model parameters in the Level-61 RPI TFT model for fitting include minimum density of deep states (GMIN=1.5E+23), knee shape parameter (M=5), and power law mobility parameter (GAMMA=0.8).

IV. Results and Discussions

In Fig. 4, the transient output voltage waveforms of the inverter at different values of C_{fo} were calculated through equation (10) and (12), and compared to the circuit simulation results. The high-to-low transition is much more significantly influenced by C_{fo} than the low-to-high transition, because the charging current through T_D is much greater than the discharging current through T_L. As expected, the calculated results fit well with the simulation results using Level-40 HP TFT model (Fig. 4(a)). More interestingly, although (10) and (12) were derived based on a constant mobility, the calculated results can also have good fitting with the simulation results for the OTFT technology with a gate voltage dependent mobility as shown in Fig. 4(b). The results indicate that the derived simple models could be applicable to a wide range of TFT technologies with a constant or gate voltage dependent mobility.

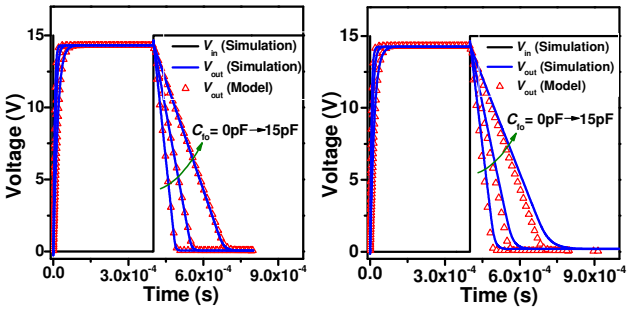


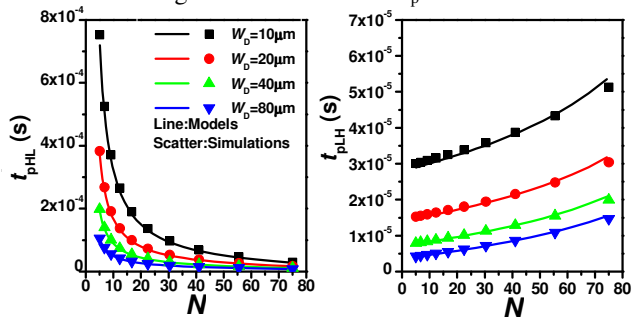
Fig. 4. Verification of the transient response model for the zero-V_{GS} load inverter by HSPICE circuit simulations (W_D=50 μm, W_L=500 μm) with (a) Level-40 HP TFT model and (b) Level-61 RPI TFT model.

In the following, with C_{fo} being fixed as 5 pF, the calculated propagation delay, power consumption and power-delay product as functions of the design parameters (N and W_D) were discussed in details, and compared to the circuit simulation results based on the constant mobility model first. Then the applicability to the OTFT technology with gate voltage dependent mobility is discussed. Finally, the influences of V_{th} on the propagation delay and power dissipation were analyzed by the models, since V_{th} is a key parameter to be considered in the circuit design.

A. Propagation Delay (t_p)

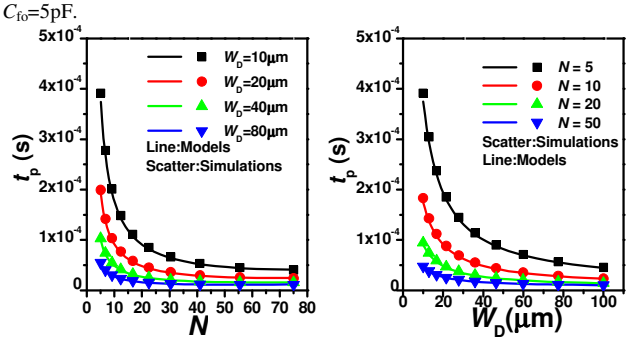
t_{pLH} and t_{pHL} are the two key parameters to decide t_p. The values of t_{pLH} and t_{pHL} for the zero-V_{GS} load inverters at different sizing of TFTs (W_D and N) and a fixed C_{fo} of 5 pF were calculated through (13) and (14), which fit well with the circuit simulation results, as shown in Fig. 5 (a) and (b). It can be seen that, as N increases, t_{pLH} rises while t_{pHL} decreases. Because t_{pHL} is much more sensitive to N than t_{pLH}, it is expected to be able to

reduce t_p by enlarging N. Fig. 6 (a) shows t_p as a function of N at different W_D. At a given W_D, the increase of N will lead to a logarithmic decrease of t_p. Similarly, Fig. 6 (b) shows t_p as a function of W_D at different N. At a given N, the increase of W_D also leads to a logarithmic decrease of t_p.



(a) (b)

Fig. 5. (a) t_{pLH} and(b) t_{pHL} obtained by calculations with the derived models and circuit simulations with Level-40 HP TFT model under different W_D, N with C_{fo}=5pF.

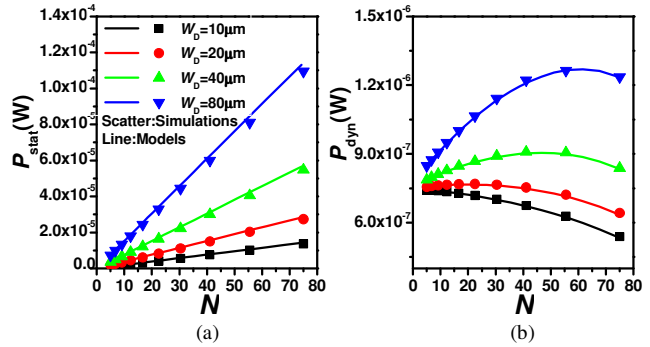


(a) (b)

Fig. 6. The t_p obtained by calculations with the derived models and circuit simulations with Level-40 HP TFT model, (a) as a function of N at different W_D and (b) as a function of W_D at different N.

B. Power Consumption

The average power consumption during a switching event (P_{avg}) composed of P_{stat} and P_{dyn} is another important figure of merit to be considered in logic circuit design. As shown in (15) and Fig. 7 (a), P_{stat} is dependent on W_D and N. While increasing W_D or N can reduce t_p as shown in Fig.6, it will also induce a dramatic increase of P_{stat}.

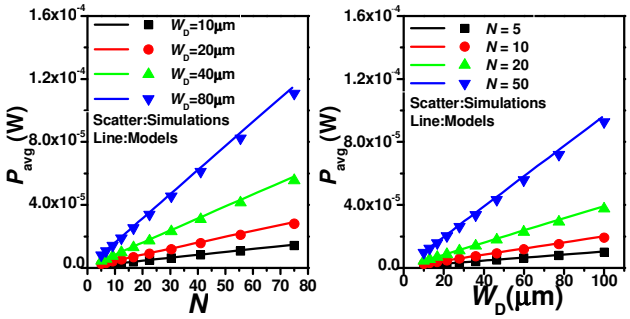


(a) (b)

Fig. 7. (a) P_{stat} and (b) P_{dyn} obtained by calculations with the derived models and circuit simulations with Level-40 HP TFT model, as a function of N at different W_D.

As other part of P_{avg}, P_{dyn} is influenced by both the load capacitance C_L, and the voltage swing V_{max}-V_{min} as described in equation (16). Generally, increasing of W_D and N will increase C_L, and thus P_{dyn}. However, as N increases from 5 to 75, since V_{max}-V_{min} decreases and the influence of V_{max}-V_{min} gradually becomes greater than that of C_L, P_{dyn} initially increases and then decreases as shown in Fig. 7(b).

Moreover, by comparing Fig. 7(a) and Fig. 7(b), it can be seen that P_{stat} is much larger than P_{dyn}, and is the dominant part of P_{avg}. Therefore, P_{avg} presents the similar dependence on N and W_D with that of P_{stat}, as shown in Fig. 8.



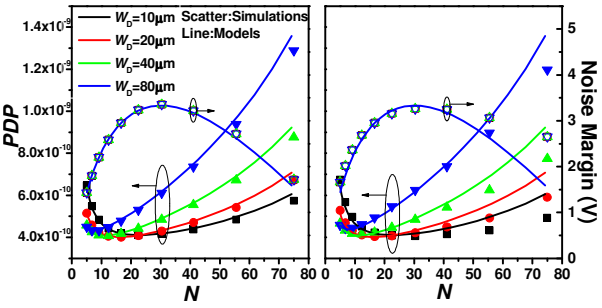
(a) (b)

Fig. 8. P_{avg} obtained by calculations with the derived models and circuit simulations with Level-40 HP TFT model, (a) as a function of N at different W_D and (b) as a function of W_D at different N.

C. Power-Delay Product (PDP)

In most cases of logic circuit design, several design constraints should be considered together, including delay, power consumption, noise margin, and layout area. From Fig. 6 and Fig. 8, it can be seen that the increase of N and W_D (layout area) can not only reduce the delay, but also increase the power consumption. To evaluate the power-delay tradeoffs in logic circuit design, the power-delay product (*PDP*) is introduced, standing for the average energy consumed per switching event, and is expressed as

$$PDP = P_{avg} \times t_p \tag{17}$$



(a) (b)

Fig. 9. The dependence of *PDP* and noise margin on N. The *PDP* and noise margin were obtained by calculations with the derived models and circuit simulations with (a) Level-40 HP TFT model and (b) the Level-61 RPI TFT model.

Fig. 9(a) shows the calculated and simulated *PDP* as a function of N at different W_D. The optimal N for a minimal *PDP* decreases with the increase of W_D. The dependence of noise margin on N obtained by the model developed in [10] is also added in Fig. 9(a) to show the design tradeoffs. The detailed derivation steps for the noise margin model are shown in the appendix.

To achieve the maximum noise margin, a relatively large N of around 30 is required for a V_{th} that approximately equals to

$0.1V_{DD}$. For smaller W_D, the N value for the minimum *PDP* is closer to that for the maximum noise margin.

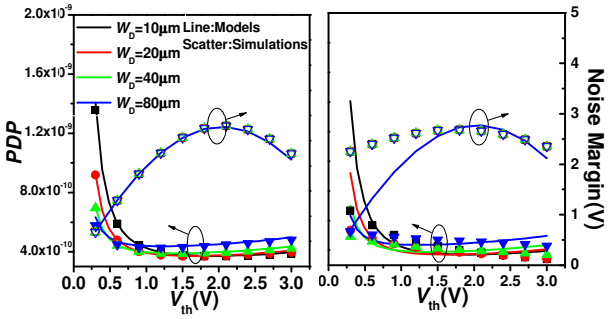
Therefore, based on the developed models, tradeoffs among design constraints of delay, power consumption, noise margin, and layout area can be easily obtained for optimal design of the logic circuits.

D. Application to an Actual Organic TFT Technology

The derived power and delay models in this work are based on a constant mobility for simplicity, while in some TFT technologies, such as organic TFTs, the mobility is generally dependent on the gate voltage [24]. To prove the universality of the models, the calculated *PDP* and noise margin were compared to the circuit simulation results for the actual organic TFT technology as given in Fig. 9(b) with gate voltage dependent mobility. As shown in Fig. 9(b), the calculated results can fit well with the circuit simulation results when N is less than 30. In actual circuit design, N needs to be small to reduce sizing disparity between the drive and the load TFT, and both the minimum of the *PDP* and the maximum of noise margin also occur in the region of $N < 30$. Therefore, the derived models are also very meaningful to the actual circuit analysis and design for TFTs with gate voltage dependent mobility.

E. Influence of Threshold Voltage

In the above discusses, V_{th} is fixed to be 0.1 V_{DD}. Considering V_{th} is an important parameter for circuit performance, the influence of V_{th} on the *PDP* and noise margin is investigated in this section. The N is selected to be 12 for the minimum of *PDP*, as shown in Fig. 9.



(a) (b)

Fig. 10. The calculated *PDP* and noise margin as functions of V_{th} are compared with the circuit simulation results based on: (a) the Level-40 HP TFT model and (b) the Level-61 RPI TFT model.

The obtained results shown in Fig. 10 reveal that *PDP* and noise margin greatly depend on V_{th}. The derived models can well predict *PDP* results obtained from simulations with both Level 40 HP TFT model and Level 61 RPI TFT model, as shown in Fig. 10(a) and (b). The *PDP* decreases dramatically as V_{th} increases from 0.3V to 1.0 V, while remaining relatively insensitive to V_{th} when $V_{th} > 1$ V. The noise margins obtained by simulations using Level 40 HP and Level 61 RPI TFT models both well agree with the derived models when V_{th} > 1.5V. Although when V_{th} < 1.5V, significant differences appear between the results obtained by the derived models and circuit simulation with Level 61 RPI TFT model, V_{th} for the maximum noise margin can still be well predicted by the derived models, as shown in Fig. 10(b). Therefore, based on the results in Fig. 10, the developed models are useful for predicting the V_{th} for achieving optimized PDP and noise margin, and providing guidelines to device-level design.

V. CONCLUSIONS

In this work, analytical models for delay and power analysis in zero-V_{GS}-load inverters were developed. The models clarify the relationships between the device and design parameters and the two key design constraints for logic circuits, and were well verified by circuit simulations. It was shown that, based on the developed models and the noise margin model developed in previous work, tradeoffs among various design constraints of delay, power consumption, noise margin, and layout area can be easily obtained for optimal design of the circuits. The models can facilitate both the first-order analysis for circuit designer, and also device performance optimization for device researchers.

APPENDIX

A. Derivation of Equation (3) and (4)

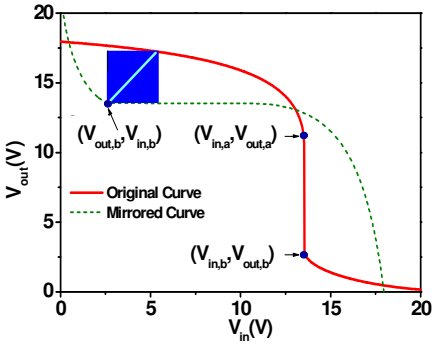


Fig. 11. Illustration of the derivation of the noise margin (NM) model based on the maximum equal criterion (MEC) for the zero-V_{GS}-load inverter.

Fig. 11 shows a typical voltage transfer curve (VTC) for zero-V_{GS} load inverters as illustrated in Fig.1 (b). Equation (1) and (2) with λ =0 are used to derive the VTC, assuming a large enough output impedance. For the convenience of analysis, two critical input voltage (V_{in}) values $V_{in,a}$ and $V_{in,b}$ are defined, to divide the VTC into three regions:

1) When $V_{in,a} \le V_{in} \le V_{in,b}$, both TFTs are operated in the saturation regime. With λ =0, $V_{in,a}$ and $V_{in,b}$ can be thought be equal to each other. Because of the same current through both TFTs, the following equation can be obtained:

$$-\frac{W_D}{2L_D}\mu_D C_{ox}\left((V_{in}-V_{DD})-V_{th}\right)^2 = -\frac{W_L}{2L_L}\mu_L C_{ox}\left(V_{th}\right)^2 \quad (18)$$

Then $V_{in,a}$ and $V_{in,b}$ can be derived as

$$V_{in,a} = V_{in,b} = V_{DD} + V_{th} - \sqrt{N}\times V_{th} \quad (19)$$

Then $V_{out,a}$ and $V_{out,b}$ can be obtained as

$$V_{out,a} = V_{in,a} - V_{th} = V_{DD} - \sqrt{N}\times V_{th} \quad (20)$$

$$V_{out,b} = V_{th} \quad (21)$$

In this region, V_{out} could be any value between $V_{out,a}$ and $V_{out,b}$.

2) When $0 \le V_{in} < V_{in,a}$, T_D is in the linear regime and T_L is in the saturation regime. The following equation can be obtained:

$$\left((V_{in}-V_{DD})-V_{th}-0.5(V_{out}-V_{DD})\right)(V_{out}-V_{DD})=0.5N(V_{th})^2 \quad (22)$$

Then, V_{out} is derived as:

$$V_{out}=V_{in}-V_{th}+\sqrt{(V_{DD}+V_{th}-V_{in})^2-NV_{th}^2} \quad (23)$$

3) When $V_{in,b} < V_{in} \le V_{DD}$, T_D is in the saturation regime and T_L is in the linear regime. The following equation can be obtained:

$$0.5\left((V_{in}-V_{DD})-V_{th}\right)^2=N\left(-V_{th}-0.5(-V_{out})\right)(-V_{out}) \quad (24)$$

Then, V_{out} is derived as:

$$V_{out}=V_{th}-\sqrt{V_{th}^2-(V_{DD}+V_{th}-V_{in})^2/N} \quad (25)$$

B. Derivation of the Noise Margin Model

Noise margin (NM) is obtained from the maximum square between original and mirrored VTCs. On the mirrored VTC of the inverter, the point ($V_{out,b}$, $V_{in,b}$) is selected as the left-bottom vertex of the maximum square, as shown in Fig. 11. From this vertex, a straight line is drawn parallel to the line of y=x, and the intersection point between this line and the original inverter curve forms the right-top vertex of the square. Then, the NM can be evaluated from the side length of the square. The detailed steps of the derivation are described as follows.

1) Define $f(x)$ as the original VTC of the inverter, and $g(x)=f^{-1}(x)$ as the mirrored VTC.
2) The left-bottom vertex of the maximum square is on $g(x)$ and defined as (Gx, Gy). Similarly, the right-top vertex of the maximum square is on $f(x)$ and defined as (Fx, Fy).
3) Since (Gx, Gy) and (Fx, Fy) are located on the straight line parallel to the line of y=x, there is $Gy-Gx=Fy-Fx$.
4) (Fx, Fy) is located in the region of $0 \le V_{in} \le V_{in,a}$, and from $Gy-Gx=Fy-Fx$, the following equation can be obtained:

$$\begin{aligned} &V_{DD}+V_{th}-\sqrt{N}\times V_{th}-V_{th} \\ &=Fx-V_{th}+\sqrt{(V_{DD}+V_{th}-Fx)^2-N\times V_{th}^2}-Fx \end{aligned} \quad (26)$$

5) Fx can thus be derived as

$$Fx=V_{DD}+V_{th}-\sqrt{\left(V_{DD}-\left(\sqrt{N}-1\right)\times V_{th}\right)^2+N\times V_{th}^2} \quad (27)$$

6) Then, NM can be obtained from $Fx-Gx$ to be:

$$NM=V_{DD}-\sqrt{\left(V_{DD}-\left(\sqrt{N}-1\right)\times V_{th}\right)^2+N\times V_{th}^2} \quad (28)$$

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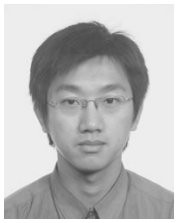

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