Featuring work from the Advanced *in vitro* Human Models Research Lab of Professor Ben Maoz laboratory, Department of Biomedical Engineering and Sagol School of Neuroscience, Tel Aviv University, Tel Aviv, Israel.

Spatial trans-epithelial electrical resistance (S-TEER) integrated in organs-on-chips

S-TEER enables to assess *in situ* the barrier properties throughout an Organ-on-a-Chip channel. The spatial information the S-TEER provides, allow to identify growth dynamic and drug assessment of a barrier tissue in an Organ-on-a-Chip platform. This work demonstrates a part of our lab work and vision, which is to provide advanced *in vitro* human models using induced pluripotent stem cells and Organs-on-a-Chip to allow better, faster and more reliable tools for studying human physiology.

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Spatial trans-epithelial electrical resistance (S-TEER) integrated in organs-on-chips†

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Transepithelial/transendothelial electrical resistance (TEER) is a label-free assay that is commonly used to assess tissue barrier integrity. TEER measurement systems have been embedded in organ-on-a-chip devices to provide live readouts of barrier functionality. Yet, these systems commonly provide the impedance values which correspond to the highest level of permeability throughout the chip and cannot provide localized information on specific regions of interest. This work introduces a system that provides this essential information: a spatial-TEER (S-TEER) organ-on-a-chip platform, which incorporates moving (scanning) electrodes that can measure electrical resistance at any desired location along the chip. We demonstrate the system's capacity to obtain localized measurements of permeability in selected regions of a cell sample. We show how, in a layer with non-uniform levels of cell coverage, permeability is higher in areas with lower cell density—suggesting that the system can be used to monitor local cellular growth *in vitro*. To demonstrate the applicability of the chip in studies of barrier function, we characterize tissue response to TNF-α and to EGTA, agents known to harm tissue barrier integrity.

Introduction

Organs-on-chips are microfluidic devices that serve as *in vitro* models to mimic tissue and organ-like physiology.[1] A key benefit that organs-on-chips provide over traditional *in vitro* cell models is the capacity to incorporate perfusion through microchannels, which is an essential function in physiological modelling and in drug screening applications.[2]

The increasing prevalence of organs-on-chips in *in vitro* modeling has created a need for technology that provides real-time readouts of cell function within these systems. One fundamental type of measurement is the permeability of cell-layers within a chip; such measurements can indicate the functionality of barrier tissues such as those found in the lungs,[3] gut,[4] blood brain barrier (BBB),[5–7] and vasculature (endothelium). Fluorescent markers are one common method of measuring permeability.[8] Another common method is impedance measurement,[9] *i.e.*, measurement of electrical resistance across a cellular monolayer. The latter method, known as transepithelial or transendothelial electrical resistance (TEER), provides label-free, rapid, and real-time measurements that correlate to the formation of tight junctions between the cells in the monolayer, thereby providing a good indication of barrier integrity.

In recent years, several methods have been developed to integrate TEER into organ-on-chip systems. These methods include: direct insertion of metal electrodes into designated placeholders[10–15]—either in individual chips or in high-throughput systems containing multiple chips,[15] patterned electrodes on glass or polymeric substrate,[16–19] or integrated electrodes with other sensors such as multi electrode arrays (MEA).[20] While these methods of TEER integration provide *in situ* information on barrier function, most of them do not capture spatial information, meaning that they cannot indicate electrical resistance values in specific parts of the chip. Rather, they provide the electrical resistance value corresponding to the highest level of permeability, *i.e.*, the "weakest link in the chain".[21] This feature may result in substantial loss of information: for example, a tissue might be confluent with good tight junctions, yet contain small imperfections that ultimately provide very low TEER values, which do not represent the overall sample.[22] Some state-of-the-art chips overcome this limitation to some degree by integrating multiple electrodes, which can be used to capture electrical resistance in specific spatial locations inside a channel of a microfluidic chip.[20,23] Yet, these locations must be chosen in advance, meaning that the technology cannot be used to identify multiple locations of

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interest in real time and to compare their TEER measurements. The capacity to dynamically combine TEER measurements with spatial information could enable researchers to obtain valuable information that is currently beyond the scope of TEER measurement methods. Such information might include, for example, the influence of flow shear stress gradient,[24] drug diffusion loss,[25] effects of local oxygen concentrations,[26] and more.

Currently, microscopy is the primary means of retrieving spatial information in organs-on-chips,[27,28] yet it is challenging to correlate microscopy data with permeability measurements. Thus far, most attempts to measure spatial permeability *in vitro*—*e.g.*, through conductance scanning methods—have focused on non-organ-on-chip systems.[29,30] One study proposed the use of multiple patterned electrodes to obtain spatial information on impedance in a microfluidic BBB model; however, the electrodes are complex to fabricate, partially interfere with cell culture visualization (unless additional steps are taken that may further complicate fabrication), and have not yet been demonstrated *in vitro*.[31]

In this work, we introduce an organ-on-a-chip platform integrated with moving (scanning) electrodes, designed and fabricated so as to provide a dynamic range of measurement points throughout the organ-on-a-chip channel. We demonstrate this new concept of spatial-TEER (S-TEER) by characterizing the growth dynamic of human epithelial colorectal adenocarcinoma (Caco-2) cells in a chip and measuring cell response to two different agents known to decrease barrier integrity: TNF-α, a pro-inflammatory cytokine;[20] and EGTA, a chelating agent that impairs barrier function of cells.[17]

Materials and methods

Chip fabrication

The developed S-TEER-Chip is a multilayer microfluidic device consisting of the following components (Fig. 1 and

SI1, Movie SI1†): (i) three polydimethylsiloxane (PDMS) substrates: a top layer and two fluidic layers, or "channels" (referred to, respectively, as the "upper channel" and "lower channel"); (ii) one bottom glass layer containing two static patterned gold electrodes, integrated with the lower channel; (iii) two stainless steel electrodes, integrated with the upper channel, and with the capacity to move along ("scan") a designated slot spanning the length of the channel; and (iv) a porous polycarbonate (PC) membrane between the PDMS channels (Fig. 1). Chip fabrication included several steps: electrode fabrication; PDMS layer fabrication; and assembly.

Electrode fabrication. To pattern the bottom (gold) electrodes, glass cover slips were rinsed with isopropanol (Avantor), dried in a stream of compressed air, and activated in oxygen plasma (Atto-BR-200-PCCE, Diener Electronic, Germany). The electrode pattern mask for the bottom electrodes was printed using a Raise 3D Pro2 Dual Extruder 3D Printer (Raise Technologies Inc., US) and consisted of two 2 mm electrodes throughout the channel, separated by 0.5 mm distance. The glass substrates were coated with 3 nm chrome and 20 nm gold in a penta magnetron sputter. For the top electrodes, stainless steel wires (316 LVM Hard wire 0.5 mm, S.A. SAGUY) were bent and trimmed to the size of 1 mm × 5 mm × 20 mm, insulated and glued together with a distance of 1 mm between them.

PDMS layer fabrication. The PDMS parts were cast into molds that were designed with Solidworks CAD software and printed with polylactic acid (PLA) using the Raise 3D Pro2, containing a 1 mm × 18 mm channel. The printed molds were glued onto plastic plates and filled with PDMS prepared by mixing in 1:10 ratio Sylgard 184® (Dow Corning, Midland, MI, USA) with the curing agent, followed by vacuum for 1 hour and curing at 60 °C for 4 hours.

Assembly. The chip was then assembled in a layer-by-layer approach. PDMS layers and glass substrate were activated in oxygen plasma (Atto-BR-200-PCCE, Diener Electronic, Germany) for 30 seconds, constructing the bottom and top microfluidic channels. The PC membrane (0.4 μm pore size, it4ip S.A., Belgium) was rinsed with isopropanol (Avantor), dried under a stream of compressed air, and activated in oxygen plasma for 1 minute (Atto-BR-200-PCCE, Diener Electronic, Germany). The membrane was then immersed for 30 minutes in 5% aqueous solution of (3-aminopropyl) triethoxysilane (APTES, Sigma-Aldrich), rinsed in water and dried with compressed air. The unassembled top and bottom PDMS channels underwent a second activation with oxygen plasma. The full chip was then aligned and kept at 60 °C overnight.

In order to avoid the formation of bubbles, all the channels were filled with medium. Using this method enabled us to have flow in the chip without bubble formation for long time periods (Movie SI2†).

Chip configurations for validation experiments. In order to validate the platform, different chip configurations were used: open-chip (Fig. 2a) – where the top and bottom parts were assembled without any membrane, half-open-chip (Fig. 2b) – where a layer of 0.5 mm of PDMS was placed
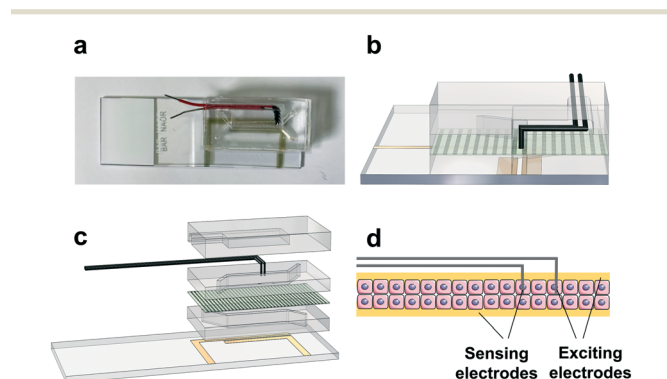

Fig. 1 S-TEER chip design. a. Photograph of the assembled chip, scale bar – 5 mm. b. CAD model – middle cut of S-TEER chip c. exploded CAD model of the S-TEER chip. Gold-plated electrodes on the glass coverslip and stainless-steel electrodes with 2 mm tip inside the channel. PDMS layers made from 3D-printed molds. d. Illustration of the impedance measurement inside the system – 2 excitation electrodes and 2 sensing electrodes. The chip dimensions provided in the "Materials and method" section and in Fig. SI1.†
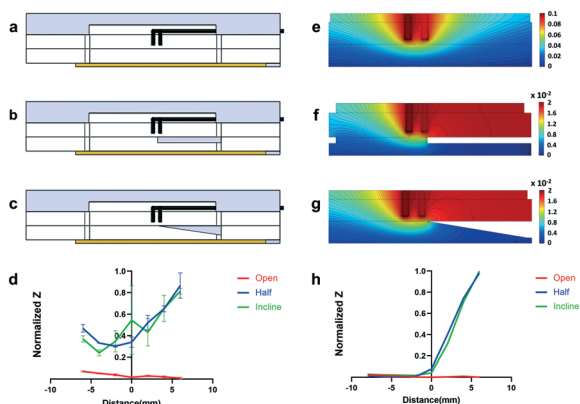
Sensing electrodes   Exciting electrodes

Fig. 2 Chip characterization. a–c. Illustration of three chip configurations: (a) open-Chip, (b) half-open chip, and (c) incline-chip. d. Impedance measurements through the channel, showing the spatial measurement distribution in the three chips. e–g. Electrical potential distribution in the three chips, (e) open-chip, (f) half-open chip, and (g) incline-chip. h. Impedance simulations throughout the channel, showing spatial measurement distributions in the three chips.

between the two channels, in such way that half of the channel remains open; and an incline-chip (Fig. 2c), in which the lower channel includes a layer of PDMS that increases in thickness from one end of the chip to the other, from 0 up to 1.5 mm.

Chip cell culture

Caco-2 cells (ATCC® HBT-37™, American Type Culture Collection, Rockville, MD, USA) were maintained in Dulbecco's modified Eagle medium (DMEM, Biological Industries), supplemented with 10% heat-inactivated fetal bovine serum (FBS, Biological Industries), 1% glutamax (Gibco), and 1% penicillin–streptomycin–amphotericin B (PSA, Biological Industries) solution, at 37 °C with 5% CO_2 in a humidifying incubator. Cells of early passages[20–30] were grown to 80–90% confluency before being seeded into the microfluidic device. The chip was pretreated on plasma for 1 minute, followed by flushing with ethanol and phosphate-buffered saline (PBS), then coated with Matrigel Basement Membrane Matrix (Corning) used at a 1 : 50 ratio with the culture medium, for 30 min in the incubator. The membrane was then rinsed with culture medium, and the Caco-2 cells, harvested with trypsin/EDTA solution (Biological Industries), were seeded in the upper channel on top of the PC membrane, at a density of 1×10^6 cells per cm^2, and cultured statically, changing the medium twice a day.

Non-confluent layers: the non-confluent layer was created in several methods, which include: 1. uneven seeding density (seeding more cells on one side of the chip then the other), 2. inducing shear in the channel right after seeding.

Immunocytochemistry

Chips were rinsed in PBS and fixed in 4% paraformaldehyde (PFA, Sigma-Aldrich) for 20 minutes at room temperature

(RT). Immunocytochemistry was carried out after permeabilization with 0.1% Triton X-100 (Sigma-Aldrich) in PBS for 10 min at RT and blocking for 30 min in FBS (5%) in PBS. Primary antibodies were applied overnight in PBS at 4 °C. The primary antibody that was used was rabbit anti ZO-1(Abcam) diluted 1 : 200 in PBS to stain the zona occludens-1. Cells were then washed three times in PBS and stained with the secondary antibody for 1 hour at RT. The secondary antibody was anti-rabbit Alexa Fluor-488 (Invitrogen) diluted 1 : 300 in PBS. After four washes with PBS, DAPI-fluoromount-G® (SouthernBiotech) was mounted to stain the nuclei as well. Imaging was carried out using an inverted confocal microscope (Olympus FV3000-IX83). To retrieve complete images of each channel, we used sequential tile scanning over the entire channel. Reconstruction and processing were done using open-source ImageJ software.[32]

Impedance spectroscopy measurements

Electrode sterilization: the electrodes were placed in UV-O for 5 minutes. In addition, the electrodes were washed with 70% ethanol.

A BioLogic potentiostat (VSP) was used to record impedance spectra. Measurements were executed by applying a 10 μA sinusoidal excitation signal in a 4 point measuring system with a frequency range of 1 Hz–1 MHz.

In experiments involving chips containing cells, S-TEER-chips were transferred one at a time from the incubator, and the measurements were taken shortly after at 4 different points within each chip. Measurement of a full impedance spectrum requires about 1 minute, and measurement at each point was repeated 4 times.

To ensure consistency in the measurement positions within and across chips, we used a caliper that was connected to the electrode. This provided accuracy of ±10 μm (Movie SI35†).

Simulations

In order to better understand the viability of the proposed system, as well as to support or challenge any experimental results, simulations of the electrical behavior of the S-TEER device were conducted using COMSOL Multiphysics® software (COMSOL Multiphysics® www.comsol.com COMSOL AB, Stockholm, Sweden). The finite-element-method-based simulations included calculation of the electrostatic field distribution for all versions of the device, in multiple configurations (the different configurations are elaborated above and in the Results section; see cross sections in Fig. 2), and for all locations of the scanning electrodes along the upper channel. The physics model used in COMSOL was "Electric Currents". Electrical impedance was calculated through extraction of the appropriate currents and voltage drops from frequency-domain simulations of the electrical currents problem (in the frequency range 1 Hz–1 MHz), performed using a flexible generalized-minimum-residual iterative solver.

Quantifying cell coverage in a channel

To quantify cell coverage in a chip, we obtained a confocal image of the chip and opened it in ImageJ. The image was converted to greyscale, and thresholding was used to identify the cells inside the chip. We split the image into equal-sized regions of interest (ROIs), with each ROI covering the entire width of the chip. We then measured the "area fraction" of an ROI: assuming that a confluent area of cells inside the channel is 100% coverage, the other areas' values were normalized accordingly.

Barrier disruption experiments

TNF-α. Stock TNF-α (H8916-10UG, sigma) was diluted in medium to 2 ng ml^{-1} and added to the chip together with 5% methanol on day 5 (Fig. SI6†), measurements were taken before the addition of the TNF-α, right after the addition, and about couple of hours after the addition.

EGTA. EGTA (E4378-10G, sigma) was prepared at 0.1 M with ddH$_2$O; pH was titrated to 9 with NaOH 1 M. EGTA was diluted to 5 mM with culture medium. To confirm that the EGTA solution indeed disrupts barrier integrity, we applied it to Caco-2 cells seeded on ThinCert inserts (Greiner) on a 24 well plate, PET membrane, 0.4 μm pore size (662 641) (Fig. SI8†). TEER was measured using a Millicell ERS-2 Voltohmmeter (Merck Millipore).

The TEER measurements were correlated with microscope images.

Statistical analysis

Results are presented as mean ± SD. Differences between measurement sites in the chip were evaluated using multiple-comparison ANOVA (GraphPad Prism 9.1.0), with $P < 0.05$ indicating a statistically significant difference between points.

Results and discussion

S-TEER-chip design

The S-TEER-chip contains four integrated electrodes: two moving (scanning) electrodes in the upper channel, with a fixed distance between them; and two static electrodes in the lower channel, where the channels are separated by a PC membrane (Fig. 1 and SI1 and Movie SI1†). Each pair of electrodes in each channel contains one excitation electrode (injecting the current) and one sensing electrode (measuring the voltage drop). The scanning electrodes are positioned within a slot spanning the length of the upper channel, and can be moved manually to any desired point along that slot, in order to measure the local impedance at that site (the electrodes are held in place while measurements are taken). This design provides a dynamic range of impedance measurements throughout the organ-on-a-chip system. In designing the device, we encountered and overcame several challenges. The main obstacle was the dependence of impedance measurements on the distance between the

moving and static electrodes. In our initial designs, the static electrodes were in the center of the chip, and we observed that the greater the distance between the moving (scanning) electrodes (top) and the fixed electrodes (bottom), the higher the impedance (Fig. SI2†), as the impedance is directly proportional to the distance. To overcome this challenge, we designed the bottom electrodes so as to cover the entire channel (Fig. 1), thereby ensuring identical distance between the top and bottom electrodes at every point in the chip and enabling direct comparisons to be made among all measurement points (Fig. SI3†).

Yet, this design created a new challenge, since covering the entire channel with metal electrodes interferes with the capacity to image the cells in the chip, which is fundamental for any organ-on-a-chip application. We overcame this challenge by making the electrodes transparent, by depositing a thin 20 nm layer of gold, as described in Henry *et al.*[17]

The choice to use four electrodes (two moving in the upper channel and two static in the lower channel) rather than, *e.g.*, one moving electrode and one static electrode, was driven by considerations regarding the electrode polarization impedance. Specifically, previous work[17,23,33] has demonstrated the importance of using a 4-point measuring system instead of 2 points, as a 4-point system enables the excitation electrode to be separated from the measuring electrode. Importantly, the two top electrodes are able to move together, remaining at a constant distance. This is extremely important, as both our experiments and our simulations (Fig. SI4 and SI5†) showed that if one of the upper electrodes is fixed, the impedance is affected.

Summing up the above, our final design eliminates impedance dependence on the distance between the electrodes, allows for cell imaging, and mitigates concerns regarding electrode polarization impedance.

We note that, for the purposes of our proof of concept, we used stainless steel to construct the scanning electrodes and gold for the static electrodes. In real-world applications, alternative metals can be used that are optimal for the experimental conditions and for preserving cell viability. Moreover, we manufactured our chips using standard tools (not photolithography) to facilitate faster and cheaper fabrication; standard micro and nano fabrication methods can be used to miniaturize the chip. It is also important to note that the choice of materials for the membrane may impose downstream constraints; for example, in our case, the use of a PC membrane required additional staining in order to better characterize the cells as bright-field or phase-contrast imaging was more challenging.

Chip characterization

In order to characterize and validate the S-TEER-chip, we created three different chip configurations, containing different resistance layers of PDMS: (i) an open-chip (Fig. 2a), in which there is no barrier between the upper and lower

channels; (ii) a half-open-chip (Fig. 2b), which is divided in such a way that half of the chip has an added resistance layer of 0.5 mm of PDMS between the channels, while the other half remains open; and (iii) an incline-chip (Fig. 2c), in which the lower channel includes a layer of PDMS that increases in thickness from one end of the chip to the other, from 0 up to 1.5 mm. We produced and studied three chips in each configuration.

Impedance measurements. Comparison of the three chips shows that, as expected, the open-chip has low impedance values along the entire channel (Fig. 2d), whereas the half-open-chip shows an increase in impedance where the PDMS layer was placed (position $X > 0$ mm, Fig. 2d). The incline-chip shows a rising slope in correlation with the thickness of the resistance layer. Each increase of 0.33 mm in the layer thickness results in an impedance increase of around 120 Ω, showing direct and linear correlation between the two. It is important to note that around point 0 (center of the chip) there is a higher error bar, as one of the top electrodes might be above the PDMS layer, and the other over the open channel, which might increase the noise of the measurement. Taken together, these measurements demonstrate that our S-TEER system can be indeed used to obtain TEER measurements corresponding to different spatial points within a chip.

Simulations. To further characterize the S-TEER-chip, we simulated the electric potential distribution in each chip configuration. As expected, in the open-chip, a symmetric distribution is seen around the electrodes (Fig. 2e and SI5d, Movie SI4†). In contrast, the half-open- and incline-chips show non-uniform potential distributions (Fig. 2f and g), which result in the non-uniform contribution of the resistance layer seen in our experiments (discussed above). Importantly, the specific impedance values calculated from the simulations were in line with our measured data (Fig. 2h). These findings highlight the importance of electric field simulations in the proper design of microfluidic chips.[22,23] Indeed, we performed such simulations on other versions of the chip, which enabled us, for example, to identify the shortcomings of using a fixed electrode in the upper channel, or of using 2-point measurements (Fig. SI5†), and to adjust our design accordingly. The results of our simulations suggest that our final design is suitable for the application we desire.

Spatial TEER measurements in a cell layer

Once the S-TEER-chip was characterized, we sought to demonstrate its potential as an *in vitro* platform by identifying changes in tight junctions of barrier tissues. Therefore, we conducted several experiments in which we seeded human epithelial colorectal adenocarcinoma cells (Caco-2 cells) inside the upper channel on top of the PC membrane. In all experiments, TEER measurements were taken at least three times at 4 consistent points throughout the channel, about 5 minutes after taking the chip out of the

incubator. The triple measurement, as well as the waiting period before measurements were conducted, mitigated the likelihood that the TEER measurements would be influenced by fluctuations in the medium temperature.[9]

TEER measurements in a confluent layer. The cells were able to form a confluent layer within 2–3 days of culture (Fig. 3a and b and SI7†). High-magnification imaging of a chip containing a confluent layer (Fig. 3b and SI7†) shows the confluency of the cell layer and gives a good overview of the whole tissue. The TEER values for the four measurement sites in the (confluent-layer) chip shown in Fig. 3b are plotted in Fig. 3c (additional data of confluent chips can be seen in Fig. 4a and SI6†). The values are similar across the four points, with the exception of a difference between points 2 and 4, which might have resulted from the fact that fewer cells were present at point 2.

TEER measurements in a non-confluent layer. We produced a non-confluent, non-uniform, "damaged" layer of cells, with low cell density, by changing the medium in such way that large shear was created between the two inlets of the upper channel (Fig. 3f and g). The spatial TEER measurements demonstrate that each point on the layer corresponds to a distinct permeability value (Fig. 3e). For example, we observe that point 4 has a substantially higher concentration of cells than the other points, and that cell concentration increases progressively from point 1 to point 4.

As a next step, we quantified the correspondence between TEER values and the percentage of cell coverage at each measurement site (Fig. 3d). It can be seen that when cell coverage is below 50% the impedance values are low (<0.4). This trend was observed in all the chips that were used in this study.

These measurements provide an indication of the valuable information that S-TEER can capture. For example, they show how our system can be used to obtain localized measurements of a tissue barrier within a sample, providing fine-grained structural information. This capacity can contribute to the accuracy of interpretation of TEER data. Indeed, it is common for the distribution of cells in a channel to be uneven (*e.g.*, Fig. 3f and g), and for distributions to vary across experiments, owing to slight variations in parameters and execution techniques. In these cases, areas with lower cell coverage may produce low TEER values that are not necessarily representative of the entire cell layer (as shown, *e.g.*, in Fig. 3d–g). Traditional TEER methods, which are heavily influenced by the "weakest link" in the sample in terms of permeability,[21] may thus not produce an accurate picture of the permeability of the complete sample.

The capacity to provide an accurate assessment of permeability in specific areas of a sample might further allow for the use of chips that might otherwise be discarded as "bad samples". Fig. 3d suggests, for example, that a region of the cellular layer with coverage lower than 50% is characterized by low impedance values that might disqualify a sample. The capacity to focus measurements on areas with
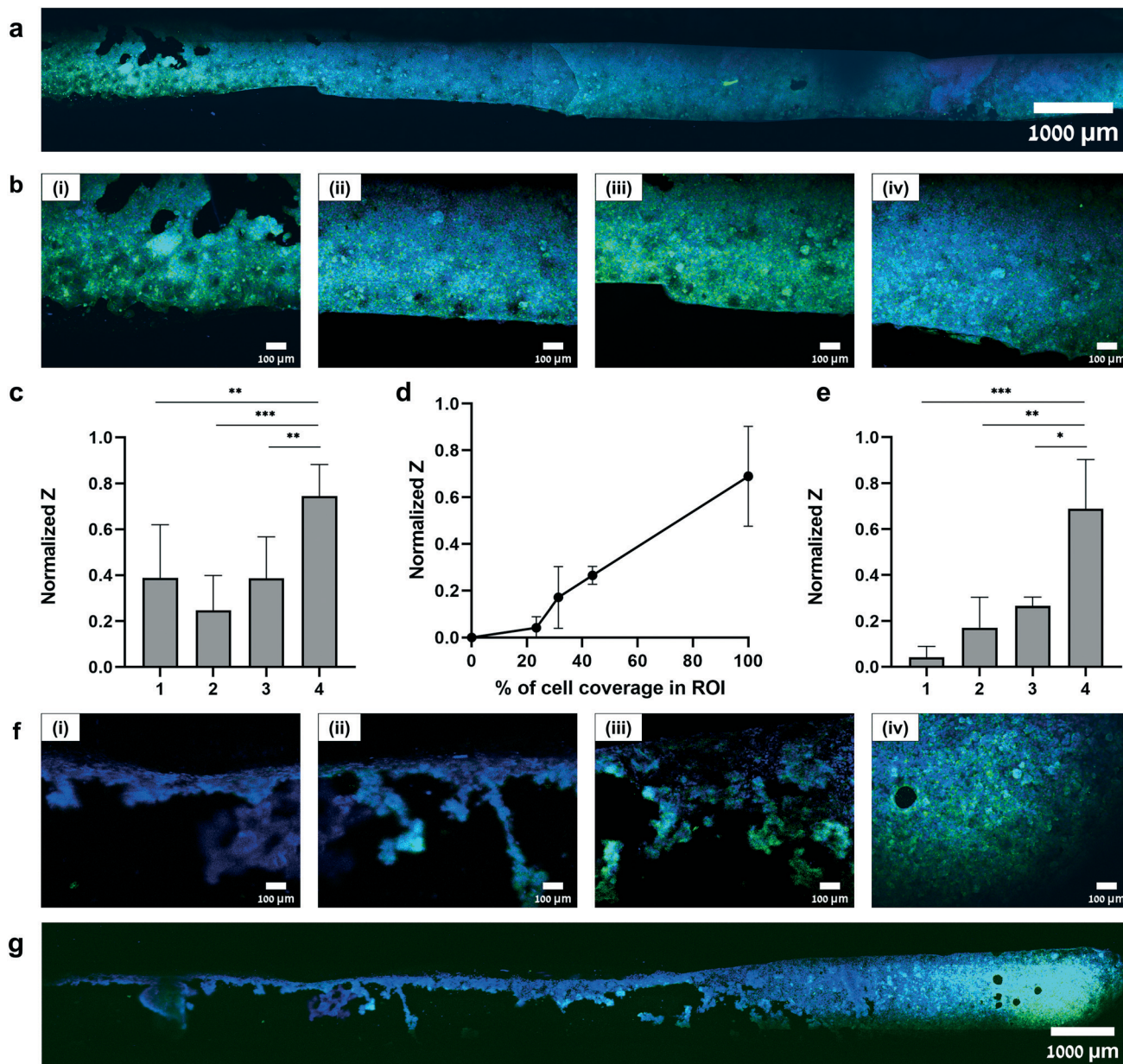
Fig. 3 Spatial TEER measurements. a. Confocal image of Caco-2 cells in a confluent channel (blue-DAPI, Green ZO-1). b. Magnified images of specific points on a confluent chip: (i) 1, (ii) 2, (iii) 3, (iv) 4. c. Normalized impedance values at 4 points on a confluent channel. d. Correlation between the percentage of cell coverage in the channel and the impedance value at the same point. e. Normalized impedance values in 4 points of a non-confluent channel. (f) Magnified images of specific points on a non-confluent chip: (i) 1, (ii) 2, (iii) 3, (iv) 4. (g) Confocal image of Caco-2 cells in a non-confluent channel (*$P < 0.05$, **$P < 0.01$, ***$P < 0.001$).

higher cell coverage might enable samples that contain sparse regions to be used nonetheless.

Our experiments further suggest that S-TEER might be used to track the growth dynamics of a cellular layer and to measure increases in tissue thickness or confluency at any site in the microfluidic device (Fig. SI6a†). Currently, in most experiments, cellular growth in a chip is monitored *via* microscope, which does not provide a means of quantifying how permeability properties change over time. S-TEER, in contrast, can be used to monitor different points in the chip over time, and to measure how the confluency and permeability change *in situ*. Such

information can be combined with microscopy data—with either bright field or immunohistochemistry—to obtain a complete characterization of the growth dynamics.

Using S-TEER to characterize barrier functionality

To demonstrate the capacity of the S-TEER-chip to indicate barrier functionality, we monitored changes in permeability due to exposure to two reagents: the cytokine TNF-α (Fig. SI7b†), and the chelating agent EGTA (Fig. 4b and c and SI8†), which are known to damage barrier integrity.
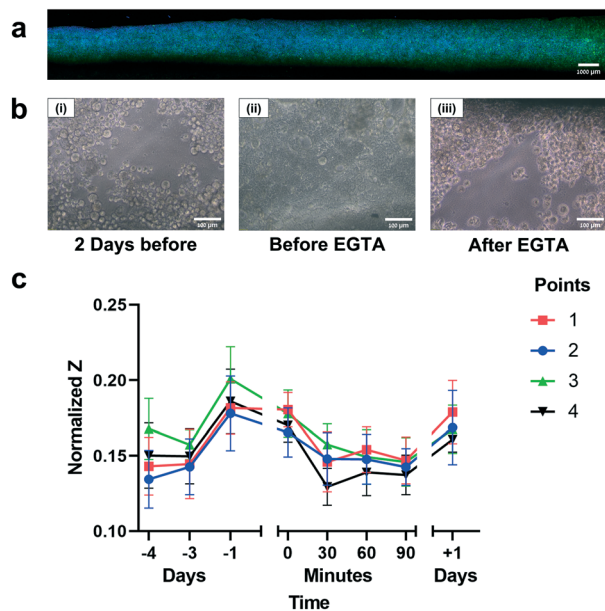
Fig. 4 EGTA effect on Caco-2 in the S-TEER chip. a. Confocal image of a confluent layer of Caco-2 in S-TEER chip. Nuclei stained in blue and ZO-1 in green. b. DIC images of Caco-2 in different stages of the experiment; (i) control chip w/o EGTA; (ii) under EGTA effect; (iii) after 1 day of recovery. c. TEER values over different time points – control over cells treated with 5 mM of EGTA solution.

EGTA. For the EGTA experiments, we seeded Caco-2 cells in the S-TEER-chip, until they got to confluency after 5 days (Fig. 4a). S-TEER measurements were taken each day at 4 different points along each chip, showing the growth dynamics of the cells throughout the membrane (Fig. 4c). When the cell layers reached confluency (as determined by imaging), 5 mM EGTA in DMEM solution was added to the chip to stress the cells and cause damage to the barrier. This concentration of EGTA was previously checked on Caco-2 seeded on Transwells and measured by a commercial TEER apparatus (Fig. SI8†). Impedance was measured at four points along each chip 30, 60 and 90 minutes after EGTA introduction. Next, we introduced fresh new medium and measured the "recovery" at the same four points, one day after treatment.

As expected, after introduction of EGTA, we observed a decrease in the impedance at each measurement point (Fig. 4c). Moreover, we observed that the impedance values varied slightly across the different measurement points, indicating that the effects of the agents on the tissue were not completely uniform, and highlighting the capacity of the S-TEER chip to provide nuanced structural information. The recovery was not complete, and as shown in differential interference contrast (DIC) images on the channel (Fig. 4b), was similar to the confluency 2 days before the measurement.

TNF-α. A similar response was observed for the experiments that were done with the TNF-α (Fig. SI6b†).

The findings of our barrier functionality experiments highlight another advantage provided by the S-TEER system. In many dual-channel organ-on-a-chip platforms, including the system described herein, it is challenging to obtain images at high magnification, owing to the relatively large distance between the cell layer and the bottom of the chip. This characteristic makes it difficult to visualize barrier breakdowns, as disintegration of tight junctions can be hard to see at low magnifications. S-TEER measurements can circumvent this limitation by identifying local effects on barrier tissue.

Conclusions

Herein we have introduced the S-TEER-chip, an organ-on-a-chip platform that provides localized impedance measurements at multiple points along a chip. Our system relies on a 4-point measuring system, using a pair of static transparent electrodes and a pair of scanning electrodes that can be moved manually along the chip to obtain impedance measurements at a site of interest. We validated our system in experiments using Caco-2 cells, showing that the S-TEER-chip platform produces spatially-dependent impedance measurements that are in direct correlation with cell concentration levels in the corresponding areas on the chip. We further demonstrated how the S-TEER system can be used to monitor spatial dynamics of cellular growth, and to identify changes in barrier integrity following exposure to either TNF-α or EGTA.

The S-TEER-chip system provides substantial benefits over current TEER measurement approaches, which rely on lowest values of electrical resistance across the entire channel and cannot provide an indication of local variations along the cellular layer. In enabling researchers to retrieve such spatial information, our platform can provide more accurate measurements and open the door to spatially dependent studies. Furthermore, in contrast to standard TEER approaches, which require full cellular confluence to produce accurate measurements, our approach may enable researchers to use chips that contain areas that are not confluent (and to focus on the confluent areas)—potentially saving time and money.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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