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TEMPERATURE MEASUREMENT OF SUB-MICROMETRIC ICs BY SCANNING THERMAL MICROSCOPY

*S. Gomès¹, O. Chapuis², F. Nepveu¹, N. Trannoy², S. Volz²,
B. Charlot², G. Tessier², S. Dilhaire², B. Cretin² and P. Vairac²*

¹ Centre de Thermique de Lyon, UMR CNRS 5008,
Institut National des Sciences Appliquées de Lyon, Université Claude Bernard Lyon 1
20 Avenue Albert Einstein, 69621 Villeurbanne cedex, France

² Groupement de Recherche Micro et Nanothermique, GDR CNRS 2503
Ecole Centrale Paris, Grande Voie des Vignes, 92295 Châtenay Malabry, France.

ABSTRACT

Surface temperature measurements were performed with a Scanning Thermal Microscope. We aim at proving an eventual sub-micrometric resolution of this metrology when using a wollaston wire probe of micrometric size. A dedicated CMOS device was designed with arrays of lines 0.35 μm in size with 0.8 μm and 10 μm periods. Integrated Circuits with or without a passivation layer were tested. To enhance sensitivity, the IC heat source was excited with an AC current. We show that the passivation layer spreads heat so that the lines are not distinguishable. Removing this layer allows us to distinguish the lines in the case of the 10 μm period.

1. INTRODUCTION

Semiconductor devices, which are continuously reduced for integration, must withstand ever higher electric fields which induce severe degradation or total failure. Spatially high-resolution determination of temperature and detection of local power dissipation in the sub- μm range have then become fundamental for microelectronics. The Scanning Thermal Microscope (SThM) [1] is a relatively new technique permitting such investigations. Indeed this method has permitted to study proximity thermal heat transfers [2-4] and materials thermophysical properties [5], it has also already allowed to map the temperature distribution on active sample surface [6-7] at a submicrometric scale. Fiege et al. [6] have demonstrated that this tool can allow the localization of failures in integrated devices at saturation or in breakdown condition. The SThM has also been used to investigate the energetical aspect of the electric degradation mechanisms inside a metal-oxide-silicon (MOS) structure submitted to an electric stress [7]. More recently, it has permitted to

measure quantitative temperature variations on PN thermoelectric couples [8].

We aim at proving an eventual sub-micrometric resolution of the SThM when using a wollaston wire probe of micrometric size. A dedicated CMOS device was designed with arrays of lines 0.35 μm in size with 0.8 μm and 10 μm period. Integrated Circuits with or without a passivation layer were tested. To enhance sensitivity, the IC heat source was excited with an AC current. We show that the passivation layer spreads heat so that the lines are not distinguishable. Removing this layer allows us to distinguish the lines in the case of the 10 μm period.

In the following, the experimental technique is presented. The results in the case where the passivation layer is present is then addressed. A finite elements based modelling allows us to analyse the data. Then the sample without passivation layer is studied. An explanation for the tip artefact is finally provided.

2. EXPERIMENTAL SET UP

The experimental set up used in this study results on the combination of a SThM and a device adapted to submit the sample to a DC or AC electric current (Figure 1).

The used SThM is a scanning probe microscope marketed by Veeco Corporation. This SThM is based on an atomic force microscope configuration with a thermal tip. The thermal probe is a thermoresistive probe consisting in a 5 μm diameter and 200 μm length platinum wire bent in form of a loop [1]. We use it in its passive mode: the DC current through the thermal probe has been chosen small enough to not electrically heat the probe. In this mode, the thermal probe is used as a resistance thermometer. It constitutes one of the legs of a Wheatstone bridge.

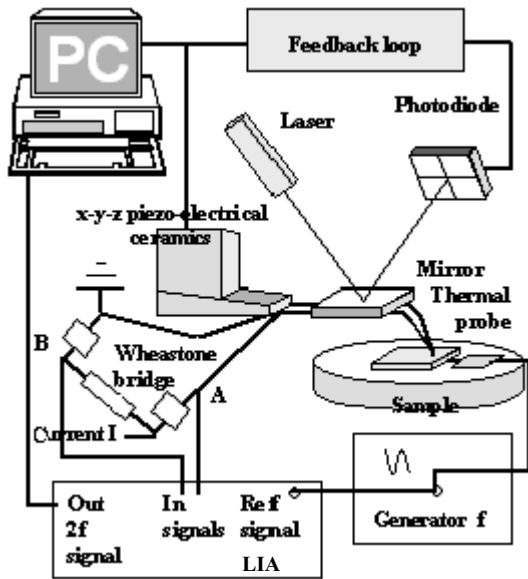


Figure 1: Experimental set up

As the temperature of the probe changes, the corresponding change in the probe resistance change the voltage balance of the bridge, changing the output voltage (V_{AB}) of the circuit. The control and the amplification of the output voltage during the scan of an hot sample surface permits to make the thermal image. The contrast of this image translates the variation of the electric resistance (the temperature) of the probe due to variation of the sample surface temperature. The SThM then permits to map qualitatively the temperature distribution of the scanned surface with a thermospatial resolution about 300 nm [7].

In the framework of resistive samples study, a second probe put on the electric contact of the considered specimen permits the current injection through the sample in order to heat it by joule effect. The resistive sample can be submitted to a sinusoidal current at a frequency f_s . In this case, the internal heating by joule effect of the sample occurs at $f = 2f_s$ and the thermal contrast is obtained by measuring the amplitude and the phase of the $2f_s$ V_{AB} harmonic by using a Lock-In Amplifier (LIA).

3. EXPERIMENTS

3.1. The samples

The submicrometric resistive elements are $0.35\mu\text{m}$ in width and $0.282\mu\text{m}$ in thickness polysilicone strips resistors. As shown in the Figure 2, the studied structure is composed with nine resistors in parallel and spaced of $10\mu\text{m}$ or $0.8\mu\text{m}$. Resistors are insulated from their polycilicone substrate by a SiO_2 layer.

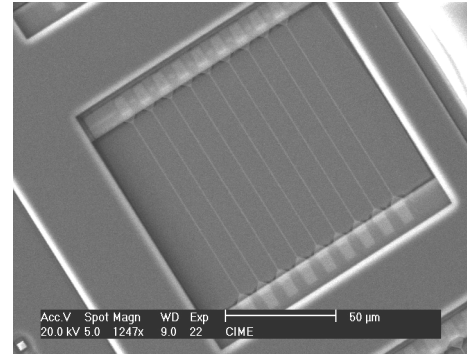


Figure 2: Electronic microscopy image of the sample

In a first and original configuration (sample1), the resistors are covered by a $3.6\mu\text{m}$ in thickness SiO_2 passivation layer. AFM images of this sample surface (figure 3) show small topographical features of a few nanometers in height at the surface, this is the signature of the resistors locations under the passivation layer.

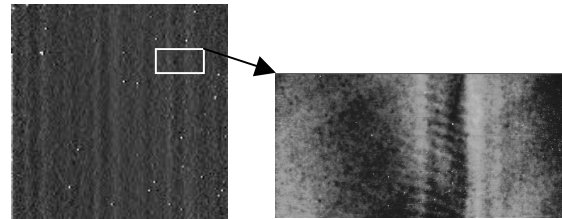


Figure 3: Topography of the sample 1 obtained by atomic force microscopy

In a second configuration, the passivation layer has been chemically etched. As shown in the figure 4, the AFM images for this sample (sample 2) show that the surface presents large and deep topographical features at the strips locations.

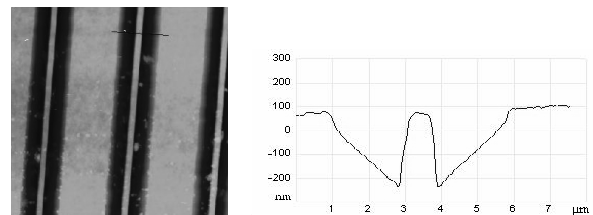


Figure 4: Topography image and profile of the sample 2 obtained by atomic force microscopy.

4. RESULTS AND DISCUSSION

The experimental set-up presented in part 2. of this paper has been used to study the temperature fields at the surface of the two samples.

4.1. Sample 1: with passivation layer

Figure 5 reports the temperature mapping of the wire array with a $0.8\mu\text{m}$ period. It clearly appears that the wires

can not be distinguished. The wires array can be modelled as one linear heat source as shown in the Figure 6.

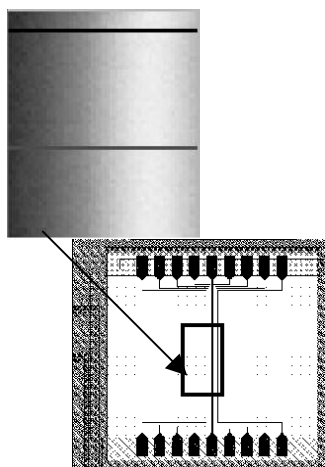


Figure 5: Image of the thermal contrast (left) of the wires array with the 0.8 μm period. The image size is 100 μm x 80 μm. The wires are covered by the passivation layer (sample 1). The schematic (right) shows the scanned area as the zone defined by a square .

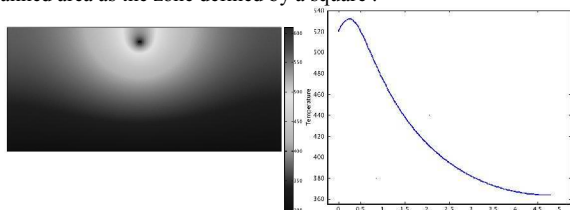


Figure 6 : Finite element modeling of the temperature field (left) around one heat source corresponding to the array in the 0.8 μm period case. The colour legend reports the temperature in K. The surface temperature is reported in the graph (right) where the vertical axis refers to temperatures in K and the abscissa to the length in meter of a radius on the surface.

Figure 7 reveals that the array with a 10 μm period still does not allow us to distinguish individual wires. The finite element simulation reported in figure 8 shows one wire in the array. It proves that the temperature field is homogeneous on the surface. Whereas the simulation represents an infinite array, the temperature gradient observed in figure 7 is due to the presence of a cold edge.

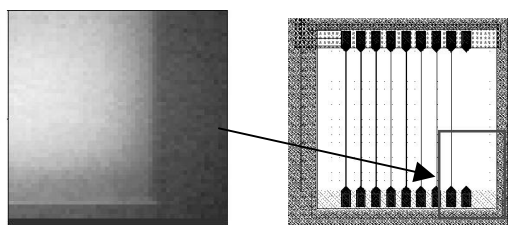


Figure 7: Image of the thermal contrast (left) of the wires array with the 10 μm period. The image size is 100 μm x 100 μm. The wires are covered by the passivation layer (sample 1). The schematic (right) shows the scanned area as the zone defined by a square .

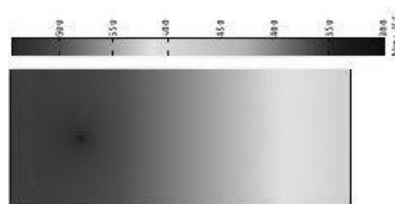


Figure 8 : Finite element modeling of the temperature field around one wire in the 10 μm period case. The top side is on the left.

Figure 8 finally shows that the spatial resolution is larger than 10 μm when scanning the passivation layer.

4.2. Sample 2: without passivation layer

Figure 9 gives the topography and the thermal contrast obtained with the SThM for the sample 2 with a 10 μm period. The array of nine resistors were submitted to a 11 mA sinusoidal current at $f_s = 110$ Hz.

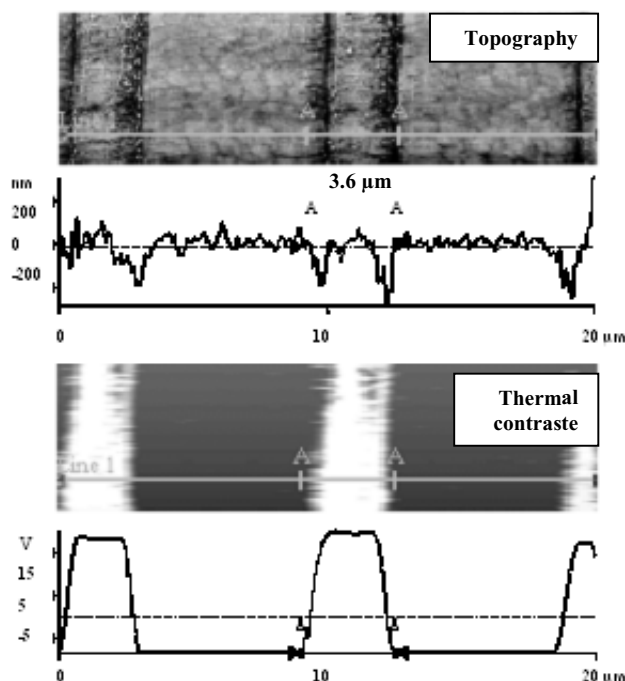


Figure 9: Topographical (top) and thermal (bottom) images (temperature frequency 220 Hz) obtained simultaneously with the SThM at the sample 2 surface.

The contrast of the thermal image clearly shows the heating of the resistors but the real wire width is not found. Due to its large curvature radius the thermal probe cannot follow the surface. As illustrated by the figure 10, this leads to surface dilatation phenomena in the topographical image obtain with the thermal probe. The contrast of the thermal image is also affected by this dilatation effect. The tip-sample heat flux is indeed directly proportional to the thermal contact surface.

This artefact is clearly due to a topography-thermal coupling. Note that the dips on both sides of the wires are insulators. If the surface were flat, heat spreading might also hide the real size of the wires.

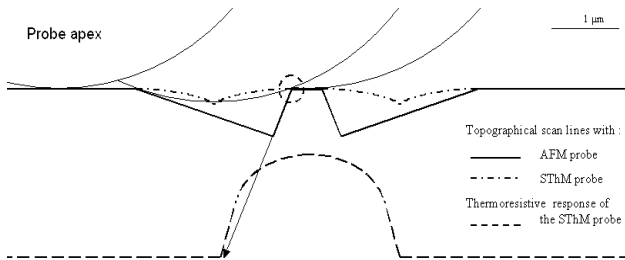


Figure 10: Illustration of the surface dilatation and of the resulting thermal contrast with the SThM probe.

5. CONCLUSION

We showed that the SThM mounted with a 5 microns in diameter platinum wire allows us to detect submicrometric elements but an artefact due to topography-thermal coupling enlarges the size of the wires by a factor of 4. This effect lowers the spatial resolution to 4 microns. When the 3.6 μm passivation layer is maintained, submicrometric elements resolution is even worse than 10 μm due to heat spreading in the layer. ICs appear as interesting tools to benchmark the spatial resolution of thermal metrologies such as SThM but the design of the structure has to be modified. It remains an adequate tool to detect hot spots on ICs surfaces.

6. ACKNOWLEDGEMENT

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