60 GHz Slot antenna integrated on SOI

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Abstract

In this paper, we propose a 60 GHz Slot antenna integrated on 0.13µm Silicon on Insulator (SOI) substrate. The antenna is composed of a CPW transmission line and the radiating slots. The design was based on electromagnetic simulations made using the CST Microwave Studio software package. The antenna exhibits a return loss of –12dB at 60GHz with a bandwidth of 10%. Backside substrate metallization has been used to improve radiation properties. The simulated radiation efficiency is 60 % with a gain around 3 dBi.

Index Term—Slot antenna, Silicon on insulator, coplanar waveguide, millimeter wave antennas

I. INTRODUCTION

Millimeter wave systems are becoming increasingly important in many military and commercial applications. The frequency range around 60 GHz presenting a band-width of 7 GHz is one of the possible solutions for the development of radiofrequency (RF) systems [1], for example with the standards IEEE 802.15.3C. With increasing use of coplanar waveguide (CPW) and related planar structures such as transmission lines for MIC's and MMIC's, particularly at millimeter wave frequencies, there is a need for a complete family of compatible printed antennas CPW transmission lines having lower radiation loss and less dispersion than microstrip lines. Furthermore, the characteristic impedance and phase velocity of CPW are less dependent on the substrate height and more dependent on the dimensions in the plane of the conducting surface. Uniplanar printed technology offers many opportunities for inexpensive production and flexible design, especially in roles complementary to those of the microstrip patch.
Recently, Silicon on Insulator (SOI) technology was found to offer alternative solutions to many problems faced in the race to higher performance and low power consumption of integrated systems [2]. At the same time, SOI does not require major changes compared to the well known complementary metal oxide semiconductor (CMOS) process flow. The performance of traditional microwave circuits such as transmission lines and antennas, on low resistivity silicon wafer, is problematic due to the high losses for example on CMOS substrate [3]. In fact, this substrate weakens the radiation efficiency of the antenna which can be greatly improved by the use of highly resistive SOI substrate. The design of integrated antennas operating at 60 GHz is a critical issue when high efficiency is required [4].
In this paper we describe the design of a CPW Transmission line (TL) and a slot antenna integrated on SOI. After the characterization of the CPW TL, it is used as the first block of the feeding system for the slot antenna. The slot antenna consists in two slots shorted at both ends to have a final impedance matching with other block such as the low noise amplifier.

II. COPLANAR WAVEGUIDE FEED LINE

Transmission lines permit antenna feeding and are used in matching networks design. At very high frequencies, the coplanar waveguide is commonly used when low loss interconnections are required. CPW TL is composed of three conductors printed on a dielectric substrate that must be half isolated to limit the dielectric losses. In case of traditional bulk CMOS silicon substrate, the situation is different; CMOS bulk substrate includes multi metallic layers, buried oxide structure and a low resistivity silicon substrate which generates considerable losses. However the recent introduction of high resistive substrate (SOI) reduces the dielectric losses, which proves the importance of SOI for the realization of low loss TL. Two quasi TEM modes are propagating in the CPW TL, odd mode where the ground planes have the same potential and the unwanted even mode that can be eliminated by the use of wire bonding or underpath vias connecting the two ground planes.

The topology of SOI substrate is presented in figure 1: a high resistive silicon layer (>1000 ohm.cm), six metals layers, buried oxide layer and finally a passivation layer. Two key parameters (characteristic impedance and attenuation factor) of such transmission line have been deeply studied to compare the performance [5]. To study such TL, an example of a printed CPW on SOI is considered. First of all the characteristic impedance can be calculated basing on the conformal mapping method by using the formula (1) below, Note that we are taking formulas for multilayer conductor backed coplanar waveguide (CBCPW) TL .[6]

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k)}{K(k')} \qquad (1)$$

Where

- Z_0 *is the characteristic impedance of the CBCPW*
- *K is the elliptic integral of k and k' factor that depend on the dimensions of CBCPW (gap and central strip width)*
- ε_{eff} *is the effective permittivity of SOI*

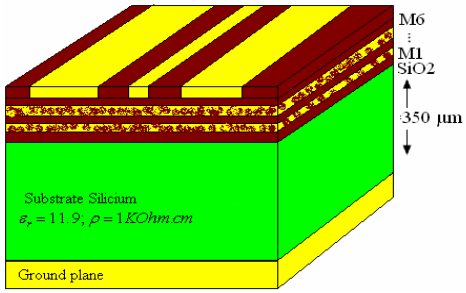

Fig. 1 CBCPW TL on SOI

The CBCPW TL is designed on SOI, and the S parameters are measured using a HP8510XF vector network analyzer. The Thru-reflect-line (TRL) calibration technique is the most accurate for determining the reflection coefficient of a nominal short having sexless connectors [7]. A TRL calibrating kit was designed and measured to characterize the CBCPW TL and to extract its characteristic impedance and its complex propagation constant. The reference impedance of this calibration is set to 50 ohms, and its reference plane is moved back to a position close to the probe tips using the methods described in [8].

Fig. 2 shows the comparison of the simulated and the measured results of the characteristic impedance for a CBCPW TL as well as its attenuation loss. The gap between the central strip width and the ground plane is 10 µm; the width of the central strip is 29µm.

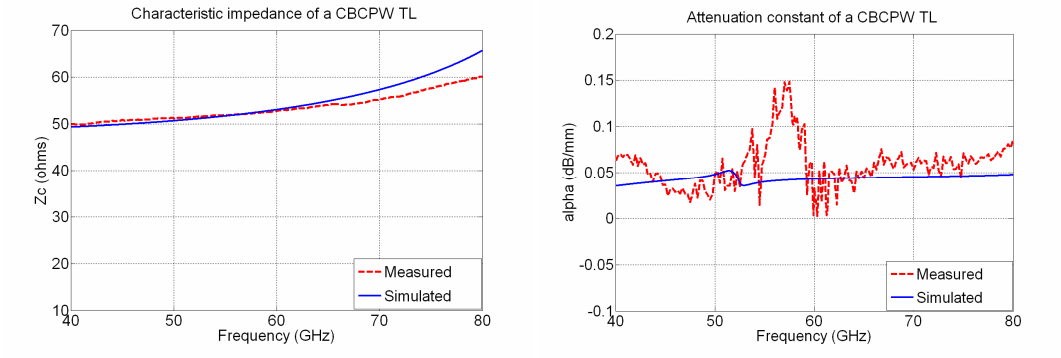

Fig.2 Characteristic of a CBCPW on SOI (w=29µm, g=10 µm)

III. ANTENNA DESIGN AND FABRICATION

The folded-slot antenna is a very popular planar antenna that has been used in a variety of applications. It consists of a folded-slot with a circumference approximately equal to one guided wavelength (λg) [9]. It can be fed with a CPW allowing for easy integration of three-terminal devices or MMIC's for microwave

amplification and reception. The basic property of this antenna is a broad bandwidth and pattern with maximum radiation at the broadside [9]. In the cases of low resistivity silicon substrate, the electric fields in the CPW must have minimum interaction with the lossy substrate that is why a thick layer of Polyimide (Dupont WE 1111) can be deposited to minimize coupling [10]. It is well known that the input impedance of N-element dipole antenna is given by $Z_{in,N} = N^2 Z_{dipole}$, where Z_{dipole} is the input impedance of an ordinary half-wave dipole (≈70 Ω).Using Babinet's principle [11,12], an N-element slot antenna would then have an input impedance given by

$$Z_{in,N} = \frac{Z_{slot}}{N^2} \qquad (1)$$

Where Z_{slot} is the input impedance of a single slot antenna (≈500 Ω in free space). The use of additional slot allows us to "engineer" the impedance of the antenna over a wide range of frequencies, when N is not too large. The fundamental operation of slot antenna relies on the ability to switch the geometry between configurations in order to optimize the resonant conditions of the antenna. For the folded slot antenna this resonant condition arises from the conference of the folded slot, which is proportional to the guided wavelength around this length. For the twin slot antenna (one driven, one parasitic and closely spaced), the resonant conditions are dictated by the overall length of the slot, also proportional to the guided wavelength [13]. The three terminal double slot antenna is fed by a CBCPW TL, as it was explained in part II , the CPW feeding is designed to have an optimum matching between the double slot input and the radiofrequency (RF) pads used in the probe feeding. In our case, the characteristic impedance of the Transmission line is 50 Ohm.

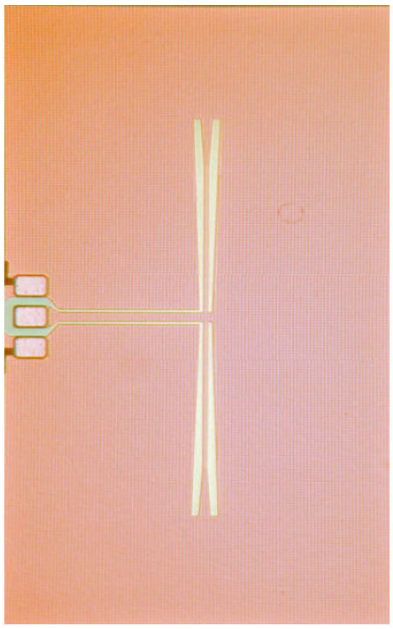

Fig. 3: Double slot antenna on SOI with Radiofrequency Pads

The design of integrated antennas operating at 60 GHz is a critical issue when high efficiency is required. The completely integrated double slot antenna is realized on 0.13 µm silicon on insulator (SOI) process. The antenna is integrated on the top metallic layer (M6) to assure the compatibility with the RF pads. The width of the central strip of the line is 29 µm with a gap between the central strip and outer ground plane of the CPW of 10 µm. The length of the slot antenna is 1200 µm which is equivalent to a half wavelength and the surface of the substrate is 2 mm² (1*2 mm²).

To respect the metal density of the SOI process, small holes are created from the antenna layer without any effect on the antenna performance.

IV. RESULTS

The design of the double slot dipole was based on electromagnetic simulations made using the CST Microwave Studio software package. The silicon substrate thickness is 350 µm and oxide layer thickness is 5 µm. The antenna was characterized experimentally using a HP 8510 XF vector network analyzer (VNA) able to measure up to 110GHz. As presented in part II, the TRL calibration technique was used to extract the S parameters of the CBCPW feed in order to de-embed the return loss (S11) of the double slot antenna measured by the VNA and finally to obtain the input impedance of the double slot antenna. In fact, due to the 50 ohm design of the CBCPW, we expect a good agreement correspondence between the measured return loss by the VNA and the de-embedded return loss.

The de-embedding procedure is performed as follows: first the antenna is measured by the VNA to have the Y parameters of the total CBCPW feed double slot antenna, second the equivalent feed CBCPW TL is measured and its Y parameters extracted, finally the Y parameters of the double slot antenna are obtained by simply subtracting the two results as follows [11]

$$[Y_{Double-slot}] = [Y_{measured\ antenna+feed}] - [Y_{measured\ CBCPW\ TL}]$$

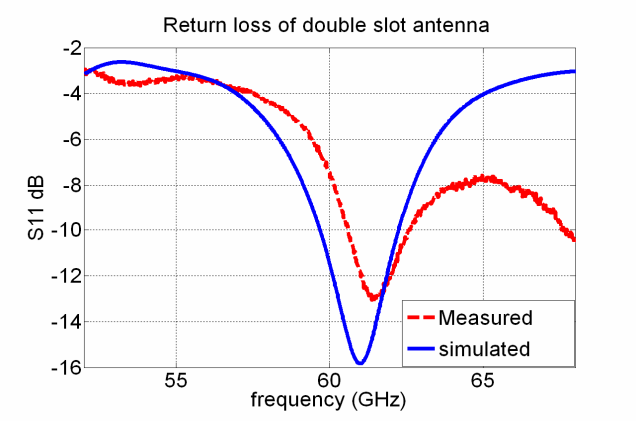

Fig.4 Measured and simulated Return loss of the CBCPW fed Double slot

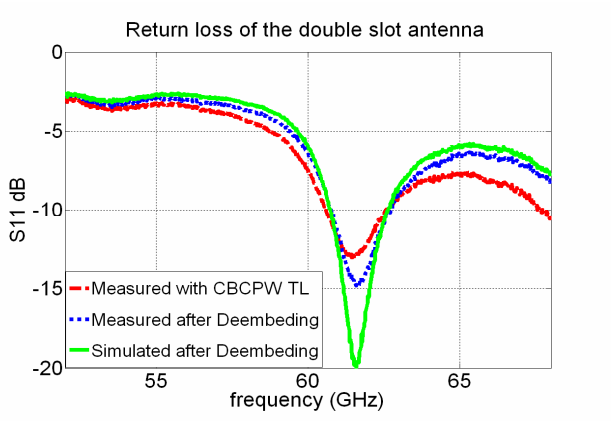

Fig.5 Measured and simulated Return loss of the Double slot antenna after De-embedding

The measured and simulated return loss of the full antenna with the CBCPW feeding is showed in Figure 4. The double slot antenna exhibit 2 GHz of bandwidth at -10 dB. To extract the return loss of the double slot antenna, figure 5 shows the comparison of the different cases: first the case where the antenna is fed directly with CBCPW without de-embedding, second the simulated and the measured return loss after de-embedding. The simulation of radiated field pattern for the double slot antenna shows that the radiation is mainly directed toward the SOI substrate, where losses occur. The backside metallization under the wafer can be advantageously used as a reflector. The radiation pattern is directed outward of the substrate when backside metallization is added. The distance between antenna and the back side metallization (355µm~ $\lambda_g/4$) is close to the optimal distance in order to minimize side lobes [11]. The efficiency of radiation is increased and it is equal to 60 % (simulated results) with a gain around 3 dBi. Measurements of antenna gain and radiation pattern are on the way…

V. CONCLUSION

This paper has presented the performance of a double slot integrated antenna on SOI. The antenna is designed at 60 GHz and exhibit a good impedance matching to the 50 ohm probe feeding. The antenna is characterized experimentally using a HP 8510 XF vector network analyzer (VNA).The de-embedding procedure is also described and the result shows the agreement between correspondence of the measured and simulated result. The back side metallization under the wafer is used to act as a reflector. . The radiation efficiency is equal to 60% with a gain around 3 dBi. This antenna is a part of on chip design using CMOS SOI technology in order to be used in the co-design process of the antenna with a 60 GHz integrated Low Noise Amplifier.

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