DESIGN OF A 3 GHz 6TH ORDER DELTA-SIGMA MODULATOR IN A 0.2 μm GaAs TECHNOLOGY

Emilie Avignon, Sylvie Guessab, Richard Kielbasa, Jean-Marc Guebhard, Nicolas Fel, Jean Russat

DESIGN OF A 3 GHz 6TH ORDER DELTA-SIGMA MODULATOR IN A 0.2 µm GaAs TECHNOLOGY

Emilie Avignon, Sylvie Guessab, Richard Kielbasa
Department of Signals and Electronic Systems
Supélec, Plateau de Moulon, 3 rue Joliot Curie
91192 Gif-sur-Yvette, France
Emilie.Avignon@supelec.fr

Jean-Marc Guebhard, Nicolas Fel, Jean Russat
CEA/DIF
91680 – BP12
Bruyères le Châtel, France
Jean-Marc.Guebhard@cea.fr

ABSTRACT
This paper presents the design of a monobit 6th order delta-sigma modulator in a GaAs 0.2 µm technology. The central frequency is 750 MHz and the sampling frequency is 3 GHz. The reached resolution is 10.5 bits over a 10 MHz bandwith. The modulator operates from ± 5 V power supplies and consumes 5.7 W. Each block of the modulator is presented at transistor level. Two drawbacks are pointed out: low pass terms of Gm-LC resonators and the lowpass characteristic of the adder. Two solutions are proposed. Finally, simulation results of the complete modulator are given.

KEY WORDS
Analog-digital conversion, Delta-sigma Modulator, GaAs circuits.

1. Introduction

The actual trend in the field of wireless communication is to imagine receiver architectures without transposition stages at intermediate frequency. Indeed, these stages are expensive on surface implementation and error sources because of theirs non-linearities. It is thus necessary to design devices allowing the direct conversion of the radio frequencies signals in the front end of the receivers. And these devices must be able to work at radiofrequencies without precision loss. Among several solutions, the continous-time delta-sigma modulators already offer some interesting prospects. Various realizations of bandpass modulators in the RF domain were published and are reported in table 1.
The general method to design such converters is to first calculate the architecture with ideal functions in order to achieve some specifications. Then, the aim is to design the functional blocks at the transistor and physical level with a particular technology. When we use the technology at the limits of its performances, some imperfections will appear in the different blocks and will have to be compensated in order not to degrade the modulator performances.
The imperfections generally taken into account when calculating continuous-time delta sigma modulators are the loop delay of the ADC and DAC [4][5]. The jitter has been studied as well [6]. Moreover, it is now well known how to compensate the weak quality factor of resonators [7], essential part of delta-sigma continuous-time modulators.
This article presents the design of a 6th order continuous time modulator in a GaAs 0.2 µm technology. This modulator has to work at the oversampling frequency of 3 GHz for a central frequency of 750 MHz and has a useful bandwith of 10 MHz. We show that at these working frequencies and regarding to technological constraints it is necessary to take into account the low-pass terms of the continuous time resonators as well as the low pass characteristic of the adder present in many modulator architectures. A methodology and compensation solutions are proposed. Used in the GaAs 0.2 µm technology, they are however usable in other technologies.
We present in section 2 the theoretical architecture of the modulator and the expected performances, the section 3 develops the block realization at transistor level, the effects of imperfections are analyzed and some corrections are proposed, and the section 4 presents characteristics of the modulator circuit as well as simulations results.

2. Modulator architecture

The ideal architecture on which we will make the considerations on the imperfections is presented in figure 1.

Table 1 : Published high-speed continuous-time band pass Delta-Sigma modulators

Paper	Technology	Order	F_0	F_s	Resonators	SNR
[1]	0.5 µm Si BJT	2	950 MHz	3.8 GHz	Gm-LC	57 dB on 200 kHz
[2]	0.5 µm SiGe HBT	4	1 GHz	4 GHz	Gm-LC	53 dB on 4 MHz
[3]	AlGaAs/GaAs HBT	4	800 MHz	3.2 GHz	Gm-LC	66 dB on 100 kHz

The method of calculation of such an architecture starting from specifications (central frequency, useful bandwidth, oversampling frequency F_s, expected resolution) has already been published [8]. The 6th order ideal architecture is composed of pure resonators. In the parallel part with three connects, the above connect insure a sufficient gain to have the expected precision, when the under connect insure the stability of the modulator [9]. The chosen structure is monobit. Indeed, different studies have demonstrated that a multibit structure will not permit to obtain better performances if dynamic element matching (DEM) is not carried out [10]. However, the realization of such a DEM, regarding to the working frequencies and the employed technology (not really adapted for logical circuits) would be difficult. The delay due to the ADC and DAC is fixed at 1.5 T_s for the calculation. Indeed this value of delay has been determined as an optimal value for the modulator performances, and a feedback gain may be added to stay in conformity with the original discrete-time calcultated architecture [4][5]. The gain of each resonator A_0 may be tunable and will affect the precision of the modulator. With a high value of A_0 the modulator is more precise, but can be close to unstability. The negative term $-A_1F_s^2$ of the entry resonator comes from the calculation of the continuous-time equivalent loop filter starting from the discrete-time one. This negative term is not realizable at transistor level, but it will not affect the modulator behaviour as shown in figure 2, where the output spectrum is given for $A_0 = 0.2$ and $A_1 = 0$.

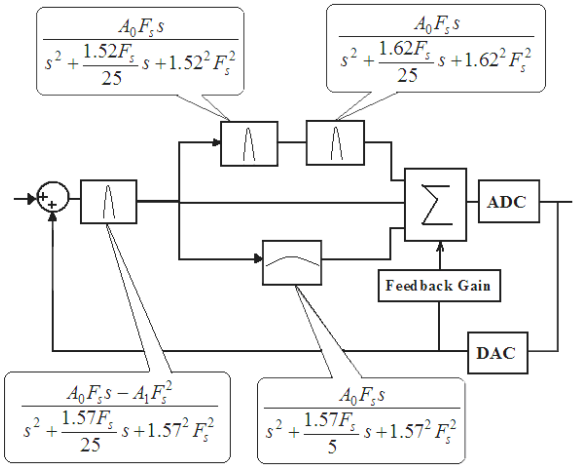

Figure 1 : modulator architecture

The input signal is at the frequency $F_0 = F_s/4$ and an amplitude of 100 mV. The output level of the modulator is ± 300 mV. The resolution is about 12 bits for a useful bandwith of $F_s/300$.

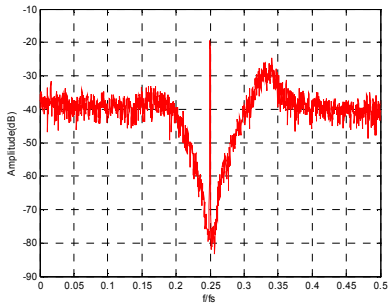

Figure 2 : output spectrum of the theoretical architecture

3. Blocks realization and corrections

3.1 Resonators

The resonators realization has been considered in two different ways: 1 – by Gm-LC, 2 - by gyrators (Gm-C). The Gm-LC solution has been temporarily chosen because of its better linearity. But in any case, it is not possible to design true resonators, because a low pass term appears due to the parasitic resistance of the inductance in the Gm-LC case or due to the output impedance of the transconductance amplifier in the Gm-C case.
The Gm-LC designed resonator is presented in figure 3. The differential architecture eliminates the second order non-linearity terms. Inductances are connected to a fixed potential, so a commun mode regulation is not necessary. The quality factor of the inductances is weak in the used technology at 750 MHz, so negative resistance compensation has to be done [7]. The transfer function of the Q-enhanced resonator is then:

$$G(s) = \frac{\frac{G_m}{C}s + \frac{R_s G_m}{LC}}{s^2 + \left(\frac{R_s}{L} - \frac{G_{neg}}{C}\right)s + \frac{1 - G_{neg}R_s}{LC}} \qquad (1)$$

where R_s is the parasitic resistance of the inductance and $1/G_{neg}$ the negative resistance.

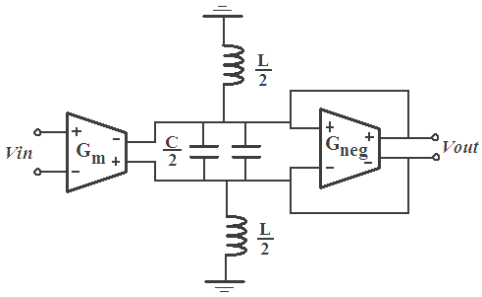

Figure 3 : Q-enhanced Gm-LC resonator

The influence of the low-pass term of the resonators on the behaviour of the delta-sigma modulator, and specially

his stability can be, under certain conditions [11], studied with the Nyquist criterion. The Nyquist diagram in open loop in the ideal case (fig. 4-a) and in the Gm-LC case (fig. 4-b), show that the modulator can be near unstability or unstable in the Gm-LC case depending on the gain of the resonators. With a poor gain A_0, the modulator will always be stable in spite of the low pass term, but the interest of the delta-sigma modulation is lost, because the resolution is strongly decreased. Then, a certain value of the gain A_0 must be kept and this low pass term has to be corrected. To carry out this correction, we add a first order high pass filter composed of the capacity and resistance C_{cor} and R_{cor}. The resulting transfer function is then given by:

$$G(s)PH(s) = \frac{\frac{R_s G_m}{LC}\left[\frac{G_m L}{R_s G_{neg}}s + 1\right]}{s^2 + \left(\frac{R_s}{L} - \frac{G_{neg}}{C}\right)s + \frac{1 - G_{neg}R_s}{LC}} \times \frac{R_{cor}C_{cor}s}{1 + R_{cor}C_{cor}s} \quad (2)$$

And R_{cor} and C_{cor} are given by:

$$R_{cor}C_{cor} = \frac{L}{R_s} \quad (3)$$

With this correction, the ideal case is restored.

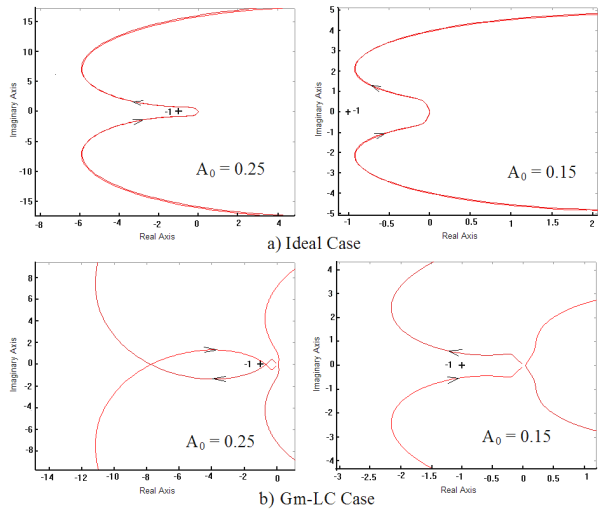

Figure 4: Nyquist Diagram

The resonator circuit at transistor level is presented in figure 5. The transconductance amplifier is biased by high impedance current sources and is linearized by a resistance. Because of the difficulty to realize linear current mirror in GaAs technology, every resonator is followed by a shift voltage stage.

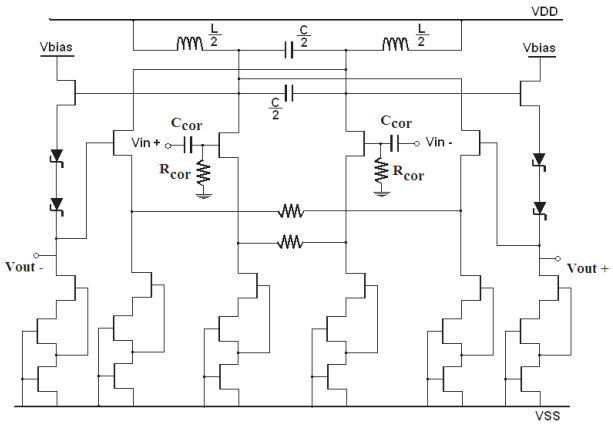

Figure 5: resonator circuit

3.2 Adder

The important specifications for the adder are: a minimum in band gain to insure the resolution of the modulator, a bandwidth adapted to the working signals and a sufficient linearity zone compared to the input signals.
A typical structure of an adder is presented in figure 6. The input signals are applied to several transconductance amplifiers Gm and the resulting current is summed in a resistance R. Cp represents the parasitic capacity due to the output stage of the adder.

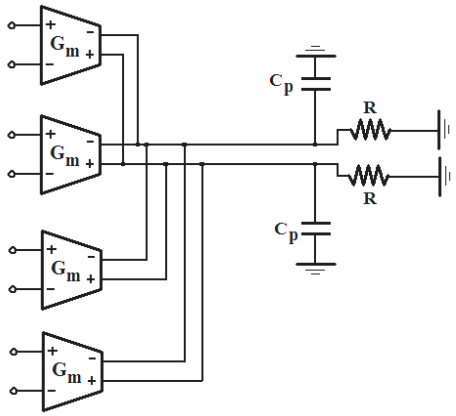

Figure 6: Typical adder architecture

So, the transfer function of the adder can be expressed as:

$$S(s) = \frac{RG_m}{1 + RC_p s} \quad (4)$$

The cut-off frequency of the adder is then given by:

$$f_c = \frac{1}{2\pi RC_p} \quad (5)$$

To demonstrate the effect of this low pass characteristic on the modulator, the noise transfer function in the discrete time domain (NTF(z)) of the modulator has been traced (fig 7). For that, the z-equivalent function of the loop filter G(s) followed by the adder S(s) is calculated with the expression (6). We observe that the NTF is deformed in a way which depends on the value of the cut off frequency f_c.

$$F(z) = (1 - z^{-1}) Z_T \left\{ L^{-1} \left[\frac{G(s)S(s)}{s} \right] \right\} \qquad (6)$$

$$NTF(z) = \frac{1}{1 + F(z)} \qquad (7)$$

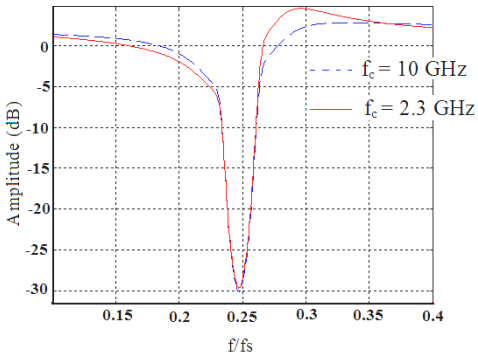

Figure 7: NTF(z) of the modulator

The observed deformation can lead to degradations of the performances, and then the bandwith of the adder has to be increased. The adder circuit at transistor level is presented in figure 8.

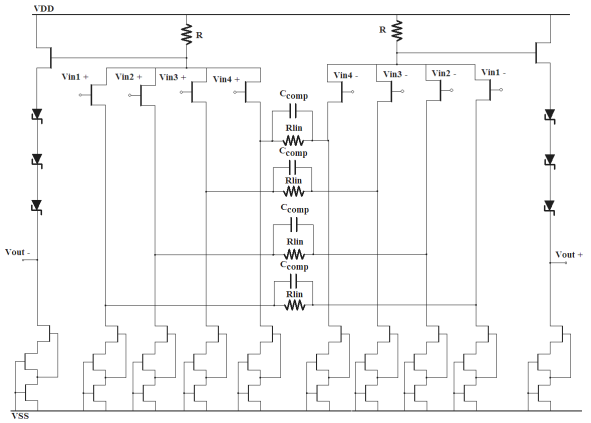

Figure 8: Adder circuit

The resistance R_{lin} increases the linearity of the transconductance amplifiers. The transfer function of this adder is:

$$S(s) = \frac{1}{1 + RC_p s} \left[\frac{Rg_m}{R_{lin} g_m + 1} \right] \qquad (8)$$

where g_m is the transconductance value without the linearization resistance R_{lin}. The bandwith of this adder can be increased by the addition of a compensation capacity C_{comp} in parallel with the linearization resistance. The transfer function becomes then:

$$S_{comp}(s) = \frac{g_m R}{g_m R_{lin} + 1} \frac{(1 + R_{lin} C_{comp} s)}{\left(1 + \frac{R_{lin} C_{comp}}{g_m R_{lin} + 1} s\right)(1 + RC_p s)} \qquad (9)$$

The cut off frequency is then pushed back more than:

$$f_{ccomp} = \frac{g_m R_{lin} + 1}{2\pi R_{lin} C_{comp}} \qquad (10)$$

As an example, the figure 9-a presents the output spectrum of the delta-sigma modulator with an adder of which the cut off frequency is 2.3 GHz, and the figure 9-b, the output spectrum when the adder is compensated with a 0.8 pF compensation capacity C_{comp}.

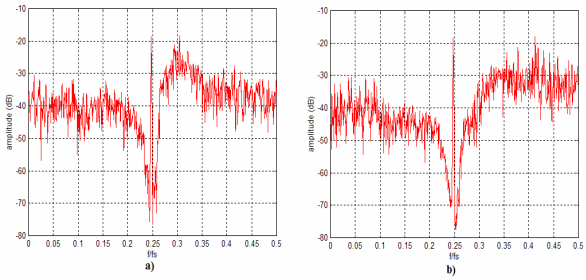

Figure 9 : output spectrum a) in the non-compensated case b) in the compensated case

We can observe that the spectrum has been corrected by the compensation capacity. Without compensation the resolution is 10.8 bits and we reach 11.5 bits with the compensation. The only drawback of this compensation is that it could degrade the linearity at high frequencies.

3.3 Comparator

The designed comparator is a NRZ one, and its principle is presented in figure 10.

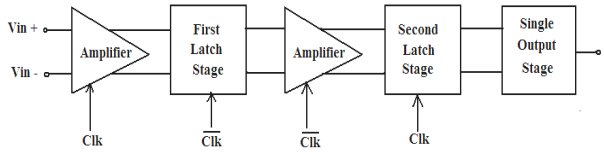

Figure 10: General architecture of the comparator

The first amplifier stage takes a sample of the signal. This sample is then compared by the first latch stage. Then, to

remove the sample part of the signal, a second stage is added (amplifier and latch) which allows holding the results of the comparison. Eventually a single stage output allows the feedback to the entry of the modulator.
The comparator circuit at transistor level is given in figure 11. The circuit is of the SCFL type (Source Coupled FET Logic) and its sizing can be done through a linearized equivalent circuit model [12]. The latched level may be chosen through the value of Ra and Rb, but these resistances have to be sufficiently weak to avoid reversed bias of HEMT junction, which can bring current in the gate. Each latched transistor are of the E-HEMT type (Enhanced type), because their higher threshold voltage facilitate the latch-mode.

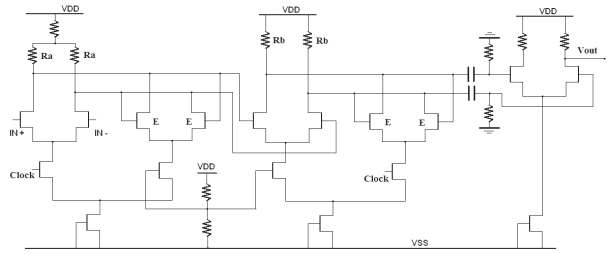

Figure 11 : Scheme of the comparator

Two comparators as described on figure 11 are placed together to reach a delay of about 1.5 T_s, which is the delay required for the modulator loop. The figure 12 shows the comparator response to a sine signal at 3 GHz clock. The response time is of 40 ps. The voltage sensitivity, the smallest input voltage difference that the circuit can resolve is about 5 mV.

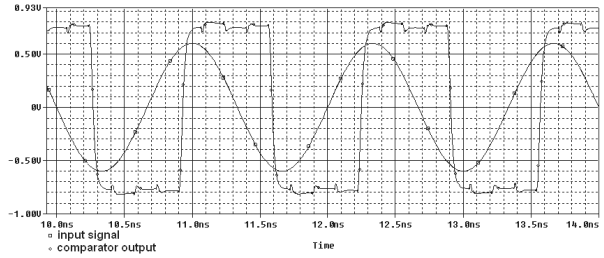

Figure 12 : comparator response at 3 GHz

3.4 Feedback gain

When the delay of the ADC and DAC is taken into account, the continuous-time equivalent modulator is no more conform to the first calculated discrete-time one. To keep the mathematical equivalence, a feedback gain is added [5].
The feedback gain is designed by a simple transconductance amplifier placed between the comparator output and the adder input, and is tunable by its bias current (fig 13).

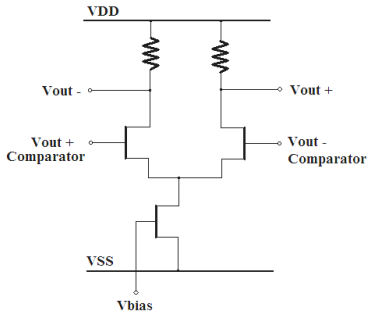

Figure 13: Feedback gain circuit

4. Complete circuit characteristics

A view of the general architecture of the delta-sigma modulator is given in figure 15. The obtained resolution is about 10.5 bits over a 10 MHz bandwith for an input signal of 100 mV and an output level of ± 300 mV. When the die will be realized, it will be hard to control the comparator delay, and then we hope to improve the performances with the tunable feedback gain.

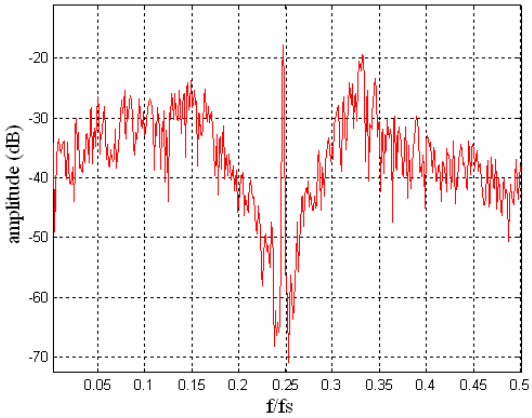

Figure 14: output spectrum of the 6th order modulator

The circuit is now being implanted. Die size is 3mm × 3mm. Its consumption is evaluated to be 5.7 W.

3. Conclusion

This article has presented the design of a 3 GHz continuous-time bandpass delta-sigma modulator, operating at a central frequency of 750 MHz. The design of the different blocks of the modulator has been presented and two encountered drawbacks have been pointed out: the lowpass terms of the resonators and the lowpass characteristic of the adder. Two solutions have been given, and can be employed in many other technologies. The obtained resolution at transistor level is 10.5 bits. In the future, it is possible to increase this resolution with a multibit structure corrected by a DEM.

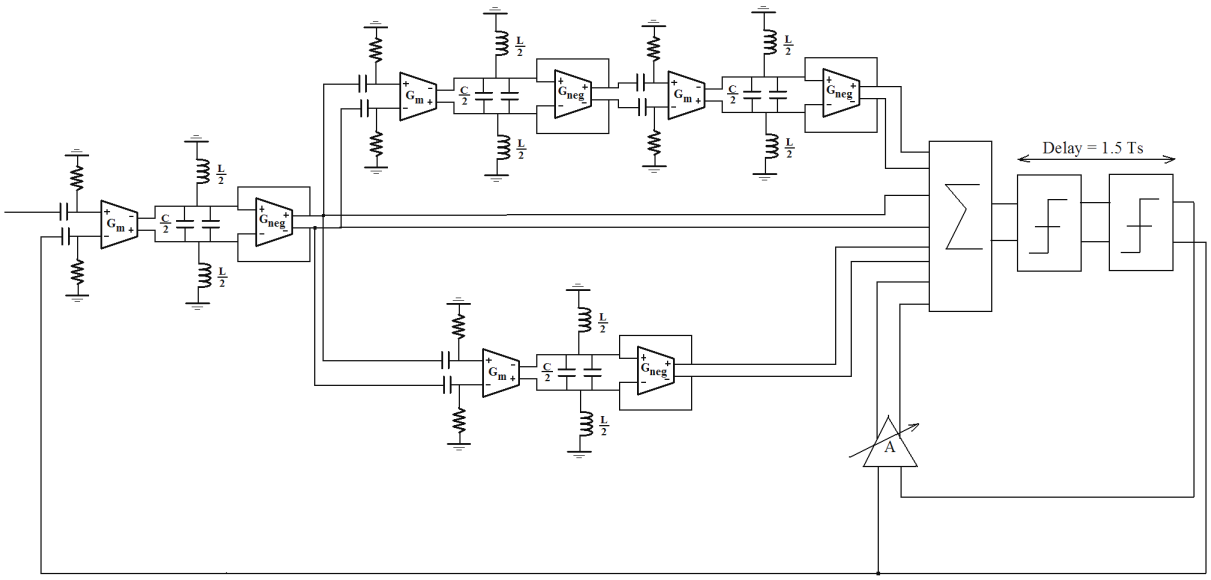

Figure 15: complete view of the modulator

References

[1] W.Gao, W. Martin Snelgrove "A 950 MHz IF Second-Order Integrated LC Bandpass Delta-Sigma Modulator" *IEEE Journal of solid-state circuit*, May 1998. vol 33, NO. 5,

[2] W. Gao, James A.Cherry and W. Martin Snelgrove "A 4 GHz Fourth-Order SiGe HBT Band Pass ΔΣ Modulator" *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, 11-13 june 1998. p. 174-175

[3] Arun Jayaraman, Peter Asbeck, Kevin Nary, Steve Beccue and Keh-Chung Wang "Bandpass Delta-Sigma Modulator with 800 MHz Center Frequency" IEEE *Gallium Arsenide integrated circuit Symposium*, 12-15 october 1997. p. 95-98

[4] James A. Cherry and W. Martin Snelgrove "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators" *IEEE Transactions on Circuits and Systems-II : Analog and Digital Signal Processing*, april 1999. Vol. 46, NO. 4.

[5] Abdeljalil Yahia, Phillippe Benabes and Richard Kielbasa "Influence of the Feedback DAC Delay on a Continuous-Time Bandpass ΔΣ Converter" *IEEE International Symposium on Circuits and Systems*, 26-29 may 2002. vol 2 II-648 II-651

[6] James A. Cherry, W. Martin Snelgrove "Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators" *IEEE Transactions on Circuits and Systems-II Analog and Digital Signal Processing*,June 1999. Vol. 46, No. 6

[7] U. Yodprasit, J. Ngarmnil, "Q-enhancing technique for RF CMOS active inductor" *ISCAS 2000 – IEEE International Symposium on circuits and systems*, May 28-31, 2000.

[8] P. Benabes, P. Aldebert, R. Kielbasa "A Matlab based tool for bandpass continuous-time sigma-delta modulators design" *IEEE International Symposium on Circuits and Systems*, Monterey, CA, june 1-3, 1998. vol.VI, pp. 274-277

[9] C. Lelandais-Perrault, P. Benabes, J.-L De Gouy and R.Kielbasa "A parallel structure of a continuous time filter for band pass sigma-delta A/D Converter" *IEEE International Conference on Electronics, Circuits and Systems*, 14-17 dec 2003. Vol 3, 954-957.

[10] Esmaeil Najafi Aghdam, Philippe Benabes , "A hardware efficient 3-bit second-order dynamic element matching circuit clocked at 300 MHz", *IEEE International Symposium on Circuits and Systems* (ISCAS 2006). Kos, Greece, 21-24 May 2006, Page:2977-2980.

[11] J-Luc Degouy, P.Benabes, C. Flouzat, J-M Hode, R. Kielbasa "A new s-domain approach for designing continuous time sigma-delta converters" *IEEE Conference on Instrumentation and Measurement Technology*, 21-23 May 2001. vol. 2 744-749

[12] Shen Feng and Dieter Seitzer "Characterization and Design of GaAs SCFL Latched Comparators Based on Improved Linearized Models" *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, june 1995. Vol. 42, No. 6.