Design and VHDL Modeling of All-Digital PLLs

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***Abstract*— In this paper, a VHDL model of a second-order all-digital phase-locked loop (ADPLL) based on bang-bang phase detectors is presented. The developed ADPLL is destined to be a part of a distributed clock generators based on networks of the ADPLL. The paper presents an original model and architecture of a digital multi-bit phase-frequency detector (PFD), and describes in details the VHDL modeling of metastability issues related with asynchronous operation of the digital PFD. This particular architecture of the digital PHD is required by the synchronised operation of the ADPLL network in the context of distributed clock generator. The whole ADPLL model have been validated by purely behavioral (VHDL) and mixed simulation, in which the digital PFD detector was represented by its transistor-level model.**

I. Introduction

Nowadays the number of sequential elements in Systems-on-Chip (SoCs) is increased with recent advances in modern VLSI technologies. Traditional clock distribution networks based on trees and grids present disadvantages for complex SoCs since no solution is considered to reduce the inaccuracy (skew and jitter problems) of the delivered clock [1]. Network of Phase-Locked Loop (PLL) oscillators coupled in phase is an alternative to guarantee the global synchronization [2]. Each PLL is synchronized with its neighbor PLLs. An implementation of this network, based on analog PLLs, is done by Gutnik and Chandrakasan [3]. However, this architecture is exclusively based on blocs of analog electronics, which rises the problem of their operation in noisy environment of digital circuits, sensitivity to process parameters and incompatibility between the analog and digital tools design. All-Digital PLLs offering the ability to achieve the performance of analog PLLs can be good candidates to overcome these limitations. Comparing to analog PLLs, ADPLLs are less sensitive to noise (since there is no analog control of the DCO), and they can be implemented exclusively with standard blocks of digital electronics. Hence, a ADPLL-based clock generation network could be a very interesting alternative to existing centralized clock distribution solutions (H-tree, grid, etc.).

Since a ADPLL network is a very complex nonlinear high order system, its system-level modeling is of paramount importance. Moreover, behavioural modeling of such a system should take into account the circuit level issues such as delay, possible metastability problems, etc... For this, a VHDL-level modeling is a good candidate, outperforming Simulink-based approach in precision and simulation time. This work targets the design and modeling of one simple ADPLL, which is an basic block of such clock network. This paper presents the result of VHDL modeling of a ADPLL. In the context of the digital distributed clock generator, the following parameters of individual ADPLL have an impact on the overal network performance: the DCO frequency resolution, the Phase-Frequency Detector (PFD) precision, the delays of logical elements. The proposed VHDL description models these issues, and as well takes into account the practical implementation issues such as limited number of bits, synchronization issues of latches, self-sampling operation, etc... This work have two original points. Firstly, the proposed ADPLL architecture uses a particular multibit digital phase-frequency detector which is necessary for a correct operation of the ADPLL network. Secondly, metastability issues are taken into account at the VHDL-based description.

This model can be used to optimize the parameters of the network with a negligible simulation time. The PFD which is the most critical component of the ADPLL is also implemented in transistor-level in order to justify the proposed VHDL model. The transistor-level implementation is done in ST CMOS $65\ nm$ technology and the results are compared with that of the VHDL model.

In section II the topology of an ADPLL is described. In section III the developed VHDL model is presented. In section IV the performance of the transistor-level implementation is compared with that of the VHDL model. Finally, conclusions are presented in section V.

II. Topology Description

The topology of the ADPLL is presented in Fig. 1. As it is shown, the ADPLL contains the following components: a phase-frequency detector, a Loop Filter (LF), a digitally controlled oscillator (DCO) and a frequency divider ($\div$ M).

The PFD is used to compare the phase/frequency of the reference clock (ref issued from one or several neighbor nodes) with the phase/frequency of the produced clock (div). The PFD produces a signed binary code. The produced code is processed by a low-pass filter in order to diminish the noise level and to eliminate the high-frequency components. Then it is used to control the DCO. The frequency divider is introduced since the frequency of clk excess the limits of the operational frequency of digital circuits. In the present case the

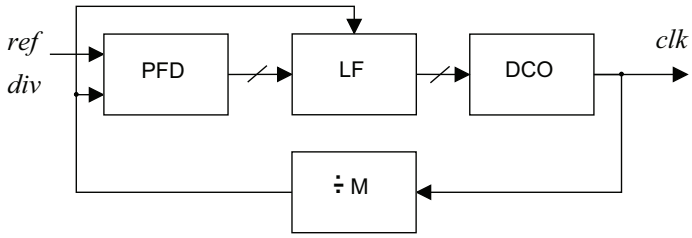


Fig. 1. Topology of the ADPLL.

divide factor (M) is set equal to 4. As a result, the operational frequency of the LF is 250 MHz rather than 1 GHz.

The structure of the PFD is shown in Fig. 3. The Bang-Bang PFD (BB-PFD) detects the sign of the phase error ($SIGN$) as well as the interval of the phase error ($MODE$), which is inspired by the work presented in [4]. A Time-to-Digital Converter (TDC) is used to convert the $MODE$ signal into a non-signed code representing its duration. Then, a signed binary code is produced by the arithmetic block through the $SIGN$ and the TDC output. The desired transfer function is given in Fig. 2.

The TDC ouptuts signal in a range [0, 2^N-2], where N is the number of bits of the output digital code. In order to have an information about the sign for small errors for which the TDC generates zero, the arithmetic bloc adds 1 to the TDC output:

$$ERROR = SIGN * (Dout + 1). \quad (1)$$

Here $SIGN$ has values of +1 or -1. Hence, for small errors, this PFD behaves as a bang-bang PFD.

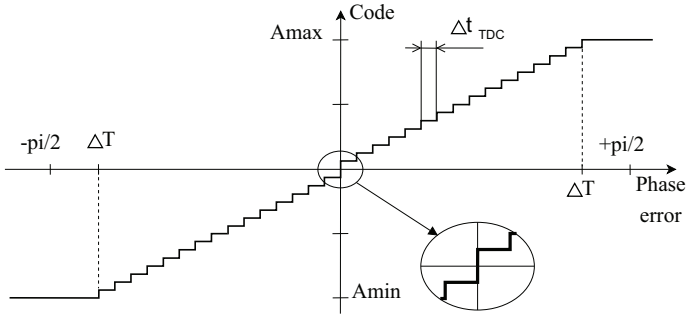


Fig. 2. PFD transfert function.

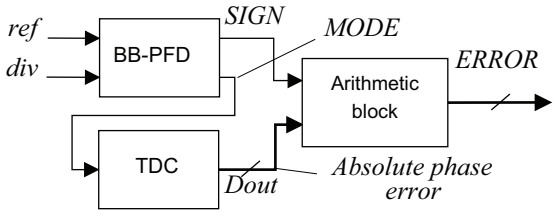


Fig. 3. Topology of the phase-frequency detector.

The state diagram of the BB-PFD containing four possible states is shown in Fig. 4. Here, an event means the arrival of a rising edge of the local (div) or reference (ref) clock since the system is sensitive to the rising edge of signals. In this

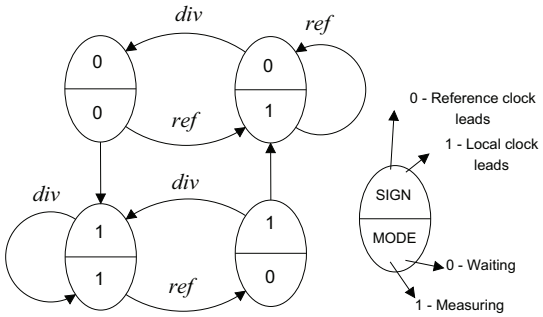


Fig. 4. State diagram of the bang-bang phase-frequency detector.

context, high-level of the $SIGN$ means that ref is leading in the current cycle. In the same way, when the $SIGN$ is in low-level, div is leading. The initial state of the $MODE$ is low-level which means that the BB-PFD is waiting for an event. When at one of the inputs an event is arrived, the $MODE$ switches to high-level and holds this state until an event arrives at the other input. High-level of the $MODE$ is called the measure mode. As a result, the interval in which the $MODE$ is in high-level corresponds to the phase difference between ref and div. It should be noted that the level of the $SIGN$ (defined at the beginning of the measure mode) depends on input which activates the measure mode. The level of the $SIGN$ is stored and is maintained until the next measure cycle.

In the following section the developed VHDL model of each component will be explained.

III. VHDL Model

A. Bang-bang detector

As it is shown in Fig. 5, a BB-PFD contains two input latches (X1 and X2), an arbiter, a save latch (X10) and a reset-logic system (X5-X8). Moreover, the $MODE$ is produced by a XOR gate (X9). The input latches detect the events at the inputs ref and div. The arbiter detect which event comes first, producing 1 or 0 at the Q output. The output latch stores the sign value, while the C-element generates the reset when the both input event were detected *and* the output flip-flop reached a well-defined state. More detailed description of this architecture can be found in [4].

The schematic of the arbiter is shown in Fig. 6. It is a mutual exclusion element including two RS-latches (X3 and X4) and a metastability filter (M1-M4). The metastability filter is used to avoid the propagation of the metastable state from the arbiter to the X10 flip-flop. Such a situation can happen when the input events arrive at the same or close time. In this case the input latches produce two falling edges, leading X3 and X4 to a metastable state. Although in this case the output of X3 and X4 is a value between 0 V and Vdd, the metastability filter

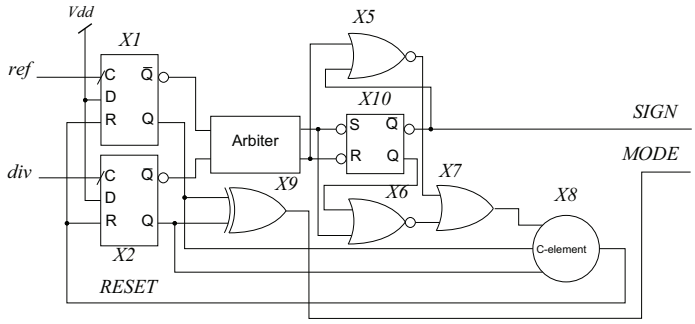


Fig. 5. Schematic of the bang-bang phase-frequency detector.

imposes high-level at outputs until the difference between the outputs of X3 and X4 reaches at least to one NMOS transistor threshold voltage.

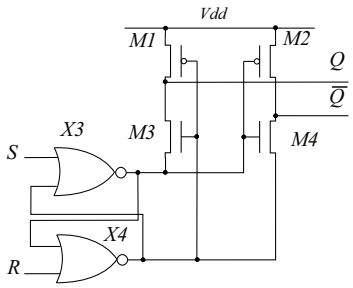


Fig. 6. Schematic of the arbiter.

The reset-logic system is used to initialize the BB-PFD when the $MODE$ switches to low-level. The C-element produces a reset signal when all its inputs have high-level. The reset signal is hold until all of them return to low-level. This is the main advantage of C-element. An alternative circuit, proposed in [5], uses a three-inputs AND gate. In this case, the reset signal changes the level even if one of the inputs change the level. This causes some problems since generally the required time to reset the input latches (X1 and X2) is not the same than that of other latches. Then the BB-PFD may not be correctly initialized.

In the present work, the VHDL model of the BB-PFD is implemented as structural description of the diagram of Fig. 5. The blocks of this diagram are described behaviourally. The arbiter is described as showed Listing 1. The particularity of this block consists in an analog function of metastability resolution achieved by the metastability filter 6. The metastability filter is modeled as an logic inverter, apart in the case when the inputs R and S receive falling edges at the same time. In this case the arbiter outputs a *random* value 0 or 1 (lines 2 and 3 of the Listing 1).

Listing 1. VHDL description of latches of the arbiter. Q and nQ are the latches outputs while R and S are the latches inputs. DELAY is the propagation delay of the arbiter.

```
if   (S = '0') and  (R = '0') and (Q = nQ)  then
        Q <= rnd after DELAY;
        nQ <= not rnd after DELAY;
elsif (S = '0') and (R = '0') then
        Q <= Q after DELAY;
        nQ <= nQ after DELAY;
elsif (S = '1') and (R = '1') then
        Q <= '0' after DELAY;
        nQ <= '0' after DELAY;
elsif S = '1'  then
        Q <= '1' after DELAY;
        nQ <= '0' after DELAY;
elsif R = '1'  then
        nQ <= '1' after DELAY;
        Q <= '0' after DELAY;
end if ;
```

B. TDC

The schematic of the TDC is shown in Fig. 7. As it is shown, the TDC contains a tapped delay line (buffers in series), a register (based on D-latches) and an encoder (CD) [6]. The $MODE$ is delayed by the tapped delay line. With the falling edge of the $MODE$, the thermometer code produced by the tapped delay line is stored in the register. This code is then converted into a non-signed binary code by the encoder. This binary code corresponds to the absolute phase error between div and ref. The VHDL model of the TDC is developed via structural description of circuits.

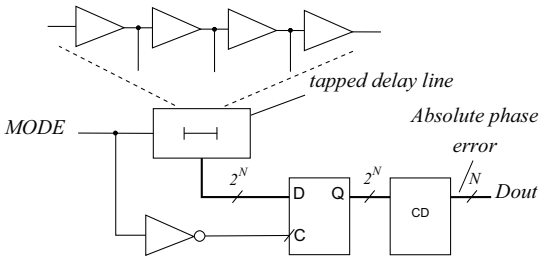


Fig. 7. Schematic of the time to digital converter.

C. Loop Filter

A proportional-integral (PI) filter is used as the loop filter. This digital filter is described as follows:

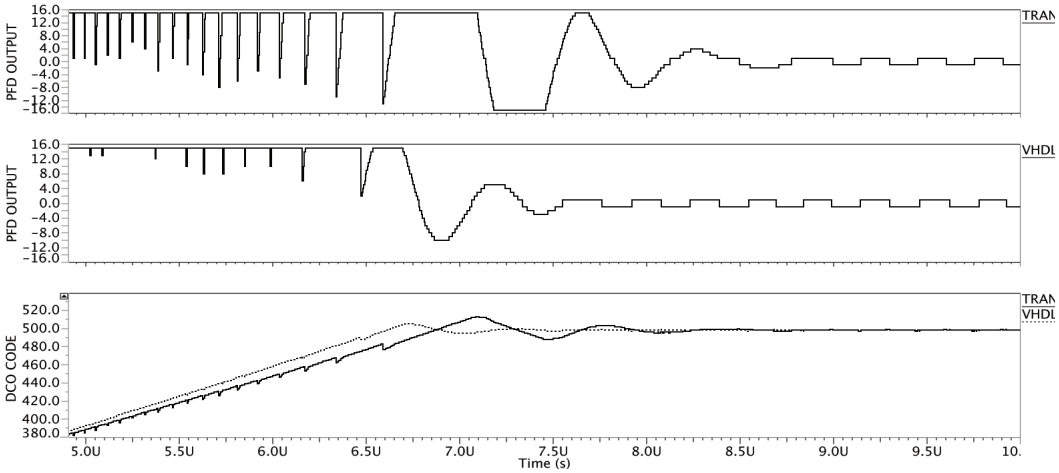
$$H(z) = K_1 + \frac{K_2}{1 - z^{-1}}, \tag{2}$$

where K_1 and K_2 are the gain coefficients of the proportional and the integral paths respectively. The VHDL model of the loop filter is described in behaviourally.

When the PFD is initialized with the $RESET$ signal, the output of the loop filter is also set to the initial value as well as the DCO output frequency. Otherwise, the $ERROR$ is processed by the loop filter.

D. Digitally Controlled Oscillator

Although ring oscillators presents disadvantages in terms of phase noise, power consumption, etc. compared with other types of DCO, it is chosen in this work for the sake of simplicity of the implementation [7]. The frequency of the DCO output can be calculated by:



Simulation parameters: $F_{ref} = 250\ MHz$, $F_{clk} = 1\ GHz$, $M = 4$, $\Delta t_{TDC} = 32\ ps$, $N = 4\ bit$, $DELAY = 30\ ps$, $K = 10\ bit$, $\Delta T_{DCO} = 1\ ps$

Fig. 8. The signed binary code (PFD output) and the control code of the DCO for fully VHDL code and transistor-level implementation.

$$F_{\text{DCO}} = \frac{1}{\Delta T_{DCO} \cdot W}, \tag{3}$$

where ΔT_{DCO} is elementary period of oscillationg tuning step, W is given by:

$$W = 2^{K+1} - \text{DIN}. \tag{4}$$

K is the length of the signed binary code and DIN denotes the signed binary code. The DCO has an analog characteristic. As a result it is impossible to develop an structural description of the DCO. The developed model in this work is then behavioral and is based on (3).

IV. Simulation Results

The signed binary code (PFD output) and the control code of the DCO are shown in Fig. 8 for two models: the presented VHDL model of the ADPLL and the same model in which the PFD is described at the transistor level, using ELDO netlis format (Mentor Graphics). The transistor-level model of the PFD was based on the ST CMOS $65nm$ technology design kit (CORE65LPLVT library). Mentor Graphic ADVance MS simulator was used for the both simulations.

At the start time, the ref is higher than the div since the produced code by the PFD is full-loaded with a positive error (corresponding to 15 at the output). Afterward, during the phase adjusting mode of the ADPLL, the signed binary code produced by the PFD changes between full-loaded states (15 and -16). Although the ADPLL reaches the locked mode in the both models, there is a small (10 %) difference between the required time to reach the locked mode. It is because the fact that the internal delay of transistors are not considered in this VHDL model. With the falling edge of the measure interval, the transistor-level PFD requires some time to reset while the VHDL model does not. As a result, the events (rising edge of the ref or div) which arrives just after the falling edge of the measure interval are not detected.

The simulation time required to obtain the plots in Fig. 8 was several seconds and 50 minutest for pure VHDL-model and mixed VHDL/ELDO model respectively.

V. Conclusion

In order to ease the optimization of distributed clock generators based on networks of the ADPLL, the VHDL model of ADPLL was developed. The practical implementation issues such as limited number of bits, synchronization issues of latches, self-sampling problems, metastability issues, etc. were considered in the developed model. The PFD was also implemented in transistor-level to justify the performance of the VHDL model. The implementation was done in ST CMOS $65nm$ technology. The simulation showed very close result between the pure VHDL model of the whole ADPLL and the mixed model, in which the critical digital PFD block was modeled at the transistor level.

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