Optimal and robust control for a small-area FLL

Carolina Albea-Sanchez, Diego Puschini, Suzanne Lesecq, Edith Beigné

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C. Albea, D. Puschini, S. Lesecq and E. Beigné

***Abstract*—Fine-grain Dynamic Voltage and Frequency Scaling (DVFS) is becoming a requirement for Globally-Asynchronous Locally-Synchronous (GALS) architectures. However, the area overhead of adding voltage and frequency control engines in each voltage and frequency island must be taken into account to optimize the circuit. A small-area fast-reprogrammable Frequency-Locked Loop (FLL) engine is a suited option, since its implementation in 32nm represents $0.0016mm^2$, being 4 to 20 times smaller than classical techniques used such as a Phase-Locked Loop (PLL) in the same technology. Another relevant aspect with respect to the FLL is the control design, which must be suited for low area hardware. In this paper, an analytical model of the system is deduced from accurate Spice simulations. It also takes into account the delay introduced by the sensor. From this model, an optimal and robust control law with a minimum implementation area is developed. The closed-loop system stability is also ensured.**

***Keywords*– Nano systems, FLL, robust control, optimization, disturbance rejection, LMIs.**

I. Introduction

The continuous increase in clock frequency together with technology scaling has generated the distribution of a single global clock over a large digital chip tremendously difficult. A Globally Asynchronous Locally Synchronous (GALS) design alleviates the problem of clock distribution by having multiple clocks, each one being distributed on a small area of the chip. A system with different clock frequency domains appears as a natural enabler for fine-grain power-aware architectures. Actually, power consumption is a limiting factor in VLSI integration, especially for mobile applications. Dynamic Voltage and Frequency Scaling (DVFS) [4] has proven to be highly effective to reduce the power consumption of the chip while meeting the performance requirements [8]. The key idea behind local DVFS is to control at fine grain the supply voltage and the frequency of an island at runtime to minimize the power consumption of the considered island while satisfying the computation/throughput constraints [3].

The DVFS techniques mainly rely on two 'actuators'. These actuators need to be dynamically controlled in order to reduce the power consumption while maintaining the required performance. More precisely, the control policy must be carefully designed in order to achieve high power efficiency at low area cost. The voltage actuator fixes the supply voltage of the Voltage and Frequency Island (VFI). It can be a classical buck converter [9] or a discrete Vdd-hopping converter [1, 10]. On the other side, the frequency actuator is a Clock Generator. Its frequency control is related to the supply voltage control in order to avoid timing faults [14]. This Clock Generator is classically based on a Phase Locked Loop (PLL) or a Frequency Locked Loop (FLL).

Another consequence of technology scaling is the in-die and die-to-die process variability (P-variability). From a practical viewpoint, it is becoming increasingly difficult to manufacture integrated circuits with tight parametric values [10]. As a consequence, in-die process variation means that the optimum functional and energetic point of the whole circuit can be found if VFI number i has its functioning frequency in the range $[F_{min,i}, F_{max,i}]$ [13]. If the clock is generated for the whole circuit, and distributed in each VFI, the maximum acceptable frequency (i.e. the one that will ensure no timing fault for any VFI) will be $F_{max,i} = \min\{F_{max,i} \quad \forall i\}$, leading to a suboptimal circuit functioning, some VFI being underclocked. Therefore, in order to obtain the best possible circuit performance, the clock must be locally generated and controlled according to Process, Voltage and Temperature (PVT) variations. Recently, control techniques have been applied to the problem of DVFS (for instance, see [1, 2]). However, these works address the closed-loop control of the voltage actuator, this latter implementing a Vdd-hopping technique.

In the context of the industrial French project LoCoMoTiV[1] circuit, an FLL is selected as second actuator due to the area constraint: in a fine-grain GALS context, the FLL can indeed be replicated in each VFI of the size of a processor in a many-core architecture. The FLL has been implemented in a $32nm$ STMicrolectronics technology. The layout presented in Fig. 1 is fully compatible with the standard cell methodology, to be easily integrated at GALS System on Chip (SoC) level. Its area is about $0.0016mm^2$; it is 4 to 20 times smaller than a classical PLL in the same technology.

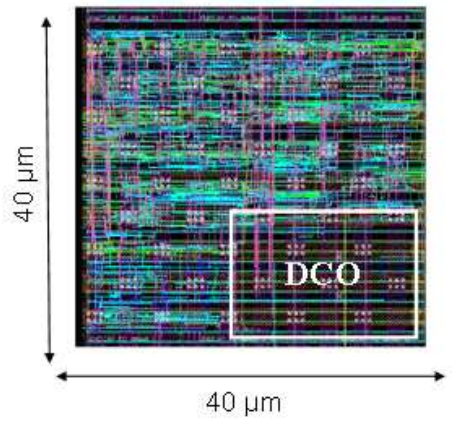

Fig. 1: FLL layout.

CEA LETI-MINATEC Campus, 17 rue des Martyrs, 38000 Grenoble, France. carolina.albea-sanchez, diego.puschini, suzanne.lesecq, edith.beigne@cea.fr

[1]Local Compensation of Modern Technology Induced Variability (LoCoMoTiV) is a CEA-Leti Minatec Project

The main objective of this paper is to design a control law for the FLL (see Fig.2) taking into account the following objectives:

- closed-loop stability;
- robustness with respect to PVT variations;
- suited performance (no overshoot, no static error, short transient period);
- low area cost and
- exogenous disturbance rejection.

Therefore, the designed controller must not only guaranty the set-point stabilization, but also other criterions.

From accurate Spice simulations, it has been seen that the DCO can be modeled with a linear model. Moreover, the sensor introduces a delay that must be taken into account and it is remarked that the system characteristic can change due to PVT effects.

A simple integral controller that requires a minimum implementation area is proposed for this system. For the tuning of the control gain, a robust and optimal control problem is formulated, for which a functional must be minimized. In order to solve this problem some Linear Matrix Inequalities (LMIs) are defined. Satisfying these LMIs within the optimal problem, all objectives above are fulfilled by the closed-loop system. Consequently, an optimal and robust control law for the FLL is reached.

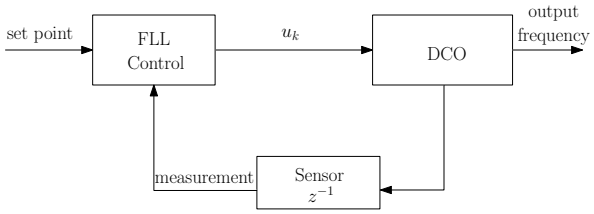

Fig. 2: FLL block diagram.

Some simulations under the Matlab/Simulink environment show the powerfulness of the proposed controller. Moreover, the closed-loop system was implemented in RTL, obtaining similar simulation results to the ones obtained by Matlab/Simulink. The resulting layout (shown in Fig. 1) was implemented in the LoCoMoTiV circuit in CMOS 32nm.

The rest of this paper is organized as follows: in Section II, the circuit model of the FLL is presented as well as their properties and the error equation. An optimal and robust problem formulation is stated in Section III. Likewise, in Section IV, this problem is solved by providing an approach to tune the control gain. In Section V, the control gain is computed, being tested and implemented in Section VI. The paper ends with conclusions and future work.

Notation. For a given $\mathcal{S}$, the notation $\mathcal{C}o(\mathcal{S})$ denotes the convex hull of the set $\mathcal{S}$. $\Delta\eta \triangleq \eta^+ - \eta^-$, where η^+ and η^- respectively are $\eta(k+1)$ and $\eta(k)$, i.e., the value of η in two consecutive sampling times. Finally, $\mathcal{L}_2$ is the space of $\{x_k\}$ with the norm: $\|x_k\|_2^2 \triangleq \sum_{k=0}^{\infty} x_k^T x_k < \infty$.

II. FLL CONCEPT

The main blocks of a FLL are modeled through design considerations and accurate simulations. The main blocks are a Digitally-Controlled Oscillator (DCO) that provides a frequency, a sensor (i.e. a counter) to measure this frequency and a controller that contains a frequency comparator between the targeted frequency and the output frequency and some 'intelligent controller'. In Fig. 3, a sketch of the FLL is shown.

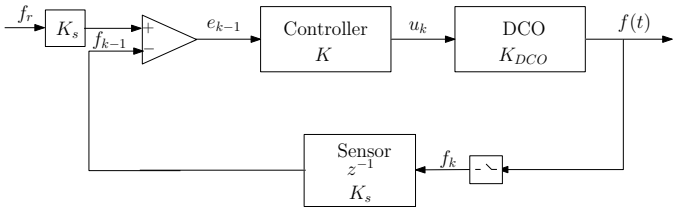

Fig. 3: FLL architecture.

Digitally-Controlled Oscillator. In order to obtain a DCO model some accurate simulations were performed in Spice. Figure 4 shows the frequency characteristics of the post-layout DCO (with extracted R & C parasitcs) in function of the input 8-bits binary word. The Y-axis corresponds to the measured raw frequency: this frequency must be divided by 2 to obtain a usable clock frequency with a 50% duty ratio. The 'nominal' case (curve in the middle) is measured at 25^oC with a $1.1V$ supply voltage. The 'best' case (top curve) is obtained with best case parasitic extract (minimum R, minimum C), 'FastFast' transistors, a supply voltage of $1.2V$ and a temperature of 125^oC. The 'worst' case simulation is performed with worst case parasitic extract (maximum R, maximum C), 'SlowSlow' transistors, at $1.0V$ supply voltage and a temperature of 0^oC.

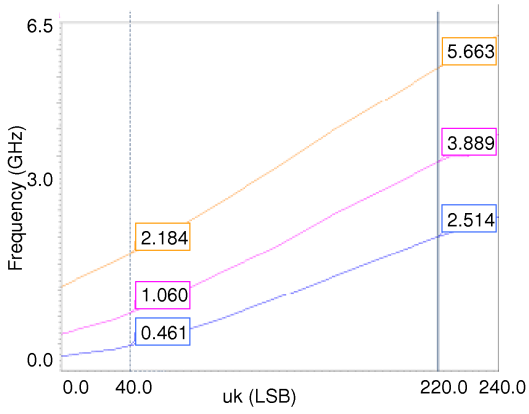

Fig. 4: DCO characteristics (measured raw frequency vs. input word)

From accurate Spice simulations, it can be assumed that the DCO has a linear model, that evolves with respect to Process variation but also to Temperature and Voltage changes (PVT) over time.

The DCO model is

$$f_k = b + K_{DCO}u_k + B_w w_k$$

$f_k \in \mathbb{R}^1$ is the analog frequency output, $u_k \in \mathbb{N}$ is coded over 8 bits between 0 and 255, respectively. b is the DC-offset, K_{DCO} is a gain. w_k is an energy-bounded signal to take account any disturbance, and B_w is a constant that defines the disturbance magnitude. In order to take into account the PVT variation effects, it is assumed that parameters K_{DCO}, b and B_w can change in the interval

- $K_{DCO} \in [K^m_{DCO}, K^M_{DCO}]$,
- $B_w \in [B^m_w, B^M_w]$,
- $b \in [b^m, b^M]$.

Sensor. The sensor, which is a counter, measures the DCO output frequency. This sensor introduces a delay of one-sampling period. The delay is present in the feedback loop

$$M_k \triangleq K_s f_{k-1}.$$

Control. Define $e_k \triangleq K_s f_r - f_k$, where f_r is the signal reference and K_s is a positive constant that represents the sensor gain. Then, the error equation is

$$e_k = -b - K_{DCO}u_k - B_w w_k + K_s f_r. \tag{1}$$

In order to limit the Silicon area and taking into account the control objectives given above, a simple digital integral controller is defined

$$u_k = u_{k-1} + K(K_s f_r - M_k) = u_{k-1} + KK_s e_{k-1} \tag{2}$$

where K is a the controller constant gain to be tuned.

From Eq. (1), it follows

$$u_{k-1} = \frac{-e_{k-1} - b - B_w w_{k-1} + K_s f_r}{K_{DCO}}$$

which gives the closed-loop system

$$e_k = e_{k-1} - K_{DCO}K_s K e_{k-1} + B_w w_{k-1} - B_w w_k$$

This can be rewritten in the following linear form:

$$e_{k+1} = Ae_k + B\bar{u}_{k+1} + B_w w_k - B_w w_{k+1}, \tag{3}$$

where

$$A = 1, \quad B = -K_{DCO}K_s$$

and

$$\bar{u}_{k+1} = Ke_k. \tag{4}$$

Note that b does not change the system response.

III. Problem statement

Equation (3) can be rewritten in the following explicit closed-loop form, in such a way that a H_∞ problem can be formulated:

$$\begin{aligned} e_{k+1} &= Ae_k + BKe_k + B_w w_k - B_w w_{k+1}, & (5)\\ z_{k+1} &= e_{k+1}. & (6)\end{aligned}$$

Problem 1: The problem is to find the optimal gain K, such that the control law (2) is robust and the system response is the shortest possible without overshooting. Besides, there exists a Lyapunov functional $V_k > 0$, such that $V_{k+1} - V_k$ along the solution of (5) fulfills

$$V_{k+1} - V_k < 0, \tag{7}$$

and for any disturbance input, there exists a minimum disturbance attenuation $\gamma^* \geq 0$, such that, for all $\gamma \geq \gamma^*$, the $\mathcal{L}_2$ gain between the disturbance vectors w_k and w_{k+1}, and the output vector z_{k+1} is less or equal to γ, i.e.

$$\|z_{k+1}\|_2^2 - \gamma^2(\|w_k\|_2^2 + \|w_{k+1}\|_2^2) < 0, \quad \forall w_k, w_{k+1} \in \mathcal{L}_2. \tag{8}$$

The solution to this problem guarantees a suited performance as well as a robust stability and robust disturbance rejection for system (5)–(6).

IV. Optimal H_∞ control design

In order to cope with Problem 1 a mathematical manipulation of Eq. (5) is performed via a variable change. This allows obtaining feasible LMIs for a robustness problem [7].

A. Model transformation

Consider

$$y_k \triangleq e_{k+1} - e_k.$$

Then, Eq. (5) is rewritten in the form [5]:

$$\begin{bmatrix} e_{k+1} \\ 0 \end{bmatrix} = \begin{bmatrix} y_k + e_k \\ -y_k + Ae_k - e_k + BKe_k + B_w w_k - B_w w_{k+1} \end{bmatrix}.$$

This system can be compactly written as:

$$E\bar{e}_{k+1} = \bar{A}\bar{e}_k + \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k - \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_{k+1},$$

where

$$\bar{A} \triangleq \begin{bmatrix} 1 & 1 \\ A + BK - 1 & -1 \end{bmatrix},$$
$$E \triangleq \text{diag}\{1, 0\}, \quad \bar{e}_k \triangleq \begin{bmatrix} e_k \\ y_k \end{bmatrix}.$$

B. Control design

Problem 1 can be formulated in terms of Linear Matrix Inequalties (LMIs) [6].

Assumption 1: There exists a Lyapunov function V_k, with condition (7) and a γ, such that,

$$V_{k+1} - V_k + z_{k+1}^T z_{k+1} - \gamma^2(w_k^T w_k + w_{k+1}^T w_{k+1}) \leq \zeta^T \Gamma \zeta < 0. \tag{9}$$

where $\zeta \triangleq [\bar{e}_k \quad w_k \quad w_{k+1}]^T$ is an augmented state vector and $\Gamma \in \mathbb{R}^{4\times 4}$ is a symmetric matrix.

V_k is defined by the Lyapunov function

$$V_k = \bar{e}_k^T EPE\bar{e}_k, \tag{10}$$

where $P \triangleq \begin{bmatrix} P_1 & P_2 \\ P_2^T & 0 \end{bmatrix}$, being $P \in \mathbb{R}^{2\times 2}$, $P_2 \neq 0$ and $P_1 > 0$.

Next, a sufficient condition for asymptotic stability and disturbance rejection is derived.

Theorem 1: Consider system (5)–(6) with $K \in \mathbb{R}^{1\times 1}$ and energy-bounded w_k and w_{k+1}. If the following LMIs are satisfied:

$$P_1 > 0 \tag{11}$$
$$\Gamma < 0 \tag{12}$$

where Γ is defined in Eq. (13) found at the top of the next page, then the equilibrium of the closed-loop system (5)–(6) is asymptotically stable and there exists a value γ^*, such that for $\gamma < \gamma^*$ condition (8) is fulfilled.

Proof: The goal is to satisfy $V_{k+1} - V_k + z_{k+1}^T z_{k+1} - \gamma^2({w_k}^T w_k + {w_{k+1}}^T w_{k+1} < 0)$ for both disturbance rejection and asymptotic stability of the equilibrium for system (5)–(6).

Lyapunov method yields:

$$\begin{aligned}
&V_{k+1} - V_k = \bar{e}_{k+1}^T EPE\bar{e}_{k+1} - \bar{e}_k^T EPE\bar{e}_k \\
&= \left\{\bar{e}_k^T \bar{A}^T + w_k[0 \quad B_w^T] - w_{k+1}[0 \quad B_w^T]\right\} \times P \\
&\times \left\{\bar{A}\bar{e}_k + \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k - \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_{k+1}\right\} - \bar{e}_k^T EPE\bar{e}_k \\
&= \bar{e}_k^T[\bar{A}^T P\bar{A} - EPE]\bar{e}_k \\
&+\bar{e}_k^T \bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_k - \bar{e}_k^T \bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} w_{k+1} \\
&+w_k[0 \quad B_w^T]P\bar{A}\bar{e}_k - w_{k+1}[0 \quad B_w^T]P\bar{A}\bar{e}_k,
\end{aligned}$$

This developed expression is applied to inequality (9), in such a way that the LMI (13) is obtained. ■

C. Robust control

Now, the uncertain parameters given in Section II are taken into account in order to guarantee the system robustness, at the same time that the closed-loop stability as well as disturbance rejection for the FLL system are also ensured. This means that a robust control under parameter uncertainties is designed For this reason, Theorem 1 is extended in the case of polytopic uncertainties.

Denote

$$\Omega \triangleq [BK \quad B_w]$$

and assume that $\Omega \in Co\{\Omega_j, \quad j = 1, 2, 3, 4\}$ namely

$$\Omega = \sum_{j=1}^{n} \lambda_j \Omega_j, \quad \text{for some,} \quad 0 \le \lambda_j \le 1, \quad \sum_{j=1}^{n} \lambda_j = 1$$

being the vertices of the polytope described by $\Omega_j = [B^{(j)}K \quad B_w^{(j)}]$ for $j = 1, 2, 3, 4$.

Pre- and post-multiplying the LMI (13) by $Q = \text{diag}\{Q_1, Q_1, 1, 1\}$ and taking $Q_1 = P_2^{-1} > 0$ and $\bar{P}_1 = Q_1 P_1 Q_1$, the following sufficient condition is achieved.

Theorem 2: Consider system (5)–(6) with energy-bounded w_k and w_{k+1}, and $K \in \mathbb{R}^{1\times 1}$. If there exist $T \in \mathbb{R}^{1\times 1}$ and $Q_1 \in \mathbb{R}^{1\times 1}$ with $K = TQ_1^{-1}$ and $\in \mathbb{R}^{1\times 1}$ such that

$$\bar{P}_1 > 0$$
$$\bar{\Gamma}^{(j)} = \begin{bmatrix} \bar{\Gamma}_1^{(j)} & \bar{\Gamma}_2^{(j)} & B_w^{(j)}Q_1 & -B_w^{(j)}Q_1 \\ * & \bar{P}_1 - 2Q_1 & B_w^{(j)}Q_1 & -B_w^{(j)}Q_1 \\ * & * & -\gamma^2 & 0 \\ * & * & * & -\gamma^2 \end{bmatrix} < 0,$$

where

$$\begin{aligned}
\bar{\Gamma}_1^{(j)} &\triangleq 2Q_1(A-1) + 2B^{(j)}T + 1 \\
\bar{\Gamma}_2^{(j)} &\triangleq \bar{P}_1 + Q_1 A - 2Q_1 + TB^{(j)}, \quad j = 1, 2, 3, 4,
\end{aligned}$$

then, in the vertices j, the equilibrium is asymptotically stable as well as the disturbances are rejected in the entire polytope.

Proof: This is an extension of Theorem 1 for polytopic uncertainties with some mathematical manipulations. Therefore, this theorem proof is straightforward. ■

D. Optimal and robust control

In order to satisfy all items of Problem 1, some assumptions are performed.

Assumption 2: For $w_k \equiv 0$ and $w_{k+1} \equiv 0$, the poles of the closed-loop system (5) are

$$Z = 1 + BK.$$

If $Z > 0$ is chosen, overshoots are avoided. In addition, if K is maximized, the response time is the shortest possible one [12]. Remind the control structure (2).

Assumption 3: There exists a functional cost

$$J \triangleq \|u_{k+1}\|_2^2 + \|z_{k+1}\|_2^2 - \gamma^2(\|w_k\|_2^2 + \|w_{k+1}\|_2^2) \tag{14}$$

The first term on the right hand side quantifies the response time. Likewise, the other terms (on the right hand side) quantify the disturbance attenuation.

Lemma 1: Suppose that Assumptions 1, 2 and 3 are fulfilled and $\bar{Z}^{(i)} \triangleq Q_1^T Z^{(i)} Q_1$. Then the optimal controller gain K for Problem 1 can be found by:

Minimize $-J$

subject to:

$$\begin{aligned}
&\bar{\Gamma}^{(j)} < 0 \quad j = 1, 2, 3, 4. \\
&\bar{Z}^{(i)} > 0 \quad i = 1, 2
\end{aligned}$$

where $\bar{Z}^{(i)} = Q_1 + B^{(i)} \quad i = 1, 2$.

Proof: The optimal Problem 1 is solved by Lemma 1 if condition (8) is fulfilled [11].

For $w_k \neq 0$ and $w_{k+1} \neq 0$ and under zero initial conditions

$$V_{k+1} - V_k \le -z_{k+1}^T z_{k+1} + \gamma^2(w_k^T w_k + w_{k+1}^T w_{k+1}).$$

The summation of both sides is

$$V_{k+1} - V_0 \le -\sum_{k=0}^{k} z_{k+1}^T z_{k+1} + \gamma^2 \sum_{k=0}^{k} w_k^T w_k + \gamma^2 \sum_{k=0}^{k} w_{k+1}^T w_{k+1}.$$

For $k \to \infty$, under the zero initial condition $V_0 = 0$ and the positive definitiveness of the Lyapunov function, it is proved

$$\begin{aligned}
&\sum_{k=0}^{\infty} z_{k+1}^T z_{k+1} \le \gamma^2 \sum_{k=0}^{\infty} w_k^T w_k + \gamma^2 \sum_{k=0}^{\infty} w_{k+1}^T w_{k+1} \\
&\|z_{k+1}\|_2^2 \le \gamma^2(\|w_k\|_2^2 + \|w_{k+1}\|_2^2).
\end{aligned}$$

■

Corollary 1: The optimal gain K obtained applying Lemma 1 guaranties both robust stability and robust disturbance rejection. It also provides a short transient period without overshoots.

$$\Gamma \triangleq \begin{bmatrix} \bar{A}^T P \bar{A} - EPE + \text{diag}\{1, 0\} & \bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} & -\bar{A}^T P \begin{bmatrix} 0 \\ B_w \end{bmatrix} \\ * & -\gamma^2 & 0 \\ * & * & -\gamma^2 \end{bmatrix} < 0, \tag{13}$$

V. Optimal robust control result

In this section, an optimal and robust control is computed for the FLL by employing the approach presented above.

Digitally-Controlled Oscillator. The DCO parameters can change within the following intervals:

$$K_{DCO} \in [10, \quad 30] \cdot 10^{-3} GHz/LSB$$

The disturbance parameter is given by

$$B_w \in [0.1, \quad 0.4]$$

Sensor. The maximum frequency at the input of the sensor is supposed equal to $5GHz$ and $K_s = 85$ (LSB/GHZ).

The optimal control problem (Problem 1) is solved, dealing to

$$K = 0.392, \tag{15}$$

together with $\gamma = 1.8$ and $P_1 = 0.2663$.

VI. Simulation and implementation Results

In this section, some simulations in the Matlab environment show the robustness of the control law proposed for the FLL. For these simulations, the data above are reported and a sampling period of $60ns$ is taken.

Remind that the FLL characteristic curve can change due to PVT variations as shown in Fig. 4. In order to validate the system robustness with respect these changes, three different models are considered (see Fig. 5):

syst 1: $K_{DCO} = 19.83 \cdot 10^{-3} \frac{GHz}{LSB}$, $b = -0.0315GHz$,
syst 2: $K_{DCO} = 14.25 \cdot 10^{-3} \frac{GHz}{LSB}$, $b = 4.5785GHz$,
syst 3: $K_{DCO} = 25.50 \cdot 10^{-3} \frac{GHz}{LSB}$, $b = 2.0785GHz$.

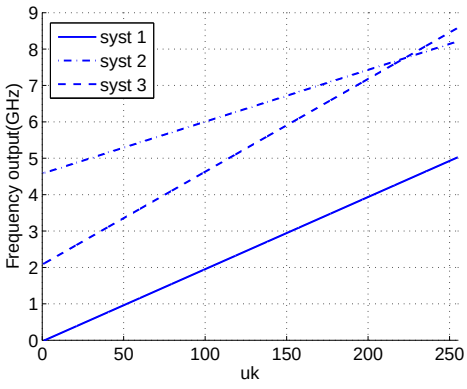

Fig. 5: Variation of the characteristic curves.

Figure 6 shows the closed-loop response of 'syst 1', 'syst 2' and 'syst 3' to a change in the reference frequency, f_r. These tests show that the equilibrium is robust with respect to the uncertainty in the characteristic curve. Note that the response time at 5% is achieved before the 7^{th} sampling time. Figure 7 shows the frequency output, when the characteristic

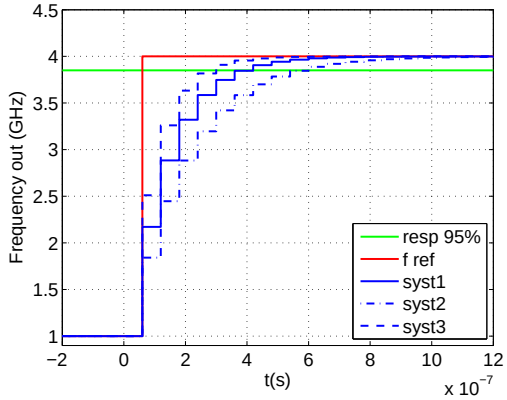

Fig. 6: Evolution of the output frequency for three different systems (blue), reference frequency (red) and response time at 5% (green).

curve changes ('syst 1', 'syst 2' and 'syst 3') and when there is some exogenous disturbances in the output of the system. This example shows the great robustness of the system when the optimal robust control tuning is employed.

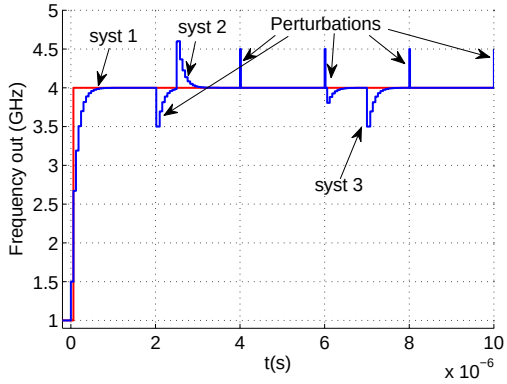

Fig. 7: Evolution of the output frequency with disturbance and for three different systems.

The FLL with the controller was implemented in VHDL, obtaining the layout shown in Fig. 1. The signal evolutions are presented in Fig. 8. Note that u_k presents a delay with respect to f_r, this is due to asynchronous issues of the chip, and it is not relevant in the closed-loop system. The delay presented by the sensor is seen in f_{k-1}. The system response is consistent with Fig. 6, and the real output, f, is also reported.

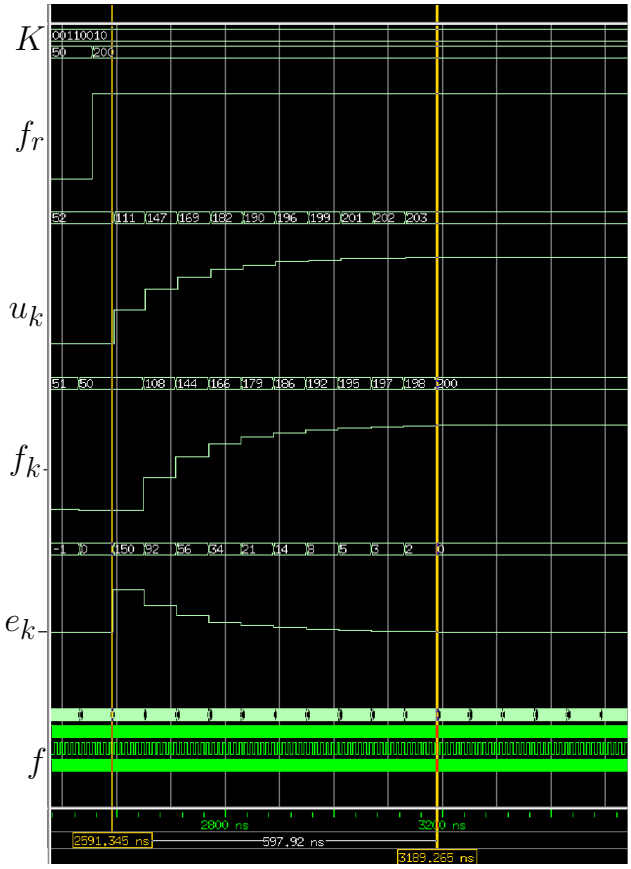

Fig. 8: VHDL Simulation of syst 1.

VII. Conclusion

In this paper, a small-area Frequency-Locked Loop (FLL) engine is employed to implement a DVFS in GALS architecture. The use of a simple control law has allowed a fully digital implementation in standard cells, attaining a small area. Implemented in a $32nm$ technology, the proposed design represents $0.0016mm^2$, i.e. from 4 to 20 times smaller than classical techniques used such as a Phase-Locked Loop (PLL) in the same technology. Likewise, this control law is optimal with respect to system performance (short transient period and no overshoot) and disturbance attenuation. Another suited property offered by the control law is the robustness with respect to PVT variations. In addition, the closed-loop system stability is guaranteed. Some simulations under Matlab show the closed-loop system robustness. Likewise, the FLL with the controller was implemented in VHDL in order to obtain the implementation layout.

First version of the FLL (included the control law proposed in this paper) has been implemented in a 32nm technology. The circuit is currently under founder and performance attained on the real chip will be show during the oral presentation.

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