ULP Variability-insensitive SRAM design in sub-32nm UTBB FDSOI CMOS

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1. Abstract

This paper describes a design approach based on optimization of embedded SRAMs that takes advantage of an Ultra-Thin Body and Box (UTBB) Fully-Depleted (FD) SOI CMOS process. Optimization is performed on an analytical model including statistical variations for Static Noise Margin (SNM) of CMOS SRAMs operating in subthreshold. Distributions of retention and read SNM are derived as a function of V_{TN} and V_{TP}. Improvements of up to 2x of the retention- and read-mode SNM μ/σ are obtained by optimizing the V_{TN}/V_{TP} ratio with back bias.

2. Introduction

In today's systems-on-a-chip (SOC) very often most of the chip area is taken by embedded SRAM, which leads in some cases to the leakage power to dominate the overall power consumption. Therefore, for low-power design, suppressing leakage current becomes crucial. The solution adopted in this work to the leakage problem is sub-threshold operation; this solution is particularly attractive, as lowering supply voltage does not only reduce the leakage in retention, but also reduces dynamic power consumption in active mode. Previous work on this subject was presented in [1], where a model for sub-threshold SNM evaluation for 45nm CMOS is presented and in [2], where it is extended for the purpose of evaluating optimum SRAM operation conditions in read and retention modes. In this work sub-threshold variability-resistant SRAM design is investigated further by taking advantage of an UTBB FDSOI process [3] with reduced-parameter variability and increased body factor. The stability of large SRAM arrays is characterized taking into account the statistical variations of device parameters, evaluating the optimum V_T ratios for best yield and the backgate bias to achieve this optimum.

3. UTBB FDSOI

The UTBB-FDSOI device [3] (Fig.1) consists of an undoped Silicon thin film on a thin Buried Oxide (BOX) layer of thickness T_{BOX} ($10nm<T_{BOX}<30nm$) covering a highly doped Back Plane (BP) (Fig.1). Reducing the BOX thickness and doping the BP (i) boosts the channel electrostatic control (ii) gives the possibility of obtaining a V_T modulation by applying different kind of BP doping using a single gate stack work function and (iii) results in a very high body factor for V_T adjustment, reaching more than 100mV/V for T_{BOX} = 10 nm.
Dopant variations are the most important factor in process variations in CMOS bulk devices. Since in this technology the thin film is undoped and the V_T is modified through the application of a different BP and/or body bias, the standard deviation σ_{VT} is expected to be almost half that of typical bulk with an A_{VT} below 1.4mVμm [4]. An additional feature is the availability of multiple V_Ts, such as high-V_T (HVT), standard-V_T (SVT) and low-V_T (LVT).

4. Static Noise margin

Static noise margin (SNM) is the key parameter for SRAM cells and was first introduced in [5]. It can be described as the biggest value of noise voltage between both inverters in a 6T memory cell (Fig. 2), for which the cell can still retain its data, graphically represented in Fig. 3 as the largest square that can fit between the "butterfly curves"; these are obtained from a direct and an inverse voltage-transfer curve (VTC) of each cell inverter. The VTCs that go between V_{DD} and 0 represent the cell in retention, and the other two VTCs are for the cell in read mode (access transistors are included).
The SNM model is implemented in Matlab and applied to optimize yield by maximizing the $\mu/6\sigma$ of the SNM in the presence of local V_T variation of $\pm 3\sigma$.

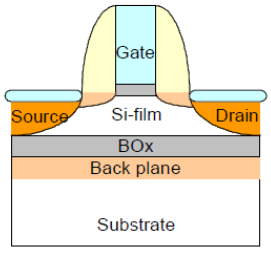

Fig.1 *UTBB-FDSOI transistor cross section*

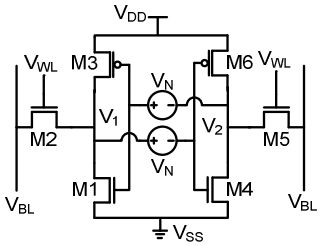

Fig.2 *SRAM cell with noise sources for SNM evaluation*

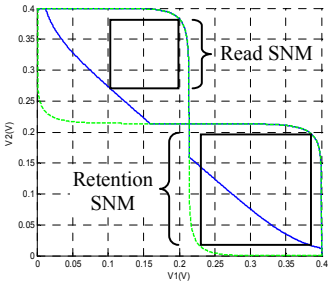

Fig.3 *Butterfly curves for read and retention operation obtained from Matlab*

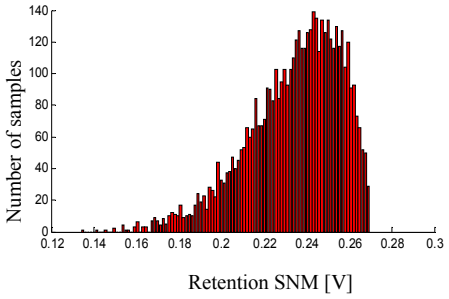

Fig.4 *Histogram representing retention SNM distribution*

5. Statistical Variation and Cell Optimization

Ideally, the SRAM array should meet the 6σ criterion, meaning that for any given process parameter variation, the mean of the SNM distribution divided by the standard deviation should be higher than 6. The focus of the analysis performed in this work is to increase the stability of a large SRAM-cell array by applying global and local parameter tolerances to the MOS transistor, and maximizing the ratio mean(μ)/σ of the derived SNM distribution by various techniques. V_{DD} can also be minimized when optimum operating conditions of the SRAM array are achieved by adjusting the V_T to the desired value using backgate bias.

A histogram of the SNM in retention for V_{DD}=0.6V, and NMOS and PMOS transistors with equal nominal $|V_{T0}|$ is plotted in Fig. 4. The SNM value and distribution depend on the V_{TN}/V_{TP} ratio. The shape of this plot can be explained by the fact that in retention mode having NMOS and PMOS transistors with the same $|V_{T0}|$, yields close to optimal SNM. Therefore, when random variation is applied, some samples will reach the highest possible SNM value (270mV vs. $V_{DD}/2$=300mV), hence the shape of the distribution is tilted towards these maximum SNMs (see Fig. 4). Fig. 5 and Fig. 6 show the μ/σ distributions of retention SNM at V_{DD}=0.3, and read SNM at V_{DD}=0.5, respectively, for various V_T values. It can be seen, that the optimum values of the N and PMOS V_Ts differ between the two plots requiring a compromise between best V_{TN}/V_{TP} ratios in retention and read, slightly below 1 and above 1.5, respectively.

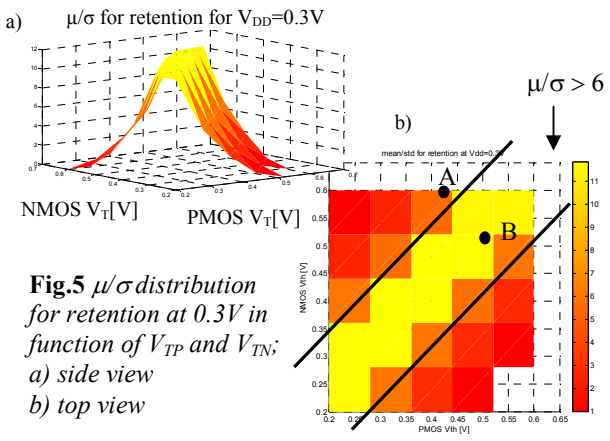

Fig.5 *μ/σ distribution for retention at 0.3V in function of V_{TP} and V_{TN}; a) side view b) top view*

Due to its high body factor and low A_{VT}, UTBB-FDSOI allows a wide range of V_T adjustment that can lead to an optimum. For the purpose of this analysis, we assume the UTBB-FDSOI transistor parameters from [3], where in a high-V_T configuration V_{TP}=-427mV and V_{TN}=604mV. These values correspond to point A in Figs.5.b and 6.b. The position of this point shows that the retention μ/σ is less than 6; however, by applying body bias to both transistors we can modify both V_Ts in the range of 100mV and can obtain a V_T ratio corresponding to point B, where μ/σ is almost 12 (2x stability gain). The initial V_T ratio (point A in Fig. 5 and 6) is almost optimal for read mode, but even higher stability and also faster read operation due to lower V_{TN} values, can be achieved by shifting V_T values to point C (see Fig. 6).

6. Conclusions

Due to a high body factor of UTBB-FDSOI it is possible to obtain up to 2x increase of μ/σ for retention and read. Appropriate body bias in each operation mode also allows setting a lower V_{DD} and can be adjusted on a post-processing basis. Analyzing the results one can notice, that the lines representing the crests of the 3D SNM plots are parallel, and a shift of $|V_{TP}|$ and V_{TN} by the same amount will not cause a change of μ/σ, as their ratio stays the same. Figs. 5 and 6, and the relations between points A, B and C, show that in order to provide the optimum stability in both read and retention operations the right value of the V_T ratio needs to be set.

References

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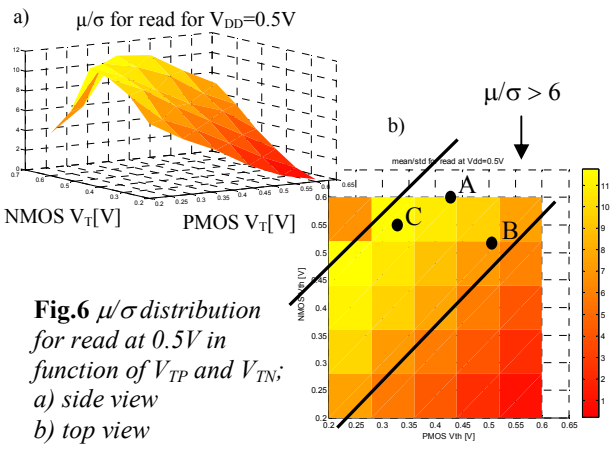

Fig.6 *μ/σ distribution for read at 0.5V in function of V_{TP} and V_{TN}; a) side view b) top view*