Stability oriented SRAM performance optimization in subthreshold operation

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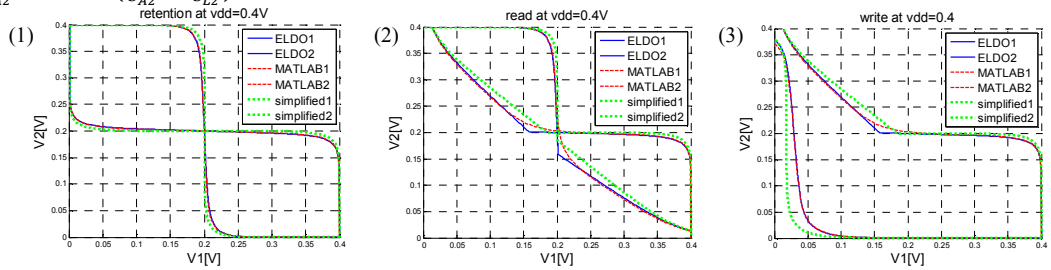
In this work we are analyzing the 6T SRAM cell operation in subthreshold using the 32nm UTBB-FDSOI [1] technology. As a first step an analytical model is developed allowing an accurate estimation of Static Noise Margin (SNM) [2] in all operation modes. The basic equations for retention and read were presented in [3]. Here, we include the DIBL, body factor and all cell voltages as parameters and demonstrate the equation for write SNM. Figs. 1-3, show an excellent correlation with SPICE simulation results, especially as compared to the simplified model as in [3]. Thus, it becomes possible to perform a complete static analysis of SRAM stability based only on a few technology parameters (DIBL, subthreshold slope, threshold voltages, body factor), which are easily extractible either from the model or silicon measurements. The optimum tradeoffs between cell transistors V_Ts for best stability in subthreshold for read and retention are presented in Fig.4,5 and are consistent with [4]. Fig.6 extends the analysis to write SNM. Due to the high steepness of write stability plot, ensuring proper operation in this mode becomes the main limitation for aggressive V_{DD} scaling (Fig.6). It should be mentioned however, that as the analysis is based on subthreshold equations, the write stability in Fig.6 for V_{TN}<0.4V is underestimated. Fig.7 depicts the influence of typical write assist techniques (under driving the bitline, modifying wordline voltage and increasing V_{SS}) on the read and write stability (for A_{VT}=1.1mVμm) for V_Ts optimized for top retention stability (V_{TN}=451mV, V_{TP}=412mV). It can be noted, that setting V_{BL}=-0.1V (write bitline voltage) gives the write μ/σ=5.66, while maintaining read μ/σ>9. As presented in Fig.7, the balance between these values can be further adjusted by increasing either V_{SS} or V_{WL}.Fig.8 depicts results of the same analysis for another V_T set, for which the read μ/σ=6 (V_{TN}=451mV, V_{TP}=528mV).

$$V_1 = -\frac{S_{D1}}{\ln 10}\left(\ln\frac{I_{D1}}{I_{A1}} + ln\left(\frac{1-\exp\left(\frac{V_{SS}-V_2}{V_{th}}\right)}{1-\exp\left(\frac{V_2-V_{BL}}{V_{th}}\right)}\right)\right) - V_2\frac{S_{D1}+S_{A1}\eta_{D1}+S_{D1}\eta_{A1}+\gamma_{A1}\eta_{D1}}{S_{A1}} + V_{WL}\frac{S_{D1}}{S_{A1}} + V_{BL}\frac{S_{D1}}{S_{A1}}\eta_{A1} + V_{SS}(1+\eta_{D1}+\gamma_{D1}) +$$
$$V_{BN}\frac{S_{D1}\gamma_{A1}-S_{A1}\gamma_{D1}}{S_{A1}} + S_{D1}\left(\frac{V_{TD1}}{S_{D1}} - \frac{V_{TA1}}{S_{A1}}\right)$$

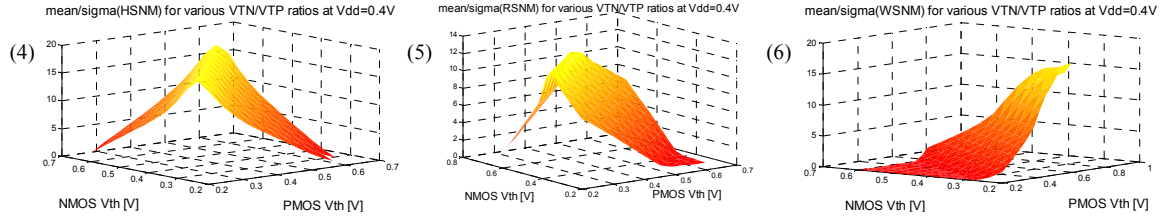
Eq.1 Read mode equation (D,A,L- Driver, Acces and Load transistors respectively; indexes 1 and 2 correspond to left and right half cells; η- DIBL; γ- body factor; I- transistor current for V_{GS}=V_T)

$$V_1 = \frac{S_{L2}}{\ln 10}\left(\ln\frac{I_{L2}}{I_{A2}} + ln\left(\frac{1-\exp\left(\frac{V_2-V_{DD}}{V_{th}}\right)}{1-\exp\left(\frac{V_{BBL}-V_2}{V_{th}}\right)}\right)\right) - V_2\frac{S_{L2}\eta_{A2}-S_{A2}\eta_{L2}}{S_{A2}} - V_{WL}\frac{S_{L2}}{S_{A2}} + V_{BBL}\frac{S_{L2}}{S_{A2}}(1+\eta_{A2}+\gamma_{A2}) + V_{DD}(1+\eta_{L2}) -$$
$$V_{BN}\frac{S_{L2}}{S_{A2}}\gamma_{A2} + S_{L2}\left(\frac{V_{TA2}}{S_{A2}} - \frac{V_{TL2}}{S_{L2}}\right)$$

Eq.2 Write mode equation (S- subthreshold slope; V_{th}- thermal voltage; V_{BN}- NMOS body bias; V_{BL}- read bitline voltage; V_{BBL}- write bitline voltage)



Figs.1-3 Comparison of equation (dashed), simple equation (dotted) and SPICE (solid) butterfly curves for retention, read and write at V_{DD}=0.4



Figs.4-6 Evaluation of μ/σ for retention, read and write in function of V_{TN}/V_{TP} ratio at V_{DD}=0.4V

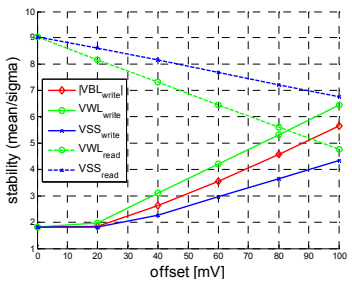


Fig.7 Assessment of write assist techniques on read and write μ/σ (from ELDO simulations) for V_Ts adjusted for top retention stability

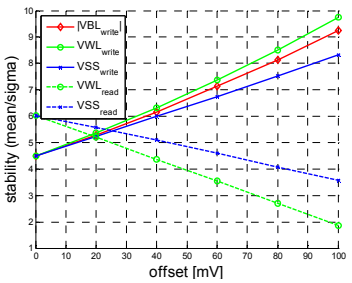


Fig.8 Assessment of write assist techniques on read and write μ/σ (from ELDO simulations) for V_Ts adjusted for initial read μ/σ=6

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