Transport properties and functional devices on CVD grown Silicon nanowires

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THÈSE

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Transport properties and functional devices on CVD grown Silicon nanowires

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par

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Foreword

So there we go! I have finally made it! After adding the last chapter and cheking the body of the manuscript I didn't find evident mistakes. Well, at least the pictures have colors and the writing is from left to right as it should be. I cannot guarantee for silly statements though. Now it's time to write the most important part of the thesis, the one which is hidden by tens of pages stuffed with hypothesis, wrong conclusions, failed experiments and few blinking glimpses of glory.

Even though my PhD cannot be really be defined as *plug and play*, it was a very valuable human experience for me. For this I thank my supervisors Silvano de Franceschi and Marc Sanquer for having welcomed me in the lab and giving me the possibility to embark this adventure. Don't take me wrong, of course I do see the advantages of entering a lab where everything is working since the very first day and the subject has been explored since decades and you simply rewrite some chapters of your predecessor's thesis. Eventually you change the sample if it is really needed. But not having even the chairs to sit (not to mention the desk) the first day you enter the lab makes this PhD a special one in the end. For the reasons written above. Because the (very) few nice good things the interested reader will eventually find in the following are the results of a real passion. The one that doesn't let you sleep at night and doesn't let you step back facing countless hours at work and unsuccessfull experiments. Every chapter in this thesis has been a fight, a fight on a virgin battlefield. And to me this is special as much as the formidable companions who backed me during the journey.

Without Giorgos and Pana nothing would have been possible. I owe them much of the results of this thesis. They were for me mentors and friends always ready to help out and support my bad moods. In other words they are for me the best labmates and most of all team players I could have ever dreamt of. Thanks to them the atmosphere in the lab (and I would say in the building) has been always cool and fresh with nice music in the air and singing echos of Dean Martin and Franck Sinatra in the corridors. Not only in the very few moments where things were going smoothly but expecially in the early days when we had "fun" while soldering tiny cables, building new sample holders, tweaking misterious electronic equipments, unvealing the secrets and the art of nanofabrication, programming and automatizing data collection and analysis, dealing with the heaviest administrative rules ever conceived by human being. *Yes man, we made it !!*.

I would also like to thank Xavier Jehl for his kindness, support and advices. He has given me a lot, always supportive and willing to proof read my papers, a real friend. Thanks Xa !!

A particular mention has to be given to Jean-Luc Thomassin, Frederic Gustavo and the technical staff of PTA for having coped with our endless requests of support in the cleanroom, trying to grasp the most intimate details of nanofabrication. Thank you

guys for your competence, professionality and patience. I would have never been able to fabricate nice nanodevices without you guys.

Many thanks to Francois Lefloch and Claude Chapelier for their competences and advices in physics, nanofabrication, project managing. Thank you for having supported me in the mighty techno-meetings of friday afternoon and for popping in the lab downstairs every now and then having fun with us on silly greek-italo subjects.

Thanks to Gerard Lapertot and Christophe Marin, the mighty D5 crew, for the support in the annealing experiments and for having opened me the doors of their marvellous laboratory plenty of cool machines. I had a lot of fun working with you guys. Thanks to you I sowed the seeds of our *manip du siècle*.

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Thanks to my friends Alex, Francesca, Eva, Mario, Georg, my thesis labmates Mathieu, Thomas, Guillaume, the Chemtronics fellows Martien, Emanuela, Big Robert, Alejandro, Isabelle. I hope I didn't forget anybody.

I want to thank also my friend Edoardo for his closeness, the trips and the evenings spent drinking beers.

Lastly, I want to thank my family for the unconditional support and nurturing love, I love you all. If I am a good man it's because of them.

Thanks to my beloved sister always ready to sustain me in my darkest hours when I had to face the toughest period of my life.

And mum, even if you didn't make it to my defense I hope you will be proud of me looking from up there in the sky. I will try to do my best.

Grazie a tutti.

Massimo

Introduction

The spectacular success of nowadays Information Technology stems from the capability to fabricate logic circuits based on Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with increasing performances in terms of speed and packing density. This revolution has been triggered by the fundamental paradigm of scaling pionereed at the beginning of 70's [4]. The basic MOSFET building block works on the principle that flowing between two electrical terminals, the so called source and drain leads, is modulated by a control voltage applied to a third terminal, the so called gate electrode. Advance in circuit performance have been obtained through progressive scaling of device dimensions which has led to an increase density of transistor per unit area, higher speed and lower cost per function. Shrinking device dimensions has been possible by applying the so-called constant electric field scaling scheme. This scheme aims to reproduce the same electric field pattern in the smaller transistor by reducing the applied voltage along with the device relevant dimensions such as the junction depth, the channel length, the oxide thickness. This scaling requires an increasing doping level. In this transformation all the important characteristic of the device are modified by a common scaling factor α. This approach gives three important results. The packing density and speed are increased because of the smaller device dimensions and parasitic capacitances. Lastly, the power dissipation per device is reduced because of the reduction of the voltage and current in each device. This is important since a bigger number of devices can be present on the chip area withouth increasing power dissipation. This trend has been followed with extraordinary success up to recent days when the current semiconductor technology has reached the 'nano' era. Current semiconductor manufacturing protocols have entered the 32nm node for the gate length of a planar MOSFET but concerns are widespreading about the real limits of a seamingly endless downscaling. Important limits could be quickly encountered in the next years due to limitations in lithographic techniques, to an increased leakage through the gate oxide and to random dopant fluctuation in the channel [16]. In this context new emerging devices based on bottom-up architectures [13], in particular nanowires, are currently being investigated as a possible alternative route to extend the stream of miniaturization even further [1]. The advantage of bottom-up nanodevices derives not only by their intrinsic smallness which makes them appealing with respect to a bare geometric scaling request, but also because their electronic properties can be taylored in-situ during the growth. Replacing the channel of a bulk planar MOSFET with a nanowire seems to be a logic choice in view of the above mentioned issues related to scaling. Both III-V and II-VI semiconductor nanowire compounds can be synthesized with a bottom-up approach but Silicon Nanowires (SiNWs) are of course a straightforward choice because they are fully compatible with CMOS technology. Among them, Schottky barrier SiNWs transistors offers many advantages concerning scaling is-

sues with respect to conventional doped source-drain contacts [11],[10].
Besides, quasi 1-D nanostructures like Silicon nanowires offer an interesting playground where rich physics of low dimentional systems could be explored. In this respect Silicon is an attractive material for electronic applications involving the spin degree of freedom of the carriers [17]. This new possibility is explored in the field called spintronics where the spin degree of freedom carries the information as opposed to the charge. This brings some advantages like the integration of electronic, optoelectronic and magnetoelectronic multifunctionality on a single device that can perform much more than is possible with today's microelectronic devices. One device which is already in use is the Giant Magneto Resistive, or GMR, sandwich structure consisting of alternating ferromagnetic and non-magnetic metal layers. Depending on the relative orientations of the magnetizations in the magnetic layers, the electrical resistance through the layers changes from small (parallel magnetizations) to large (antiparallel magnetizations) [2]. This effect is the working principle of the data storage in nowaday's hard-disks.

Moreover, there are other proposals to use single spins as quantum bits [7], [12] and to encode the information in a quantum superposition of two levels (spin-up, spin-down). A key requirement for the implementation of quantum computing schemes is to prepare, manipulate and read the quantum bit. Coherent control of one and two spin states has been already accomplished in III-V etherostructures [15],[9], but efforts are going towards group IV materials like silicon, for which the spin lifetimes are expected to be larger due to the absence of hyperfine coupling with the nuclear spin moments and the absence of spin-orbit interaction. Read-out of a single spin in silicon has been accomplished in a device consisting of a top-down implanted phosporus donors coupled to a metal-oxide-semiconductor single-electron transistor [14]. The measured spin lifetimes approaches 1 second. Chemically sinthesized bottom-up nanostructures, on the other hand, offer the unique advantage that their properties like doping, size, composition can be taylored in-situ during the growth. This is an advantage as compared to top-down planar silicon devices where the critical feature sizes are defined by etching or lithography and doping achieved by implantation. This means that control of these important parameters cannot be extended to the atomic scale. For bottom-up silicon nanowires, the first evidence of transport through a single quantum structure with discrete energy levels was observed early as 2005 in molecular scale nanowires with diameter comprised between 3 and 6nm [18]. Electronic transport through these system is truly 1-D at low temperatures (4K) with typical subband spacing around 300meV. In these systems a single quantum dot accomodating few tens of holes could be formed between the leads with separations up to 400nm. The source-drain separation defined the dot size and suggested that structural variation or dopant fluctuations are to a large degree absent. Quantum computation with spins requires not only the isolation of single charges, but also the identification of single spins, a task that can only be accomplished in very small nanowires due to the relatively high electron and hole effective mass in silicon. This was done [19] by forming silicide/silicon/silicide nanostructures with a silicon channel length as small as 12nm. Lastly, charge detection on a double dot system [6] has been accomplished demonstrating the potential of these nanostructures for implementing solid-state spin quantum bits.

This work is devoted to the study of transport properties of Silicon Nanowires obtained by a bottom-up approach. The choice for the material system has been limited

to undoped SiNWs because they are considered as the ultimate choice for ultrascaled devices. Doping can in fact be challenging in very small nanostructures due to effects related to quantum confinement [8], surface segregation [5], and the increase of the ionization energy for the dopants as the nanowire diameter decreases [3]. The reduction of the wire diameter is on the oher hand unavoidable for tackling short channel effects in scaled transistors. The choice of undoped nanowires brings some drawbacks related to the presence of Schottky barriers formed at the contacts, rendering the problem of an effective carrier injection in the semiconductor particularly important. The thesis covers technological aspects related to the use of silicon nanowires as potential building blocks for nanoscale electronics and at the same time explores some opportunities offered in term of single-electronic devices, by developing fabrication techniques outperforming conventional nanolithography.

Chapter I describes the techniques employed for the fabrication of the nanowire devices investigated in this PhD work. The protocol developed for the formation of nickel silicide contacts is described in detail.

Chapter II deals with the study of a Gate-All-Around Schottky barrier transistor. Multiple gates are used to discriminate between different device switching mechanisms occurring either at the source and drain contacts, or at the level of the silicon channel. The gate dependent Schottky barrier height is measured for each of the contacts by means of a field emission model. The contact gates are proved be effective in suppressing the Schottky barrier enabling carrier injection at low temperature. Moreover, a p-n diode is formed by gate induced electrostatic doping in an undoped silicon nanowire. Lastly, a two inputs logic NAND gate with gain is assembled taking advantage of the local gate modulation of carrier injection at the contacts.

Chapter III reports a novel technique for the fabrication of metal silicide contacts to individual silicon nanowires. This technique, based on an electrically-controlled Joule annealing process, has enabled the realization of silicide-silicon-silicide tunnel junctions with silicon channel lengths down to 8nm. The transport behaviour of these short junctions were measured at low temperatures. The silicidation of silicon nanowires by Nickel and Platinum could be observed in-situ and in real time by performing the experiments of Joule assisted silicidation in the chamber of a Scanning Electron Microscope.

Chapter IV describes resonant tunneling through an isolated Platinum silicide nanocluster acting as a metallic Quantum Dot enbedded in a Silicon tunnel junction fabricated by Joule assisted Platinum silicidation. In particular, the Zeeman splitting of the ground and the excited states of a single nanocluster orbital could be measured by tunneling spectroscopy in a magnetic field.

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Chapter 1

Device fabrication

Considerable effort throughout this thesis has been put on the device fabrication. The fabrication of a working nanoscopic electronic device goes through multiple steps each of them as much important as the previous one. Basically, one intends to attach macroscopic electrodes to the nanometer sized objects like the nanowires and build an electronic circuit. For this purpose, we extensively used lithographic techniques which allow the patterning of custom designed contact electrodes. Although lithography is a very important step in the fabrication, a finished device is rather complex since different steps like cleaning, etching, thermal treatments, oxide deposition, sample bonding and mounting must be carefully done.

1.1 Nanowire growth

In this section I describe the growth process of the silicon nanowires studied in this thesis. The majority of devices were fabricated from undoped Silicon nanowires grown in the Laboratoire Silicium, Nanoelectronique, Photonique et Structure (SiNaPS) located in CEA-Grenoble. The nanowires were grown following a bottom-up approach through Low Pressure Chemical Vapour Deposition (LPCVD) [6] based on the Vapor-Liquid-Solid (VLS) mechanism [19]. The growth was catalyzed by size-calibrated catalysts from a gold colloid solution (Ted Pella) deposited on top of a (111) silicon substrate cleaned in alcohol and deoxidized into an ammonium fluoride mixture. Deposition of gold colloids dispersed in water was done in an electrochemical cell where the control of the density is accomplished by using an external electric field to drive the motion of the nanoparticles on the substrate. Besides, control over the nanowires diameter is set by the dimension of the seed colloids. After deposition of the catalysts the sample is introduced in the LPCVD reactor and annealed under H_2 flow in the temperatures range $450 - 750°C$. After this annealing step temperature is decreased to the $400 - 500°C$ range and silane (SiH_4) is introduced in the reactor initiating the growth fig.(1.1a). The silane decomposes and Si atoms condense into Si-rich liquid nanoclusters. The metallic clusters will be supersaturated by silicon which will start to crystallize below the gold particle promoting the growth from the top of the substrate.

Occasionally, other kinds of devices were instead processed starting from wires grown in LITEN laboratory [3] at CEA-Grenoble and consists of either homogeneoulsy or modulation doped silicon nanowires. The doping was achieved in-situ through addiction

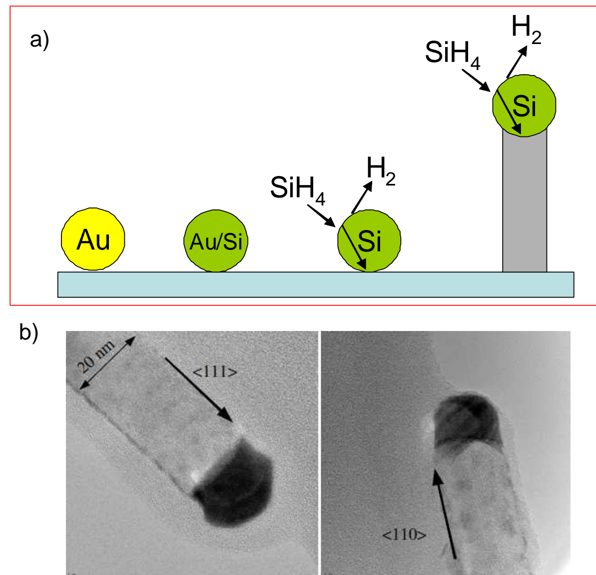

Figure 1.1: *a) Schematic of the VLS growth mechanism. b) High Resolution Transmission Electron Microscopy of two 20nm diameter silicon nanowires. From ref. [6]*

of phosphine (1% PH_3 in hydrogen) with a P:Si ratio set to 2×10^{-2}. The modulation doped nanowires consisted in a n^{++}-i-n^{++}, with n^{++} corresponding to the highly doped parts and i to the intrinsic or unintentionally doped part.

1.2 Electron beam and optical lithography

The fabrication of nanowire based devices described in this thesis is pursued by taking advantage of lithographic techniques. Two main lithography schemes were adopted: optical and e-beam lithography. The lithographies have been performed on top of a $5 \times 5\text{mm}^2$ substrate consisting of a degenerately doped p^{++} silicon wafer covered by a 285nm thick dry thermal oxide. The presence of a highly doped silicon substrate is useful when a global back gate field is needed. The basic process flow for both of these fabrication techniques is described schematically in fig(1.2). It goes through 4 sequential steps:

- spinning of the resist
- exposure of the resist by an electron beam current or by an ultraviolet lamp shined on the sample through an optical mask
- metal deposition
- lift off

The choice of the lithographic technique to be used is dictated by the particular type of experiment one intend to perform. The optical lithograpy is inherently faster than the e-beam one and is mostly useful when a parallel processing is needed. The nanowires are multiply contacted randomly by specifically designed electrodes. This parallel processing has been extensively used for annealing tests as described in more details in the following

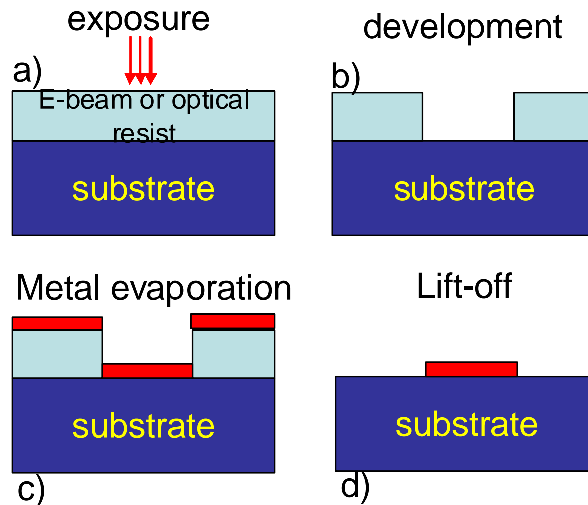

Figure 1.2: *Schematic process flow for the fabrication of the samples by optical or e-beam lithography. a)The layer of resist is exposed to an UV lamp (optical lithography) or to a beam of electrons (e-beam lithography). The development b) in a suitable solution opens up a window in the exposed area of the resist. With a low pressure $P \approx 10^{-7}$ mbar e-beam metal evaporation, a layer of metal is deposited on the sample c). The thickness of the metal layer is kept smaller than the thickness of the resist such that the metallic film is not continuous over the exposed area. The excess metal is removed everywhere d) except in the patterned areas by dissolving the polymer in acetone at $50°C$ for 10 minutes.*

sections. With the electron beam lithography, on the other hand, we can address individual nanowires. For this purpose the samples dedicated to e-beam lithography need to have additional structures already patterned on them. These additional structures are the alignment markers and the bonding pads. The alignment markers have a double function: they help on localizing the exact position of the nanostructures we want to contact and provide a reference system to the software governing the beam of electrons. The e-beam samples were fabricated with the aid of a JEOL Scanning Electron Microscope equipped with a beam blanker. The accuracy in repositioning of such a system is limited to around 300nm and the smallest features that could be routinely patterned on the resist layer depend on the particular e-beam resist and write field used. For the fabrication of the e-beam samples described in this thesis I have used a layer of polymethyl methacrylate (PMMA) spun on the subtrate for 60 seconds at 4000rpm and subsequently baked at 180° C for 5 minutes. The exposure of the PMMA layer by the electron beam causes the breaking of the chemical bondings in the polymer such that the resist becomes soluble in a developer. After e-beam exposure the samples are developed in a solution of methyl-isobutyl-ketone (MIBK): Isopropyl-alchool (IPA) $1:3$ for 60 seconds followed by a final 60 seconds rinse in IPA. The samples are then finally gently blown dry with a nitrogen flow. The typical devices processed by means of e-beam lithography consists of four cells covering areas of 100×100 nm^2 or 250×250 nm^2 fig.(1.3a). Each cell defines the actual active area of the sample where the nanowires are contacted to the micrometer sized predefined bonding pads. In each of these four cells an array of alignment markers is patterned to allow for the identification of the nanowire to be contacted. The

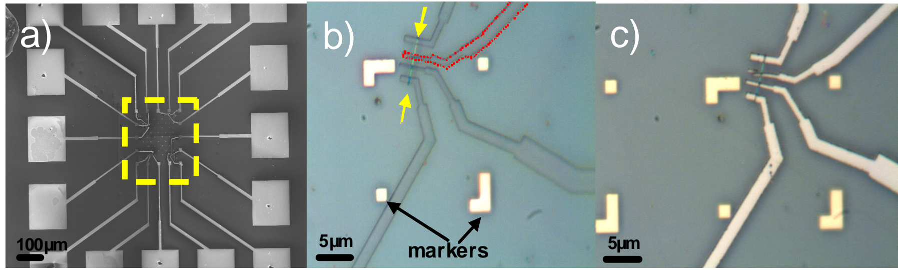

Figure 1.3: *a) SEM picture of one of the four subcells. The active part of the device, highlighted by the yellow dashed box, is enclosed in macroscopic sized contact pads already predefined on the sample along with alignment markers. b) Optical micrograph showing the contacts patterned in the resist right after the developing step described in 1.2 and c) the finished device after metal evaporation and lift-off.*

nanowires coming from the growth substrate, are deposited on the substrate by direct transfer, or released from a solution. The direct transfer technique consists simply on pressing gently the growth chip against the target substrate. Otherwise the growth chip can be inserted in IPA followed by a small ultrasonic agitation. The nanowires are then dispersed on the substrate with the aid of a micropipette. Few droplets of the solution are let dry on top of a hot plate at moderate temperature. After the sample had dried the chip is rinsed in acetone and IPA followed by nitrogen blow. This step is helpful in cleaning the bonding pads by organic residuals that could complicate the bonding. The as dispersed nanowires are located with respect to the alignment markers either by an optical microscope or by SEM inspection. Wires whose diameter is between 50 to 100 nm can be easily imaged by an optical microscope. In this case we import digital optical images of the wires in areas of the chip containg at least 4 markers fig.(1.3b) after the resist has been spinned. Imaging the wires after resist spinning is important since 100 nm diameter wires are prone to move in the spinning step. Small ($\approx$ 20nm) diameter wires are instead imaged by SEM. In both cases the images are imported in a Computer Aided Design (CAD) software and the pictures are superimposed to the markers pattern. Individual electrodes to the nanowires (red dotted line fig.(1.3b)) are computer generated and the sample is then ready to be loaded in the e-beam lithography system. The metallization step fig.(1.3c) is performed in general by e-beam metal evaporation under a pressure of $3 \cdot 10^{-7}$mBar at deposition rates of 0.1 nm/sec. Prior to the deposition of metal the samples undergo to a 5 seconds wet etching under a solution of Buffered Hydrofluoridric Acid (BHF) to remove the layer of native oxide, typically few nanometers thick from the surface. Nickel electrodes are then evaporated to a thickness of 120 nm. After metal deposition and lift-off the samples are then ready to be eventually tested in a probe station but in most of the cases they are directly mounted on a 24 pin chip carrier either by gluing them with silver paint or with carbon tape. The samples glued with silver paint are subsequently bonded and are ready to be measured, eventually to cryogenic temperatures, while samples glued with a conductive carbon tape can be easily unmounted from the chip-carrier and reprocessed.

1.3 Metal Silicides

The attractiveness of silicon nanowires as material system to build functional nanoscale circuits stems from its intrinsic compatibility with Silicon technology. The basic building block for the absolute majority of today's electronic systems is the Metal-Oxyde-Semiconductor-Field-Effect-Transistor (MOSFET). Silicon nanowires are considered as the natural evolution of a bulk silicon transistor into the nanoscopic world and hold promise as the final candidates in ultrascaled circuits. Due to this compatibility with the existing fabrication technology it is natural to extend to silicon nanowires the same contacting schemes which found success in modern Silicon Integrated Circuits (SICs). In

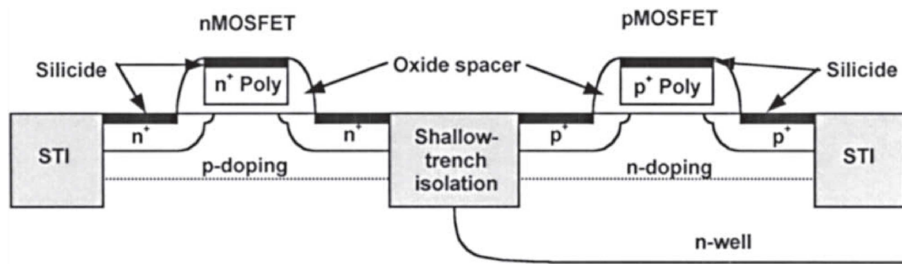

Figure 1.4: *Cross section of modern CMOS transistors where the source, drain and gate terminals are contacted with metal silicides.*

a modern MOSFET, the source, drain and gate terminals are contacted with a metallic silicide fig.(1.4). A silicide is basically a compound of Silicon with another element of the periodic table fig.(1.5). The most famous one is perhaps silicon dioxide (SiO_2)which is the most abundant compound found on Earth's crust. The use of a silicide as contacting material has been driven by the continuous demands for increasing the speed of a switching circuit. To this end parasitic capacitance and series resistance should both be minimized to reduce the RC delay time and increase the clock frequency [17],[13]. For this purpose metal silicides meet the basic requirements to lower the parasitic resistances at the level of the source drain and gate terminals. Metallic silicides used for contact metallization and local interconnections have the desired low specific resistivity and low contact resistivity to both $p-$ and $n-$ type silicon. Moreover, since the gate length in nowadays MOSFET has reached 32nm the resulting low channel resistance demands for an increased reduction of the parasitic series resistances in the source and drain regions.

The most important silicides for SICs are formed by combining silicon and a transition metal and fall in the category called Intermetallics. These compounds behave more or less like metals, and were first introduced in SICs essentially as contacting materials.

1.3.1 Self aligned silicide

In modern silicon industry the contacting process for the source, drain and gate terminals is done in one step without the use of a mask, through a technique which allows the metallisation of these three terminals in a self aligned fashion. The process is called Self ALIgned siliCIDE (SALICIDE) fig.(1.6) [22]. In the SALICIDE process a layer of a transition metal is deposited over all the MOSFET structure fig.(1.6a). With a first

Figure 1.5: *Periodic table of silicides. (Adapted from [14])*

annealing step at a suitable temperature the metal react with the silicon allowing the formation of a silicide phase on the source, drain and gate leaving unaltered the oxides fig.(1.6b). The excess metal is then removed by a selective wet chemical etching. The etching step will only remove the metal which didn't react with silicon. After the etching process other thermal treatments could be eventually performed to form different silicide phases of lower resistivity. The choice of a particular silicide over the others is made taking into account several requirements, namely

- a low resitivity
- easiness of fabrication
- existence of a selective etching process for the excess metal
- minimum silicon consumption
- good thermal stability
- smooth interface with silicon

The most important silicides used in the SALICIDE process have been those with the rather low resistivity of $10 - 20\mu\Omega$cm, i.e. $TiSi_2$, $CoSi_2$ and NiSi. Hystorically, $TiSi_2$ was the first silicide used for metallization. $TiSi_2$ occur in two different crystallographic structures C49 with high resistivity and C54 of low resistivity. The transition between the high to low resistivity phase is difficult to accomplish as the gate length of the devices approaches 100nm. $CoSi_2$ has been used up to 40nm gate lengths but as for $TiSi_2$,when the production of transistors reaches gate lengths significantly shorter, the formation of cobalt silicide contacts becomes more difficult mainly due to a increase of the resistance for very thin lines (fine line effect). Nickel silicide has been envisioned to

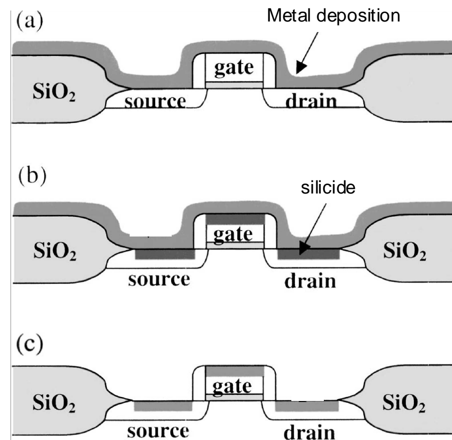

Figure 1.6: *Flow chart for the SALICIDE process. a) The metal layer is deposited over the MOSFET structure. b)A themal annealing promotes the formation of the silicide on the source,drain and gate terminals, no reaction takes place on the oxide spacers if the metal atoms are the dominant diffusing species like in the case of Nickel. c) After a selective wet chemical etch the excess metal is removed.*

be the ultimate silicide [10],[7], since it brings some advantages as compared to the other silicides. It can be formed at relatively low temperatures between 250 and 500°C which translates into a lower thermal budget for the fabrication of ICs, it has a low resistivity and consumes less silicon, characteristic very important for shallow junction transitors fabricated on Silicon On Insulator (SOI). Moreover in NiSi, nickel is the main diffusing species such that there is no lateral silicidation over the sidewalls of the dielectric and problems related to shortening of the source, drain and gate (bridging) are avoided. Lastly, the interface between the nickel silicide and silicon can be atomically sharp, thus avoiding early breakdown of the devices when bias is applied due for istance to the high electric field at the gate edges.

1.3.2 Ni-Si solid state reaction

In this section we briefly describe the formation of nickel silicide phase in thin films. The solid state reaction of nickel thin films on silicon gives rise to a quite complex phase diagram fig(1.7) [15]. Up to eleven phases in the Ni-Si phase diagram can be counted, six of which being stable at room temperature: Ni_3Si , $Ni_{31}Si_{12}$, Ni_2Si , Ni_3Si_2, NiSi and $NiSi_2$. It has been observed that the formation of the Nickel silicide through solid state reaction of Nickel thin films deposited on a silicon subtrate is sequential [16]. Without loss of generality, the formation of the silicide in thin films is governed in a first stage by the reaction of the metal (M) and the silicon (Si) at the interface. The first phase which is formed in the early stages of the reaction is the metal rich phase M_2Si. Once the metal layer has been totally consumed, the formation of the monosilicide phase (MSi) starts to take place at the expenses of the metal rich phase. The final silicon rich phase MSi_2 will grow to consume totally the monosilicide layer. Although formation temperatures for the M_2Si and MSi phases can be as low as 250°C, the silicon rich phases are in general observed at higher temperatures around 700-800°C and their formation

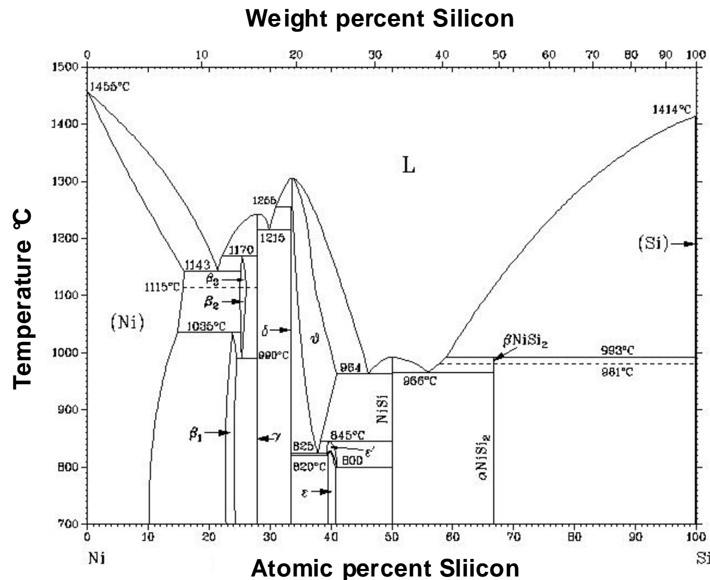

Figure 1.7: *Phase diagram for the Ni-Si binary system.*

is instead governed by nucleation [12]. For top-down transistors fabricated on bulk *p*-*n* junctions or thin SOI the SALICIDE fabrication process aims to reach the growth of the nickel monosilicide phase which has the lowest resistivity. In the framework of the above described kinetics for the nickel silicide phase formation, the monosilicide phase can occur only after the total consumption of the metal layer in the form Ni_2Si. To achieve the monosilicide in shallow junctions the first annealing step promoting the formation of the metal rich phase could be followed by a second thermal treatment done after etching the excess metal layer [4]. The above described mechanism for the metal-Silicon binary system is relatively well understood in the case of thin films on bulk substrates, where the metal thickness t_M is usually much less than the silicon thickness t_{Si}. In the opposite case $t_M >> t_{Si}$ different metal rich phases could be present in the early stages of the silicide formation [2]. This aspect is important for the point of view of device application, since different phases of the metal silicides could have different resistivities and in turn affect the performances of ultrascaled devices. In this thesis we are interested in controlling the extension of the metal-like silicide phase into the silicon regardless of the phase sequence underlying its formation.

1.3.3 Silicidation in silicon nanowires

In current MOSFET technology, the process of silicidation has been conceived to provide a suitable contacting scheme for the terminals of the active device like source, drain and gate. As explained in the previous sections, research on the contact metallisation through silicides has been triggered by the demand of lowering the parasitic series resistances arising from the contact. An important aspect in the technology of metallisation in common transistors is the fact that the contact silicides are in general shallow. The amount of silicon consumed in the process of silicide formation must be minimal [9] to allow smaller design rules. In this thesis we have adapted the silicidation technique by

nickel already developed in the case of bulk planar transistors for defining the contact regions for the nanowires. Our contacting schemes differs from the process flow adopted in the case of top-down defined transitors. In particular:

- our geometry is not planar
- the metal silicide-silicon interface is not shallow
- we don't make use of the selective etching process to remove the excess metal as in conventional MOSFETs
- we promote lateral silicidation

The contact metallization procedure through silicides has been applied with success in the case bulk junction transitors and SOI thin films. In both cases the metal-silicon interaction occurs at the plane of the interface. A nanowire is inherently different in its geometry and the early stages of silicide reaction takes place in the radial direction [8]. Moreover, the interface in our devices is never shallow since we are not concerned about vertical scaling issues which are instead governed by the nanowire diameter. Another difference is that a completed device doesn't go through the metal etching process typical of the SALICIDE technique. In our silicided nanowires the metal layer provides at the same time the material for the solid state reaction and the connecting path for the complete circuit in which the nanowire is embedded. The last and most important difference is that we are expecially interested in promoting a lateral silicidation for our devices. We can speak about lateral silicidation when the nickel silicide-silicon interface is not only moving parallel to a fixed interface plane but the silicide formation kinetics allow for the growth of the silicide phase in a plane orthogonal to the metal/silicon interface. The lateral silicidation can occur in ultrathin SOI MOSFETs when the contact metallization is done with a nickel film thicker than the silicon. The lateral penetration of the nickel silicide under the isolation spacers towards the channel is strongly detrimental for the transitor operation because if the silicide extends to the low doped channel region, the source and drain contact exihibit a Schottky behaviour [18]. Although the actual growth mechanism of the silicide phase in silicon nanowire is not well understood, through thermal annealing we promote radial and longitudinal diffusion of nickel in the nanowires. This is accomplished by taking advantage of the unique property of nickel in the binary nickel-silicon system to be the dominant diffusion species. The formation of Ni-silicides by means of solid state reaction of lithographically defined nickel contacts on Si nanowires has been demonstrated in a few earlier works [21], [20], [1]. The actual growth mechanism of the nickel silicides leading to the axial intrusion of the metallic phase in the nanowire is thermally activated and involves different processes like volume, surface and interface diffusion and lateral growth of Ni silicide [8]. The thermal energy is provided typically by heating sources like lamps or lasers in the case of a Rapid Thermal Process (RTP) or more simply by resistive elements in furnaces. Conventional semiconductor device manufacturing is done by using RTP techniques because they are faster and provide high throughput. The silicidation of silicon nanowires in this thesis was instead performed in a furnace. The samples contacted with the lithographic techniques described before were loaded in a quartz tube attached to a vacuum system. Prior to the thermal annealing, the quartz tube was pumped by primary vacuum pumps

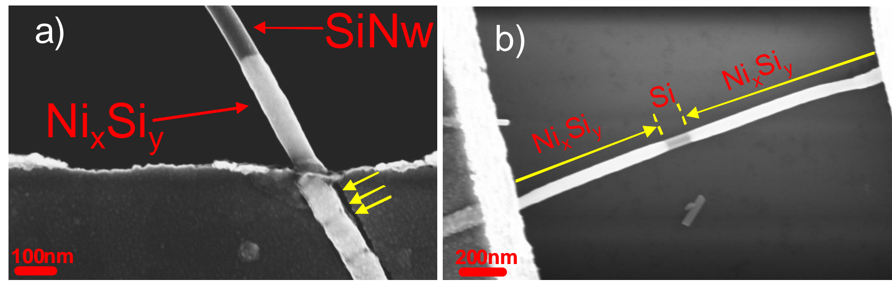

Figure 1.8: *a)SEM micrograph of a nanowire reacted with a nickel film afer a thermal annealing. The brigher region in the nanowire is the metallic nickel silicide phase grown by the thermal annealing performed at* $500°C$ *for* 5 *minutes. The lithographically defined metal film covering the nanowire has been deposited to a thickness comparable to the nanowire diameter* $d \approx 100$nm *causing the discontinuity of the metal contact on top of the nanowire (yellow arrows). b)Nickel silicide/silicon/Nickel silicide etherostructure formed on a* 50nm *diameter silicon nanowire. After the silicidation an unreacted silicon portion of* 120nm *could serve as channel for a transistor.*

to a pressure $P \approx 4 \times 10^{-2}$mBar and subsequently purged with a constant Argon flow for several minutes. This cycling through vacuum was done to prevent any oxygen contamination. Subsequently, the quartz tube was guided into the furnace heated at the desired temperature and the samples annealed for various time intervals. Scanning electron microscopy is a powerfool tool that can be used in order to study the solid state reaction occurring during the silicidation. Fig.1.8a is a Scanning Electron Microscope (SEM) picture which shows a 100nm diameter Silicon nanowire contacted by a nickel electrode after a process of thermal annealing. The bright contrast along the nanowire axis is due to a metallic nickel silicide phase protruding from the electrode. Through this lateral silicidation we promote the diffusion of nickel along the nanowire axis to form an abrupt interface between the nickel silicide and the silicon. The nickel electrode has the role of a reservoir for the nickel atoms which have to diffuse in the silicon lattice of the nanowire. If the amount of metal covering the nanowire and its radius are comparable, a long annealing of several minutes could provoke the craking of the metal film just on top of the nanowire, as enlighted by the yellow arrows in fig.1.8a and a consequent failure of the electrical contact defined by lithography. The promotion of a lateral silicidation in silicon nanowires offers intriguing possibilities in terms of device fabrication. This is enlighted in fig.1.8b which shows a silicon nanowire bridging two nickel electrodes after an annealing step. The diffusion of nickel into the nanowire from both the contacting electrodes forms two metal-like extensions of the contacts leaving an unreacted silicon portion in the middle of the device. The ability to control the lateral silicidation can give then access to nanoscale device architectures with applications ranging from ultrascaled transistors or quantum devices like quantum dots or tunnel junctions.

1.3.4 Control of the silicidation process

Control of the lateral silicidation is very crucial from the point of view of device applications. If, for istance, the silicidation process is used to define the channel of a transitor

like in fig.1.8b then, one needs a fine control on the lengths of the two silicide extensions. This is important since in principle different transistors on the same chip should have the same channel length. This is also true for other devices like Single Electron Transistors (SETs) or tunnel junctions which could be fabricated through a lateral silicidation process leading to the definition of a very small area of a semiconductor sandwiched between two metallic leads. Controlling the lateral silicidation is necessary also for fundamental studies aimed at understanding transport phenomena like carrier injection and field emission occurring at the interface between the metal silicide and the silicon. This is of fundamental importance expecially when the overall electrical behaviour of the devices is determined by the interface properties. This point is clarified in fig.1.9 where a single nanowire is contacted by three equidistant metal contacts. The thermal annealing leads to the formation of three different unreacted parts in between two adjacent contacts of different dimensions. The silicide propagates into the same nanowire at differents growth rates. Many factors could actually be responsible for the observed

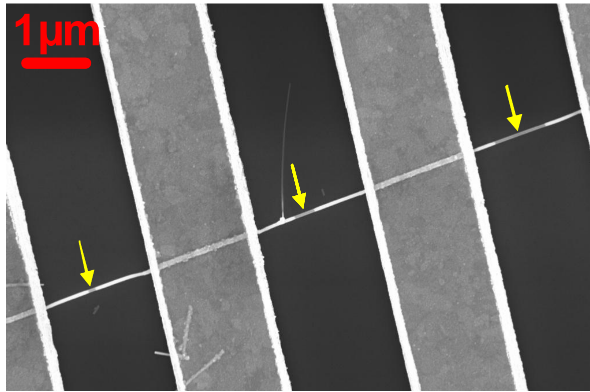

Figure 1.9: *SEM micrograph of a 10μm long nanowire contacted with three equidistant contacts. The silicides extending from the contacts grew at different rates and as a consequence the three unreacted silicon portions highlighted by the yellow arrows have different dimensions.*

non-homogeneties in the silicide growth. The presence of a native oxide layer on the surface of silicon nanowires is known to have a detrimental effect since it could act as a diffusion barrier layer to stop or delay the reaction between the metal and the silicon [11]. Moreover, there could be organic residues on the surface of the nanowires, coming from the lithography and/or from the solutions in which the nanowires are dispersed. Purity, roughness and mechanical adhesion of the metal layer deposited could also have an influence on the overall process.

To better understand and control the silicidation process in the nanowires, we studied the statistical distribution of the lengths of the silicides in two different sets of samples. In the first set called *set*1 there are wires obtained through a growth catalyzed by gold nanoparticles obtained by dewetting a thin layer of gold deposited on the substrate; in the second set called *set*2 the nanowires are instead catalyzed by gold colloids. The difference in the two sets of samples are mainly ascribed to the dispersion and average diameters of the nanowires. The samples of the *set*1 are charaterized by an average diameter 89 ± 23nm with a relative dispersion of 26% in the diameters. Samples of the *set*2 obtained by colloidal nanoparticles have an average diameter of 28 ± 6nm with a

relative dispersion of 20%. The wires of *set*1 and *set*2 are contacted randomly by means of optical lithography to assure high throughput and statistical significance or by e-beam lithography for specific device geometries. The metal thickness is chosen according to the wire diameter and it's always bigger the nanowire diameters in both sets. The ratio between the metal thickness deposited and the nanowire diameter is between 1.7 and 3.4 for *set*1 and between 3.6 and 9 for *set*2. These ratios are big enough to guarantee enough supplying material from the metal reservoirs in the process of diffusion. Different parameters can influence the silicide growth. The most important ones are:

- the annealing temperature
- the nanowire diameter
- time

Although a nickel silicide phase could be formed at temperatures as low as 130°C [10] the annealing experiments were performed by keeping fixed the temperature at 500°C. This value is high enough to cause the formation of a silicide phase on the time scale of several minutes but lower than the temperature where other effects, like agglomeration and formation of the high resistive Si-rich phase, start to take place [12]. Fig.1.10 summarizes

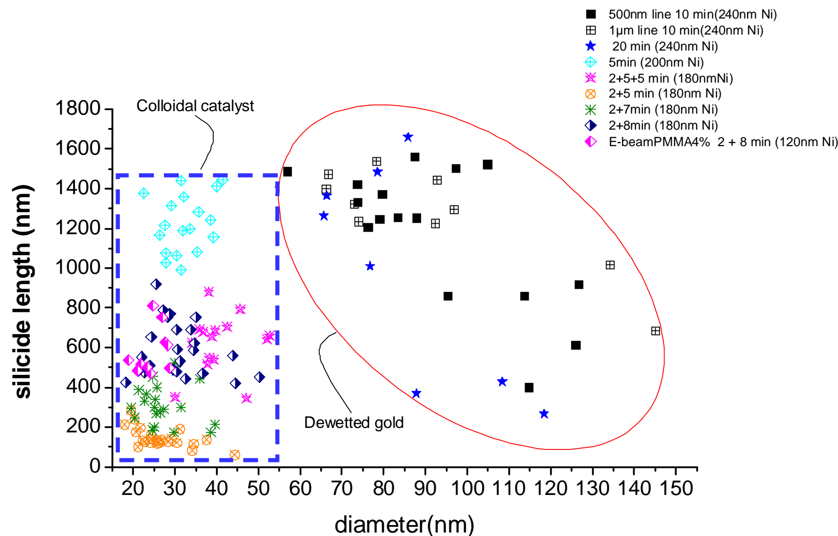

Figure 1.10: *Silicide lengths as a function of diameter for different annealing protocols.*

the results obtained for the penetration length of the silicide after the annealing process. Two blocks of data are shown: data on *set*1 enclosed by the red circle referring to wires catalyzed by dewetted gold on the surface and data on *set*2 highlighted by the dashed blue box, summarizing the results for the wires catalyzed by colloidal particles. The wires from *set*1 have been subjected to annealings of 10 and 20 minutes. A volumetric effect [1] in the silicide penetrations is visible for this set of data, leading to a decrease of the silicide length as a function of the nanowire diameter for both the annealing times. The electrode's width, varied from 1μm→ 500nm, for the wires annealed for 10 minutes

doesn't have influence on the average silicide length for the two set of data overall silicide length for a given diamater. Interestingly, doubling the annealing time doesn't have a dramatic effect on the silicide growth rate and the subset of data corresponding to the 20 minutes annealing, shows almost the same dispersion of the silicide lenghts as a function of diameter. This fact allows us to exclude that the phase growth is assisted by a linear-parabolic law [5]. According to this picture, in the early stages of the phase formation metal and silicon are always available at the interface and the thickness of the silicide increases linearly with time. When the silicide thickness increases, the growth becomes limited by the flux of the supplying nickel atoms through the growing phase towards the interface with silicon, leading to a growth mechanism which is diffusion limited, with a characteristic square root dependence on time. The situation is much more complicated if two or more phases are present in the early stages of the reaction. In this case the growth rates of the existing phases are coupled resulting in a different kinetics for the phase formation. On the set of nanowires annealed for 5 minutes, belonging to the *set* 2 we measure an average penetration comparable to the one observed for 10 and 20 minutes annealing times which amounts to 1224 ± 144nm while a volume effect due to the dispersion of the wires diameters is not visible. This is most probably due to a rather smaller dispersion in the wires diameter for this subset of samples where the average diameter is 32 ± 5nm, leading to a relative dispersion of around 16%, whereas the relative dispersion for the subsets of data belonging to *set* 1 ranges between $22 - 30\%$. Indeed, the volumetric effect manifests itself in the fact that the same average penetration lenghts for the silicides can be obtained by reducing the time and the diameter of the nanowire accordingly.

As an attempt to limit the statistical dispersion of the silicide lengths, we modified the annealing procedure by performing thermal cyclings for the wires belonging to *set* 2. The samples were firstly annealed at 500°C for 2 minutes and then annealed for different periods of time (at the same temperature) in a second step. The time for the second annealing step was ranging from 5 to 8 minutes. In between the two steps the silicidation process was left quenching at room temperature for a period of time of about $10 - 15$ minutes under a constant Argon flow. As is evident from fig.1.10 the thermal cycling process has as first effect to limit the growth rate of the silicides. This conclusion is drawn by confronting the silicide lengths for the subset of samples annealed for 5 minutes and the lengths obtained by thermally cycling the samples through two thermal treatments. Although the total annealing time for the subset of samples which received the second annealing step can be $1.4 - 2$ times bigger than the single 5 minutes step time, the average penetration lenghts are smaller for the same nanowire diameter. The first annealing step is then effective on limiting the lateral growth of the silicides by posing an interfacial barrier layer for the diffusion of the Nickel atoms in the second step.

To summarize, we have performed a systematic study of the formation of silicides in Silicon Nanowires with the aim to control the length of the lateral silicidation. Our goal was to find a recipe for the annealing treatments capable to promote the silicidation growth in a reproducible way. The dispersion in the lenghts of the silicide phases is mainly ascribed to the dispersion in the wire diameters for a given annealing temperature. The smaller will be this dispersion the better we can control the penetration lengths. The main advantage of the double step annealing technique as compared to the single step is that we are able to avoid excess lateral silicidation. SEM inspection of samples which

received only the first 2 minutes annealing step showed a slight lateral growth of the silicides amounting to $10 - 20$nm from the edge of the contact, revealing that the first step is long enough to promote a fully radial silicidation and to start the lateral one. The silicidation lengths measured for wires of *set* 2 corresponding to an annealing of 5 minutes differ by a factor of more than 60 with respect to the 2 minutes step reveiling that the growth rates are far from being linear or assisted by a bare diffusion process. Through a double step we can reasonably control the silicidation process and obtain penetrations between $140 - 580$nm by changing the annealing time in the second step on a minute time scale.

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Chapter 2

Contacts on Silicon nanowires.

2.1 The Schottky barrier

For electronic applications using Silicon nanowires making satisfactory contacts is of crucial importance. In semiconductor technology the issue of carrier injection from metallic leads to the semiconductors is vital because in all the applications is very important to model and taylor the contact properties for a correct device operation. Metal-semiconductor contacts have been studied extensively since the beginning of the 20th century and the widely accepted model is called Schottky barrier (SB)[24]. When a metal is put in intimate contact with a semiconductor a barrier is formed at the interface fig.(2.1). Its height and width controls the carrier injection from the metal and collec-

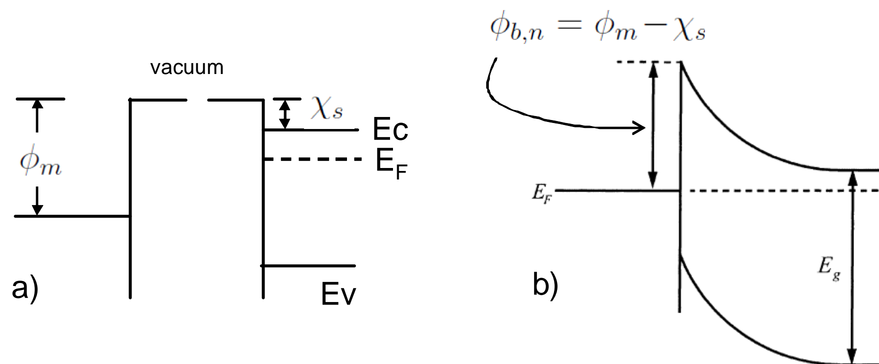

Figure 2.1: *Schematic energy band diagram between a metal and a semiconductor when a) they are separated or b) form an interface*

tion from the semiconductor. The formation of the barrier is due to the misalignment between the Fermi levels in the metal and semiconductor. At equilibrium the two Fermi levels must line up and this is accomplished by a charge transfer from the metal or the semiconductor throught the contact interface. Depending wheter the semiconductor is n or p-type its Fermi level lowers or raises respectively with respect to the metal Fermi level by an amount equal to the difference between the two working functions of the

two materials. The working function is just the energy gap between the vacuum level and the Fermi level. The charge transfer builds up an electric field extending in the semiconductor through a region depleted of carriers whose width depends on the doping level of the semiconductor. The space charged region in the semiconductor is balanced by a surface charge layer equal in magnitude and opposite in sign on the metal. The SB is the misalignment at the interface between the metal conduction band and the semiconductor conduction or valence band. This misalignment poses a barrier to the carrier flow, either electrons or holes depending on the majority type of carriers in the semiconductor. To a first order, for a n-type semiconductor the Schottky Barrier Height (SBH) is given by

$$\phi_{b,n} = \phi_m - \chi_s \tag{2.1}$$

where ϕ_m and χ_s are the metal work function and the semiconductor electronic affinity respectively. Conversely, for a p-type semiconductor

$$\phi_{b,p} = E_g - (\phi_m - \chi_s) \tag{2.2}$$

where E_g is the energy gap of the semiconductor. In practice however these simple expressions for the barrier heights based on the bare knowledge of the working function and electronic affinity of the materials don't apply in the majority of cases and deviation of the SBH from the simple predictions of equations (2.1),(2.2) are caused by the presence of interface states which can have different origin. The height and width of

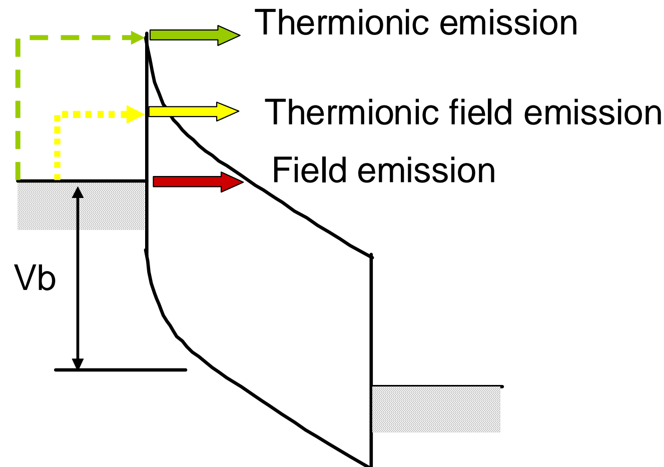

Figure 2.2: *Schematic of the principal transport mechanisms occurring across a biased interface between a metal and a n-type semiconductor where a sizeable SB is present.*

the SB influences the carrier injection from the metallic contact and several transport mechanisms can be identified across the barrier. For simplicity we can limit ourselves to the three transport mechanisms depicted schematically in fig.(2.2). With or without external applied bias the carriers can be thermally emitted over the SB since at any non zero temperature the carrier density at any finite energy is not zero due to the Fermi- Dirac statistics. In presence of an external bias voltage the curvature of the semiconductor bands at the interface can be modified such that the carriers can be firstly thermally emitted to an intermediate energy between the Fermi level of the metal and

the top of the SB and then tunnel through the SB. Lastly, the carriers can be subjected to a bare field emission across the barrier which is a pure tunneling process not assisted by the thermal energy. The complete expression at a given temperature T for the current density across a metal-semiconductor interface taking into account thermionic, field emission and tunneling reads:

$$J = A^{\star}T^{2}exp\left(-\frac{q\phi_b}{kT}\right)\left[exp\left(\frac{qV}{kT}\right)-1\right] \tag{2.3}$$

where ϕ_b, $A^{\star}$ and V are the SBH, the Richardson constant and the potential applied respectively. Equation 2.3 describes the transport across a metal-semiconductor junction commonly referred as Schottky junction. In the limit of low SBH and/or high doping level for the semiconductor the resistance associated to the barrier can be made negligibly small as compared to the total resistance of the semiconductor device. In this case the contact is said to be ohmic. To better understand the role of the SB in the device electrical performances I fabricated devices from different types of silicon nanowires: undoped, with heavily doped edges and uniformly doped. The doping of the nanowires was achieved in-situ during the growth using phosphine (PH_4) as precursor gas to incorporate phosphorous atoms giving rise to n-type doping. It was possible also to grow modulation doped nanowires by removing the feeding gas carrying the dopant precursor. In this way n-type/intrinsic/n-type (nin) nanowires could be grown. The nanowires were doped with a feed gas ratio P:Si=2×10^{-2}. Fig.(2.3) compares room temperature

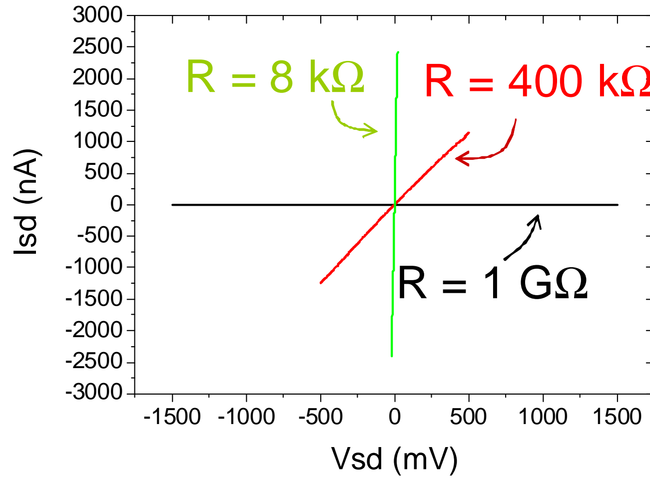

Figure 2.3: *IV comparison between nanowires with degenerate uniform n-type doping (green curve), heavily doped sections with an intrinsic channel (red curve) and undoped (black curve). In all the three cases the contacting material is Nickel and the channel length is* $1\mu m$.

IV characteristics for the three kinds of samples contacted by nickel electrodes without silicidation. Doping has a substantial effect on the overall electrical resistance. Although the channel length for all the three devices was 1μm the highly doped device has a metallic behaviour with a resistance of 8kΩ while the nin nanowire with the contacts

patterned on top of the heavily doped sections has a resistance of 400kΩ. These resistances are orders of magnitude lower than the device resistances for undoped nanowires. In these devices transport is strongly limited by the SB. The SB in all the three cases is the same since the nanowires were contacted with the same metal. However, doping the nanowires has the effect of thinning down the SB and enhance the tunneling component of transport across it such that the contact behaviour becomes ohmic. Although both the uniformly doped and the modulation doped nanowires had low contact resistances allowing an easy carrier injection even at low temperatures (4K), we prefered focus our attentions on intrinsic nanowires for different reasons. Nanowires with uniform doping, have metallic character which translates in a poor or even absent electrostatic control of the carrier density in the channel. This is an important requirement for all the studies which focus on carrier interaction in low dimensional systems. The modulation doped nanowires on the other hand could not be grown with enough flexibility in terms of length and diameter of the intrinsic channel. Ideally the channel length and thickness should be sufficiently small for single electronic effects to take place. In view of these difficulties we focused our attention on undoped nanowires that could be grown with diameters as small as 20nm. Moreover, the conductance of these undoped wires could be modulated over several orders of magnitude with the aid of a gate voltage.

2.2 Undoped Silicon nanowires: impact of the silicidation on the electrical properties

In this section the results obtained for the control of the silicide formation will be used for the fabrication of devices with specific architectures. Silicidation of the contacts has an important impact on the transport properties of silicon nanowires [11]. This is particularly evident in the case where the nanowires are not intentionally doped during the growth. As grown undoped silicon nanowires have a residual *p*-type background doping arising most probably by acceptor states introduced by the gold catalyst [28]. Fig.(2.4a) shows the IV characteristics of an undoped silicon nanowire contacted by Nickel electrodes before and after a thermal treatment leading to the formation of two silicide extensions extending from the contacts. The formation of the silicides greatly improved the two point resistance of the device. Before the annealing the current flowing in the device is vanishingly small and its detection is beyond the instrumental capabilities. A final resistance around 130MΩ is achieved after annealing the contacts for 5 minutes at 500°C. A rectifying behaviour fig.(2.4b) is instead observed in the case where just one contact is silicided. The formed silicide will ease the transport of carriers across the Schottky barrier at the corresponding contact.

2.3 Transport properties of multigated Schottky barrier transistors

Functional devices built from CVD grown silicon nanowires have drawn particular attention in view of their potential to fulfill the demands for the ultimate downscaling of conventional MOSFETs.

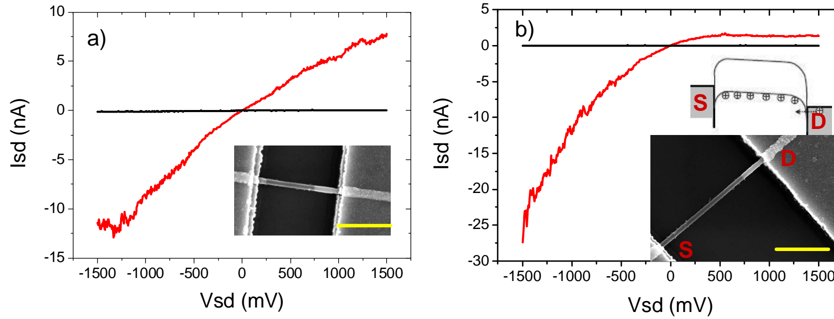

Figure 2.4: *IV comparisons before and after annealing of the contacts (red and black curves respectively) for* 100nm *diameter undoped nanowires leading to the formation of a Nickel silicide. The unannealed devices have extremely high resistances and current flow was not detectable. In a) the silicide was extending from both the contacts and the IV characteristic after the annealing is symmetric. In b) only the drain contact was silicided and the characteristic shows a rectifying behaviour. Holes can be efficiently injected from the silicided contact having a lower Schottky barrier as compared as to the non silicided one. The inset shows a schematic band diagram for a negative source-drain bias. Holes are injected from the silicided drain contact while for positive bias the higher Schottky barrier at the source contact limits the carrier injection. Insets: SEM micrograph of the devices, scale bar* $1\mu m$

Concerning the use of Silicon nanowires (SiNWs) as MOSFETs, the ultimate request of scalability and device performance demands for the use of intrinsic material to avoid issues associated with dopant diffusion and fluctuation [4] and to tackle the request for low power static consumption.

A key point for the successful operation of electronic devices assembled from bottom-up nanostructures like semiconductor nanowires or carbon nanotubes is to achieve efficient carrier injection. This becomes particularly challenging when no intentional doping is present in the nanostructures since a sizeable Schottky barrier develops between the metal and the semiconductor which is not thinned down in the region close to the contacts by the local field produced by the ionized dopants.

Undoped silicon nanowires with metallic source and drain leads made out of silicide, can be considered as good candidates to face the challenges of extreme device downscaling. This option takes advantage from the very low parasitic contact resistances of the metal silicide as compared to heavily doped source/drain silicon contacts, from high scalability in terms of channel length and width which can be pushed well beyond the limits of conventional lithography, from the low thermal budget required for the formation of the silicide contact [17]. Bottom-up silicon nanowire transistors have been extensively reported in the literature [9],[11],[25],[26],[19],[13],[8] but an exhaustive description of their transport properties is still lacking. The operation of such devices is strongly influenced by the contact properties where transport is determined by a combination of field and thermionic emission over the SB. These two physical mechanisms compete between them to give the overall current response and they can be ultimately controlled by the action of a gate induced electric field producing a band bending in correspondence of the contact regions.

The approach pursued in my PhD work is local gating of the contact SB. I have investigated the possibility to individually control the contacts and the channel region of a silicon nanowire device by means of independent gate electrodes. The capability to address independently in the same device the gating fields allows not only a quantitative extraction of the energy barrier at specific locations but also the implementation of different functionalities on one single nanowire. This local gating approach requires two or three independent gates. A key issue for controlling the carrier injection and extraction is the physical identification of the contact regions. In our system this is obtained through the controlled formation of metallic nickel silicide phases protruding from the contacts. The formation of such metallic phases is accomplished by a thermal annealing process which promotes the diffusion of nickel atoms through the silicon lattice to form a sharp interface between the silicide and the silicon. Injection and extraction of the carriers is taking place at these interfaces which are away from the as-deposited metal contact to allow for efficient gating. A substantial band bending at these interfaces can be achieved since the gating fields are not screened by the large contacts defined by lithography. The gating of the nanowire in correspondence of the injection junctions is accomplished via a Gate-All-Around geometry which gives the best electrostatic coupling [23]. Fig.(2.5) describes the process flow adopted for the fabrication of the samples. The preparation

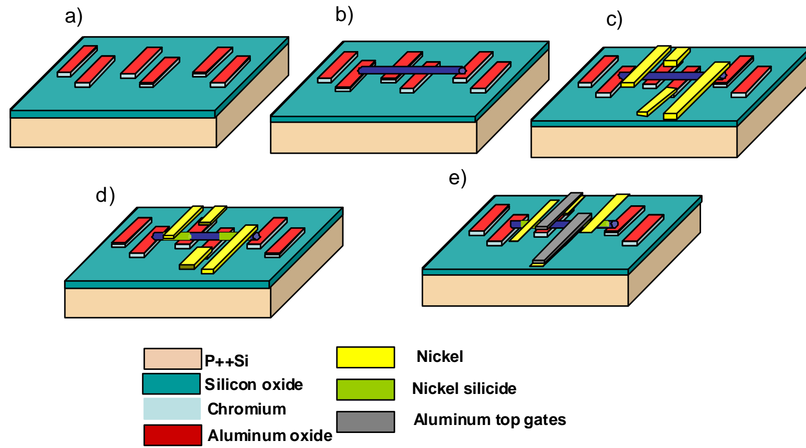

Figure 2.5: *Process flow for the fabrication of the samples: a) The bottom gates (Cr/Al 10/5nm) are defined on top of the substrate, b) Silicon nanowires are randomly dispersed and some of them will bridge at least a couple of bottom gates, c) these nanowires are contacted along with the bottom gates, d) the thermal annnealing cycle promotes the formation of two metallic nickel-silicide contacts, d) deposition of the aluminium top gates. Each top gate is shorted with the corresponding bottom gate leading to a gate-all-around geometry.*

of the samples starts by defining with e-beam lithography, metal deposition and lift off an ordered array of gates (Cr/Al 10/5 nm) spaced by $500nm$ on top of an oxydized heavily doped silicon substrate ($p^{++}\ Si/SiO_2$). After a brief sonication in isopropanol, the as-grown silicon nanowires are released from their growth substrate and drop cast on the substrate with the already predefined alignment markers and bottom gates. The wires bridging a couple of bottom gates are located with respect to the markers and subsequently contacted along with the bottom gates by e-beam lithography. Prior to the deposition of the metal, the native oxide on the nanowires is etched away by dip-

ping the sample for 5s in buffered HF. This step is also removing the layer of native oxydized aluminum of the bottom gates leaving the underlying chromium layer unaffected to allow for an electrical contact with the deposited Nickel. The contacts to the nanowires are separated from the bottom gates by a distance of 300nm. This distance is given by the repositioning resolution of our e-beam lithography system limited around 200nm and allows to avoid electrical shortening of the leads with the bottom gates. After contacting the wires we perform a double step thermal annealing process following the recipy described in chapter 1 in order to align the nickel silicide/silicon interface in correspondence of the bottom gates. Taking into account the bottom gates widths and the position of the contacts with respect to the bottom gates a sequential double step annealing of 2 and 8 minutes is chosen to have average penetrations of 588 ± 136nm. The double step allows to position the silicide front on the bottom gates fig.(2.6a). The nickel

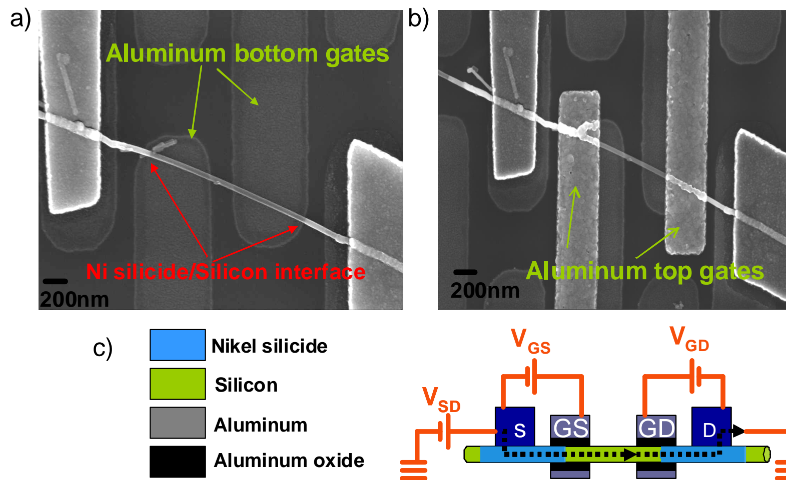

Figure 2.6: *a)SEM micrograph of a nanowire contacted by two nickel electrodes. The brighter regions in the nanowire correspond to the metallic Nickel silicide phase. The interface between the Nickel silicide and the silicon is right on top of two corresponding split gates which locally gate the nanowire. b) After a second step of lithography two additional top gates are aligned on top of the interface in a Gate-All-Around geometry.c) Schematic view of the sample: S=source,D=drain, GS=Source Gate, GD=Drain Gate. The Nickel silicide regions (light blue) extend from the Source and Drain terminals and the potentials at the interfaces with Silicon (green) are controlled by the corresponding gates*

silicide/silicon interface extending up to the position of the bottom gates allows for an electrostatic control of the contact gating potential and in turn the carrier injection. Another step of e-beam lithography is performed afterwards to overlap a couple of top gates fig.(2.6b). The aluminum top gates are isolated electrically from the nanowire by the oxydation of four layers of aluminum each of them of nominal thickness 1.5nm. Each layer of aluminum is oxydized in the e-beam metal evaporation chamber right after its deposition under pure oxygen at a pressure of 200Torr for 10 minutes. Assuming that each layer of aluminum of nominal thickness 1.5nm is completely oxydized, the overall top dielectric thickness is around 6nm which is comparable to the thickness of the bottom layer dielectric. The large overlapping area between the top and the bottom gates and the thin layer of oxide insures that the potential of the top gate follows the potential

of the bottom gate.

2.4 Bulk and contact switching

The independent gating scheme allows to study the transport properties of a nanowire Schottky Barrier Field Effect Transistor SB-FET in its different regimes of operation and to discriminate transport mechanisms occurring in the channel and on each of the contacts. This is an advantage with respect to single-gate nanowire SB-FETs [27] where the gate field acts at the same time on the contacts and on the channel. Following the process flow described in fig.(2.5) I have fabricated devices with two or three gates. Fig.(2.7) shows an SEM micrograph of a device in which an additional thin top gate called in the following plunger gate is patterned for gating the middle portion of the nanowire.

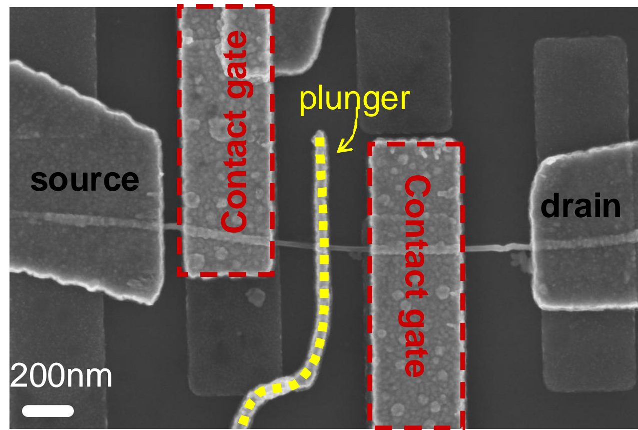

Figure 2.7: *SEM micrograph of a Silicon nanowire (diameter $d \approx 35nm$) device with three independent addressable gates at the contacts (dashed red boxes) and in the middle portion of the nanowire (dashed yellow line). The injection of carriers at the source and drain Schottky contacts is controlled by two surround gates while a thin ($\approx 70nm$) plunger gate controls the channel potential*

Fig.(2.8) shows the output characteristic of the device in fig.(2.7) when we operate the gates at the contacts and the inner plunger gate independently. The transistor action is different according to different dominating transport mechanisms. When the voltages of the contact gates (black curve fig.(2.8)) are swept together towards negative values, while leaving the plunger grounded, current in enhanced by the increased field emission of holes through the contact Schottky barriers as for a normal p-type SB-FET. Once the contact gates are left to a sufficiently negative bias $V_{GS} = V_{GD} = -2V$, carriers are injected from the contacts by tunneling through the SB and populate the portion of the device controlled by the plunger. Now transport can be controlled by the plunger gate which in this case can deplete the channel populated by holes (red curve fig.(2.8)). Two important features are evident from fig.(2.8): 1)the contact swiching leads to a slow saturation for large gate biases, due to a tunneling dominated transport through the contact Schottky barriers; the channel starts to become populated by the carriers and consequently the movement of the bands operated by the contact gates slows down [1]

2) as soon as the contact gates are polarized to turn the transistor into the on-state, the plunger gate can no longer enhance the current through the device which is fully controlled by the transmissivity of the contacts. The plunger gate can in this case only deplete the channel posing a potential barrier to the carrier flow. In this configuration the device operation is more similar to conventional p-type MOSFETs working in depletion mode. We can define this behaviour as 'bulk' switching as opposed to the 'contact' switching mode where on and off states of the transistor are set by the onset of field emission through the contact Schottky barriers [2]. Note how the linear region in the transconductance plot of fig.(2.8) (red curve), where the subthreshold slope for bulk switching is extracted, extends over five orders of magnitude in current, and also the change of the threshold voltage towards a more positive value. The transistor of fig.(2.8) shows very good performances in terms of subthreshold slopes as low as ≈ 173mV/decade and ≈ 134mV/decade for contact and bulk switching respectively, I_{on}/I_{off} ratio and current densities. Hysteretic effects don't change significantly the switching behaviour for the contact and bulk switchings. The threshold voltages are always negative in the case of contact switching and positive for the bulk switching. They disappear completely in the case of bulk switching if measurements are taken under vacuum.

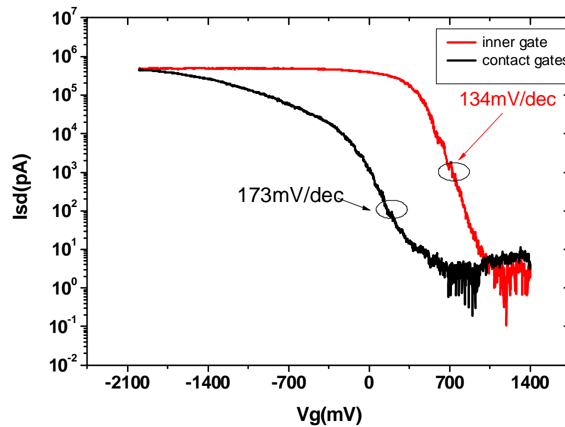

Figure 2.8: *Transfer characteristics of the device in fig.(2.7).The curve in red is the current through the device taken as a function of the potential applied to the contact gates $V_{GS} = V_{GD}$ while leaving $V_P = 0$. The red curve is taken by leaving the contact gates polarized at $V_{GS} = V_{GD} = -2V$ and sweeping the plunger gate. In all the measurements $V_{SD} = 100mV$. Subthreshold slopes extracted in the linear region of the transfer characteristics are ≈ 173mV/decade and ≈ 134mV/decade for contact and bulk switching respectively. Maximum conductance and current density at the saturation are $G \approx 570\mu S$ $j_d = 0.06MA/cm^2$ respectively. All the measurement are taken at room temperature in ambient pressure.*

2.5 Barrier height estimation

2.5.1 Plunger gate barrrier

The device described so far has two switching behaviours, one dominated by the injection of the carriers at the source and drain contacts through tunneling and another one governed by the channel potential barrier modulated by the plunger gate. Fig.(2.9) shows

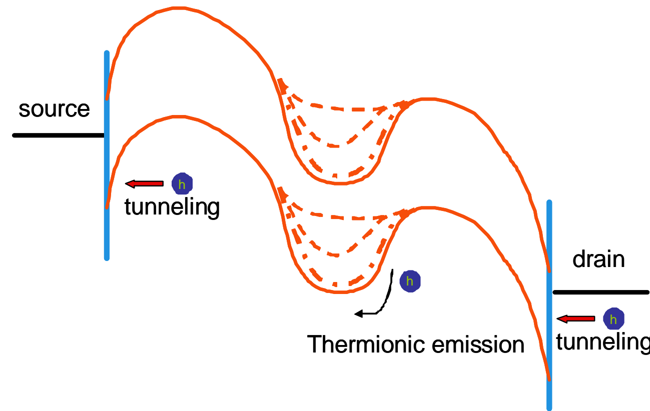

Figure 2.9: *Schematic diagram of the band bending for $V_{SD} < 0$ at the contacts and in the channel due to the combined action of both contact and plunger gates. The contact gates control the band bending at the source and drain while the plunger gate controls the bulk. If the source potential is sufficiently large and negative the current saturates as a consequence of a thermally activated transport across the bulk potential barrier controlled by the plunger.*

the qualitative band diagram of the device following the application of large negative voltages to the contact gates and for different values of the plunger gate voltage. The extraction and injection of carriers to and from the contacts is particularly efficient due to the suppressed SBs. In this regime transport through the device is controlled by the plunger gate. The potential barrier created by the plunger gate can be surmounted by the holes through thermionic emission since direct tunneling is strongly hindered by the large effective mass of the holes and by the rather large width of the tunnel barrier (the plunger gate is $70nm$ wide). Fig.(2.10) shows a series of IV characteristics as a function of temperature for a particular plunger gate gate voltage. The source-drain current tends to saturate for negative values of the source-drain bias voltage. Also, the current raises with temperature revealing that the scattering in the channel is not the limiting process and that transport is in fact thermally activated. In this regime the potential applied across the device is mainly dropping on the region which is controlled by the plunger gate since at the two contact junctions the barriers are strongly reduced due to tunneling. To quantify the height of the potential barrier created by the plunger gate we performed temperature-dependent transport measurements in the $100K \div 260K$ range. Temperature was increased in steps of 10K and, for each temperature the thermally activated current through the device was measured as a function of the plunger gate voltage. The values of the current measured at a fixed bias voltage $V_{SD} = -1V$, were

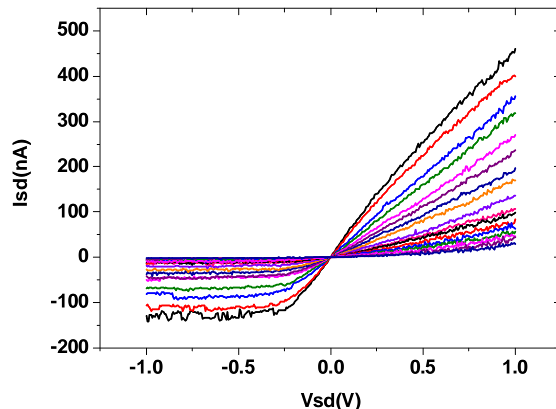

Figure 2.10: *IV characteristics for a fixed plunger gate, $V_{plunger} = -480mV$ from $100K \div 260K$ in steps of $10K$. Temperature is increased from the dark blue curve to the black curve. The current plateaus for negative bias correspond to a transport mechanism dominated by thermionic emission over a plunger gate dependent potential barrier. All the measurements are taken with a fixed polarization on the two contact gates $V_{GS} = V_{GD} = -3.2V$.*

fitted to an Arhenius plot fig.(2.11)

$$\ln \frac{I}{T^2} = \ln(SA^\star) - \frac{q\phi_{V_P}}{K_B T} \tag{2.4}$$

where ϕ_{V_P} is the plunger gate dependent barrier height in the middle of the channel, $K_B = 8.617eV/K$, $A^\star$, and S being the Boltzmann constant the Richardson constant and the conducting nanowire section respectively.

Fig.(2.12) shows the transfer characteristic of the transistor operated in the bulk switching mode with the contact gates negatively biased and the extracted values of the barrier height obtained in the saturation regime at $V_{SD} = -1\text{V}$. The extracted barrier height values tend to saturate for values of the plunger gate $V_P \approx -1500\text{mV}$. In this regime the channel resistance becomes more important and the activation energy method is no longer applicable. As the plunger gate voltage is made less and less negative the barrier height tends to increase with the same subthreshold slope as predicted by equation(2.4) and for $V_P = 0\text{V}$ reaches a value of $\approx 0.13\text{meV}$.

2.5.2 Contact Schottky barriers

It is clear from the above discussion how transport in SiNWs is governed by the presence of different potential barriers, the SBs at the contacts and the barrier in the middle of the depleted channel. along the channel. The geometry of our device with three independently addressable gates enables us to study the main dominant transport mechanisms occurring in the same device, at the contacts and in the bulk, and by varying the potentials applied to these split gates we can give a quantitative estimation of all the barrier heights eventually present. Up to now our discussion has been restricted to the bulk of the device giving an estimate of the plunger gate voltage corresponding to the flat band

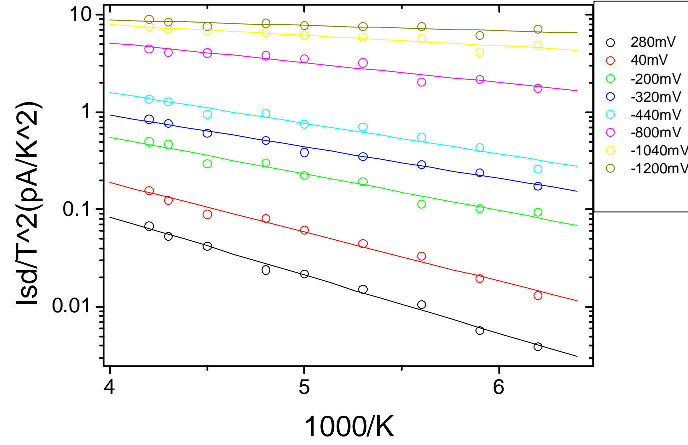

Figure 2.11: *Arrhenius plots for the extraction of the plunger gate barrier*

condition. We can use this information to extend the same procedure of barrier height extration to the Schottky contacts.

By simultaneously suppressing one of the contact barriers (e.g. at the source contact) and the channel barrier, current transport becomes entirely dominated by the other SB (e.g. that of the drain contact). This is apparent in fig.(2.13) which shows I-V characteristics of the device taken by polarizing together with the plunger one, or both contact gates at the same time. Fig.(2.13) shows how, with the help of the contact gates and the plunger we can modify the behaviour of the device switching it from an ohmic resistor(with all the three gates polarized to negative voltages) to two Schottky diodes by using only one of the two contact gates polarized at a sufficiently negative potential to render ohmic the correspondent Schottky contact. With all the three gates polarized there are no barriers for current flowing and the device has an ohmic behaviour, but when only the drain(source) gate contact is polarized with a negative voltage, holes can be injected from the drain(source) side and collected by the source(drain) contact depending if this contact is at a negative(positive) voltage with respect to the other. On the other hand when the source(drain) terminal is at a negative(positive) potential with respect to the drain(source), holes are blocked by the rather large Schottky barrier present at the correspondent metal-semiconductor junction and transport is therefore strongly suppressed. The device is then behaving like a Schottky diode with the current plateaus corresponding to the reverse bias saturation current of the source or the drain Schottky diodes. The reverse saturation current of each of the source or the drain diodes is directly related to the barrier height which in turn can be modulated by the contact gate. For each value of the contact gate the thinning of the barrier and the subsequent increasing of the tunneling current gives rise to a lowering of the effective barrier height [3]. Again, by looking at the evolution of the saturation current of the reverse biased junction diode with respect to the temperature we can study the thermally activated current over the barrier and extract as a funtion of the gate the effective barrier height for each of the two SB contacts. An activation energy method was again employed by

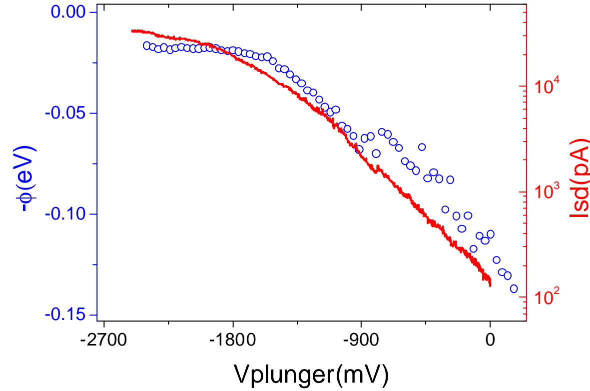

Figure 2.12: *Extracted barrier heights as a function of the plunger gate (blue curve) and the transfer characteristic of the transistor (red curve) taken with $V_{SD} = 100mV$ and $V_{GS} = V_{GD} = -3.2V$ at room temperature and in a vacuum tube at a pressure of 10^{-6}mbar.*

measuring the leakage current through the reversed-bias Schottky diode at the source and drain contacts by temperature dependent measurement between 300K to 370K in steps of 10K. This is shown in fig.(2.14) where are represented the extracted barrier heights from an Arrhenius plot as a function of the corresponding contact gate.

As is evident from fig.(2.13) the two current plateaus corresponding to the reverse bias saturation currents for the drain and source Schottky diodes differs by more than one order of magnitude reflecting the fact that in the same device the two contact barriers can be different. This is also seen in fig.(2.14) where although the two curves have the same slope revealing identical couplings with the surrounding gates they have different intercepts to the zero voltage gate axis which translates in two different barrier heights at zero gate voltage. The limited temperature range of our setup prevented the extration of the barrier height in the vicinity of zero gate axis for the source contact where the thermally activated currents are strongly suppressed, but a linear extrapolation allows for an estimation of the actual barrier height which for the drain Schottky barrier is around 0.35eV while for the source 0.45eV. The validity of this approximation is further confirmed by looking at the ratio between the two reverse saturation currents for the source and drain diodes taken from the green and the blue curves in fig.(2.13), which according to equation 2.4 reads

$$\frac{I_{sourcediode}}{I_{draindiode}} \propto \frac{\exp -\frac{\phi_{sourcediode}}{K_B T}}{\exp -\frac{\phi_{draindiode}}{K_B T}} \approx 0.02$$

having used $\phi_{draindiode} = 0.35eV$ and $\phi_{sourcediode} = 0.45eV$. The measurements of fig.(2.14) were obtained by taking IV characteristics in the voltage ranges of interest $V_{SD} \in [0, +1V]$for the source Schottky contact and $V_{SD} \in [0, -1V]$ for the drain contact. To avoid hysteretic effects observed when ramping gate voltages up and down on relatively short time scales (typically of the order of minutes) [13], measurements were carried out by ramping temperature at fixed gate voltages. The gate voltage controlling the SB under investigation was varied in small steps between successive temperature sweeps. It's

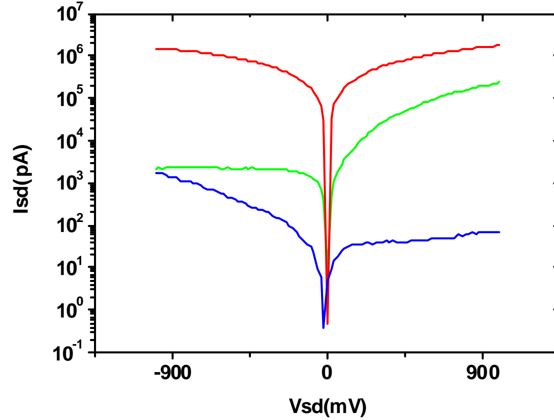

Figure 2.13: *$I_{SD}-V_{SD}$ characteristics for the source (blue) and drain (green) Schottky diodes taken with a fixed polarization $V_{Plunger} = -2500mV$ on the plunger gate so as to suppress any barrier in the middle of the channel. The blue curve is obtained with $V_{GD} = -3.2V$ and $V_{GS} = 0V$ while the green one is obtained with $V_{GS} = -3.2V$ and $V_{GD} = 0V$. The red curve correspond to the ohmic case with all the three gates polarized $V_{GD} = V_{GS} = -3.2V$, $V_{Plunger} = -2500mV$*

worth to point out here that the observed discrepancies between the values of the two SB could be due to mesoscopic fluctuations and that this should be taken into account when designing scaled Schottky barrier MOSFETs.

2.5.3 Low temperature carrier injection

Through this local gating approach we are able to give an estimation of the gate dependent barrier heights at the contacts and in the device channel. In particular fig.(2.12) and fig.(2.14) have shown that if the control gates are set to sufficiently negative values, all of these barriers can be made negligibly small. The complete vanishing of the barriers is further confirmed by low temperature measurements taken at $T = 4$K. At such low temperature a measurable current can flow through a cooperative action of the split gates. Fig.(2.15) shows a measurement of the source-drain current as a function of the plunger gate voltage at 4K with a polarization voltage $V_{SD} = 100$mV. When the contact gates at sufficiently negative potential $V_{GS} = V_{GD} = -3.2$V to allow for carrier injection and extraction through tunneling, transport through the device is inhibited by the residual channel barrier of ≈ 130meV which cannot be sourmounted by holes having a thermally broadened energy of ≈ 0.3meV. As soon as also the plunger gate becomes sufficiently negative, transport can take place revealing a sequence of current peaks arising from tunneling of the carriers through a series of islands of localized holes connected in series. This series of islands may arise due to surface induced potential fluctuations along the channel and/or to defects. The role of the plunger gate is then to modify electrostatically the energy level arrangement between the quasi 1-D localized hole gas.

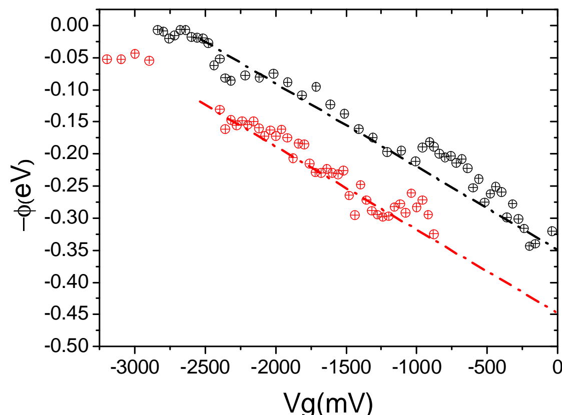

Figure 2.14: *Extracted effective barrier heights from the Arrhenius plots for the two Schottky contacts as a function of the corresponding gate. The intercepts to the zero gate voltage axis are the SBH for the source and drain contacts and they differ by* $\approx 100meV$*. Dashed lines are guide to the eye.*

2.6 Multifuction circuits

2.6.1 pn junction

The extracted values for the source and drain Schottky barriers heights are in close agreement with the reported values in the literature [14], [16],[20],[22], [6] for bulk junctions. Small deviations are sample dependent and could be ascribed to surface contaminants or interface defects formed during the fabrication process, which can alter the SB height. Variations in the barrier height can change the switching behaviour of the nanowire transistor from unipolar, like the one described so far, to ambipolar, in which transport of electrons and holes can be observed at positive and negative gate voltages, respectively. This is a direct consequence of the fact that the sum of the barrier heights for electrons and holes is the corresponding bandgap, so then an increase(decrease) of the barrier height for holes implies an equal decrease(increase) of the barrier for electrons. Fig.(2.16) shows the output characteristic of a device similar to that in fig.(2.6) which exhibits ambipolar behaviour. The price to pay for an activation of an electron-type conduction mode is a reduction of device performances, (e.g. the on-current and the subthreshold slope) in the hole type transport regime. This is due to the increased SB height for holes. The subthreshold slopes, $d\,|\log I_{SD}/dV_{GD}|$ extracted from fig.(2.16) are 354mV/decade and 438mV/decade for the hole and electron branch, respectively. These anomalously large values suggest a larger density of surface trap states, possibly due to an incomplete oxygen saturation of the silicon dangling bonds. The switching behaviour is governed by the two contact gates that enable transport of holes through the valence band for negative gate bias and transport of electrons through the conduction band for positive polarizations. A more interesting behaviour is instead observed when the two gates are polarized at opposite voltages. Fig.(2.17) shows that the device in this case behaves like an electrostatically doped *pn* diode. In the forward bias polarization the

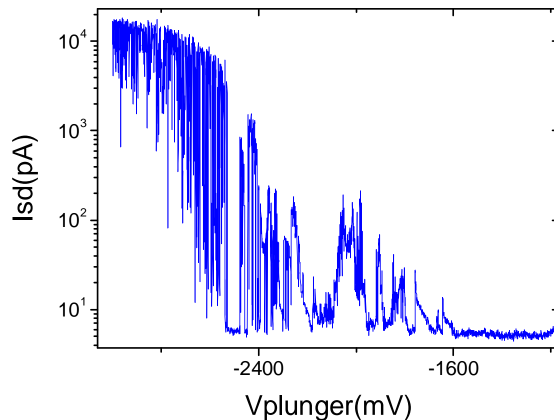

Figure 2.15: *$I_{SD} - V_{Plunger}$ characteristic at $T = 4K$. Transport is activated for a plunger gate voltage $V_{Plunger} < -1600mV$ where the residual barrier can be made neglibly small. $V_{SD} = 100mV$*

side of the nanowire populated with holes has a higher electrochemical potential than the side populated by electrons. The barriers created by the split gates becomes smaller and can be surmounted by thermally activated carriers. This results in a diffusion current of holes from the p-lyke to the n-like region and an electron current in the opposite direction. The two diffusion currents add up to give the overall forward current. In the case of reverse bias polarization, transport of electrons and holes is hindered by the high potential barriers created by the gates leading to a negligible current. As opposed to the case of a bulk junction, here the built-in potential arise because of the gradient in the free carrier population obtained through electrostatic doping of an undoped semiconductor and not on the potential of the fixed ionized impurities belonging to a space charge region. The rectifying behaviour is far from being ideal mainly because the split gates partially overlap the contact regions leaving the central part of the channel poorly affected by the doping fields, the resulting doping profile is far from being abrupt like in conventional diodes and a substantial recombination might take place in the channel between the two gates [18],[21].

2.6.2 Logic gate with gain

We have seen how starting from a single undoped nanowire we can add by locally gating the junction regions different functionalities due to the peculiar transport mechanisms taking place through the Schottky barrier. The interests in combining some of these functionalities together stems from the fact that it is possible in this way to build more complex circuits capable to implement logic functions which are the basis of computation. In conventional planar silicon technology the three big families of logic gates (Diode-Transistor-Logic, Transistor-Transistor-Logic and Resistor-Transistor-Logic) assemble together the basic circuital building blocks like transistors and diodes to perform the logic operations. Logic gates built from carbon nanotubes and nanowires have already

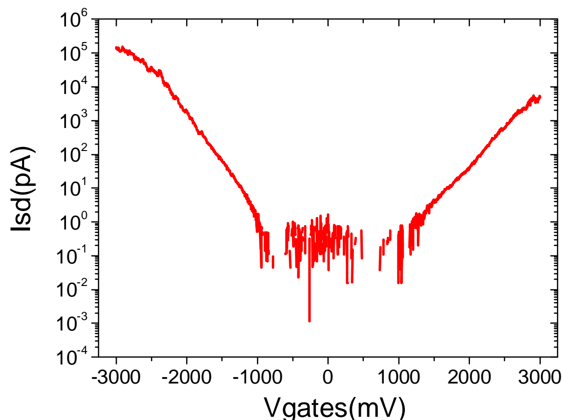

Figure 2.16: *Room temperature output characteristic of the transistor. Measurement is taken with* $V_{SD} = 500mV$. $V_{gates} = V_{GS} = V_{GD}$

been reported [5], [12], [10], [15] along with more complex circuits like ring oscillators [7] which extends the digital operation in the high frequency domain. All the reported devices adopt a complementary assembly of p and n type nanowire building blocks or nanotube transistors integrated together, which require sequential and hyerarchical processing. Here we demonstrate the implementation of a logic gate making use of a simple assembly of two intrinsic nanowires controlled by local gates acting at the contact junctions. This approach doesn't require a complementary doping thereby simplifying the device processing. The most important logic gate is the NAND gate which is a combination of AND and NOT operations. A NAND gate accepts at its inputs two different voltage levels corresponding to the binary characters 0 and 1. In our circuit a logical 0 corresponds to the voltage level $V = 0V$ while a logical 1 corresponds to the voltage level $V = -1V$. The truth table of a NAND gate is shown in table 2.1.

inputs (V_1,V_2)	output
(1, 1)	0
(1, 0)	1
(0, 1)	1
(0, 0)	1

Table 2.1: *Truth table for the NAND logic gate*

To implement such an operation starting from dual-gate nanowires we used an architecture comprised of two stages as shown in fig.(2.18): one stage hosting the two voltage inputs and the second stage acting as a feedback to force the output of the logic gate. The input stage is a dual-gate nanowire with the two input lines feeding the two contact gates; this input stage is then connected to the feedback stage consisting of another nanowire which has one of the contact gates at a fixed negative polarization while the second one is connected to the output of the logic gate to serve as a feedback. Each

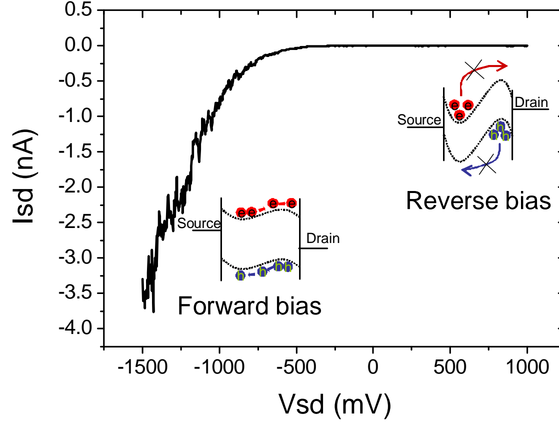

Figure 2.17: *IV characteristic showing the rectifying behaviour of the device working as a p-n diode and schematics of the band bending in forward and reverse bias. The measurement is taken with $V_{GS} = 2V$ and $V_{GD} = -2V$.*

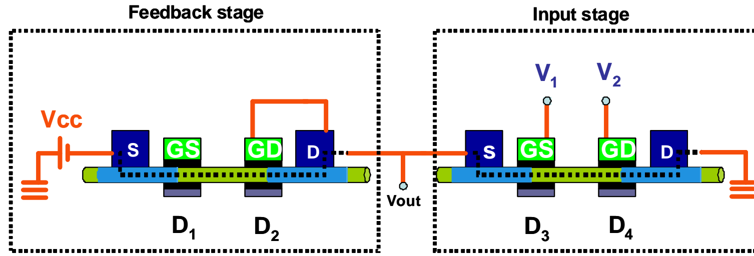

Figure 2.18: *Schematics of the circuit. $V_1$and V_2 represent the input voltages. $D1$,$D2$,$D3$,$D4$ correspond to the interfaces between the Nickel silicide and the silicon and are represented as Schottky diodes. The gate voltage controlling $D1$ is kept at a fixed value $V_{GS} = -3V$. The alimentation voltage is $V_{cc} = -1.5V$*

of the nanowires can be represented by a series of two back to back Schottky diodes called as $D1$,$D2$,$D3$,$D4$ each diode being associated with the gated interface between the nickel silicide and the silicon channel. Each diode is addressed by a corresponding gate which controls the transport at the interface. From a circuitry point of view each of the stages of the logic gate can function as a transistor or as a rectifying diode depending on the voltages applied to the control gates. For instance, when the two input gates controlling $D3$ and $D4$ are at logical 0 the input stage is highly resistive because the transistor is in the off state. As a consequence the bias voltage, V_{cc}, falls mostly across the input stage and the output terminal acquires a value $V_{out} = -1.2$V corresponding to a logical 1. The presence of an electrical connection between the output terminal and the control gate for D2 produces a positive feedback. In fact, a negative value on the contact gate suppresses the corresponding Schottky barrier, making the impedance of the feedback stage lower hence forcing the approach of V_{out} to V_{cc}, i.e. logical output 1. When, on the contrary, the input gates are at logical 1 the input stage transistor starts

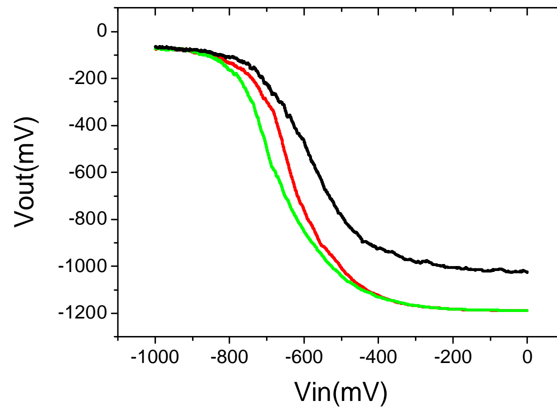

Figure 2.19: *Output characteristic of the logic gate as a function of the logic address level input. Black curve:* $V_{in} = V_1$, $V_2 = -1V$ *corresponding to the transition from the address level inputs* $(1,1) \leftrightarrow (0,1)$*; red curve:* $V_{in} = V_2$, $V_1 = -1V$ *corresponding to the transistion* $(1,1) \leftrightarrow (1,0)$*; green curve:* $V_{in} = V_1 = V_2$*; corresponding to the transistion* $(1,1) \leftrightarrow (0,0)$.

to conduct and the bias voltage falls mainly on the feedback stage, corresponding to an output voltage $V_{out} \approx 0$ (logical 0). Because of the feedback line, $V_{out} \approx 0$ makes the impedance of D2 high reinforcing the impedance of the feedback as opposed to that of the input stage therefore favouring the approach of V_{out} to 0, i.e. to logical output 0. At the intermediate regimes when one of the two input gates is at logical 0 and the other is at logical 1 one gated Schottky junction is suppressed while the other is not. In this case, the presence of the feedback line is crucial in producing a stable configuration with $V_{out} \approx -1$V, i.e. logical output 1. In fact, under this condition both of the SBs at D1 and D2 are suppressed leading to a lower impedance of the feedback stage as compared to the input stage. Since in actual logic gates the output of one gate can serve as the input of another gate, an important figure of merit of each logic gate is its gain, defined as the slope of the linear portion of the output characteristic. A high-gain logic circuit has the capability to drive another circuit without the need of signal restoration. From the data in fig.(2.19) we can extract a gain between 2.6 and 4.7. Another important thing to note is that our circuit is working at lower voltage levels as compared to other similar logic gates built from nanowires [10], [15], which translates in lower static power dissipation.

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Chapter 3

Silicidation by Joule effect

3.1 Silicidation by Joule effect

The thermal annealing process described in chapter 1 has its limitations in the poor control of the solid state reaction between the metal and the silicon which leads to the formation of the metal silicides. We can only infer average quantities with respect to the length of the silicides formed. We already concluded that the relative error in the lengths of the silicides is partly due to a spread in the wire diameters. This, together with other extrinsic factors (e.g. inhomogeneities in the surface oxide), prevents the possibility to achieve an accurate control of the silicidation process with minimal fluctuations between devices. This becomes particularly critical if one intends to define channel lengths in the range of a few tens of nanometers. Reducing the uncertainties in the silicides formation could be accomplished by a finer control on the dispersion of the wires diameter which are determined by the catalyst size. But also in this case fluctuations between devices cannot be avoided to other factors such as inhomogeneities and fluctuations in the surface structure of the nanowires (in particular the native oxide) and lithographic uncertainties. In this chapter a new method for the formation and control of the silicides in silicon Nanowires is presented. The method allows the formation and in-situ electrical control of the silicide phase. The thermal energy required to activate the protrusion of the metal species into the nanowire is provided by a local Joule heating of the contacts. This requires an appositely designed contact geometry enabling the flow of a heating electric current through each of the contacts. Upon measuring the current through the silicon nanowire during the silicide formation it is possible to control the length of the silicon channel between the silicided edges of the nanowire itself. This technique offers unique advantages as compared to conventional thermal treatments performed in an oven:

- the technique is not sensitive to the dispersion in wire diameters
- it allows the reproducible fabrication of ultrascaled transistors with channel lengths down to 10nm
- there is no need for searching optimum conditions regarding the time and the annealing temperature

- it can be easily extended to other contact metals that form silicides and, possibly, to any type of contact and nanowire or a generic nanostructure which requires an annealing step

Moreover by joule effect, the local temperature can be varied over a wider range and a faster time scale than what can be done with the oven. This is because the local temperature achieved on the contact follows almost instantaneously the value of the heating current. The technique was developed starting with a simple circuit depicted schematically in fig.(3.1a). The nanowires were contacted with metallic striplines connected lithographically to macroscopic bonding pads. These striplines defined by optical lithography are then current biased in order to locally generate thermal energy by Joule effect. The power dissipated in a generic circuit comprising a resitance subjected to a potential difference ΔV between its two terminals is simply given by $P_{Joule} = \Delta V i$. Due to the microscopic dimensions of the circuits we are dealing with, it is more convenient to introduce a local power density $P_{Joule}(\vec{r}) = J^2\rho$ with J being the modulus of the current density vector, and ρ the resistivity of the metal. It is then clear that the power dissipated in the circuit is actually dominated by the regions with higher current density. Due

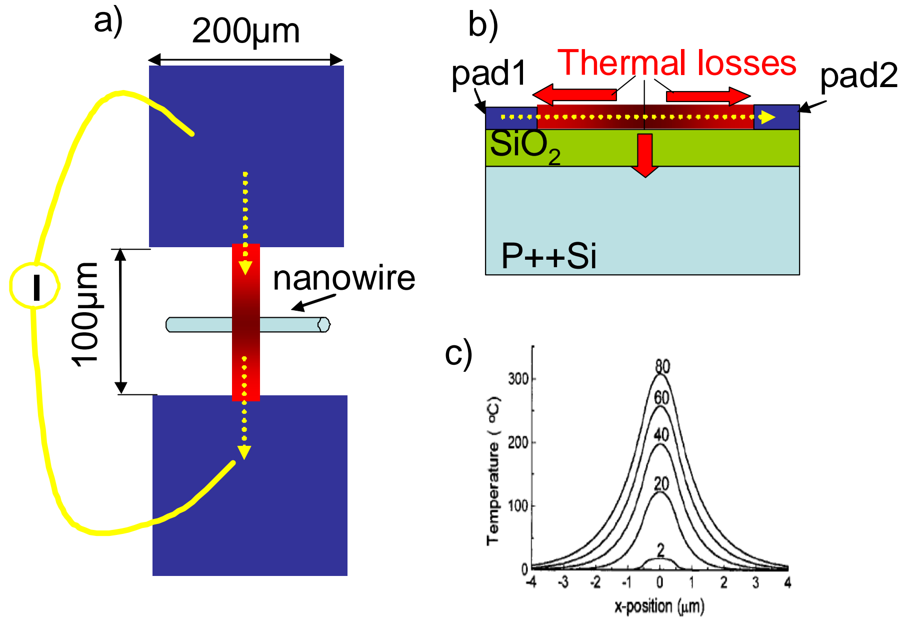

Figure 3.1: *a)Schematic view of the samples defined by optical lithography: two large bonding pads are linked by a 2μm wide stripline. The bonding pads are attached to an external current generator driving a fixed current in order to heat by Joule effect the stripline which contacts a nanowire. b) The thermal losses of the Joule heated stripline are towards the large bonding pads acting as thermal reservoirs and to the substrate. c) Calculated solutions of the heat equation 3.1 showing the temperature profile along a 20nm thick 1μm long Au stripline carring $2 \times 10^{12} Am^2$ for several oxide thicknessess (Adapted from ref.[5])*

to the shape anisotropy between the bonding pads and the stripline, the current density in the part of the circuit comprising the bonding pads and the macroscopic bonding wires is orders of magnitudes lower than the current density in the stripline. This means

that the external circuit contacting the stripline can be regarded thermodynamically as a thermal bath at temperature T_0 while a thermal gradient develops very locally on the stripline. The actual profile for the thermal gradient can be found by solving the heat equation for the system. At equilibrium, denoting κ the thermal conductivity of the stripline the temperature profile $\Delta T(\vec{r}) = T(\vec{r}) - T_0$ obeys the equation [5]

$$-\kappa \nabla^2 \Delta T + \gamma \Delta T + \frac{J^2(\vec{r})\rho}{k} = 0 \tag{3.1}$$

This equation describes the temperature profile in the stripline subjected to a local Joule heating source delivering the input power density $P_{Joule}(\vec{r}) = J^2(\vec{r})\rho$ taking into account a rate of energy losses to the contacts, described by the term $-\kappa\nabla^2\Delta T$ and to the substrate by the term $\gamma\Delta T = \Delta T \kappa_{sub}/td$, with κ_{sub}, being the thermal conductivity, d the thickness of the substrate, and t the thickness of the stripline. The actual solution of this equation depends on the boundary conditions of the problem and on the values for the thermal conductivities of the substrate and the stripline. The first one will affect the rate of power losses to the substrate. It is reasonable to think that at the contact region of the stripline with the bonding pads the temperature profile as well as its derivative are continuous. Moreover at the center of the stripline the net thermal flow is towards the substrate, since due to symmetry, equal amounts of heat will flow towards the ends of the stripline which are thermodynamically at equilibrium with the bath. Actual solutions of the equation3.1 have been proposed, [5],[8],[7], by solving the heat equation with the boundary conditions stated above. Some qualitative conclusions can be drawn following the reported literature and can be summarized as follows:

- the temperature is maximum at the center of the stripline and falls symmetrically towards the edges
- the temperature profile depends on the coupling of the stripline to the substrate, if the power losses are mainly to the substrate the temperature profile will be uniform
- for a given current density the temperature profile depends both on the stripline thickness and length

These facts underline the importance of the stripline geometry. Important parameters in the problem are then the stripline width, length and thickness which affect not only the dissipated power density but also the power losses. Ideally one wants to minimize the power losses to the substrate in order to achieve a very localized heat dissipation.

3.2 Current driven experiments

The early experiments were conducted in order to confirm the possibility to have on a stripline enough thermal energy to promote the silicidation process on a nanowire. The nanowires were dispersed randomly on the substrate and contacted randomly by nickel striplines fabricated by optical lithography. The striplines had typical widths of 2μm and lengths of 100μm and were connected to large bonding pads fig.(3.1a).

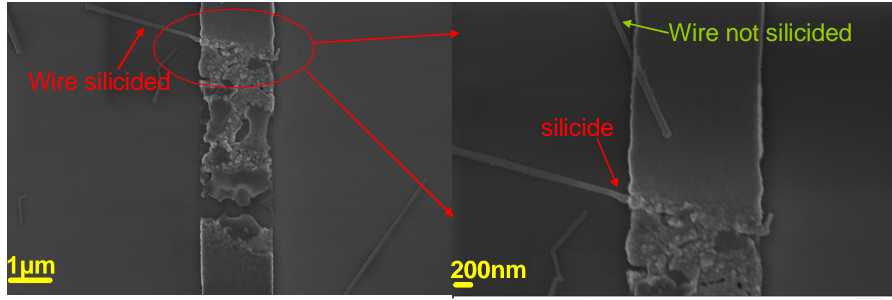

Figure 3.2: *a) SEM micrograph of a nickel stripline defined by optical lithography which broke up near its middle point due to severe Joule heating. b) Magnified view of the region close to the break. Before the break occurred the local increase of the temperature was sufficient to cause the silicidation of the nanowire lying beneath the metallic line in the proximity of the breaking point. At the same time a second nanowire lying further away and indicated by the green arrow remained apparently unaffected.*

Fig.(3.2) shows a SEM micrograph of a typical device fabricated with optical lithography. The current was gently ramped up to a value of 28mA corresponding to a current density $j = 1.16 \times 10^{11}\mathrm{A/m^2}$, for which the stripline failed due to severe Joule heating. The failure point is roughly placed in the middle of the stripline where the maximum temperature is expected. The thermal energy provided by the current was able in this case to promote the silicidation on one of the two wires found beneath the contact, precisely the wire lying closer to the midpoint of the stripline. The other wire, indicated by the green arrow, and located about $\approx 2\mu$m away from the first one doesn't show any sign of a metal silicide protrusion from the stripline denoting the presence of large thermal gradients along the stripline. This phenomenom was consistently observed on all the samples processed in this way. The silicidation of the wires was accomplished at the expenses of an irreversible circuit failure. The failure mechanism of the striplines is due to electromigration fig.(3.3)[2]. When a metallic stripline is electrically stressed at high current density, it heats up, and consequently the metal atoms become more mobile. The transport of mass is fueled by the current through momentum exchange of the carriers with the ions of the lattice and by the electric field driving the current. The net force acting on single ions is generally dominated by the 'electron wind' component since the electronic cloud shields the external electric field. The failure of the line is then provoked by voids formed in the metal due to an unbalance between the fluxes of masses leaving and entering the region of highest temperature where the ions are more mobile. Failure of the line can be caused also by the mechanical stress which develops due to mass transport and the actual failure mechanism will depend on the microscopic structure of the metal line. Current driven experiments are limited by a positive feedback acting on the power dissipation due to electromigration. The power density dissipated by joule heating is proportional to the resistivity of the stripline and this latter will increase if the stripline is subjected to microscopic modifications propelled by electromigration due to an increase of the density of scattering centers. As a consequence also the power dissipated will increase causing a runaway process that leads to the stripline rupture.

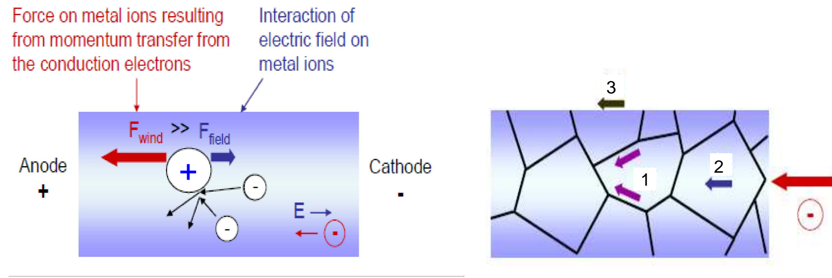

Figure 3.3: *a) Schematic representation for the phenomenon of electromigration. The metal ions become mobile under the action of an intense current density which increases locally the temperature. On the ions two forces are exerted one due to the external field applied and one due to scattering with electrons. b) Schematic view of a polycristalline metal. The mobile ions can follow paths along 1)the grain boundaries, 2) single grains 3) the surface.*

3.2.1 Electrical characterization of the striplines

Circuit failures caused by the irreversible modifications of the striplines were consistently achieved for current densities in the range $1 - 2 \times 10^{11}$A/m^2. The actual dispersion in the failure current densities can be ascribed to variations in the microstructure of the as deposited material. As an example, conventional household copper wires can sustain current densities up to 10^8A/m^2 before melting. The 3 orders of magnitude increase in the attainable current densities for these thin films are explained by the good thermal coupling with the substrate which acts as a heat sink. The limiting factor for obtaining high temperatures is not the melting point of the metal but the occurrence of electromigration. Deposition of the nickel electrodes was achieved by electron beam evaporation under a pressure of 3×10^{-7}mBar. The as deposited material is polycristalline and its conduction properties depend on the spatial arrangement of the grains. As the metallic wire is stressed by passing a current through it, the thermal energy dissipated can cause a spatial rearrangement of the single grains, consequently the overall resistance of the wire can change irreversibly due to the modification of the contact area between neighboring grains. The transmission probability of the electronic waves impinging on the grain boundaries can either increase or decrease due to the growth or restructuring of the grains. This is particurarly evident in the case of our nickel striplines. Fig.(3.4) shows a typical plot of the resistance as a function of the total dissipated power. The plot was obtained by gently ramping the current (provided by a Keithley 6430) up to 30mA where the resistance started to decrease. The ramping rates were chosen sufficiently slow to ensure constantly an equilibrium state for each value of the driving current. The constant Joule heating of the metallic line caused a considerable lowering of about 15% of its resistance and a consequent decrease of the power dissipated with a constant current. Once the new equilibrium value for the resistance was reached the stressing current was slowly ramped to zero. The measured resistance undergoes irreversible changes driven by the current which has the effect to heal the microscopic grain structure of the as-deposited metal line [16],[10],[14]. Importantly, these changes affect only the overall resistance while the slope of the curve doesn't change for the two directions of the ramp.

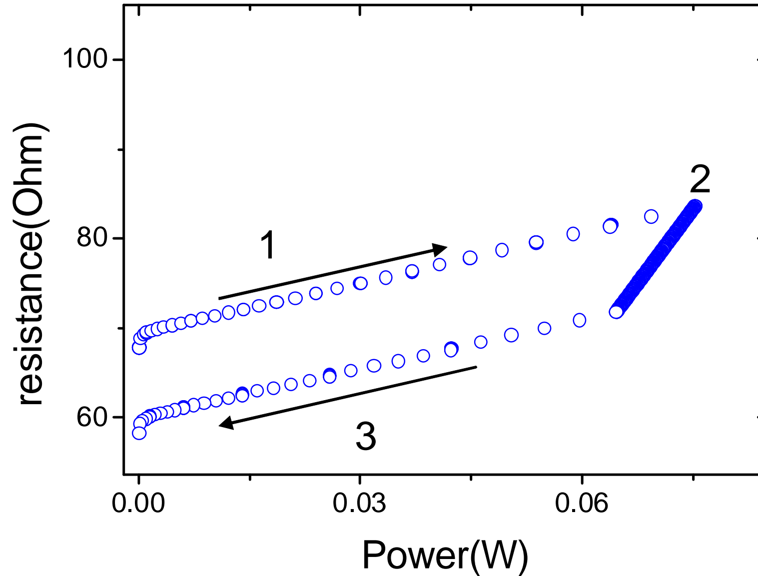

Figure 3.4: *Resistance of a typical stripline defined by optical lithography as a function of the power dissipated. 1. The current is ramped up by a current generator and the resistance increases due to Joule heating 2. For a fixed driven current of* 30*mA the resistance shows a transient behaviour and starts to decrease as a function of time. 3. Once the new equilibrium value is reached the current is ramped down to zero.*

As is evident from the plot in fig.(3.4), the resistance is proportional to the dissipated power as expected for a reversible process. As the current is increased the stripline heats up and its resistance increases in a reversible way up to a certain value of the driving current which activates a substantial restructuring of the grain boundaries.

3.3 Constant voltage biasing and measurement apparatus

To avoid thermal runaway phenomena conducting to a rapid and incontrollable failure of the circuits, we employed a different current stressing scheme based on constant voltage biasing [11]. The constant voltage biasing has the advantage to mitigate the irreversible phenomena leading to the circuit failure ascribed mainly to electromigration. In fact if in some part of the stripline there is a local increase of the resistance due to the formation of defects, the current is correspondingly reduced limiting at the same time the dissipated power. This negative feedback mechanism allows a better control of the process expecially for the high current densities required to have a substantial increase of the local temperature capable to promote the silicidation process. Voltage-biased experiments were mainly conducted on striplines defined by e-beam lithography. This has two advantages: it allows to custom define the shape and geometry of the overall metallic

line and it enables contacts to single nanowires. Controlling the shape of the stripline used for contacting the nanowires is of capital importance if one intends to achieve a highly localized heating. A key requirement in the geometry of the striplines is to have a high aspect ratio between the portion of the metallic contact defined on the nanowire and the connecting lines to the large bonding pads. This shape anisotropy ensures that the local current density $J(\vec{r})$ is sharply peaked in close proximity of the contact region. In fact nickel striplines were designed in order to have a constriction right on top of the silicon nanowire crossed by the stripline. The typical length and width of the constriction is around 3μm and 500nm respectively. The width of the stripline is gradually increased away from the contact region in order to have the maximum dissipation power at the location of the nanowire. To obtain a better control of the silicidation we adopted the electrical circuit described in fig.(3.5). Each nanowire is contacted with two nickel striplines: a first stripline is used to promote the silicidation by joule heating and simultaneously polarize with a bias voltage the nanowire, while one terminal of the second stripline is connected to an amperometer. This circuit enables an electrical control of the silicidation process and it is based on the capability to drive a tunable current through the first stripline to induce Joule heating, and to independently apply an adjustable voltage bias across the nanowire. The heating current and the potential applied are decoupled in the sense that we can vary the bias potential on the nanowire while keeping fixed the heating current. In a first attempt I used Keithley sources to apply two independent voltages at the edges of the striplines. However, these sources appeared to be insufficiently stable and presented electrical spikes capable of destroying the samples. Therefore, I used a homemade electrical circuit which I designed with the help of the electrical engineers of the SPSMS. This circuit is represented in fig.(3.5). Two

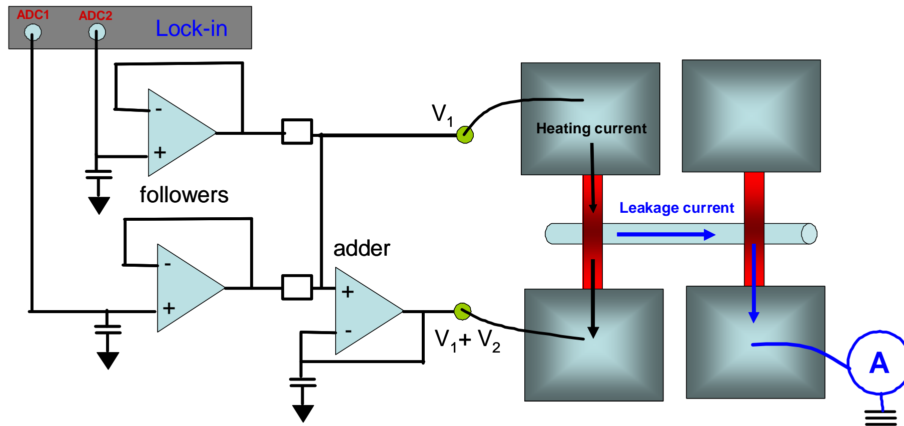

Figure 3.5: *Schematics of the experimental set-up used to decouple the heating voltage used to drive the heating current through the stripline from the biasing voltage falling on the nanowire. The heating current and the biasing voltage can be varied independently allowing a simultaneous measurement of the leakage current flowing into the nanowire as a function of the heating current and the bias potential.*

independent voltages V1 and V2, obtained by the auxiliary DACs outputs of a lock-in amplifier (7265 Signal Recovery), are fed in the circuit through two op-amp followers. In this way, they can be decoupled from the ground since the input impedance of the op-amp is very high, giving an effective isolation of the output from the signal source.

The two signals are then summed up by the summing amplifier. The output consists then of two voltage levels $V_A = V_1$ and $V_B = V_1 + V_2$. The edges of the first stripline used for heating are then connected to these two voltage levels. The circuit is battery operated and can be linked to the same ground of the amperometer which measures the leakage current flowing into the nanowire during Joule heating. It is important to point out here that the biasing potential across the nanowire is well defined in case the overall resistances of the lines comprised between the contact to the nanowire and the lead connected to one of the two potentials V_A or V_B are not very different.

3.3.1 Temperature estimation

Following the model of heat transport described by equation 3.1 the actual temperature profile is largerly dependent on the source term $P_{Joule}(\vec{r}) = J^2(\vec{r})\rho$ describing the input power density from Joule heating. Although equation 3.1 can be solved in an idealized case when the stripline is forming the connection between two large electrodes acting as ideal thermal baths, the main departures from reality are related to the assumptions one makes on the functional form of the source term. In our case the source term has a smooth transition from the large pads to the constriction making the temperature simulation a difficult task. Moreover, in film subjected to high current densities, phenomena like electromigration and grain boundary reconstruction can give rise to microscopic modifications of the metal which could alter significantly its resistivity, and as a consequence the power dissipated. For high current densities the system is out of equilibrium and the system is described by the thermodynamics of irreversible processes. To estimate the temperature achieved by Joule heating we fabricated metallic striplines and measured their resistivity in a four-probe configuration. A SEM micrograph of a typical four probes device defined by e-beam lithography is shown in fig.(3.6a). The stripline

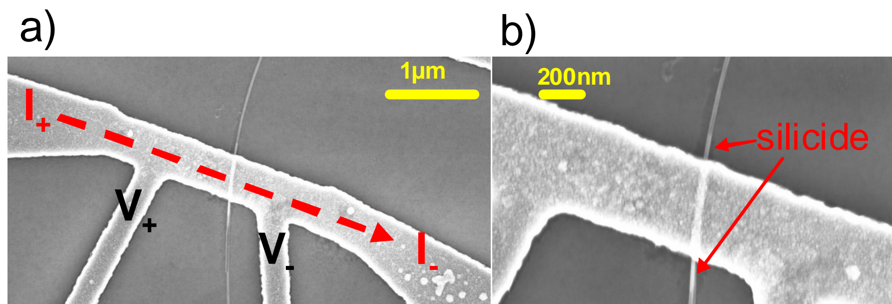

Figure 3.6: *a)SEM micrograph of a sample used for the temperature estimation of the stripline. The potential drop $V^+ - V^-$ falling between the inner probes is measured while a current flows through the constriction under a constant voltage bias. The stripline contacts a nanowire sitting between the voltage probes. b) Close up view of the contacted nanowire. The red arrows shows the silicides formed after Joule heating.*

was stressed by biasing the outer contacts with a fixed voltage while measuring the voltage drop falling between the two inner probes attached to the constriction fig(3.6a) by a nanovoltmeter (Keithley 167). These four-probe measurements allowed the extraction of the resistivities of the as-deposited nickel films as a function of the current density directly related to the local dissipation power. The intrinsic resistivities ρ_0 of the deposited

films in absence of joule heating were determined by low frequency lock-in measurements (Stanford SR-830) using an AC polarization current of 100μA and ranged between 0.16 and 0.19 $\Omega \cdot \mu$m. The extracted values for the resistivity are mapped into temperature by using the temperature coefficient of the resistivity

$$\alpha = \frac{1}{\rho(T_0)} \frac{\rho(T) - \rho(T_0)}{T - T_0}$$

For nickel thin films $\alpha = 0.0051$/K in the temperature range $298 - 700$K [6]. Fig.(3.7a) shows a plot of the estimated temperature as a function of the current and time. In this plot, the biasing potential across the stripline was stepped in amounts of 100mV and for each step in bias voltage the current flowing was recorded as a function of time along with the four-probe resistance of the constriction. It's possible to distinguish three different regimes as a function of the current flowing in the constriction. For moderate currents up to 13mA the constriction heats up and the resistance increases accordingly in a reversible way. The values of the resistance follow a linear dependence on the dissipated power fig.((3.7b)) and the local temperature increment ΔT corresponding to this value of the current is around 80K. After this linear regime, increasing further the bias voltage results in a transition regime where the current gradually increases as the stripline resistivity decreases due to the healing effect described in the previous section. This healing effect on the resistivity has a characteristic time depending on the bias voltage after which the system goes into an equilibrium state. The current increase leads to an increased power dissipation which counteracts the resitivity lowering. The two mechanisms compete between them and a new equilibrium configuration is achieved after a characteristic time. For the temperature estimation we used the temperature coefficient of the resistivity α defined as the relative increment of the resistivity per unit temperature. According to the Mathiessen's rule, the resistivity of thin metal films can be expressed as a sum of two terms

$$\rho = \rho_r + \rho_T$$

where the temperature dependent term ρ_T, arises from phonon scattering and varies linearly with temperature for most metals above 298K, and the residual resistivity ρ_r is to a first approximation temperature independent and given by the sum of resistivities coming from surface scattering,impurities, magnetic disorder effects, grain boundaries and intragranular defects. The healing effect can be associated with a modification of the ρ_r component as a consequence of a microscopic rearrangement of the grain boundaries. This means that a temperature estimate based barely on the temperature coefficient α is not strictly valid in a regime where irreversible modifications of the resistivity are taking place. What can be extracted from the plot in fig.(3.7a) is a lower bound on the temperature increment ΔT which is comprised between $135 - 160$K in regime 2. The healing effect takes place in the current interval $14 - 18$mA. By increasing further the polarization voltage, we enter the regime 3 where the current is almost constant to a value of 19mA corresponding to a temperature increase between $260 - 270$K. The constant value of the current tells that the microscopic modifications of the grain boundaries are activated for a certain current density interval. For a current value around 19.5mA we enter the regime where the resistivity starts to increase as a function of time. For this current value, phenomena related to electromigration start to develop [17],[14]. The

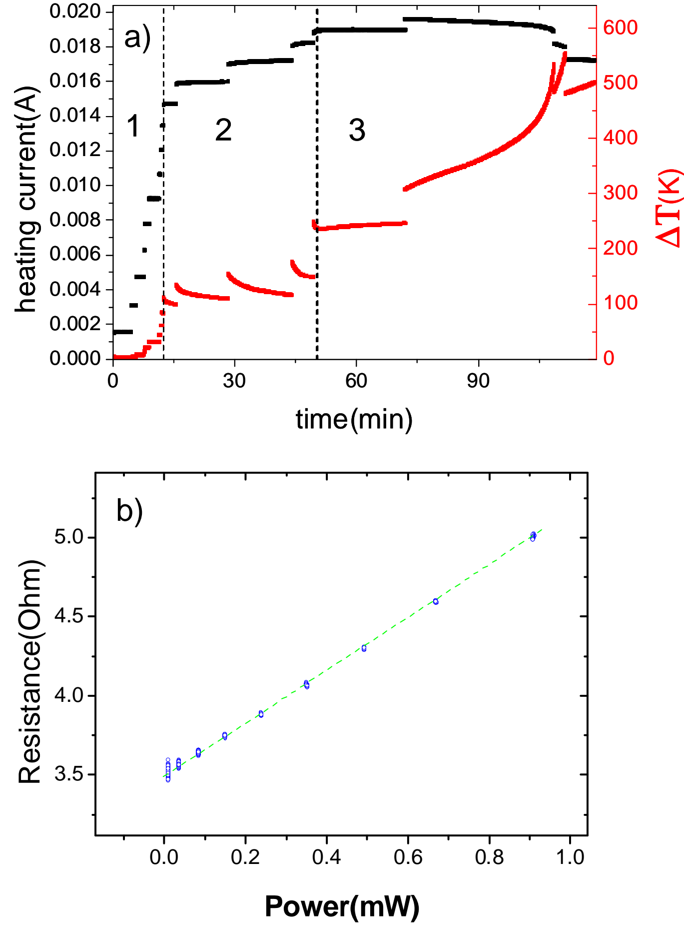

Figure 3.7: *a)Black line: time evolution of the current flowing in the constriction by stepping the polarization voltage by ±100mV. Red line: estimated value of the local temperature by mapping the resistivity variations of the constriction. Dashed vertical lines separate the three regimes described in the text.b) Linear dependence for the resistance of the constriction R in the regime 1 as a function of the power dissipated $P = RI^2$. All the measurements were conducted in vacuum at a pressure $P \approx 5 \times 10^{-6}$mBar*

transport of mass along the constriction promoted by the high current density alters the electronic path between the single grains in an irreversible way and leads eventually to the failure of the circuit when the voids merge together. The progressive increase of the resistance follows from the time evolution of the defect density. The point at which the electromigration starts to become important is when the resistance begins to have a positive slope with respect to time. A more accurate way to define the actual starting point for the electromigration process is to define a critical flux of metal atoms in the constriction. This in turn will depend both on the current density and on the temperature. When the electromigration starts to develop in the constriction, the resistance increases linearly with time with a slope of 900μOhm/s . The slope becomes steeper after a time interval of 20 minutes. To avoid the breaking of the stripline the polarization voltage was

reduced to zero. The temperature values extracted in this regime are an upper bound of the real local temperature since the residual resistivity ρ_r at room temperature may have changed. Fig.(3.6b) shows a SEM micrograph of the device after the Joule heating tratment. The localized Joule heating of the stripline caused the formation of a nickel silicide in the nanowire contacted. The local temperature achieved was enough for the solid state reaction of the metal with the silicon. Fig.(3.8a) shows a SEM micrograph

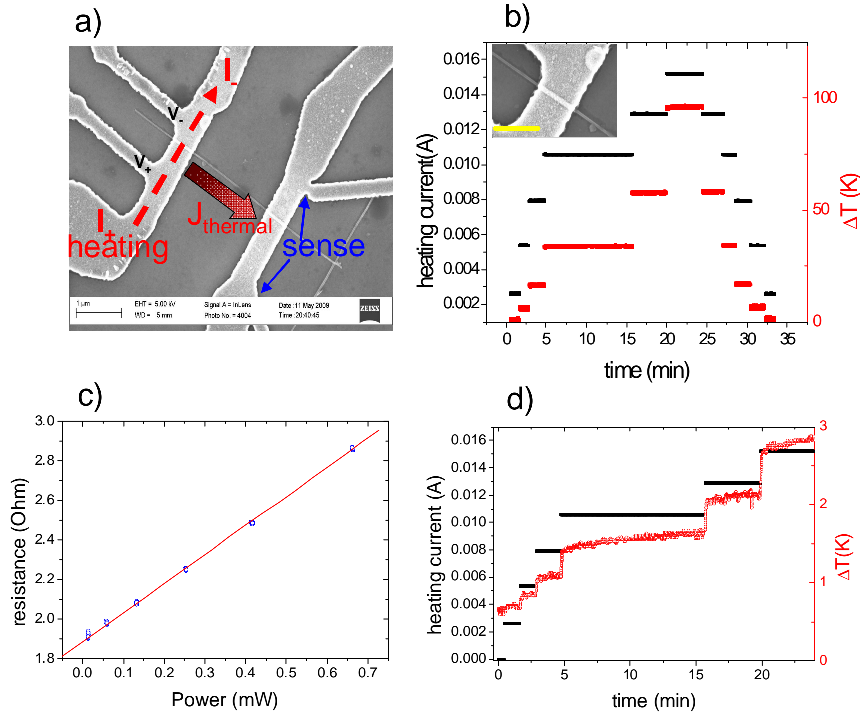

Figure 3.8: *a)SEM micrograph of a nanowire contacted by two striplines. On each stripline addictional probes are patterned for resistivity measurements. One of the two stripline is current stressed and b) the relative variation of the resistivity is mapped into temperature. The heating current was cycled up and down to confirm that no irreversible processes are present related to microscopic modifications of the stripline. The maximum increase in the local temperature is aroud* $100K$ *for a current density of* $0.25 \times 10^{12} A/m^2$. *For this value of the current density Joule heating is not sufficient to promote the silicidation of the nanowire shown in the inset (scale bar* $500nm$*) c) The resistance changes of the constriction are proportional to the power dissipated over all the range of the current values. d) Current flowing in the heater and temperature increase of the second stripline used as a thermometer plotted versus time. The thermometer is* $2\mu m$ *away from the heating stripline.*

of a nanowire contacted by two striplines separated by 2μm. On each striplines we can measure in a four probe geometry the resistance of the constriction defined on top of the nanowire. The first stripline is used as heater while the second one is used as a thermometer. The four probes resistance of the first stripline was monitored as a function of the current flowing into it by attaching to the inner probes a nanovoltmeter (Keithley 167) while driving a current at a fixed voltage (Keithley 6430). The 4 probes resistance of the second stripline was instead measured with a lock-in (Stanford SR 830) with an

AC current of 10μA. Before the experiment, the first stripline was healed by passing for one hour a current of 19mA to activate the processes related to grain boundary reconstruction described previously which led to a variation of the resistance at a fixed bias voltage. The estimated temperature raise of the first stripline in this experiment reached a value around 100K as shown in fig.(3.8b)) for a current of 15mA. The resistance of the stripline is proportional to the power dissipated fig.(3.8c). For each current value the resistance is constant in time since after the healing step the stripline reaches a new stable configuration of the grain boundaries. The increase in the resistance by Joule heating is totally reversible and effects related to electromigration or grain boundaries reconstruction are absent on the experiment time scales. The local temperature increase was not sufficient to promote the silicidation of the nanowire fig.(3.8b))(inset) due to a relative lower value of the resistivity of this particular stripline which, for a given current, translates in a lower Joule power density. Each current step in the first stripline acting like a heater causes a small variation of the resistivity of the second stripline used here as a thermometer fig.(3.8d). The relative increase of the temperature of the second stripline due to power losses through the substrate barely reaches 3K for the highest value of the power dissipated (0.65mW). The power losses through the underlying 300nm thick silicon oxide are responsible for a thermal gradient between the hot and cold side of the device. For a moderate power dissipation up to 100μW the temperature gradient between the heater and the thermometer is around 0.5K/μm in accordance with reported values in the literature [13]. Moreover, the linear relation between the temperature difference ΔT between the heater and the thermometer fig.(3.9) with respect to the power dissipated in the heater allows to extract the thermal conductivity of the substrate. It is important

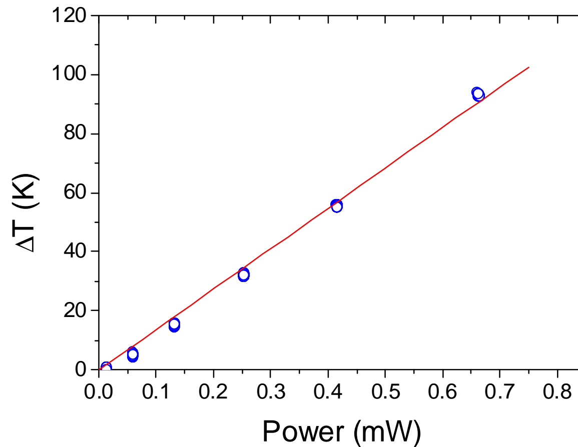

Figure 3.9: *Temperature difference between the heater and the thermometer as a function of the power dissipated in the heater. From the slope of the curve we can extract the thermal conductivity κ of the substrate which amounts to $0.3W/mK$.*

to note that the temperature values extracted by four point measurements give only a rough estimation of the actual temperature. Major sources of error could arise from the value of the temperature coefficient of resistivity α. In an attempt to determine its value I tried to measure the resistivity of the striplines directly in an quartz tube

inserted in an oven. For this experiment a special sample holder was designed enbeding a calibrated Platinum thermocouple in close proximity of the sample for an accurate temperature estimation. Platinum wirings to the sample were then soldered to the chip carrier to allow for electrical characterizations at high temperatures but the set-up suffered from outgassing of the soldered joints to the chip carrier leading to an important contamination of the sample. Although as explained before we cannot infer from the resistivity measurements an accurate value for the local temperature in the case where non equilibrium phenomena like electromigration start to become important, we can nevertheless extract from the two experiments described important informations about the temperatures and current densities required for the solid state reaction to take place. A local temperature increase of 100K is not enough to promote the lateral silicidation and a more reasonable value is beyond 300K. The current densities must be around $3 \times 10^{11}\mathrm{A/m^2}$ close the maximum current density sustainable by these striplines, which for the geometry employed can be around $4 \times 10^{11}\mathrm{A/m^2}$. We will see later how these estimates are to a large degree correct, corroborated by the in-situ observation of the silicidation.

3.4 Electrical control of the silicidation

The device described in fig.(3.5) allows, as already explained, the simultaneous monitoring of the leakage current flowing in the nanowire as a function of the voltage drop across the nanowire and the current density in the stripline used as heating element. The formation of the silicide is accomplished through the thermal energy dissipated which promotes the diffusion of the nickel atoms in the silicon lattice. The technique enables the lateral silicidation of the nanowires for lengths up to $100 - 150$nm. The silicidation done in a conventional oven is triggered by the thermal energy provided by an extended heat source. The sample temperature at equilibrium is constant and equal to the temperature of the oven. In the Joule annealing process heating is very localized, and steep thermal gradients could establish depending on the thermal conductivity of the substrate. This leads to a substantial reduction of the lengths of the silicides since once the silicide is formed on the hot side of the sample, its interface moves towards the cold side and eventually stops when the local temperature has become too low for the silicide motion. Because of the thermal gradients, the lateral silicidation process is self limited, also taking into account that the amount of power the stripline can dissipate is limited by electromigration.

In this section I will describe a process based on Joule heating which allows to control electrically the formation of the silicides for the fabrication of scaled transistors with channel lengths down to 10nm. For this process nickel striplines contacting the nanowires are fabricated following the geometry described in the previous section. The typical separation between them is around $150 - 250$nm. This spacing was chosen to be just smaller than twice the maximum silicide length (≈ 150nm) attainable by this Joule heating method. This is the condition for being able to form devices with arbitrarily short silicon channel. The plot in Fig.(3.10) shows the current flowing in the nanowire as a function of time and the heating current used to locally heat the stripline. We start by applying a bias of 1V across the nanowire. The resulting current is due mainly to thermally activated holes over the Schottky barrier of the heated contact. However,

thermally activated transport could only be seen if the impedance of the second contact is not too high. If this is not fulfilled the thermally emitted carriers at the reverse biased contact cannot be collected at the forwarded biased junction and the current level is dominated by this latter junction. Because of the high impedance of the as

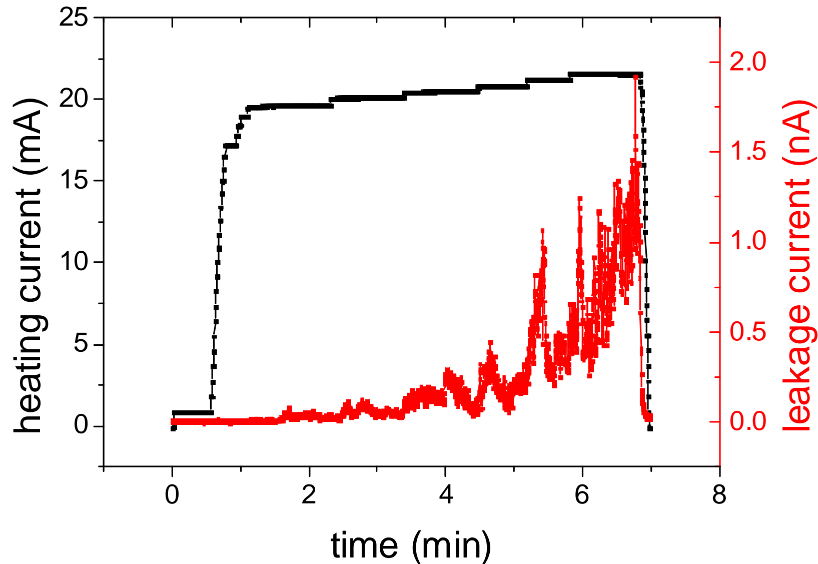

Figure 3.10: *(red curve). Leakage current flowing in the nanowire as a function of time and the heating current on the first contact. The nanowire is polarized with a fixed bias voltage while the heating current is ramped up to* 20.5*mA. When the leakage current reaches a value around* 1*nA the heating current is brought to zero.*

deposited contacts the current flowing in the nanowire is practically negligible. The heating current is then ramped to a value of 20.5mA and the current in the nanowire (called in the following leakage current) corresponding to a fixed bias of 1Volt increases from the noise level up to a value around 1nA. Leakage current levels of few nanoamperes provide an indication that a silicide is formed on the first contact as proved by SEM investigations. After having reached this leakage current value the heating current is brought to zero and the current flowing in the nanowire decreases to a negligible value following the decrease in the local temperature. The injection of carriers in the nanowire during Joule heating is favoured by the heated contact that promotes thermionic emission over the Schottky barrier and is influenced by the formation of the silicide phase. It's very likely that the steps in the leakage current observed are directly related to the growth of the silicide although a conclusion cannot be drawn based only on transport data. However, the leakage currents measured while annealing the first contact never exceed a value of 10nA even for the maximum power dissipated in the stripline and the typical lengths for the formed silicides is below 150nm. In all the experiments we stopped the silicidation process on the first contact after reaching a leakage current of few nanoamperes. This value is just a figure of merit and it is not related to any physical process. During the annealing of the first contact the transport of carriers is strongly

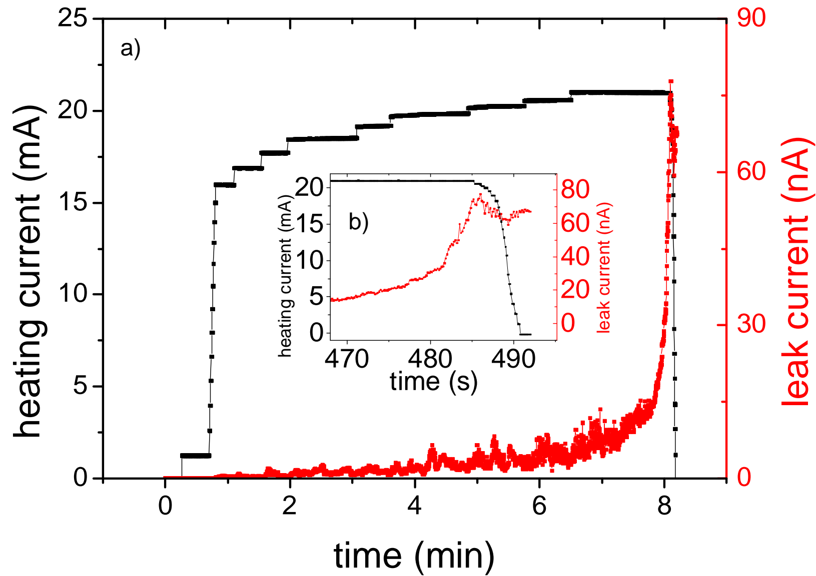

Figure 3.11: *a)Leakage current measured on the first contact while the second one is been heated by the current flowing in the second stripline. b) Close up view of the region with steepest slope for the leakage current in a).*

dominated by the second contact and silicidation was observed even with a leakage current of few hundred picoamperes. After this first step the roles of the two contacts are inverted. The heating current is then applied to the second contact while the first one is connected to the amperometer to measure the leakage current. The nanowire is again polarized with a fixed voltage bias of 1Volt and the heating current is again ramped gradully up to 21mA. During the current ramp-up the leakage current gradually increases following the steps in the heating current fig.(3.11a). In correspondence of the last heating current step the leakage current increases in time following a steeper slope fig.(3.11b) and reaches a maximum value around 75nA after which the heating current is rapidly ramped to zero. Fig.(3.12a) is a SEM micrograph of the nanowire processed in this way after the annealing. The lateral silicidation was accomplished on both contacts leaving an unreacted silicon portion of 8nm. From fig.(3.11b) it's possible to extract important informations. The leakage current values in presence and absence of heat are comparable, meaning that transport across the silicon channel is not influenced by the temperature. If we assume that the temperature right at the interface with silicon is the same as the contact we can conclude that the transport mechanism across the silicon channel is based on tunneling rather than thermionic emission. Fig.(3.12b) compares the room temperature IV characteristics of the nanowire taken before and after the Joule annealing process. Following this procedure on a large set of samples it is possible to build a calibration curve by plotting the measured leakage current as a function of the silicon channel length between the two silicide fronts. This is shown in fig.(3.13). The plot shows that the leakage current is very small for channel lengths above 30nm. In this length range no clear dependence is found between the channel length and the leakage

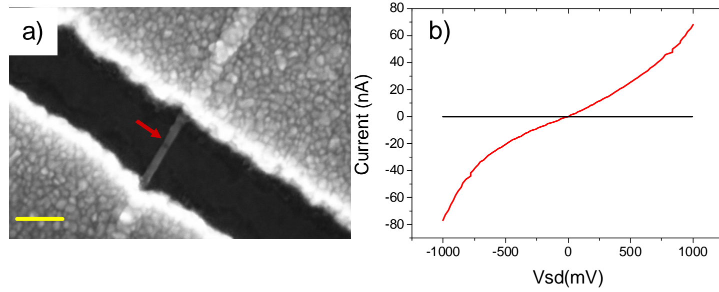

Figure 3.12: *a) SEM micrograph of the nanowire after the Joule heating annealing on both contacts. The unreacted silicon channel (red arrow) is 8nm long. Scale bar 100nm. b) IV characteristics of the nanowire taken before (black) and after (red) the annealing.*

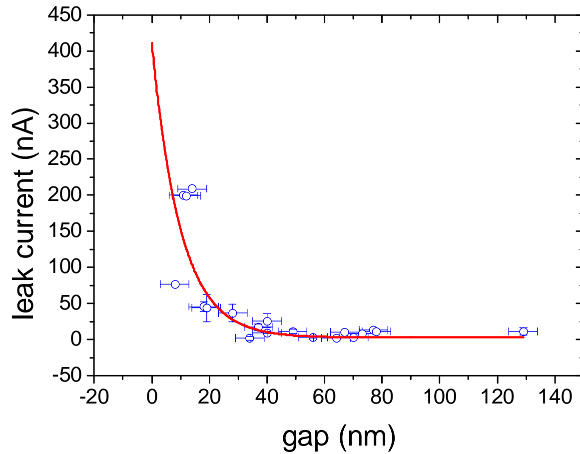

Figure 3.13: *Calibration curve showing the leakage current measured for a given length of the silicon channel as inferred from SEM observations of the samples after the annealing.*

current. Below 30nm, however the leakage current increases rapidly as the gap shortens. The data can be fitted by an exponential. It is important to note that the values of the leakage currents for these short channel devices can be sensitive to fluctuations in the polarization voltage applied across the nanowire. These fluctuations can arise for instance from a not perfect definition of the biasing potential falling on the nanowire due for instance to asymmetries in the striplines or to thermal voltages. Small deviations in the polarization voltage could cause differences in the leakage current between devices. This is due to the fact that when the silicon channel becomes as short as a few tens of nanometers the electric field due to a bias voltage of 1V is of the order of 10^8V/m, i.e. large enough to enable significant Fowler-Nordheim tunneling across the contact SB. In this large field limit, current becomes exponentially sensitive to the applied bias voltage and to the channel length. The silicon channel sandwiched between the two silicide fronts could behave as a short circuit if these phenomena act together and the rapid increase

of the leakage current cannot be controlled with enough precision. From the calibration curve in fig.(3.13) we can extract a figure of merit for the actual value of the leakage current one needs to measure to control the silicon channel length. Channel lengths below 30nm can be readily accessed if the measured leakage current is higher than 30nA.

3.4.1 Electrical characterization: tunnel devices and Random Telegraph Signal

The technique described in the previous section allows the fabrication of short channel transistors in a tunable way by defining the channel length through a controlled formation of metallic silicides. To characterize their switching behaviour an additional lithography step was performed to pattern a top gate. The top gate is partially overlapped with the source and drain contacts and is separated from them by a thin layer of oxide. For the electrical characterization of the transistors we deposited either alumina (Al_2O_3) by sputter deposition or hafnia (HfO_2) by Atomic Layer Deposition (ALD) to a nominal thickness around 5nm. Fig.(3.14) shows the transfer characteristic of a top

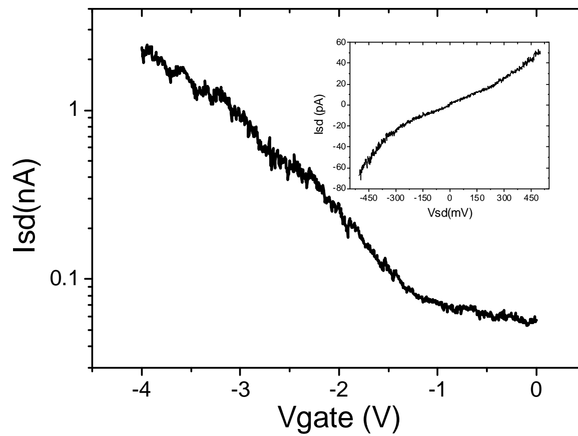

Figure 3.14: *Transfer characteristic (V_{sd}=500mV) of a top gated Schottky barrier transistor with a channel length of 78nm and 5nm HfO_2 gate oxide deposited by ALD. Inset: IV characteristic*

gated transistor with channel length of 78nm prepared with the method described in the previous section. The gate voltage can modulate the conductance of the channel by one order of magnitude but the on-state resistance is around 250MΩ. The switching behaviour of the top gated devices is strongly degraded by short channel effects. The top gate potential is strongly screened by the contacts. Other devices with similar channel length but smaller gate oxide thickness did not show much of an improvement. Lowering the channel length has two major effects on the transport properties. The gate coupling is less effective due to screening from the contacts and its control of the channel potential is completely lost for channel lengths below 40nm. On the other hand the channel resistance lowers correspondingly and the resistances of devices with a channel length

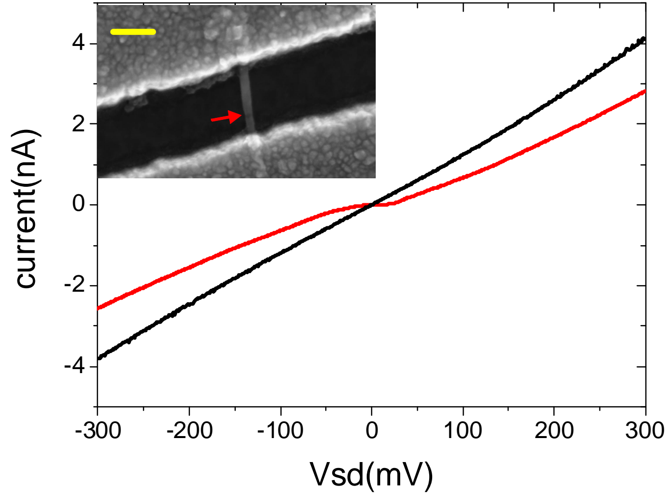

Figure 3.15: *I-V characteristic of a device with a channel length of* 10nm *between room temperature (black curve) and* 230mK *(red curve). Inset: SEM micrograph of the device before top gate patterning. Scale bar* 100nm*. The silicon channel is highlighted by the red arrow. Transport in the device is governed by direct tunneling through the channel. The device after deposition of* 5nm *HfO_2 oxide and top gate patterning doesn't show any gate induced modulation of the channel current.*

less than 20nm is in the range $10-100\mathrm{M}\Omega$. Fig.(3.15) compares the IV characteristics of a device with a channel of 10nm between room temperature and 230mK. The resistance of the device increases only by about a factor of two at the lowest temperature meaning that the principal transport mechanism in the channel is direct tunneling of carriers from source to drain through a silicon barrier. If the current in the channel would be activated thermally over the Schottky barrier of 400meV at low temperature transport should be completely suppressed. The device could be modeled as a metal/insulator/metal junction and the generalized expression of the current density at $T = 0$K can be expressed by the formula [12]

$$J = J_0 \left[\phi exp(-C\sqrt{\phi}) - (\phi + V) exp(-C\sqrt{\phi + V}) \right]$$

where ϕ is the barrier height of the tunnel junction. The non linearity in the IV characteristic observed at low temperature leading to a suppression of the current around zero bias could be due to localization of carriers in a small island between the source and drain. The poor top gate coupling with the channel prevented the possibility to shed light on the actual mechanism responsible for the suppression of the current. For istance a modulation of the gap around zero bias by an external voltage would clearly indicate the presence of charging phenomena leading to the Coulomb blockade effect [18].

Tunnel devices often show other interesting behaviour at low temperature as shown in fig.(3.16). In the I-V characteristic taken at 4.2K for this device with a 9nm channel length, several switches in the current trace are observed depending on the bias

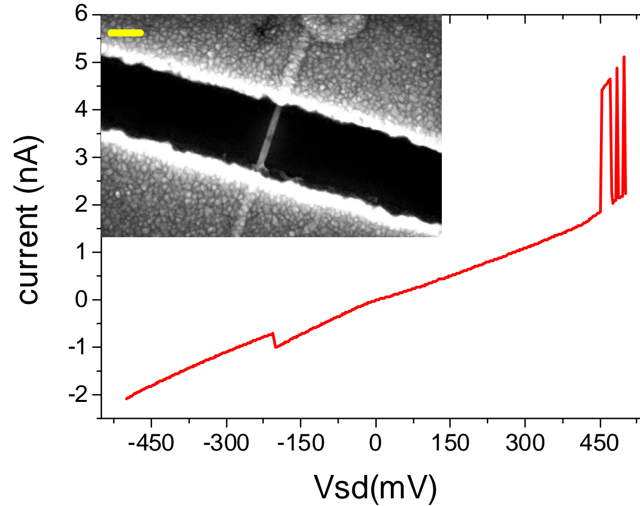

Figure 3.16: *I-V characteristic of a device with a channel length of* 9*nm (inset, scale bar* 100*nm) taken at* 4.2*K. Current switches due to electrostatically coupled charge traps are seen for both* V_{sd} *polarities.*

voltage. These current switches are maybe caused by charge traps located probably in the silicon channel or in its close proximity [15]. The charging and discharging of the traps is reflected in a multistable current flow between the source and the drain. This behaviour reflects a modification of the energy barrier encountered by the carriers in the leads operated by the electric field generated by the charge traps. The traps can switch between two charge states corresponding to an empty or filled site. The transitions between an empty and filled state induce variations in the local electric field. Fig.(3.17)

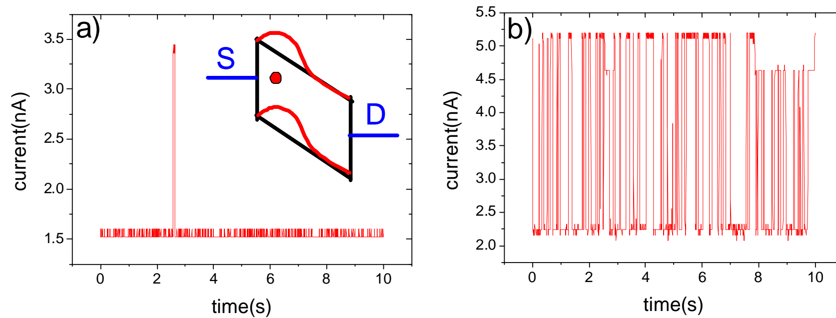

Figure 3.17: *Time domain* $I(t)$ *traces taken at* 4.2*K over a time period of* 10 *seconds for the device in fig.3.16 taken with a source-drain polarization of a)* 400*mV and b)* 500*mV. The current switches between different levels with a time dinamics strongly dependent on the bias applied. Inset: simplified schematics illustrating the effect of a single trap site which modifies the potential barrier experienced by the carriers between the source and drain terminals.*

shows two time scans $I(t)$ taken at $V_{sd} = 400$mV and at $V_{sd} = 500$mV with a digital oscilloscope (Tektronix TDS 1001B). The time traces show that the current switches between different levels with characteristic times depending on the bias voltage. The switching events are voltage dependent because the external source-drain bias V_{sd} modifies the charging and discharging rates by deforming the potential barriers around the trap site. The nature of the trap sites could be ascribed to surface states at the interface between the silicon and the native silicon oxide. Given the nanowire diameter and the channel length, a typical interface state density of $D_{it} \approx 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ [1] may account for the few charge traps responsible for the observed multistability. It is important to note that current switchings are often observed for these short channel transistors also in the absence of a top gate contact. This indicates that charge traps must be located within the nanowire, probably at the silicon/silicon oxide interface.

3.5 In-situ observation of silicidation

In this section I will describe the experiments done in order to monitor the formation of the silicide *in-situ*. Experiments of this kind were recently reported in the literature [9],[3],[4]. In these experiments the formation of the Nickel and Cobalt silicides were imaged with Transmission Electron Microscope equipped with a heated sample holder and lattice resolved images of the propagating interface between the silicide and the silicon could be recorded in real time. The interstitial diffusion of the metal atoms through the silicon lattice was promoted by a point contact reaction between randomly crossed metal-silicon nanowires. Our approach was intended to study the Joule assited silicidation by imaging with a Scanning Electron Microscope the devices described in the previous section. This gave us the possibility to extract important informations on the process and, beside that, to have working electronic nanodevices. The solid state reaction leading to the formation of the silicide was observed in real time with the aid of two SEMs: JEOL 840A and Hitachi4100S. Although the second one has a much better resolution, it remained under maintenance for several months. Therefore, I decided to start my experiments in the SEM which was directly available. To add transport

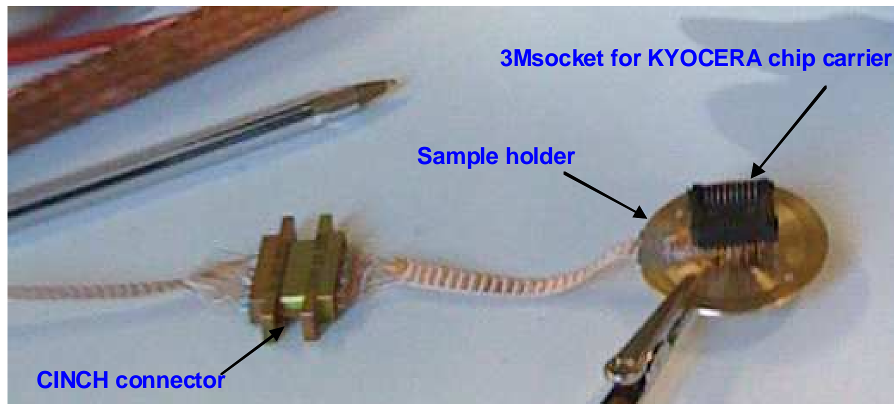

Figure 3.18: *Sample holder for the JEOL 840A*

capabilities to the JEOL 840A, I have designed a sample holder for the KYOCERA Chip

carrier to be fixed to the SEM sample stage. This is shown in fig.(3.18). A 12 twisted pair-woven loom connects the chip carrier to a vacuum feedthrough Fischer connector mounted on a flange. Actually, the woven loom is interrupted by a pair of CINCH connectors allowing removing the assembly. To mount a new sample, the vacuum of the inner chamber has to be broken and the SEM chamber opened. The chip was mounted on its dedicated sample holder outside the SEM and then installed in the SEM. The electrical contact is done by clipping the two CINCH connectors. Subsequently, the SEM is sealed and pumped. This procedure has the disadvantage to require an important time for pumping out the chamber of the SEM. Besides, experiment time was limited by the tungsten filament lifetime. However, this experimental set-up allowed doing the

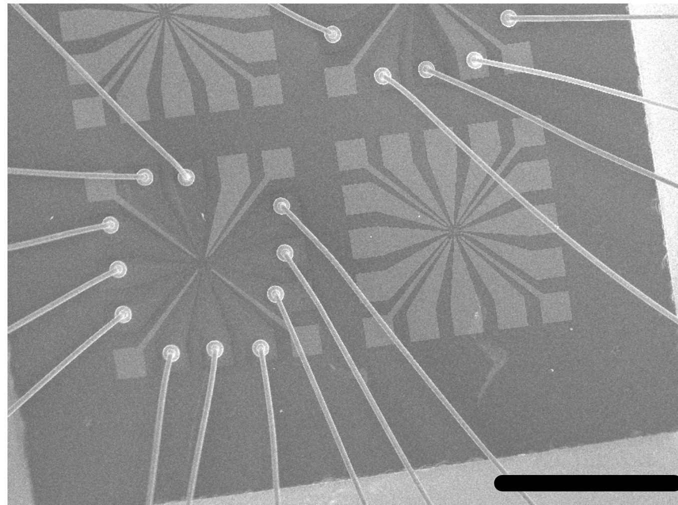

Figure 3.19: *SEM micrograph of a typical sample. The bonded pads left floating develop an important static charge when exposed to the electron beam and they appear darker than the other bonding pads. Scale bar 1mm.*

first tests and the first characterizations and some important insights were obtained regarding sample handling. During all these measurements, the backgate of the sample as well as the contact pads have to be grounded to prevent important charging effects fig.(3.19). Any metallic region left floating developed an important charge leading to its destruction if it was subsequently grounded. Therefore, it was important to keep all devices grounded when they were exposed to the electron beam.

The Hitachi4100S has a higher resolution and is equipped with a homemade electrical characterization sample holder specifically designed in order to be compatible with the traditional load-lock chamber system of the SEM. This is an advantage since loading the sample in the chamber does not require breaking the vacuum of the main chamber each time a new sample is loaded which eases the procedure. The sample is glued on a PCB board with a carbon tape and wire bonding is done on the 9 big bonding pads defined on top of the PCB board. The PCB board is plugged into the sample holder socket and subsequently inserted in the chamber through a load-lock stage. Of the nine bonding pads available for wiring one is directly connected to the ground of the microscope while the remaining 8 are used to connect two samples each consisting of a nanowire contacted by two striplines. The direct observation of the Joule assisted silicidation was

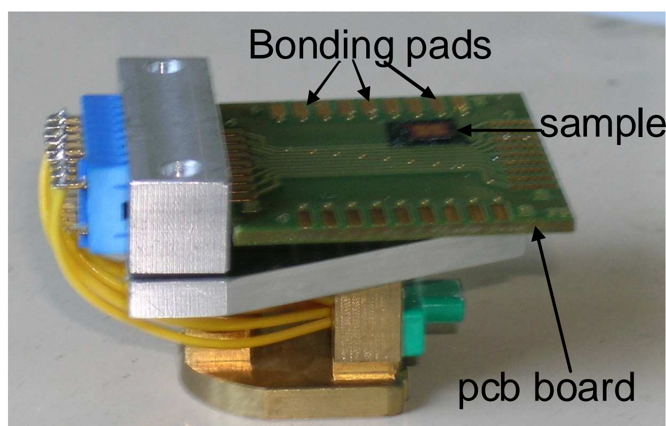

Figure 3.20: *Sample holder for the Hitachi 4110S.*

accomplished using the same measurement set-up already described and the images were obtained scanning the sample with a 5keV beam under a working distance of 7mm. The simultaneous measurement of the leakage current was difficult to achieve due to the interaction of the electron beam with the sample. Some of the nanowires suffered for a severe electrical degradation when subjected to both the electron beam and the voltage bias most probably due to the interaction of the energetic electrons impinging on the nanowires and the strong biasing electric field. However some important conclusions could be drawn relating directly the silicide growth to the current levels used to create Joule heating. This is shown in fig.(3.21) where a time series of the silicidation growth is taken by stepping the heating current flowing in the nickel stripline. The sample is continuously scanned and each image is obtained with a 20 seconds integration time to have a sufficiently high definition. The stripline initially stressed with a current of

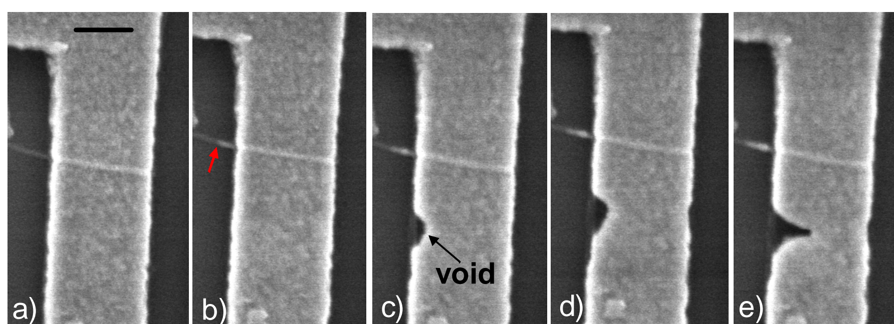

Figure 3.21: *Real time observation of the Joule assisted silicidation by varying the heating current I_h. Starting with a value of 16mA a), the current was stepped to 20mA b) leading to a formation of the silicide (red arrow). Formation of a void was observed at 22nA c) and progressed in the next two image scans d)e). Scale bar 300nm*

16mA fig.(3.21a). After 3 minutes the current in the stripline had raised to 16.5mA due to the healing effect but no silicidation was observed. We then stepped the bias voltage across the stripline to reach a current of 20mA fig.(3.21b) leading to the lateral growth of the silicide up to about 100nm. The images were continuously recorded in the

following 7 minutes but the silicide front did not progress appreciably. In fig.(3.21c) the current was increased to 22nA leading to the formation of a void due to electromigration. The silicide appeared to increase in length up to 150nm. The void extention continued to progress further in the following two image scans fig.(3.21d,e) taken consecutively. The stripline failure was avoided by removing the bias potential. From the sequence showed in fig.(3.21) several conclusions could be drawn. First of all the Joule assisted silicidation is a process with a threshold. The silicide grows only if a certain value of the heating power is reached. If we set a lower bound to the heating current value around 15mA this translates in a local threshold power of 700μW. Once the heating power reaches the threshold, the silicide is formed on a time scale which is at the most of few seconds since fig.(3.21b) has been taken with a total scan time of 20 seconds. Once formed the silicide front progressess up to a certain extension and then stops. This may be explained by the presence of a strong thermal gradient along the growing silicide due to heat losses towards the substrate and the increased energy required for a nickel atom to diffuse through the as formed silicide up to the interface with silicon. Increasing further the current leads to voids formation in the stripline and eventually to its failure. The fabrication of a short channel transistor has been monitored in-situ following the procedure described. Fig.(3.22a) shows a time trace of the leakage current flowing into the nanowire during Joule annealing. For a heating current of 18mA the silicide was formed on the first contact fig.(3.22b) (yellow arrow) up to a length of few tens of nanometers. The leakage current measured barely reached 0.4nA. Interestingly, in the time trace of the leakage current appear peaks equally spaced with a period of 20 seconds. This is just the raster scanning period of the SEM beam that when scanned over the nanowire creates electron-hole pairs swept by the biasing field. After detecting the formation of the silicide the imaging was stopped to refine the focus of the beam and to characterize the sample by IV characteristics. In a second run fig.(3.22c) the heating current was ramped up to 20mA. The silicide front continued to propagate along the nanowire up to a distance of 100nm from the contact and the leakage current reached a value around 1nA. Fig.(3.22e-f) show the leakage current measured and the final SEM image of the device when inverting the roles of the two contacts. The leakage current measured on the first contact while heating the second reached a value around 20nA and the final channel length of the device was aroud 50nm.

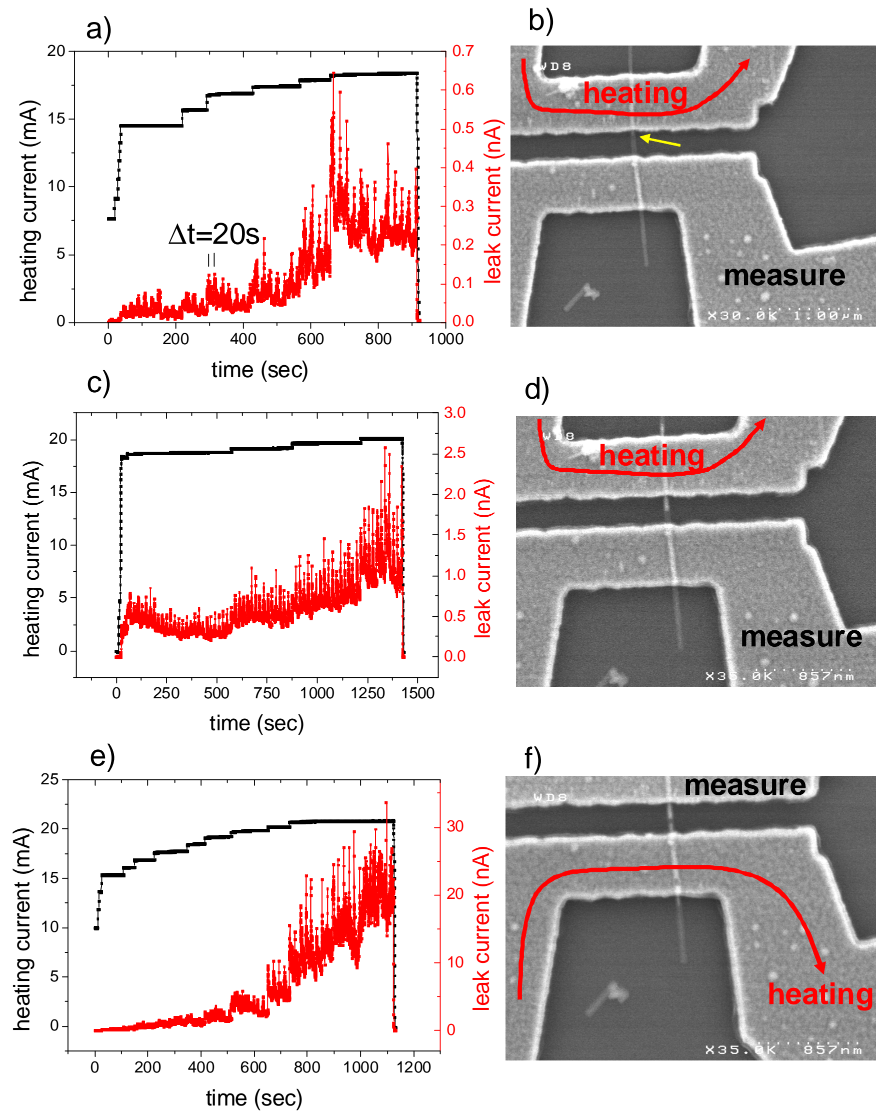

Figure 3.22: *a)-d) Leakage current and corresponding immages of the nanowire taken at the end of each time series for the first heated contact. e) Same time trace when inverting the role of the two contacts and f) final device.*

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Chapter 4

PtSi clustering in silicon probed by transport spectroscopy

4.1 Introduction

In semiconductor technology a key role is played by impurities. Their prominent characteristic is to provide extrinsic carriers in the host material of different type (electrons and/or holes) and to tune correspondingly its electrical behaviour. In recent years, due to the progressive miniaturization of the electronic components, a renewed attention is developing which aims at the control of semiconductor doping at the ultimate level [47]. Beside that, there are proposals which investigate the possibility to actually use single dopants or impurities as active devices in quantum computing schemes [24],[53]. For conventional top-down Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) this approach is already mature and have led to interesting results concerning the isolation of single dopants in the channel of a nanoscale transistor [37],[45],[41]. The same approach could be eventually extended for semiconductor nanowires obtained by a bottom-up growth where doping is typically achieved by in situ incorporation of impurities during the catalytic growth. Although much progress has been made for the understanding of the actual mechanism of dopant incorporation in bottom-up nanowires, isolation of a single impurity center for such nanostructures is still challenging. The fabrication technique described in the previous chapter could be very useful for this purpose since it allows the fabrication of short channel devices in a controlled way without limitations dictated by lithography. A short channel device is needed to isolate electrically active single dopants or impurities. These sites can often accomodate localized states whose signature could be detected at low temperatures. In this chapter I will describe phenomena related to resonant tunneling through an impurity level localized in the channel of a silicon nanowire transitor fabricated by the controlled Joule annealing process of the contacts. The fabrication of the sample was obtained by promoting the silicidation of the contacts by Platinum and the impurity level is associated to a nanocluster of PtSi in the silicon channel acting as a metallic Quantum Dot.

4.2 Platinum as contact material

In the recent years extensive research has been devoted to the replacement of the heavily-doped silicon contact regions of conventional metal-oxide-semiconductor fied-effect-transistors (MOSFETs) with metallic binary compounds of silicon and a transition element, generally referred to as metal silicides [28]. This approach aims at reducing source/drain contact resistances and, simultaneously, relaxing the constrains imposed by doping-profile control. In addition, a lower thermal budget can be expected from the use of relatively low-temperature silicidation processes, as opposed to the high-temperature annealing cycles required for dopant activation. The removal of heavily doped contact regions is not priceless though. In fact, an undesirable Schottky barrier (SB) is introduced with a negative impact on device performances. The SB reduces the on-state current and decreases the sub-threshold slope, leading to a poorer switching performance of the MOSFET. This problem can be mitigated by choosing silicides with low SB height. The high working function of platinum silicide (PtSi) makes this compound the best candidate for contacts to p-type silicon channels. The reported values for the SB height, ϕ_B, in PtSi/p-Si junctions range between 0.15 and 0.27eV [14]. The attractiveness of PtSi is not only limited to p-channel SB transistors. This metal silicide has been successfully used also for the fabrication of inverters in complementary MOS technology where it forms the contact material of both p-type and n-type transistors [27]. In the latter case, the formation of the silicide is accompanied by the accumulation of n-type dopants (typically As or P) close to the PtSi/n-Si interface leading to a suppression of the effective SB height. This approach avoids the integration of a second silicide for n-type contacts, typically ErSi[22] or YSi[56]. Furthermore, PtSi is routinely used in p-type Schottky diodes for infrared photo detection [46, 30]. In view of the relevant technological importance of this contact material I adapted the Joule assisted silicidation technique also for this metal. The technique turned out to work fine also with this material and short (less than 20nm) channel devices could be fabricated following the same procedure adopted for Nickel. The Joule assisted silicidation for Nickel and Platinum are very similar in many respects. Platinum silicides obtained through Joule annealing form at the same heating current interval as compared as to Nickel. This is a direct consequence of the comparable values of the film resistivities and temperature coefficient of the resistance [17] for the two materials. The main important difference is technological and stems from the fact that unlike Nickel, Platinum films deposited by e-beam metal evaporation suffer of scarce adherence on the SiO_2 substrates. This is why Platinum films were deposited by RF-sputtering followed by lift off.

4.3 Electronic properties of Platinum in Silicon

The electrical properties of Platinum in silicon have been studied thouroughly over the past 30 years because of the attractiveness of this material as efficient minority carrier recombination center for fast recovery silicon junction devices [11],[32]. It is widely recognized [26],[6],[36],[57] that Platinum introduces three main substitutional energy levels deep in the silicon band-gap. Reported values in the literature account for an acceptor level located between 0.23 to 0.26eV below the conduction band, a donor level between 0.317 and 0.355 eV above the valence band and an acceptor level 0.1 eV above the valence

band. In addiction, Platinum is capable to form complexes in silicon with Hydrogen [44], oxygen [23], a two atom cluster [51],or a 6 -Platinum atom cluster [21] doping Silicon wafers in a chlorine-containing atmosphere. All of these complexes introduce additional near mid-gap levels mainly acceptor-like. The identification of such levels was carried out in bulk p-n junctions using different techniques such as Deep Level Transient Spectroscopy or Thermally Stimulated Current measurements, which allow the determination of the characteristic lifetimes and capture cross sections for each recombination center. Generally speaking, transition metal impurities in silicon give rise to a sequence levels in the band gap of the host material often corresponding to different charge states of the impurity. Substitutional impurities of transition metals near the end of the $3d^n$, $4d^n$, $5d^n$ are well described by the vacancy model[54]. By removing a silicon atom from the lattice a vacancy is created. The four dangling bonds from the four tethraedrally coordinated neighbors of the missing silicon atom originate molecular orbitals for the defect. Two of these molecular orbitals lie deep in the valence band while the other two are in the silicon badgap. By inserting a Platinum atom in the silicon vacancy, the weak interaction of its d states with the vacancy band gap states of the same symmetry give rise to bonding and antibonding states [2]. The electrical activity of the defect is accounted for the antibonding orbitals lying in the bandgap. In the case of the Pt^- center the antibonding orbitals accomodate three electrons and its electronic structure is very similar to the V^- vacancy center in silicon which has the same spin $S = 1/2$ and the same point group symmetry $C_{2\nu}$. By taking into account the Jahn-Teller distorsion of the lattice and the spin orbit coupling, the vacancy model explain the observed large anisotropies of the g-tensor for the Pt^- center [3] and the strong departure from the spin only value $g = 2$ [55]. Moreover, Photoelectron Paramagnetic Resonance of the Pt^- center in silicon [38] had unambigously assigned this level as the acceptor level measured at $E_C - 0.23eV$.

Although the diffusion of Platinum in silicon is already known, little is known about how this diffusion occurs and what are the implications of this phenomenon with respect to the electrical properties of nanometer scale electronic devices.

4.4 PtSi nanocluster agglomeration

PtSi, and metal silicides in general, are formed through a thermally activated process. Upon annealing of a thin Pt film on Si, the two materials diffuse into each other [42]. (This differs from the case of other commonly used silicides, e.g. nickel silicide, where essentially only the metal element acts as a diffusing species.) Contact fabrication relies on an accurate control of this inter-diffusion process, which leads to the formation of a silicide phase. In particular, the achievement of sharp boundary between PtSi and Si is important in order to meet the demand for device scaling down to characteristic channel lengths of only a few tens of nm. Non-abrupt interfaces, and the possible simultaneous diffusion of metal impurities into the channel region, can alter important figures of merit such as the sub-threshold slope of the on-state current leading to an unacceptably high device variability [4]. Although thermal annealing can result in atomically abrupt silicide/silicon interfaces [31], often this is not the case and various degrees of interface roughness can be found[13, 29, 33]. In addition, several experimental evidences of unintentional Pt impurities in the channel of silicon MOSFETs have been reported [8, 9, 10]. Such Pt atoms originate during the silicidation process as a result

of a diffusive motion from the PtSi/Silicon interface into the Si channel. Yet little is known about their most favorable arrangement within the silicon crystal and, in particular, about how this arrangement is affected by collective interactions among multiple Pt impurities. In this Letter we address this problem through a combined theoretical and experimental study involving atomistic simulations and transport measurements in short-channel PtSi/Si/PtSi SB transistors.

We begin from the simplest case of a single Pt impurity in a Si lattice. Some experimental studies suggest that isolated Pt impurities can indeed be found in the Si region adjacent to a PtSi/Si interface [35, 43]. It has already been shown experimentally and theoretically that in such a case the substitutional position (i.e. a Pt impurity at the place of a Si atom) is the most energetically favorable configuration [54, 2, 3, 55]. Here we consider the problem of multiple Pt impurities in a Si lattice. We intend to evaluate the possibility that nearby impurities out-diffusing from a PtSi contact can aggregate into small clusters. We also intend to find the most stable cluster structure.

In order to tackle the problem of multiple Pt impurities we used numerical calculations based on density-functional theory [1]. Starting from a single substitutional Pt, we identified the most energetically favorable position for a second substitutional Pt. This identification was accomplished by comparing three different options: first, second, and third neighboring lattice site. As a next step, starting from the most stable two-atom configuration, we studied three possible scenarios for the addition of a third Pt atom. Notice that, given the large difference between the formation energies of interstitial and substitutional single Pt, we ruled out aggregates involving interstitial Pt.

A branched diagram summarizing the results of these total-energy calculations is shown in Fig. 4.1. Two observations can be made: (i) a driving force promoting aggregation exists each time the formation energy per atom decreases following the addition of Pt atom; (ii) given a set of possible configurations promoting aggregation, substitution as a second neighbor of the pre-existing Pt atom(s) is always preferred. Hence, both first- and second-neighbor substitution are favored for the two-impurity aggregate, as the formation energy per atom decreases from 0.92 eV to 0.77 and 0.5 eV, respectively, the latter being the most stable. When a third Pt atom reaches the second-neighbour two-atom aggregate, on the other hand, the only configuration that leads to an increased stability is the one where all the Pt atom are second neighbors. The other cases considered feature an increase of the formation energy per impurity (0.71 and 0.96 eV) [1].

These results suggest that even a moderate supply of Pt atoms into a Si lattice would lead to the formation of PtSi clusters initially adopting the zincblende structure imposed by the host crystal. In order to test the validity of this conclusion for large numbers of Pt atoms, we considered a PtSi cluster with a diameter of approximately 1 nm, embedded in a 512-atom bulk Si supercell. In Fig. 4.2 we plot the density of states decomposed in the contributions from bulk Si atoms, and from Pt and Si atoms in the PtSi cluster. It can be seen that a complex structure of peaks appear in the Si band-gap, which reveals the metallic character of the cluster.

As the cluster grows in size, a phase transition to the bulk PtSi structure (favored by 0.55 eV/PtSi pair) is expected to occur. For this reason we have explicitly addressed the

[1]For the sake of simplicity we are assuming that, in the slow-rate limit, Pt atoms reaches the clustering zone one by one. We believe, however, that this simplified model is enough to capture the physics of the aggregation process.

structural relaxation of a PtSi cluster of similar size with the thermodynamical stable structure, and we have found that for a cluster diameter of 1 nm relaxation to the host zincblende lattice is still thermodynamically favored.

We have also considered the formation of all-Pt clusters, examining both clusters where Pt adapts to the host zincblende symmetry or clusters where Pt takes the fcc symmetry of its bulk form. Although the formation energies of Pt or PtSi inclusions depend on the chemical potentials of the respective constituent species (which have a large degree of uncertainty), the differences in favor of PtSi clusters are so large that all-Pt clusters can be safely discarded.

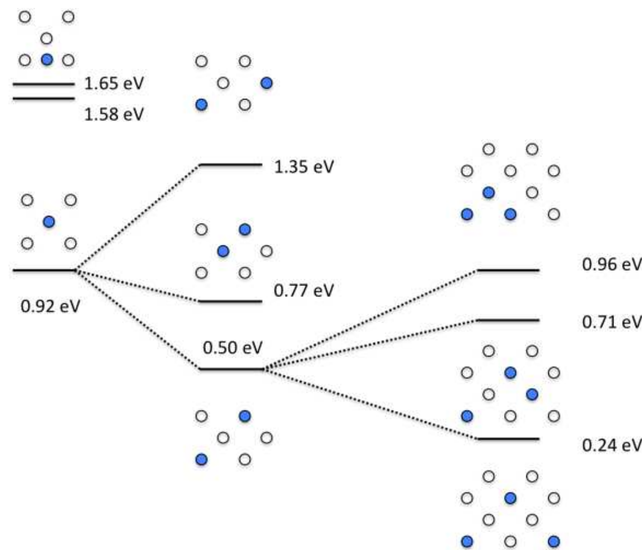

Figure 4.1: *Energy scales involved in the formation of a substitutional Platinum defect in the silicon lattice. The most stable configuration of a multi-atom defect is the one in which Platinum atoms are second neighbors. Left column: formation energy of Pt point defects, i.e. substitutional (0.92 eV) and interstitials (1.58 and 1.65 eV). Center column: formation energy per Pt atom of two-atom aggregates. First- and second-neighbors clusters favor aggregation, while a third-neighbor cluster does not. Right column: addition of a third Pt atom to the most stable of the two-atom clusters, i.e. the second-neighbor aggregate of the center column. The formation energy per impurity decreases only for the all-second-neigbour cluster (0.24 eV against 0.5 eV of the two-atom aggregate).*

4.5 Resonant Tunneling phenomena

The device essentially consists of a silicon tunnel junction obtained through the controlled formation of two metallic Platinum silicide contacts to an individual chemically synthetized undoped silicon nanowire. Each Pt electrode consisted of a 500-nm-wide and 3-μm-long strip whose edges were connected to *two* Cr(10nm)/Au(65 nm) bonding pads via progressively wider Pt metal lines defined in the same deposition step. In order to promote the formation of PtSi contacts, the Pt strips were annealed one at a time by means of Joule effect. To this aim, an electrical current of $\sim$10 mA was sequentially applied through each Pt strip causing a local increase of the temperature and hence

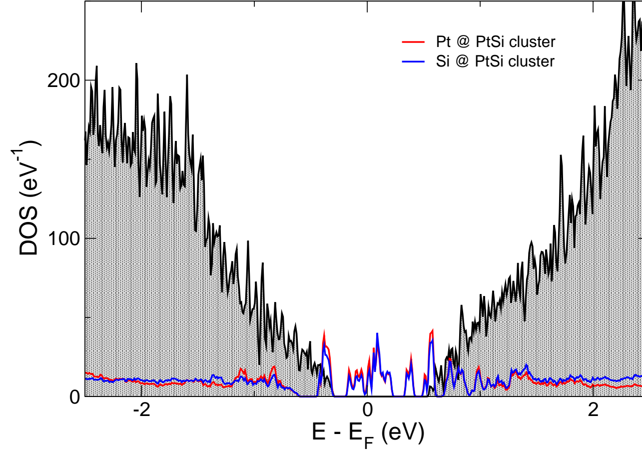

Figure 4.2: *Total DOS for a PtSi cluster of 1.3 nm containing 32 Platinum atoms. The black shaded curve represents the DOS for bulk Silicon*

promoting the silicidation of the contacts. This silicidation technique, was applied to obtain PtSi/Si/PtSi NW junctions with controlled Si channel length down to ∼10 nm (Fig.4.3(a)). Each NW junction was capped by a 5-nm-thick aluminium-oxide (Al_2O_3) layer, grown by Atomic Layer Deposition, and a Cr(10nm)/Au(60nm) top-gate electrode defined by e-beam lithography, metal evaporation, and lift-off.

Due to the absence of intentional doping and to the short channel length, the fabricated devices were found to operate as SB transistors [28]. In these transistors, the silicon channel is fully depleted. The conduction- and valence-band edges have essentially flat spatial profile (see Fig. 4.3(c), left panel) and their energy position relative to the Fermi levels of the PtSi contacts is set by the n- and p-type SBs, respectively. Since the p-type SB (ϕ_p) is significantly smaller than the n-type SB (ϕ_n), electrical conduction is dominated by hole-type carriers.. Fig.4.3(b) shows the source-drain current, I_{sd}, as a function of source-drain bias voltage, V_{sd}, for two different temperatures. At room temperature (black trace) and for $V_{sd} << \phi_B$, transport through the silicon region is dominated by the thermionic emission of holes over the reverse-bias p-type SB. At 7 K (red trace), thermionic emission is entirely suppressed, and the residual conduction is due to temperature-independent tunneling through the silicon section, which acts as tunnel barrier [48]. A finite differential conductance, $G = dI_{sd}/dV_{sd}$, is observed throughout the entire $I_{sd}(V_{sd})$, thus including the linear regime around zero bias. The linear conductance, G, decreases with the gate voltage, V_{gate}, as shown by the measurement in Fig.4.3(d), which was taken at 0.24 K. This p-type transistor behavior is characteristic of hole-dominated conduction. Once again, this follows from the fact that $\phi_p < \phi_n$. An increase of V_{gate} causes a downward band bending in the silicon section leading to a higher tunnel barrier for holes (Fig. 4.3 (c)), and hence a lower conductance. Yet, due to a short-channel effect (the nanowire diameter is about four times the channel length), the gate effect is largely screened by the metallic PtSi contact. As a result, the $G(V_{gate})$ exhibits a moderate modulation over the accessible gate-voltage range. In particular, $G(V_{gate})$ remains finite up to the highest gate voltage applied (no higher voltages could be achieved due to the onset of significant gate leakage). A negative gate voltage produces an upward bending of the valence-band profile. Even for the largest

V_{gate}, however, the valence-band edge remains well below the Fermi level of the contacts, such that no hole accumulation is induced in the silicon channel. This is consistent with the absence of Coulomb blockade behavior, which would be expected in concomitance with a gate-induced formation of a hole island in the silicon region (see, e.g., Ref. [58]).

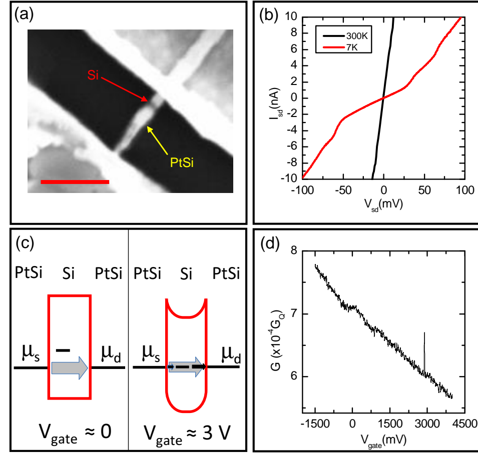

Figure 4.3: *(a)Scanning Electron Micrograph of the device before top gate patterning, showing the thin semiconductor region (highlighted by the red arrow) sandwiched between the brighter platinum silicide contacts. The silicon channel between the two silicides is* $12nm$ *while the nanowire diameter is* $40nm$. *Scale bar 200nm. (b) Current-voltage characteristics taken at room temperature and 7K of the device in (a). (c) Simplified picture of the band diagram. At gate voltage* $V_{gate} = 0$, *where we assume flat-band condition in the silicon section, the cluster electrochemical potential lies above the Fermi levels of the contacts. In this regime, transport is due to mainly hole-like direct tunneling through the silicon band gap. At* $V_{gate} \approx 3V$, *the downward bending of the silicon bands results in a higher tunnel barrier for holes leading to a decrease in the direct-tunneling conductance. Simultaneously, the cluster electrochemical potential lines up with the Fermi levels of the leads resulting in a resonant-tunneling current. (d) A resonance peak appears over the background differential conductance measured at* $230mK$ *with a lock-in excitation voltage of* $100\mu V$.

Interestingly, a sharp conductance peak is observed at a positive gate voltage close to 3 V, superimposed on the slowly varying background conductance. As shown in the inset to Fig. 4.4(a), following the subtraction of this background, the conductance peak can be fitted very well to a Lorentzian function [15, 5], revealing an underlying resonant-tunneling transport channel. The fitted peak width w gives a measure of the tunnel coupling between the resonant state and the leads. The temperature dependence of the observed conductance resonance is shown in Fig. 4.4(a). As expected for resonant-tunneling, the conductance peak gets smaller and wider upon increasing temperature from 0.24 to a $\sim$ 5 K. Above $T \sim 5K$, the peak height increases again as shown in the lower inset of Fig. 4.4(b). On the contrary, w, exhibits a monotonic temperature dependence as shown in Fig. 4.4(b)(main panel). To a closer look, however, w is roughly constant below 0.6 K (see upper inset to Fig. 4.4(b)). In this low-temperature regime, the peak width is dominated by the life-time broadening of the resonant state due its tunnel coupling to the source and drain leads. Precisely, $w \approx \hbar\Gamma = \hbar(\Gamma_S + \Gamma_D)$, where Γ_S and Γ_D are the tunnel rates to the source and drain contacts, respectively. Between

0.6 and 4 K, w increases linearly with temperature according to the expectation for tunneling through a single discrete resonant level, i.e. $w = 3.52K_BT$ ((Fig. 4.4(b), green line). This linewidth matches exactly the thermal broadening of the Fermi distribution function in the source and drain leads. A linear temperature dependence is observed also above 8 K, yet with a larger slope corresponding to the expectation for tunneling through an ensemble of closely spaced levels, i.e. $w = 4.35K_BT$ (Fig. 4.4(b), red curve). Therefore, the crossover temperature $T^\star \approx 6$ K identifies the transition from quantum (single level) to classical (multiple levels) regime [12]. This finding suggests that the observed conductance peak arises from resonant tunneling through a quantum dot with characteristic mean-level spacing $\delta E \approx k_BT^\star \approx 0.5meV$.

4.6 Tunneling Spectroscopy

To further support this conjecture we present in Fig. 4.5(a) a measurement of dI_{sd}/dV_{sd} as a function of (V_{gate},V_{sd}). The color plot (stability diagram) exhibits an X-shaped pattern which is typical for Coulomb-blockaded transport in quantum-dot systems [19, 25]. The crossing point, which corresponds to the conductance peak in the linear regime, represents the boundary between two consecutive Coulomb diamonds. In each diamond, transport through the quantum dot is blocked and the quantum dot hosts a well defined, integer charge state. Additional multiple dI_{sd}/dV_{sd} lines parallel to the diamond edges can be seen in Fig. 4.5(a). Such types of lines are typical signatures of tunneling via the excited states of the quantum dot. Their positions relative to the diamond edges are set by the excitation energies of the corresponding quantum-dot states. The irregular spacing between the lines implies that the quantum-dot levels are not equally distributed in energy. Yet we can infer a characteristic mean-level spacing of the order of 1 meV, which is consistent with our earlier estimate based on the temperature dependence of the linear-conductance resonance.

The next step is to understand what kind of quantum dot could be responsible for the observed Coulomb-blockade features. Based on the gate dependence of Fig. 4.3(d) we already concluded that the silicon channel is fully depleted throughout the entire gate-voltage range. This allows us to rule out the possibility that the quantum dot is formed by confinement in the short silicon section. Thus we are left with the sole option of a Pt-based metallic nanocluster. Assuming that electrons in the nanocluster can be described to a good approximation as non interacting quasi-particles in spin degenerate levels [52], the mean-level spacing can be derived from the cluster diameter, d, using the relation $\delta E \sim 2\pi^2\hbar^2/mk_FV$, where m,k_F and V are the electron mass, metal Fermi wavevector and nanoparticle volume, respectively. From a level spacing of ∼1 meV, using $k_F \sim 3 \cdot 10^{10}\text{m}^{-1}$, we find $d \sim 4$ nm. The data shown in Fig. 4.5(a) was focused on a narrow range around the observed tunnel resonance. From a similar measurement on a much larger (V_g, V_{sd}) range (see 4.6) we estimate a charging energy $U \sim 50meV$, which is consistent with a cluster diameter of a few nm.

We now consider the effect of a magnetic field, B, on the observed resonant level. Figure 4.5 (c)-(f) shows a set of stability diagrams measured at $B = 3$, 5, 7, and 9 T (in all these measurements B was applied perpendicularly to the substrate). We first note that by increasing B the X-shaped structure shifts progressively towards less positive V_{gate} values. This behavior can be ascribed to the Zeeman effect. To show that, let us

label the gate-voltage position of the charge degeneracy point (i.e. the position of the resonance in the linear conductance) as $V^\star$; then let us start with the hypothesis that the nanocluster has an even number of electrons and a spin $S = 0$ for $V_{gate} < V^\star$, and an odd number of electrons and S=1/2 for $V_{gate} > V^\star$. Under this hypothesis, an applied magnetic field should result in a negative shift of $V^\star$ proportional to the Zeeman energy shift ΔE_Z of the spin-1/2 ground state.

Figure 4.5(b) shows the gate-voltage shift, $\Delta V^\star$ as a function of B. The dashed line is a linear fit to $\Delta V^\star = \alpha \Delta E_Z = -\alpha g \mu_B B/2$, where α is a lever-arm parameter given by the ratio between the gate capacitance and the total capacitance of the cluster [2], μ_B is the Bohr magneton, and g is the electron g-factor, used as fitting parameter. The linear fit yields $g = 2.0 \pm 0.1$.

While the charge-degeneracy point undergoes a B-induced leftward shift, the edges of the Coulomb diamond on its left are expected to split due to the removal of spin degeneracy. This effect is clearly seen on the lower diamond edge as highlithed by the white arrows in Figs. 5(c)-(f). The Zeeman energy can be directly measured from the position of the line associated to the excited spin state, as illustrated in the inset of Fig. 4.5(c). With this procedure we find $g = 1.95 \pm 0.1$, which is consistent with our previous estimate.

The fact that the measured g-factor coincides (within the experimental uncertainty) with the bare-electron value allows us to make some considerations about the nature of the quantum dot. To begin with, this finding constitutes further (indirect) evidence that the observed resonant channel cannot be associated with an isolated Pt impurity. In fact, valence electrons in Pt impurities are known to have anisotropic g-factors generally different from the bare-electron value [55, 2, 3]. This is because platinum is a heavy element with strong spin-orbit coupling. For the same reason, significant deviations of the g-factor from the bare-electron value have been observed in platinum metal structures [20] (and refs. therein), including Pt nanoclusters [34] (we are aware of only one work [16] whose results do not agree with this trend). Therefore, our g-factor measurement provides an experimental indication against the hypothesis of a cluster consisting of pure platinum. The hypothesis of PtSi cluster, as suggested by our ab initio calculations, appears more plausible. With the aid of adequate numerical tools, it would be interesting to perform a calculation of the g-tensor in PtSi. Intuitively, one may indeed expect the g-factor to approach the bare electron value as a result of the considerable silicon content in the cluster. This tendency should be further reinforced by surface effects associated with the leakage of the electron wave-functions of surface atoms into the silicon host matrix [50, 7, 18].

In summary, through atomistic simulations and electronic transport measurements we have provided evidence of platinum clustering in silicon devices employing PtSi contacts. Our experiment on a short-channel PtSi/Si/PtSi SB transistor revealed the emergence at low temperature of a single-electron tunneling channel. This transport channel, which causes current resonances in the full-depletion (i.e. off) regime, is ascribed to a Pt-based metallic cluster embedded in the silicon section. Our atomistic simulations suggest the cluster to be most likely composed of PtSi. The cluster has discrete electronic levels with a characteristic energy spacing of 0.5 meV, corresponding to a diameter of a few nm, which is comparable to the characteristic length scales of the device. In addition,

[2] α is a conversion factor which relates the potential on the gate to the potential in the nanocluster

the cluster has a charging energy of 50 meV, which explains why single-electron effects survive up to relatively high temperatures. In the perspective of ultrascaled transistor devices, this study shows that the possible formation of PtSi clusters during the silicidation process can have important consequences on device performances. This issue can lead to significant device variability undermining the gain from using metal silicides and doping-free devices. Hence, we expect our results to have an impact in the engineering of a wide class of emerging electronic devices, including fully-depleted nano-transistors and ultra-fast PtSi Schottky barrier photodetectors.

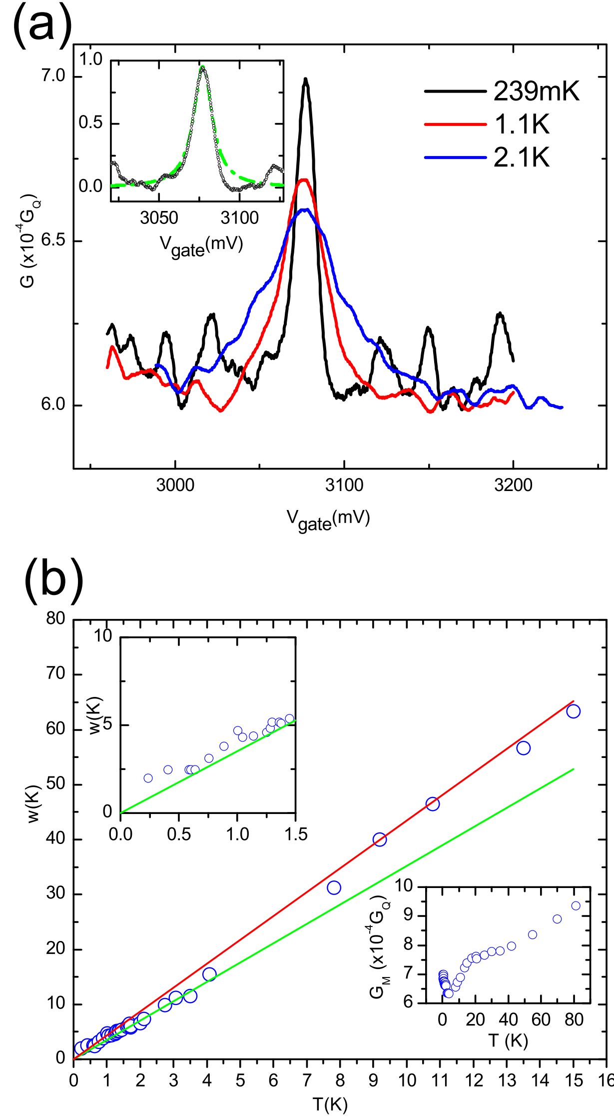

Figure 4.4: *(a)Thermal broadening for the resonant peak as in Fig. 4.3(d). As the temperature is lovered the resonance goes in the quantum regime and the peak becomes narrower and higher. The small shift in the gate voltage position of the resonant peak as compared as to Fig. 4.3(d) is due to offset charges induced by a large gate voltage sweep. Inset: Conductance peak fitted by a Lorentzian (green dotted line) after substraction of the background current. The peak is fitted with the function* $G(E) \propto \frac{e^2}{h}\frac{\Gamma_S\Gamma_D}{(E-E_0)^2+w^2}$ *where* E *is the gate voltage-dependent energy of the resonant level and* E_0 *the Fermi level in the leads, to give an intrinsic width,* w*, of the level of about* $170\mu eV$ *at 230mK. (b)Temperature dependence of* w *at* $V_{sd} = 0$*. The red and green solid lines are the expected slopes* $3.52k_B$ *and* $4.35k_B$ *for the quantum and classical transport regimes respectively. Upper left inset: close up view of the main panel at low temperatures where* w *becomes temperature independent below* $600mK$*. Lower right inset: Conductance peak height plotted versus temperature.*

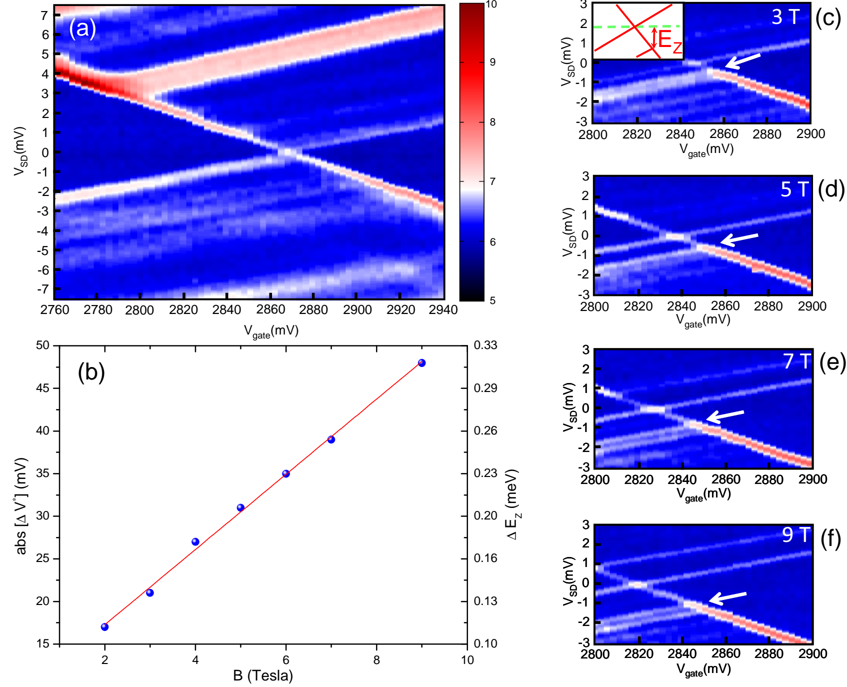

Figure 4.5: *a) Differential conductance in units of $10^{-4}e^2/h$ measured by varying the bias potential and the top gate voltage at magnetic field $B = 0$. Lines of enhanced conductance due to the alignment of the resonant level to the Fermi energies in the leads, mark the separation between even and odd electron occupancies of the nanocluster. Using a conversion factor determined by the slope of the differential conductance lines it is possible to convert in energy the positions in gate voltage ($V^\star$) of the resonant peak at $V_{SD} = 0$. The difference $|\Delta V^\star| = |V^\star(B) - V^\star(B = 0)|$ is then converted into energy (right vertical scale, panel b) and a linear fit to the data (red line) gives a g-factor equal to 2.0 ± 0.1 c)-f) Same plot as in a) for $B = 3$, 5, 7, and 9 T, respectively. The white arrows highlight the evolution of the excited-spin-state resonance. The inset is c) shows how the Zeeman energy is related to the position of the excited-spin-state resonance.*

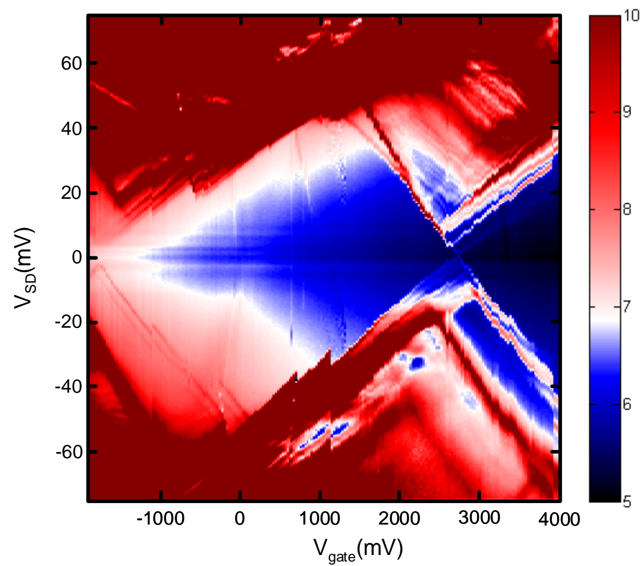

Figure 4.6: *Stability diagram measurement (in units of* $10^{-4}e^2/h$*) spanning the largest gate-voltage range accessible without incurring in significant gate leakage. Due to the relatively small capacitive coupling between the PtSi cluster and the gate, only one charge-degeneracy point around 3V is found in this extended gate range. Nevertheless, a large portion of the Coulomb diamond on the left side of this charge-degeneracy point can be appreciated. The vertical size of this diamond provides an estimate of the associated charging energy (≈ 50 meV). Unfortunately, several charge-switching instabilities are observed on such a large gate voltage sweep.*

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[1] Theoretical first-principles calculations have been performed within density-functional theory (DFT), as implemented in the Siesta package [49, 39]. We have used an optimized double-ζbasis set plus polarization functions for the valence electrons, while core electrons are accounted for by means of norm-conserving pseudopotentials of the Troullier-Martins type. The exchange-correlation energy is treated within the Generalized Gradient Approximation (GGA) [40]. Pt point defects and 2- and 3-atom aggregates are studied n the $3 \times 3 \times 3$ supercell of the 8-atom bulk Si unit cell, while the ~ 1 nm clusters were created in a larger $4 \times 4 \times 4$ supercell. The Brillouin zone was sampled with a $2 \times 2 \times 2$ grid of k-points, though a finer $8 \times 8 \times 8$ was used for an accurate determination of the densities of states in Fig.4.1. All the structures have been optimized until the force on the atoms were lower than 0.04 eV/Å.

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Conclusions and perspectives

This thesis has been devoted to the study of the transport properties of Silicon Nanowires obtained by a bottom-up catalytic growth. The use of an undoped semiconductor greatly demanded for a development of fabrication techniques oriented to improve the carrier injection in the devices. This was accomplished by employing annealing treatments of the contacts aiming at the formation of metallic silicides. The metallic silicide alone is not sufficient for lowering the contact resistance of the devices and this first step has to be followed by other fabrication techniques oriented to tune electrostatically the large Schottky barrier developing at the contacts. For this we used the results obtained for the control of the silicidation process, to gate independently the interfaces between silicon and the metallic silicide where the injection of carriers takes place. More precisely, we developed an annealing protocol to promote a lateral silicidation of the contacts to have the injection interfaces placed at certain distances from the leads. This was intended for aligning the interfaces on existing predifined bottom gates. The devices were then completed by patterning top gates to have a gate-all-around geometry for the best electrostatic coupling. This approach indeed proved useful for tuning electrostatically the Schottky barrier height and the resulting contacts could be switched from a rectifying to an ohmic behaviour. Temperature dependent measurements were employed for a quantitative estimate of the Schottky barrier at each contact as a function of the gate voltage. A large discrepancy between the extracted values of the Schottky barriers was found which can be be ascribed to the presence of surface/interface charges in close proxymity of the silicon/silicide interface. These charges can alter the band profile of the semiconductor, leading to a variation of the effective SB height. This result shows how in nanometric contacts large fluctuations of the Schottky barrier could arise due to the reduced dimensionality. This is an important factor to consider for designing scaled devices. Moreover, carrier injection at cryogenic temperatures for a Schottky barrier transistor was demonstrated with signatures of localization for the hole gas. The tuning of the Schottky barrier achieved by local gating gave us the intriguing possibility to add electronic functionalities into a single undoped nanowire device without the need of doping. Basic building block circuits like a tunable Schottky and *p*-*n* diode were demonstrated. Moreover, a two input NAND logic gate with gain could be assembled.

Another part of the thesis was devoted to develop a novel fabrication technique aiming at the electrical control of silicide formation through Joule assisted annealing. A protocol was developed to promote and control the lateral silicidation of silicon nanowires. The solid state reaction leading to the formation of the metal silicides for both nickel and platinum contacts could be observed by real time Scanning Electron Microscopy. Silicon tunnel junctions of lenghts as small as 8nm could be fabricated in a reproducible way. Reactive-Ion-Etching performed on these silicon tunnel junctions, showed that it

is possible to etch away selectively the silicon channel leaving the nickel silicides electrodes unaffected. This led to the fabrication of nanometer scale gaps between the silicide contacts.

By electrostatic doping of an undoped silicon nanowire it has been possible to embed in a single nanowire device different electronic functionalities. It could be possible to combine these electronic functionalities with optics. This could be accomplished by using the electrostatically defined *p*-*n* junction to build for instance nanoscale avalanche photodetectors. These devices can have large photomultiplication and subwavelength spatial resolution for detection.

The technique of Joule assisted silicidation could be improved by adding a feedback control on the heating current so to increase the accuracy on the length of the silicon channel. It should be also possible to study the formation of the silicides on suspended structures and study their formation in the absence of thermal losses to the substrate. The process could be extended to nanowires doped by shallow impurities. The short (less than 10nm) tunnel junctions that can be fabricated, have dimensions comparable to the Bohr radius of the donor or acceptor orbital. This could give access to the study of single-dopant signatures also for bottom-up nanostructures paving the way to the manipulation of single dopant orbitals. Moreover, these nanostructures are extremely sensitive to local charges in the vicinity of the nanowire as evidenced from the Random Telegraph Signal and could be used as charge detectors. Moreover, by using molecular-scale undoped silicon nanowires with diameters of few nanometers it could be possible to verify the ultimate scalability for a Schottky barrier transistor.

The Joule heating technique applied to platinum contacts has revealed the agglomeration of Pt atoms into PtSi clusters. This can have important consequences on the electrical properties of a device. In particular, we show that such silicide clusters behave as metallic quantum dots introducing a quasi-continuum of electronic states deep in the silicon gap. Since they are typically located close to a PtSi/Si contact interface, these PtSi clusters can introduce intra-gap resonant tunneling channels as observed in our experiment.

Through low-temperature transport spectroscopy we unambiguously identify important physical properties like its electric and magnetic behavior without disruptive analysis and ensemble averaging over a collection of chemically synthesized clusters. This scenario is likely to be relevant for other metal silicides too. Hovever, the corresponding electronic structure calculations should be performed for each case to assess the validity of this hypothesis.

The size of the silicide cluster, estimated from the observed characteristic energy-level spacing, is non-negligible if compared to the characteristic length scales of the device. In addition, the energy required to add (remove) a single electron charge to (from) the cluster is of the order of the thermal energy at room temperature. As a result, the presence of the cluster has important consequences of the device transport properties.

These findings have substantial practical implications for two main reasons: 1) In the perspective of ultrascaled transistor devices, PtSi clusters formed as a result of the silicidation process can severely degrade device performances introducing significant device variability. This issue, can severely undermine the gain from using doping-free device approaches. Hence, important implications in the device engineering of a wide class of emerging electronic devices, including ultrascaled low-dissipation transistors and

PtSi Schottky barrier photodetectors, can be expected. 2) Tunnel junctions of the type studied in this work, i.e. consisting of a Metal/Nanowire/Metal sandwich, can have potential applications in the domain of ultrafast (opto)electronics. Because of their small capacitance (of the order of atto-Farads), these devices can work as tunnel diodes with extremely high (> 1 THz) cut-off frequencies [6, 5, 1]. Such devices can find applications in various fields, e.g. as biological, security or aerospace detectors [8, 3, 7]. Moreover, tunnel junctions with extremely high cut-off frequencies can find application in solar-energy harvesting [2, 4].

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