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**Abstract**

This abstract presents an electrical model of an SRAM cell exposed to a pulsed Photoelectrical Laser Stimulation (PLS), based on our past model of MOS transistor under laser illumination. The validity of our model is assessed by the very good correlation obtained between measurements and electrical simulation. These simulations are capable to explain some specific points. For example, in theory, a SRAM cell under PLS have four sensitive areas. But in measurements only three areas were revealed. A hypothesis was presented in this paper and confirm by electrical simulation. The specific topology of the cell masks one sensitive area. Therefore the electrical model could be used as a tool of characterization of a CMOS circuits under PLS.

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# Electrical modeling of the photoelectric effect induced by a pulsed laser applied to an SRAM cell.

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## 1. Introduction

A Single Event Upset (SEU) [1] is the inversion of the logical state of a memory cell caused by ions or electromagnetic radiation striking one of its sensitive nodes. SEU were first described in 1954 during nuclear testing, when some anomalies were observed in electronic equipments. Nowadays, SEU is a major threat for semiconductor manufacturers. The robustness of chips against SEU could be tested in a cyclotron or by pulsed laser stimulation. This kind of experiments could be very expensive and time consuming. Though physical (e.g. TCAD) simulations may be used, but Spice simulations are faster. In this context, it is interesting to use a tool in order to simulate with a good accuracy the effect of pulsed laser on a chip to analyze its sensitivity to SEU. In this paper, we present an electrical model of the Photoelectric Laser Stimulation (PLS) of an SRAM cell in 0.25µm technology. We used a pulsed laser at 1064nm wavelength to conduct the PLS experiments.

Electrical models of PN junctions under pulsed PLS (N+ on Psubstrat and P+ on Nwell) were previously introduced [2]. We have also already introduced electrical models, based on preliminary studies made from measurements and TCAD simulations [3, 4] for continuous PLS at laser power under ~100mW, which create only photoelectrical effects [5, 6]. This model consists in a simple current source controlled by voltage to model the laser-induced photocurrent. The novelty of the model presented in this paper is that it is one of the first models of a CMOS gate under pulsed photoelectrical laser stimulation which takes into account the interaction between the layout and the Gaussian intensity profile of the laser beam.

This article is organized as follows. Section 2 is a remainder of our past model of PN junction under PLS. Section 3 reviews the SEU mechanism which occurs when an SRAM cell is exposed to PLS. In theory four sensitive areas were expected, however, three were revealed by experiments. A hypothesis is then introduced, based on the topology of the cell, to explain this discrepancy. In section 4 it is proposed to validate our hypothesis by electrical stimulation. Finally, our findings are summarized in the concluding section 5.

## 2. Electrical model of a PN junction under PLS

### 2.1. Laser beam centered on the PN junction

The Drain/Psubstrate junctions of an NMOS and a PMOS transistor (W=L=10µm) in 90nm technology were used in these experiments. From the measurements, we were able to model the photocurrent $I_{ph}$ , induced by a pulsed laser passing through the middle of a reverse biased PN junction, with a first order polynomial function (1):

$$I_{ph} = a \times V + b \qquad (1)$$

where $a$ and $b$ are functions of the laser power $P_{laser}$.

As reported in fig. 1a and 1b, a very good correlation is obtained on the N+/Psubstrate and P+/Nwell junctions between practical measurements and electrical simulations (made with this model).

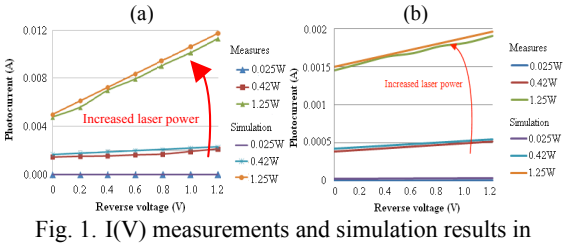


Fig. 1. I(V) measurements and simulation results in reverse biasing conditions for different laser power on (a) N+/Psubstrate and (b) P+/Nwell junctions.

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*2.2. Spatial dependance of the induced photocurrent*

The distance between the laser spot and the PN junction has a strong impact on the value of the generated photocurrent. A mathematical approximation was found in order to model this effect (2) which has a Gaussian shape:

$$\alpha_{gauss}(d) = \left[\beta \times \exp\left(-\frac{d^2}{c_1}\right) + \gamma \times \exp\left(-\frac{d^2}{c_2}\right)\right] \times w \quad (2)$$

where $d$ is the distance between the spot and the closest edge of the junction (µm). $\beta$, $\gamma$, $c_1$ and $c_2$ were found different for each optical lens. Moreover $w$ is a function normalized which takes into account the reduction of the width of the Gaussian profile, when the pulse width decreases under the µs. Hence, equation (3), that incorporates the spatial dependency (and also the junction area $S$), is obtained by multiplying equations (1) and (2).

$$I_{ph} = (a \times V + b) \times S \times \alpha_{gauss} \times V_{laser\_trig} \quad (3)$$

$V_{laser\_trig}$ is a double exponential normalized input signal which trigs the voltage controlled current source. The user thanks to this input signal could choose the moment and the duration of the laser pulse illumination in its electrical simulation.

This model was then used to derive the model of a more complex structure: an SRAM cell, as explainedin the next section.

## 3. SEU sensitivity analysis of an SRAM cell

*3.1. Presentation of the CSRAM cell*

The cell studied in this paper is a configuration SRAM (CSRAM) made of five transistors (see fig. 2) similar to those used to store the configuration bitstream in programmable devices (FPGA). However, we will rather use the term SRAM in this paper, since we believe its main results may be generalized to 6 transistors SRAM.

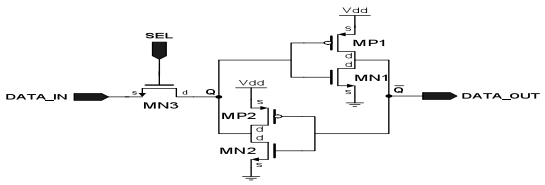


Fig. 2. Schematic of the SRAM cell (CSRAM).

*3.2. Study of the SEU sensitivity of the SRAM cell*

In this subsection, the SRAM sensitivity is studied from a theoretical point of view (considering its schematic and its state).We refer to state one (respectively state zero) when the node *DATA_OUT* is in high state (resp. low state). The sensitivity of the cell can be investigated by considering which PN junctions are the most reverse biased in function of the SRAM state. Indeed two cases are considered: states "1" and "0". The red arrows in figure 3 also give the directions of the induced photocurrents between the Drain or the Source and the Bulk of the different transistors. The thick arrows represent strong photocurrents, the thin arrows smaller ones.

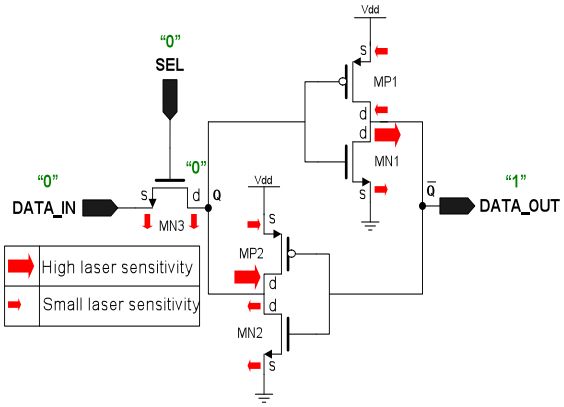


Fig. 3. Schematic of the SRAM cell and laser sensitivity in state "1".

In state "1", the two most sensitive areas to laser illumination are the drain junctions of *MN1* and *MP2*.

In state "0", the intensities of the induced photocurrents are inverted in comparison with the case where the SRAM is at the state of "1". In this case the two most sensitive areas are the drains of *MP1* and *MN2*/*MN3(These two transistors share their drain)*.

Therefore four sensitive areas are expected: two in a state "0" and two others in state "1".

*3.3. Measurement of the SEU sensitivity of an SRAM cell*

The SRAM test series was performed with a pulsed laser equipment. The laser beam at the output of the lens has a spot diameter equal to 1µm. It illuminates the front side of the SRAM cell. The dark red color are used to represent the location of the laser spot when the logical value is modified from "0" to "1", and the dark blue color from "1" to "0" for a laser power equal to 1.1W (See Fig. 4). Secondly the light colors represent

the extension of areas when the laser power is equal to 1.6W.

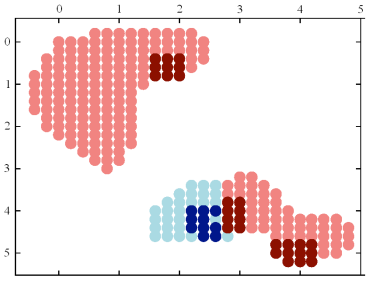

Fig. 4. Cartography of the SEU sensitivity at 1.1W and 1.6W laser power – Experimental results.

Only three sensitive areas were revealed (see fig. 4), despite four were expected according the theory.

### *3.4. Hypothesis of a sensitive area masking effect*

Due to the Gaussian intensity profile of the laser beam on silicon and the reduction of the gate size, it becomes very difficult to illuminate only one junction without creating effects on the others. It is the reason why it is needed to take into account the topology of the cell and the effect of the laser on several junctions at the same time.

The layout of the studied SRAM cell is depicted on figure 5. Note that transistors *MN2* and *MN3* have a shared drain diffusion (which is close to the drain of *MP2*).

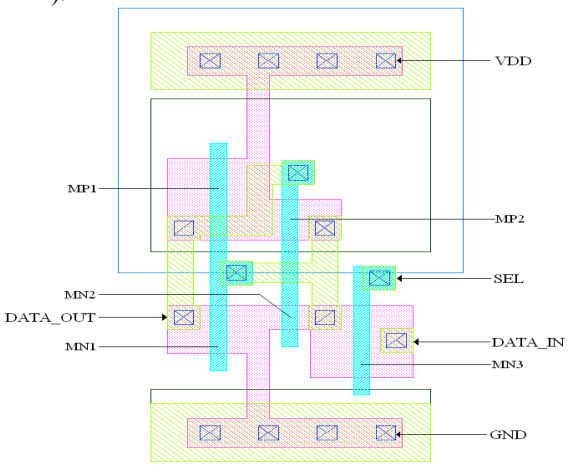


Fig. 5. Layout of the SRAM cell.

We made the hypothesis that this layout has the effect to mask the sensitivity of the drain of *MP2*. Figure 6 illustrates this masking effect which originates from the photocurrent generated by the drain shared between *MN2* and *MN3* (blue arrows) that counterbalances the effect of the photocurrent induced in the Drain/Nwell junction of *MP2* (crossed arrow). This effect lies in the proximity between the drains of *MP2* and *MN2/MN3*, and also in their sizing.

Therefore with a Gaussian approach there is only one sensitive area in state "1" which is the Drain/Psubstrate junction of *MN1*. There is no such similar counterbalancing effect in state "0".

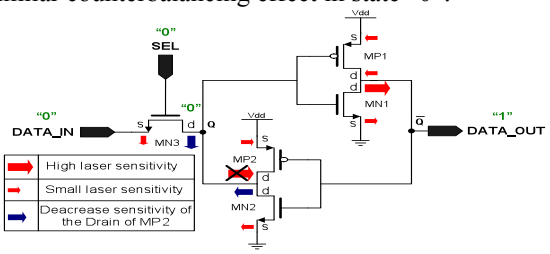


Fig. 6. Illustration of the sensitivity masking effect in state "1".

It is then proposed to illustrate thanks to electrical modeling these effect of topology which give us only three sensitive areas, while four are expected in theory.

## 4. Electrical model of the SRAM cell under PLS

In this part we present an electrical model of the SRAM cell under Photoelectrical Laser Stimulation.

The aim of this modeling is to validate our methodology in order to explore some specific results with a very fast calculation time. It could be a great help to understand some physical phenomenon which occurs when a CMOS gate is exposed to a pulsed PLS.

For each PN junction, a sub circuit *Iph_Diode* is added to the netlist of the SRAM cell (See Fig. 7).

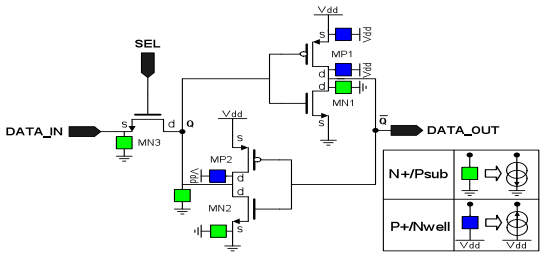


Fig. 7. Electrical model of the SRAM cell under PLS.

In this layout, some junctions are shared (Sources of *MP1* and *MP2*, sources of *MN1* and *MN2*, and drains of *MN2* and *MN3*).

### *4.1. Principle of cartography by electrical modeling*

In order to well model electrical laser cartographies of the SRAM cell a simple procedure is used. Firstly it is necessary to create a meshing on the layout of the cell. For each point of the mesh, the distance between this point and all the PN junction centers of the SRAM cell are measured. Mainly thanks to equation (2), for each point of the mesh, the photocurrent generated by every PN junction is simulated. This methodology permits to create electrical laser cartographies of the SRAM cell under PLS.

*4.2. Electrical cartographies*

In this section, cartographies made from our electrical model are presented and compared to measurements.

Firstly the laser used in electrical simulation is at a low level. The ELDO simulator (based on a Spice language) probes the output of the SRAM *(DATA_OUT)*. The dark red color is used to represent the location of the laser spot when the logical value is modified from "0" to "1", and the dark blue color from "1" to "0" (See Fig. 9). Secondly the light colors represent the extension of areas when the laser power is at a high level.

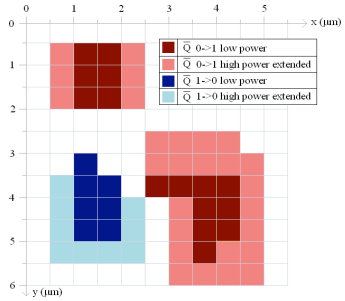


Fig. 9. Cartography of the SRAM SEU sensitivity for two different laser powers – Electrical simulation.

A very good correlation is attained between the cartographies drawn from experiments (see fig.5) and those drawn from electrical simulations (fig. 9). This confirms the good results already obtained on single test transistor and also proves that these models still hold for more complex logic gates.

The waveforms of the photoelectric currents and node voltages involved in the masking effect will be added in the final version of this paper. They make it possible to confirm the hypothesis introduced in subsection 2.2.

## 5. Conclusion

An electrical model which permits the SPICE simulation of an SRAM cell was built, and validated by the very good correlation obtained with measurements. It is also could be a characterization tool of laser effects on CMOS circuits before manufacturing.

In the case of our SRAM cell, the electrical simulation permits us to understand some specific points. In theory four sensitive areas to PLS are expected on an SRAM. But, the modeling of the cell permits us to validate our hypothesis of masking of one sensitive area due to the topology of the cell. In term of perspective this tool presented in this paper will permits to understand some specific effect, and help designer in order to find and simulated countermeasures against SEU. The very good correlation obtained between the cartographies drawn from simulations and measurements shows the relevance of this approach. It will offer to designers the ability to test the fault or SEU sensitivity of logic gates at design time (before an actual test chip is issued).

## References

[1] P. E. Dodd, Physics-Based Simulation of Single-Event Effects, Device and Materials Reliability, IEEE Transactions on , vol. 5, N°3, 2005.

[2] A. Sarafianos, J-M Dutertre, O. Gagliano, M. Lisart, V. Serradeil, A. Tria, " Electrical modeling of the photoelectric effect induced by a pulsed laser applied to an NMOS transistor.," IRPS 2013. "In press"

[3] R.Llido, A. Sarafianos, O. Gagliano, V. Serradeil, V. Goubier, M. Lisart, G. Haller, V. Pouget, J.M. Dutertre, A. Tria, Characterization and TCAD Simulation of 90nm Technology NMOS Transistor Under Continuous Photoelectric Laser Stimulation for Failure Analysis Improvement, IPFA 2012.

[4] R.Llido, A. Sarafianos, O. Gagliano, V. Serradeil, V. Goubier, M. Lisart, G. Haller, V. Pouget, J.M. Dutertre, A. Tria, Characterization and TCAD Simulation of 90nm Technology NMOS Transistor Under Continuous Photoelectric Laser Stimulation for Failure Analysis Improvement, ISTFA 2012.

[5] A. Sarafianos, R. Llido, O. Gagliano, J.M. Dutertre, M. Lisart, V. Serradeil, V. Goubier, V. Pouget, D. Lewis, A. Tria, Building the electrical model of the Photoelectric Laser Stimulation of an NMOS transistor in 90nm technology, ISTFA 2012.

[6] A. Sarafianos, R. Llido, O. Gagliano, J.M. Dutertre, M. Lisart, V. Serradeil, V. Goubier, V. Pouget, D. Lewis, A. Tria, Building the electrical model of the Photoelectric Laser Stimulation of an PMOS transistor in 90nm technology, ESREF 2012.