Efficiency Comparison of Inductor-, Capacitor- and Resonant-based Converters Fully Integrated in CMOS Technology

Pascal Yoann, Gael Pillonnet

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Y. Pascal and G. Pillonnet

***Abstract*—The full integration of DC-DC converters offers great promise for dramatic reduction in power consumption and the number of board-level components in complex systems on chip. Some papers compare the numerous published on-chip and on-die converter structures, but there is the need for an approach to accurately compare the main basic DC-DC conversion topologies. Therefore, this paper presents a method to compare the efficiencies of CMOS integrated capacitive-, inductive- and resonant-based switching converters. The loss mechanism of each structure in hard-switching conditions is detailed and the analytical equations of the power loss and output voltage are given as a function of few CMOS technology parameters. The resulting models can be used to accurately predict converter efficiency in the early design phase, to compare the basic structure in particular the technology node or to orient the passive choice. The proposed method is then applied to design, optimize and compare fully-integrated power delivery requirements on a 1mm^2 on-die area in 65nm CMOS technology over three decades of power density. The results also underline the high efficiency of the promising resonant-based converter.**

***Index Terms*—integrated switching power supply, on-chip voltage regulator, switched-capacitor converter, inductive power converter, resonant converter**

I. Introduction

MOST modern circuits on a single chip in deep submicron CMOS technology integrate various blocks such as multicore digital processing, memories, sensor, actuator interfaces and wireless transmission. Each function often requires a dedicated and variable supply voltage for power-saving techniques and high performance issues. In addition, numerous step-down and step-up DC-DC converters are needed to convert the continuous energy source (generally from a chemical battery in the embedded system) into lower or higher DC power rails. As the power distribution network is at a higher scale (e.g. country level), the power tree definition in modern circuit and board levels is a great challenge to provide multiple power rails with high efficiency and low cost in a small footprint area.

DC-DC switching converters are always composed of the four main functions illustrated in Figure 1. The switching cell is used to modulate the power flow from the battery to the source through the intermediate energy storage. The control block changes the switch state to deliver constant and regulated output voltage against line, own variation, and load variations. The converters are categorized according to the intermediate energy storage type i.e. capacitor-, inductor- or resonant-based converters. Here, the linear regulator is out of scope for it dissipates the intermediate energy into thermal energy, implying low power efficiency, at best equal to the conversion ratio (defined by output to input voltage ratio).

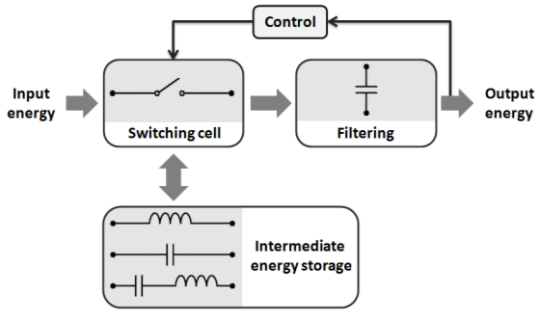

Fig. 1. Switched power converter principle.

Use of an off-chip converter is currently the most efficient way to provide multiple power domains but it is a bulky solution mainly due to the extra components needed around the powered circuit on the motherboard footprint. Nowadays, on-chip power management seems to be a suitable solution to provide clean, fine, high speed and granular power supply modulation for the modern circuit without bulky external components or additional circuits. This paper discusses the integration of a DC-DC converter for chip-scale power management.

There are two levels in which the on-chip power supplies can be integrated. These are the in-package and on-die solutions. In-package converters combine different technologies to integrate the switching cell, and the passive and control in the same package as the powered circuit [1]. Using non-standard processes such as deep-trench capacitors [2], magnetics on silicon [3] or wide band-gap technology [4] lead to the converter being potentially smaller and having a higher power efficiency than an on-die solution, though the 3D heterogeneous assembly of the converter and its load could be a cost issue. The second integration level i.e. on-die consists of the integration of the converter on the same

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Y. Pascal and G. Pillonnet are with Univ. Grenoble Alpes, F-38000 Grenoble, France, and CEA, LETI, MINATEC Campus, F-38054 Grenoble, France (e-mail: gael.pillonnet@cea.fr).

Y. Pascal is also with the École polytechnique, Département de Physique, 91128 Palaiseau, France.

technology as the powered circuit [5], [6]. The key issue is the integration of the passive for intermediate energy storage (Fig. 1). Some research proposes numerous design refinements to overcome the low energy capability of the integrated passive components. For example, high switching frequency [7] [8], series-parallel switching cell connection [9] [10], or coupling of passives [11] help to improve the converter performance. However, the recently published on-die power converters still achieve performance far from the industrial targets [12] in terms of power density, voltage regulation, efficiency versus conversion ratio or direct battery connection compatibility.

The integration of magnetic material and the permeability at high frequency in standard CMOS technology are the major roadblocks [13] which account for the fact that most publications focus on on-die capacitor-based converters. By using numerous design refinements, this previous work confirms that the switched capacitor topology is suitable in order to maintain about 80% of the efficiency for a 1W power delivery on a 1mm² die area [6], though capacitor-based converters still suffer from low power efficiency outside their discrete conversion ratios and efficiency limitation for higher power density. Other converter topologies could overcome the above limitations such as inductor-based converters [7], hybrid structures [14] or resonant-based converters [15], these topologies being widely used in higher power electronic applications. However, these are not studied mainly due to the poor energy density of their intermediate storage elements on a mm^2 scale [12].

In the on-die context, there is a need to compare converter architectures fully-integrated in CMOS technology, even the two simplest step-down topologies: the buck and switched capacitor converter. Numerous papers compare published results but it is difficult to know if the converter performance comes from the technology or from the topology itself. Work in [16] provides a general design survey for the capacitive- and inductive-based converters, but the compact expressions of the converter efficiencies are not given. Discussion in [17] only compares the inductive converter across the range of technologies from 0.35µm to 90nm. However, [18] shows some fundamental limits of the converter topologies but it does not provide a complete efficiency comparison in the same context. Based on the state-of-the-art, the system-level designer does not have any compact model to compare the expected performance, in a particular silicon technology, even with the two basic and well-spread inductive and capacitive hard-switching converters. Therefore, this paper aims at comparing those basic topologies and the recently emerging resonant converter [15, 23, 24] for on-die DC-DC conversion. We give the analytical expressions of the efficiency for the three converters using few silicon technology parameters which are extracted from basic simulations. Based on our modeling, we optimize the power efficiency of the three particular converters over a three decade power range (from 0.1 to 10W) using 65nm CMOS technology under similar conditions to derive our approach. Those on-die converters are fully-integrated (active and passive), the passives of each are integrated on 1mm² of die.

In this paper, sections II, III and IV detail the basic operations and key loss mechanisms of capacitive, inductive and resonant converters using basic topology without refinements (i.e. no interleave or soft-switching). In 65nm CMOS technology, these three particular topologies are then compared in Section V. The annexes give the general assumptions of the paper and describe the unified constants used in the paper.

II. Capacitor-Based Converter

The capacitor-based converter topology operates in two phases to transfer the power from the input V_{in} to the output V_o through an on-die flying capacitor C_{fly} as shown in Figure 2 where R_s models C_{fly} equivalent series resistance, and C_{bot} models C_{fly} capacitive coupling with the substrate. In the first phase, both MOSFETs M2 and M4 are closed and the capacitor C_{fly} is charged from the input source through the output load R_{ld}. In the second phase, the energy previously stored in C_{fly} is transferred to the output using transistors M1 and M3. Then, the voltage ripple across the flying capacitor is proportional to the transferred energy and the output power can be expressed as:

$$P_o = f_{sw} C_{fly} V_o \, \Delta V_{C_{fly}} \quad (1)$$

where $\Delta V_{C_{fly}} = V_{in} - 2V_o$.

A. Loss mechanism

Since this topology is well-studied in the literature [6], [19], [25], [26] this section briefly describes the loss mechanism for further comparison with inductive- and resonant-based converters.

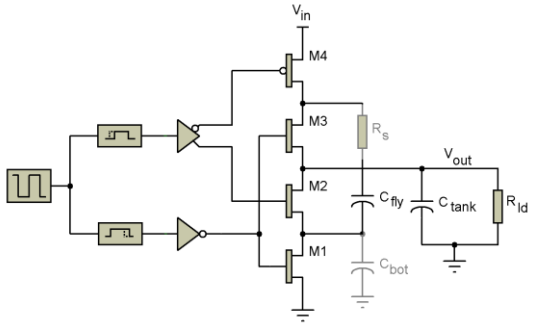

Fig. 2. Capacitor-based converter schematic.

The total losses of the converter, valid both in SSL an FSL regions [6], can be expressed as:

$$P_{loss} = P_{sw} + P_{cond} + P_{trans}$$

where the switching losses P_{sw} are due to the switching of the transistors M_1 to M_4, P_{cond} is the transistor conduction loss due to the load current, and the transfer loss P_{trans} is caused by the flying capacitor being partially charged and discharged by the bottom plate capacitance C_{bot} and lastly by the equivalent series resistance R_s. P_{trans} is dissipated in the power transistors but it is separated to give a unified approach and highlight the loss difference between the converter topologies.

According to previous work [6, 9, 19, 23], the total loss can then be expressed by the following equation:

$$P_{loss} = \underbrace{\lambda_{C_{in}} f_{sw} V_{in}^2 \sum W_i}_{\text{MOSFET input capacitance}} + \underbrace{\frac{1}{2} I_o^2 \sum \frac{\Lambda_i}{W_i}}_{R_{ds_{on}}} + \underbrace{I_o^2 R_S}_{\substack{\text{Flying capacitor} \\ \text{ESR}}} + \underbrace{V_o^2 k_{bot} C_{fly} f_{sw}}_{\text{Bottom plate}} + \underbrace{I_o^2 \frac{1}{4 C_{fly} f_{sw}}}_{\substack{\text{Switched Capacitor} \\ \text{impedance}}} \quad (2)$$

where $\{f_{sw}, W_i\}$ are the design freedom parameters.

The different notations are defined in Table 2 and the Annex. Equation (2) may be rewritten to highlight the part of each free parameter $\{f_{sw}, W_i\}$ so that:

$$P_{loss} = A f_{sw} \sum W_i + B \sum \frac{\Lambda_i}{W_i} + C \left(1 + D f_{sw} + \frac{E}{f_{sw}}\right) \quad (3)$$

where (A, B, C, D, E) are constants depending on the technology used and the design constraints (Table 5).

Increasing $(W_i)_i$ leads to a decrease of P_{cond} but to an increase of P_{sw}. Likewise, increasing f_{sw} diminishes P_{trans}, though it magnifies P_{sw}. Therefore, an optimal point can be found to maximize the power efficiency η, defined by:

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{V_o^2}{V_o^2 + R_{ld} \cdot P_{loss}} \quad (4)$$

From these equations, it should be highlighted that the flying capacitor value C_{fly} has to be maximised to improve the power efficiency. The efficiency of this topology is then closely linked to the capacitance density allowed by the technology, which enables comparison of previous work using very delicate heterogeneous technologies.

B. Output voltage

The output voltage V_o has to be determined to solve equation (2) to then find the overall efficiency (4). As described in [8], the capacitor-based converter can be modeled in steady-state as an output impedance R_o and an ideal voltage source with 2:1 conversion ratio. According to previous publications such as [6], V_o can be expressed as:

$$V_o = \frac{R_{ld}}{R_{ld} + R_o} \frac{V_i}{2} \quad (5)$$

where $R_o = \frac{1}{4 C_{fly} f_{sw}} + \frac{1}{2} \sum \frac{\Lambda_i}{W_i} + R_s$

III. Inductor Based-Converter

The schematic of the inductive converter (i.e. buck converter) is given in Fig. 3. For CMOS compatibility, an air-core inductor is used for the intermediate energy transfer; R_{ind} models the inductor parasitic resistance. In the first phase, the transistor M_1 allows energy to fly from the source to both the inductor and the output; in the second phase, the circuit is free-wheeling and part of the energy stored in the inductor is transferred to the output. The energy transfer is proportional to the average current in the inductor, and the output power can be expressed as $P_o = V_o \langle I_L \rangle$, where $\langle I_L \rangle$ is the mean coil current.

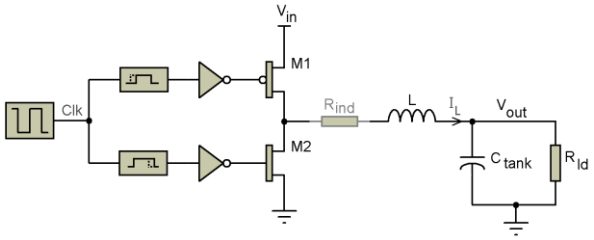

Fig. 3. Buck converter schematic.

A. Loss mechanism

Since the inductive topology is well-known in the power electronic field, this section briefly describes the loss mechanism and gives compatible expressions with capacitive- and resonant-based converters for further comparison. The effect of the design parameters is also underlined for clarifying the optimization performed in Section V.

In CCM, the expression for the switching and conduction losses $P_{sw} + P_{cond}$ is the following:

$$\lambda_{C_{in}} V_{in}^2 f_{sw} \sum W_i + I_{L_{RMS}}^2 \left(D_c R_{ds_{on}}(M_1) + (1 - D_c) R_{ds_{on}}(M_2)\right) \quad (6)$$

where $I_{L_{RMS}}$ is the RMS current flowing through the coil and $D_c \cong V_o / V_{in}$ is the duty cycle of the clock signal. Assuming that the coil current is triangular ($\frac{L}{R} \gg T_{clk}$), its RMS value is given by:

$$I_{L_{RMS}}^2 = I_o^2 + \frac{1}{12} \left(D_c \frac{V_{in} - V_o}{L f_{sw}}\right)^2 \quad (7)$$

Then, the conduction loss due to the DC and ripple currents can be directly expressed from the design freedom parameters $\{f_{sw}, W_i, L\}$ as:

$$P_{cond} = \left(I_o^2 + \frac{1}{12} \left(D_c \frac{V_{in} - V_o}{L f_{sw}}\right)^2\right) \left(D_c \frac{\Lambda_1}{W_1} + (1 - D_c) \frac{\Lambda_2}{W_2}\right) \quad (8)$$

The transfer loss due to the inductor series resistance R_{ind} can be expressed as:

$$P_{trans} = R_{ind} I_{L_{RMS}}^2 = \frac{L}{FoM_L(S)} \left(I_{out}^2 + \frac{1}{12} \left(\frac{V_o}{V_{in}} \frac{V_{in} - V_o}{L f_{sw}}\right)^2\right) \quad (9)$$

where $FoM_L(S)$ is the Figure of Merit (FoM) L/R_{ind} of the inductor of surface S.

The sum of the losses described above can be factorized to highlight the effect of the free design parameters$\{f_{sw}, W_i, L\}$:

$$P_{loss} = P_{sw} + P_{cond} + P_{trans} = A f_{sw} \sum W_i + \left(F \left(\frac{1}{W_1} + \frac{G}{W_2}\right) + JL\right) \left(1 + \frac{H}{L^2 f_{sw}^2}\right) \quad (10)$$

where F, G and H are constants depending on the CMOS technology used and the design constraints (load, input voltage).

Only CCM is studied here because this technique is well-spread for high power density converters [16, 17]. Then, DCM and BCM are out of the scope of this paper. The soft-switching technique for an inductive-base converter could be a relevant solution to decrease the switching loss but we decided to compare the three converter families with the most basic behavior to show the root limitations of each structure without design refinement. As shown in the state-of-the-art, there is a lack of comparison even using the simplest design structures.

As for the capacitor-based converter, the inductor-based converter exhibits an optimal sizing maximizing the power efficiency under particular input and output voltages, die area

and load value. Section V gives the optimization results under the specifications targeted in this paper.

B. Output voltage

For the same reason as in Section 2, the value of the output voltage has to be found in order to calculate the loss expression (10) and the efficiency. At steady-state, the linear model of the converter is the same as that of a capacitor-based converter (cf. Section 2.*B.*), except for the value of R_0 and that the ratio of the ideal transformer is $1:D_c$. V_o can then be expressed as:

$$V_o = D_c V_i \frac{R_{ld}}{R_{ld}+R_o} \tag{11}$$

where $R_o = \frac{L}{FoM_L(S)} + D_c\frac{\Lambda_1}{W_1} + (1-D_c)\frac{\Lambda_2}{W_2}$

IV. Resonant-Based Converter

Although numerous architectures of resonant-based converters exist, the topology, shown in Figure 4, has been selected for its intrinsic performance (low switch count and straightforwardness) and to provide the finest comparison with the capacitive converter. The structures of those circuits are indeed similar, except that the flying capacitor of the capacitive converter is replaced by an LC tank as published in [15, 20, 21, 23, 24].

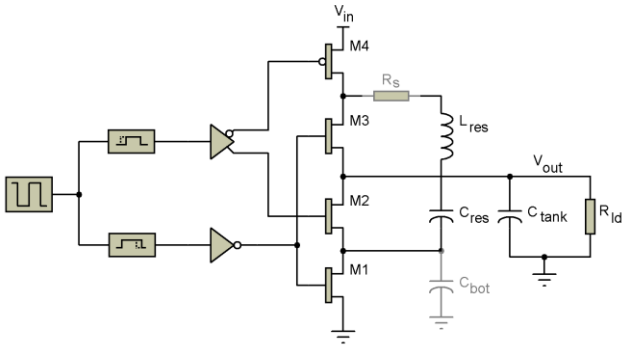

Fig. 4. Resonant-based converter.

A. Loss mechanism

The resonant topology exhibits its highest efficiency at the resonant frequency, here $f_{res} = \left(2\pi\sqrt{L_{res}C_{res}}\right)^{-1}$. With a high-Q tank at its resonant frequency, and by considering only the fundamental of the Fourier decomposition of the current and voltage signals of the converters, there is no large error and the analysis is greatly simplified. This approximation is used below to describe the loss mechanism.

The switching and conduction losses can be expressed as:

$$P_{sw} + P_{cond} = \lambda_{C_{in}} f_{sw} V_{in}^2 \sum W_i + \frac{1}{2} I^2_{res_{RMS}} \sum R_{ds_{on}}(M_i) \tag{12}$$

where $I^2_{res_{RMS}}$ is the RMS current in the resonator.

At the resonant frequency, the RMS LC tank current can be expressed thus:

$$I_{res_{rms}} = \frac{\pi}{2\sqrt{2}} I_o \tag{13}$$

Then:

$$P_{cond} = \frac{\pi^2}{16} I_o^2 \sum \frac{\Lambda_i}{W_i} \tag{14}$$

The transfer losses are due to the tank parasitic resistance R_s and the bottom plate capacitance C_{bot} of C_{res} so that:

$$P_{trans} = I^2_{res_{RMS}} R_s + k_{bot} C_{res} f_{sw} V_o^2 = \underbrace{\frac{\pi^2}{8} I_o^2 \frac{R_{cap}(S)}{\alpha}}_{\text{Capacitor's ESR}} + \underbrace{\frac{I_o^2}{32 f_{sw}^2 \alpha\sqrt{1-\alpha}\, S\, \lambda_C FoM_L(S)}}_{\text{Inductor's ESR}} + \underbrace{k_{bot}\alpha S \lambda_C V_o^2 f_{sw}}_{\text{Capacitor's bottom plate}} \tag{15}$$

where α is the fraction of the resonator die area dedicated to integrating the resonant capacitor.

Finally, considering only the parameters yet to be optimized $\{W_i, f_{res}, \alpha\}$, the power loss can be expressed as follows (N.B. valid only at the resonant frequency):

$$P_{loss} = A f_{res} \sum W_i + \frac{\pi^2}{8} B \sum \frac{\Lambda_i}{W_i} + \frac{K}{\alpha}\left(1 + \frac{N}{f_{res}^2\sqrt{1-\alpha}}\right) + Q\alpha f_{res} \tag{16}$$

where K, N and Q are technology- and design-dependent constants. As for the other topologies, the resonant-based converter exhibits optimal sizing thus maximizing the power efficiency.

B. Output voltage

The linear model of this converter is identical to that of the capacitive-based converter. Hence, the expression for V_o is:

$$V_o = \frac{R_{ld}}{R_{ld}+R_o}\frac{V_i}{2} \tag{17}$$

and at resonance $R_o = \frac{\pi^2}{8}\frac{R_{cap}(S)}{\alpha} + \frac{1}{32 f_{sw}^2 \alpha\sqrt{1-\alpha}\, S\, \lambda_C FoM_L(S)} + \frac{\pi^2}{16}\sum\frac{\Lambda_i}{W_i}$.

The next section compares the power efficiencies of the topologies under study in similar conditions.

V. Topology Comparison

A. Loss distribution comparison

The expression of the switching, conduction and transfer losses of the three topologies are summarized in Table 1.

TABLE I
Summary of the Expressions of the Losses

	Inductive	Capacitive	Resonant *At resonance*
P_{sw}	$\lambda_{C_{in}} f_{sw} V_{in}^2 \sum W_i$	$\lambda_{C_{in}} f_{sw} V_{in}^2 \sum W_i$	$\lambda_{C_{in}} f_{sw} V_{in}^2 \sum W_i$
P_{cond}	$\left[I_o^2 + \frac{1}{12}\left(D_c\frac{V_{in}-V_o}{L f_{sw}}\right)^2\right]\cdot \left[\frac{V_o}{V_{in}}\frac{\Lambda_1}{W_1} + \frac{V_{in}-V_o}{V_{in}}\frac{\Lambda_2}{W_2}\right]$	$\frac{1}{2} I_o^2 \sum \frac{\Lambda_i}{W_i}$	$\frac{\pi^2}{16} I_o^2 \sum \frac{\Lambda_i}{W_i}$
P_{trans}	$\frac{L I_o^2}{FoM_L(S)} + \frac{(V_{in}-V_o)^2}{12 L f_{sw}^2 FoM_L(S)} D_c^2$	$I_o^2 R_s + V_o^2 k_{bot} C_{fly} f_{sw} + I_o^2 \frac{1}{4 C_{fly} f_{sw}}$	$\frac{\pi^2}{8} I_o^2 \frac{R_{cap}(S)}{\alpha} + \frac{I_o^2 \cdot (\alpha\sqrt{1-\alpha})^{-1}}{32 f_{sw}^2 S\, \lambda_C FoM_L(S)} + k_{bot}\alpha S \lambda_C V_o^2 f_{sw}$

From this table, it can be seen that the values of the free variables are different in each topology, depending on the global optimization of the overall losses. Compared to the capacitor based-converter, the conduction loss in the resonant topology is $\frac{\pi^2}{8}$ times lower with the same total width $\sum W_i$. The resonance phenomena avoids the charge-sharing loss of the capacitive topology (E/f_{sw}) but adds loss due to the

equivalent series resistor of the LC tank. Further general comparison is difficult due to the effect of each constant value (A to Q) depending on the technology, and input and output constraints.

The authors have chosen a particular application target, similar to the common industrial specification, to compare the three structures. It is important to note that *the compact equations given above could be quickly solved by an IC designer to find their own optimal design parameters for other converter constraints and technology node*. The following sections therefore only illustrate one particular result from the proposed method.

B. Converter specifications and process parameters

The three topologies are compared using the same following constraints:

- Technology = 65nm CMOS technology from STM is chosen to integrate the converters in a standard technology.
- Die-size = a constant 1mm² die area is dedicated to the passive components transferring the energy i.e. C_{fly}, L, $\{L_{res}, C_{res}\}$. The size of the switching cell is not considered in the first step.
- Input/output characteristics = the input supply voltage V_{in} is set at 1.8V, provided by an external DC-DC converter; the output V_o is ideally bypassed to limit its ripple to 5%.
- Load = the converters are loaded by a resistor R_{ld} inducing 0.1, 1 and 10W power dissipation under ½ conversion ratio (i.e. $V_o = 0.9\text{V}$). Thus, nine circuits i.e. three topologies at three different power levels are studied.
- Switching cell design = switches are MOSFET-type transistors with thick oxide. The double oxide option is used to have 2.5V breakdown voltage transistors. Although the voltage applied to the transistors of the capacitive-based converter is equal to $V_{in}/2$ at steady state for a conversion ratio of ½, it is as high as V_{in} at start-up and if the output voltage is modulated. Input voltage rated transistors are therefore required. Dead-time effects are also incorporated in the simulation results.
- On-die capacitor = n-well polysilicon and metal-metal capacitors are stacked to achieve the highest capacitance density in the considered technological node [22]. The MIM option is not used.
- On-die inductor = the inductors are a stack of five layers of metal (M3-M7). Metal layers M1 and M2 are not used to minimize the coupling with the substrate. Coils are planar and octagonal, and designed to maximize the L/R_{ind} ratio.

Table 2 summarizes the process parameters used in the following optimization.

C. Consideration of the energy densities of the passives

We know that the output power of a capacitor-based converter is proportional to the voltage ripple across its flying capacitor whilst that of an inductive-based converter is proportional to the mean current in its coil. We have observed that there is no direct correlation between the maximum energy densities of integrated passives and the output power of the converters using them. Extreme care should therefore be taken when attempting to compare topologies according to the stored energy density of their passives. The energy density of an inductor being a decade lower than that of a capacitor (see Table 4) should not lead one to believe that the power density of the inductive converters is intrinsically lower than that of the capacitive ones.

TABLE II
65NM CMOS PROCESS PARAMETERS

Parameter	Notation	Value	Unit
N-MOSFET channel resistivity (1)	λ_R	1.3	kΩ. µm
N-MOSFET threshold voltage(1)	V_T	0.51	V
Gate capacitance per transistor unit length (1)	$\lambda_{C_{in}}$	1.7	fF/µm
Integrated capacitance density for C_{fly} and C_{res}(2)	λ_C	16	fF/µm²
Bottom plate capacitance coefficient $C_{bot} = k_{bot}C_{fly}$ (2)	k_{bot}	2	%
Figure of Merit L/R_{ind} of an integrated inductor for 1mm²	$FoM_L(S)$	7	nH/Ω
Equivalent Series Resistance of an integrated capacitor of surface S (3)	$R_{cap}(S)$	0	Ω. µm²

Note: (1) Thick oxide 280nm-long channel transistor, driving voltage 1.8V; (2) Stacked thin oxide polysilicon and metal capacitors; (3) Although the analytical study takes into account the capacitor series resistance, it is neglected in the transistor level simulations.

D. Two-step optimization procedure

The optimization focuses on the ½ step-down conversion ratio since it achieves the best results for the capacitor- and resonant-based converters.

1) Global optimization

Based on equations (2), (10) and (15), the optimization procedure finds the peak efficiency with respect to the free design variables. Three converters of each topology are optimized using different load resistors, according to the specifications stated above. When a ½ transfer ratio is achievable (i.e. in the inductive converter), we maximize the efficiency at this conversion value; otherwise, the optimization aims to achieve the highest possible efficiency, while disregarding the associated transfer ratio.

Optimization aims at giving the best values to the set of parameters $\mathcal{F}_{topo}$ describing each topology. The analytical computation of the partial derivatives of P_{loss} with respect to the converter parameters provides the optimum values of these parameters in the models described in Sections II to IV. For each topology, we hence solve the system $\mathcal{S}_{topo}$ such that:

$$\mathcal{S}_{topo} = \left\{ \frac{dP_{loss}}{dx} = 0 \;\middle|\; x \in \mathcal{F}_{topo} \right\},$$

$$\begin{cases} \mathcal{F}_{capacitive} = \left\{ \{W_i\}_{i\in[\![1,4]\!]}, f_{sw} \right\} \\ \mathcal{F}_{inductive} = \left\{ \{W_i\}_{i\in[\![1,2]\!]}, f_{sw}, L \right\} \\ \mathcal{F}_{capacitive} = \left\{ \{W_i\}_{i\in[\![1,4]\!]}, f_{res}, \alpha \right\} \end{cases}$$

2) Local optimization

A local post-optimization of these parameters is then conducted through transistor-level simulations in order to take into account the losses neglected in the proposed models such as MOSFET output capacitance. As shown in Table 3, the analytical equation and transistor-based simulation gives similar results. The second step i.e. local optimization

improves the result accuracy.

TABLE III
ANALYTICAL MODEL AND TRANSISTOR-BASED SIMULATIONS UNDER $R_{ld} = 0.81\Omega$

Power efficiency [%]	Analytical model	Transistor-based simulation	Error [%]
Capacitive converter	64	65	2.1
Inductive converter	66	63	−5.3
Resonant converter	77	79	2.6

3) Two- step optimization results

The effective metric of the technology used and the optimal component sizing are given in Table 4 when all free variables are adjusted to achieve the highest efficiency close to 1.8V to 0.9V conversion.

TABLE IV
OPTIMAL PARAMETERS FOR THE USE-CASE

Topology	Parameter	Value			Unit
All	Load	8.1	0.81	0.081	Ω
	Power density (1)	0.1	1	10	W/mm^2
Capacitive converter	On-die capacitor	16	16	16	nF
	Cap energy density	6.5	6.5	6.5	nJ/mm^2
	Switching frequency (2)	15	50	400	MHz
	Switch surface	0.02	0.11	0.56	mm^2
Inductive Converter *CCM mode, hard-switching*	On-die air-core inductor (3)	4.2	0.9	0.2	nH
	Inductor FoM (L/R_{ind})	8.5	8.4	6.5	nH/Ω
	Inductor energy density	0.065	0.3	0.85	nJ/mm^2
	Switching frequency	160	170	145	MHz
	Switch surface	0.02	0.06	0.6	mm^2
Resonant converter	On-die air-core resonant inductor (3)	0.53	0.3	0.06	nH
	Inductor FoM (L/R_{ind})	5.3	5	5	nH/Ω
	LC quality factor (4)	0.4	1.7	1.9	-
	Tank energy density	4.5	4.7	6.0	nJ/mm^2
	Resonant frequency	67	88	200	MHz
	Switch surface	0.03	0.06	1.4	mm^2

Note: (1) targeted, given at $V_o/V_{in} = 0.5$; (2) at maximum efficiency; (3) value at the switching frequency; (3) including all parasitic resistances in the resonator ($R_{ds_{on}}$, R_s).

E. Discussion of optimal design parameters

In the inductive and resonant converters, the inductor value diminishes with the output load, thus decreasing its losses and allowing a higher energy transfer. Likewise, this phenomena is responsible for the switches of capacitive-based converters being narrower than that of a resonant-based converter.

In buck converters using discrete inductors, potentially exhibiting high efficiency and high inductance, the inductor current ripple $r = \Delta I_L/I_L$ is often set to about 20% [13]. Nonetheless, in our circuit using a low value inductance and a high switching frequency, simulations have shown that it is best to choose $r > 100\%$, hence remaining in continuous conduction mode whilst allowing negative current to flow into the coil.

The C_{tank} value required to maintain less than 5% output ripple in non-interleaved converters is at most 450nF and is not integrated on-die. Interleaving allows reduction of C_{tank} [15], but the need for a bypass is greater in a resonant than a capacitive converter because the flying capacitor of the capacitive topology inherently bypasses the output [6].

In resonant mode, the overvoltage appearing across the resonant capacitor induces stress thus prohibiting the use of high-density thin oxide polysilicon capacitors (1.2V max in CMOS 65nm). A thick oxide polysilicon capacitor (2.5V max) is thus mandatory, decreasing its density. This topology uses a small inductor to resonate. Small rising and falling times induce high di/dt and dv/dt, which are potentially detrimental to the circuit. However, the simulations do not incorporate parasitic inductances which would limit the actual stress on the components.

The FoM of the switches and the capacitor are only technology dependent whereas that of inductors depends on the design. In fact, for first order and for a planar inductor, $FoM_L(S) \propto \sqrt{S}$. This highlights the fact that inductive-based converters are best suited for high power and large die-area applications.

Figure 5, deduced from (10), shows the influence of the FoM of the inductor of the inductive converter optimized according to the specifications stated in Section V.B at $R_{ld} = 0.81\Omega$ on the overall efficiency at $V_o/V_{in} = 0.5$. All the parameters but FoM_L are those of the 65nm CMOS technology. The point on the x-axis at $8.4\text{nH}.\Omega^{-1}$ indicates the FoM of the coil used in this work. This clearly shows that implementing the inductor of the lowest achievable resistance should be the first concern of the IC-designer.

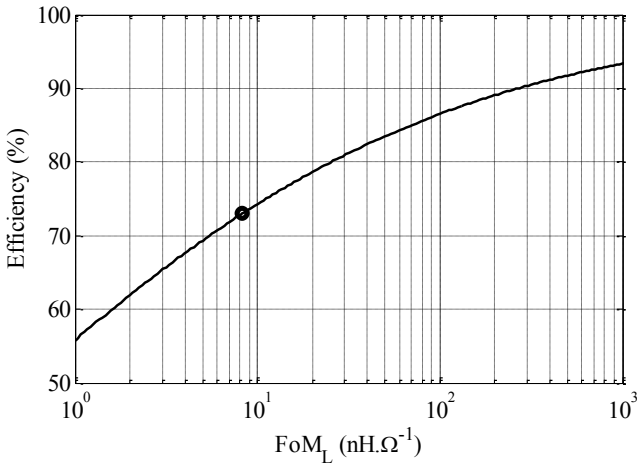

Fig. 5. Efficiency of the optimized inductive-based converter vs. FoM$_L$ at $V_o/V_i = 1/2$ and $R_{ld} = 0.81\Omega$.

F. Efficiency comparison of the optimized converters

In an inductive converter, varying the duty cycle of the control signal modulates the output voltage without reducing the efficiency. In the capacitor- and resonant-based converters, the conversion ratio is modulated by the switching frequency, which leads to additional energy transfer losses. Based on transistor level simulations, Fig. 6 shows the power efficiency over the conversion ratio of the nine optimized converters (three per topology, three per load value), where all free variables are adjusted.

The inductor-based topology appears to maintain a more constant efficiency over a wide voltage range, although the study does not include reconfigurable topologies for switched capacitors nor resonant converters.

Using the results from Fig. 6, Figure 7 shows the peak power efficiencies of the optimized converters vs power density.

At the lowest power density i.e. at $R_{ld} = 8.1\Omega$, the capacitor and resonant-based converters achieve the best performance. The high switching frequency of the inductor-based converter (160MHz, see Table 4) required to maintain low current ripple, decreases the efficiency at high R_{ld} values. At higher power density, the resonant-based converter is superior to other topologies, due to quite a high LC quality factor and lower switching frequencies. The inductor-based converter dominates the capacitor topology at the highest power density. The higher energy density of the capacitor compared to the inductor (10 times here) does not directly lead to higher efficiency. At those three points, the capacitor-based converter works in SSL [6].

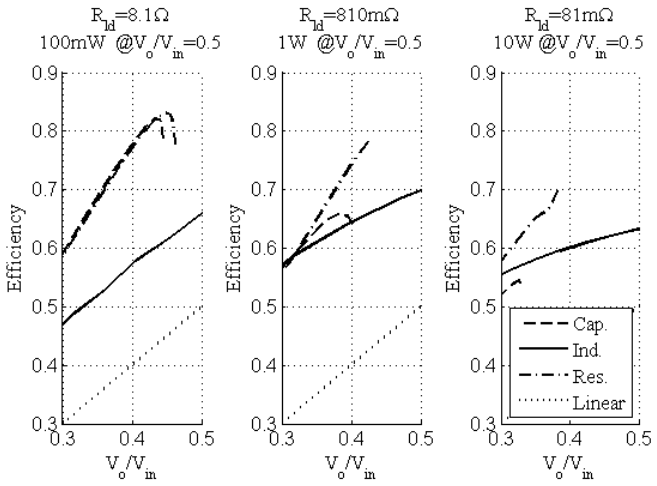

Fig. 6. Transistor level simulation results: efficiency of the nine converters v. transfer ratio for three nominal loads, for 1mm² passive areas.

Nonetheless, the switch voltage stress could be a key issue at high input voltage in inductive and resonant-based converters if thin oxide transistors were used. In fact, in those topologies, voltages up to $V_{in} + V_f$ (where V_f is the threshold voltage of a body diode) are applied to transistors, while it does not exceed $V_{in} - V_o$ in a capacitive-based converter, in steady-state.

It is also important to highlight that the results could vary at other technology nodes or with additional options (high capacitance density or low resistivity metal layer) or using numerous design refinements (interleave, multiple ratio, variable sizing, multiple inputs) or using 3D integration.

Finally, this paper underlines the superior efficiency of the resonant topology compared to the capacitor one mainly because the charge-sharing loss is avoided.

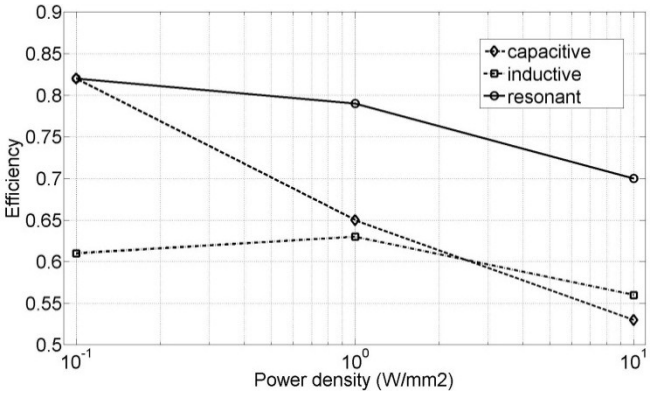

Fig. 7. Peak efficiency of the three topologies under test vs power density.

VI. Conclusion

This paper provides a technology independent method and a practical use case to compare three particular, but well-spread, DC-DC converter topologies for chip-scale power management. The compact analytical equations of the power losses based on a few CMOS technology parameters are given for three hard-switching converter topologies (capacitive-, inductive- and resonant-based). Derived from these technology independent models, the loss mechanism analysis reviews the loss distribution between the conduction, switching and energy transfer losses and the energy requirement in the intermediate storage element. This method could help the system-level designer to select the passive nature of the converter, predict the achievable efficiency in hard-switching conditions, validate a CMOS technology choice, or compare some technologies. As only three particular topologies are studied here, the circuit-level designer has to find the best design refinement e.g. interleave or coupled passives in the family converter and technology node chosen by the system-level designer.

To derive the proposed method, a common standard 65nm CMOS technology has been chosen to fully integrate the active and passive elements of the converters. Based on the analytical derivations, the three monolithic topologies under study were then designed and optimized over three decades of power delivery on a 1mm^2 passive die area with a focus on the ½ conversion ratio. Refined using transistor-level simulations, the study confirmed that the capacitor-based converter is a good candidate to provide efficient on-die step-down power up to 1W/mm^2, corresponding to one decade less than the industrial target for an on-chip digital core supply [9]. Above this power density, other topologies appeared more appropriate, especially the resonant-based converter, mainly due to the best passive energy utilization. This promising topology provides more lossless energy transfer than the others, but further research has to study its lossless controllability and its active and passive component stress management related to low voltage CMOS technology.

VII. Annexes

A. Assumptions

This paper focuses on a non-isolated DC-DC converter fully

integrated in CMOS technology (active and passive parts). For process compatibility, only air-core inductors are considered here. All intermediate energy storage includes an equivalent series resistor and a bottom plate capacitor. The output is ideally bypassed to model the output as an ideal voltage source and simplify the analytical expression. The resonant frequency of the inductive part is assumed to be at least 10 times higher than the switching frequency (verified using a specific tool). For the optimization, we assume that the predominant area is consumed by passives. The areas given in Section V include the passive elements for energy transfer, but not the bypass capacitor C_{tank}. The comparison is made without design refinement (no soft-switching, interleave, or DCM) or feedback control to maintain a fair comparison between the power stages of "basic" power transfer topologies.

B. Λ_i parameters

For each topology, the losses have been divided into the switching loss P_{sw} mainly due to the input capacitance of the power transistors, the conduction loss P_{cond} due to the load current into the on-state resistance of the power transistors, and the transfer loss P_{trans} caused by the energy transfer mechanism itself. f_{sw} is the switching frequency. W_i is the width and $R_{ds_{on}}(M_i)$ is the on-state resistance of the transistor M_i. Moreover, for each transistor M_i, we define coefficient $\Lambda_i = W_i \cdot R_{ds_{on}}(M_i)$ which characterizes the polarity and gate drive level of each transistor. In fact, in some cases (cf. section III) the actual driving voltage V_{gs} is not the same for all transistors. Moreover, a P-MOSFET is more resistive than the N-MOSFET of the same geometry. Those parameters are accounted for in parameter Λ_i, which can also be expressed as:

$$\Lambda_i = \lambda_{R_i} \frac{V_{gs_0} - V_T}{V_{gs_i} - V_T} \text{ or } R_{ds_{on}}(M_i) = \frac{\Lambda_i}{W_i} \qquad (18)$$

where λ_{R_i} is the resistivity of the transistor M_i driven by V_{gs_0}, V_T is the threshold voltage and V_{gs_i} is the actual driving voltage. It must be emphasized that Λ_i is not a free parameter to be chosen by the designer but constrained by the design. Λ_i might be seen as an effective channel resistance.

C. Unified constant expressions

The unified constant expressions are given in Table 5.

TABLE V
EXPRESSION OF THE TECHNOLOGY AND CONVERTER-SPECIFICATION RELATED CONSTANTS

A	$\lambda_{C_{in}} V_{in}^2$	E	$\left(4C_{fly}R_{cap}(S)\right)^{-1}$	J	$\frac{V_o^2}{R_{ld}^2\, FoM_L(S)}$
B	$\frac{1}{2}\frac{V_o^2}{R_{ld}^2}$	F	$\frac{V_{out}^2}{R_{ld}^2} D_c \Lambda_1$	K	$\frac{\pi^2}{8}\frac{V_o^2}{R_{ld}^2} R_{cap}(S)$
C	$\frac{V_o^2}{R_{ld}^2} R_{cap}(S)$	G	$\frac{1-D_c}{D_c}\frac{\Lambda_2}{\Lambda_1}$	N	$\left(4\pi^2\, \lambda_C S\, R_{cap}(S)\, FoM_L\right)^{-1}$
D	$\frac{k_{bot}\, C_{fly}\, R_{ld}^2}{R_{cap}(S)}$	H	$\frac{R_{ld}^2 D_c^2}{12}\left(\frac{V_{in}-V_o}{V_o}\right)^2$	Q	$k_{bot} V_o^2 \lambda_C S$

Note: S designates the die surface dedicated to the integration of C_{fly} or L or L_{res} & C_{res}.

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Y. Pascal was born in Vannes, France, in 1991. He received his MSc. in electronics from the École polytechnique, Université Paris-Saclay, France, in 2014 and is currently a student in power electronics at the Royal Institute of Technology (KTH), Stockholm, Sweden.

His research interests include the design of DC-DC converters.

G. Pillonnet (S'05-M'07) was born in Lyon, France, in 1981. He received his master's degree in Electronic Engineering from CPE Lyon, France, in 2004 and a PhD from INSA Lyon in 2007.

Following an early experience as an analog designer in STMicroelectronics in 2008, he joined the University of Lyon in the Electronic Engineering department. During the 2011-12 academic year, he held a visiting researcher position at the University of California, Berkeley, USA. Since 2013, he has worked as a researcher at the CEA-LETI, a major French research institution.

His research focuses on integrated power converters and actuators including modeling, circuit design and control techniques. He has published about 50 papers in these areas, especially in loudspeaker drivers.