Investigation of the power-clock network impact on adiabatic logic

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***Abstract*— Adiabatic logic is architecture design style which seems to be a good candidate to reduce the power consumption of digital cores. One key difference is that the power supply is also the clock signal. A lot of work on different adiabatic logic families has been done but the impact of the power supply and the power-clock network still remains to be studied. In this paper, we investigate the power-clock network effect on adiabatic energy dissipation. We derive closed-form analytical formulas to represent the output signal voltage and energy dissipation while taking into account the parasitic impedance of the power-clock network with respect to switching frequency such that adiabatic conditions are still met. Experiments, based on simulation, show that the power-clock network impacts both the energy efficiency of the circuit and its frequency.**

Keywords—Adiabatic Logic, Power-Clock Distribution Network, Power Efficiency

I. INTRODUCTION

The power consumption in electronics system is one of the main concerns both in embedded systems and high performance computing. There are many research and industrial efforts that look into methods for reducing power consumption. They can mainly be categorized into three main axes: novel technologies and devices, circuit- and system-level design and new architecture design style.

Adiabatic logic is a different design style to build a digital circuit in order to reduce power dissipation. Although the principle is known for decades [1-5], CMOS-based adiabatic logic suffers non-negligible leakage power dissipation due to MOSFET devices. These devices introduce non-adiabatic losses which detriment overall energy efficiency of adiabatic logic. Additionally, frequency achieved in adiabatic circuits is far lower than in conventional CMOS logic [6,7].

Aggressive scaling of bulk MOSFETs have also introduced effects such as short channel effects and increased leakage currents. Current advancements in integration technology and novel devices have brought again interest on adiabatic logic. Novel devices such as nano-electro-mechanical switches (NEMS), carbo nanotube based field effect transistors (CNTFETs) or vertical slit field effect transistors (VESFETs) are potential replacements of MOSFETS to further reduce non-adiabatic energy dissipation and achieve higher switching frequencies [7,8]. Thanks to these novel switches, the adiabatic logic may be a promising alternative for ultra-low power circuit design.

Adiabatic logic can be supplied by both inductive and capacitive power supply. The energy efficiency is dependent of the efficiency of the power-clock supply. We can rely on several studies which has shown its impact on the conventional logic [9].

Similarly, power delivery networks have also been a lot studied due to its impact on the energy efficiency [10]. As the power-clock networks deliver both the supply and the clock signal, they even play a more important role on the adiabatic energy efficiency. Parasitic impedance of power-clock networks can hamper the overall energy efficiency and also it may prompt to lowering switching frequency such that the logic functions in adiabatic conditions. It is the objective of this paper to show the impact of the network parasitic resistance and derive analytical formulas to quantify its effect on energy efficiency. The rest of this paper is organized as follows: in section II, we introduce adiabatic logic. In section III, we describe the models utilized on this work. Then, in section IV, we present our analysis for computing energy dissipation. Section V concludes this paper.

II. INTRODUCTION OF ADIABATIC LOGIC

In this section, we will introduce the concepts to understand how the adiabatic logic works.

A. Adiabatic Charging

The adiabatic logic is based on the optimal way to charge a capacitor: using a voltage ramp [11]. When a logic gate is active, it can be described as the equivalent resistor, R_{GATE}, between the output and the supply input which is charging the equivalent load capacitor of the next gate, C. Thus, the energy lost during the charge is:

$$E_{CHARGE} = \int_0^T R_{GATE} i(t)^2 dt \quad (1)$$

where T is the ramp time of the power-clock supply voltage V_Φ.

To maintain the adiabatic conditions, the capacitor voltage should be equal to the supply voltage, hence $T >> R_{GATE}C$. Thus, the stored charge is $Q(t)=CV_\Phi(t)$. The flowing current is constant in the adiabatic conditions, so it can be write as $i(t)=I=\Delta Q/\Delta T$ and the dissipated energy for charging C is as:

$$E_{CHARGE} = \frac{R_{GATE}C}{T} CV_{DD}^2 \quad (2)$$

where V_{DD} is the maximum value of V_Φ.

It can be easily shown that the same energy loss occurs to discharge the capacitor. Then, the total adiabatic energy loss is as:

$$E = 2\frac{R_{GATE}C}{T}CV_{DD}^2 \quad (3)$$

B. Adiabatic Logic Gate

The structure of an adiabatic gate differs from the conventional gates. Any adiabatic gate delivers the result of the function and its inverse as illustrated in Fig.1a.

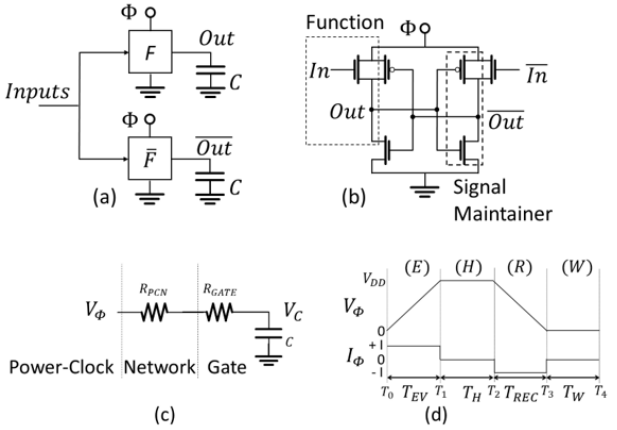

Fig. 1: (a) Adiabatic Logic Gate, (b) PFAL buffer, (c) RC modeling of one gate and power clock network, (d) Voltage and current of the power clock signal

Besides, there are additional transistors required to create the inverse and maintain the signal, e.g. the positive feedback adiabatic logic, PFAL buffer shown in Fig.1b. PFAL logic is one of the commonly logic use due to its high energy savings. However, the adiabatic logic has a lot of families differentiated by presence of the inverse function, number of clock phases and how the gates are connected.

The other difference is the number of signal needed to drive an adiabatic circuit. For conventional logic, there are the supply voltage, ground, and a clock signal while for most of adiabatic logic families, there is a need of four 4-phase power-clock signals and ground.

C. Adiabatic Logic Functioning

In order to define a circuit as an adiabatic circuit, it has to satisfy two conditions: 1) the switches have to stay ON when the current is flowing and 2) current has to remain constant, i.e. the ramp time has to be long enough. This leads to the condition $T >> R_{GATE}C$.

Another property of the adiabatic logic is that the activity factor is always one. Indeed, as the gate delivers both the result of the function and its inverse, the gate is always on.

Adiabatic logic power-clock signal has four phases: evaluation (E), hold (H), recovery (R) and waiting (W). The power clock signal is shown in Fig.1d. During the evaluation time, the power clock voltage ramps up from 0 to V_{DD}. Then, in the hold phase, the power clock is maintained at V_{DD}. In the recovery phase, the power clock voltage ramps down to 0. Finally, the power clock remains at 0 during the waiting phase which is required to ensure a symmetrical signal.

If the result of the function is the logic state '1', then the capacitor voltage will follow V_Φ, otherwise it will remain at zero.

III. Energy Efficiency Modeling

A. Modeling of the Energy Loss Considering Parasitics of Power-Clock Network

Power-clock network (PCN) can be designed in a tree, mesh or hybrid mesh-tree type topology. PCN interconnects can be represented by their parasitic inductance, capacitance and resistance with respect to their geometries. In this work, we take into account their parasitic resistance only as the capacitive and inductive effect can be ignored for a first order model. Thus the total resistance of the charging capacitor is as:

$$R = R_{GATE} + R_{PCN} \quad (4)$$

where R_{PCN} is the PCN parasitic resistance. The complete model is presented in Fig.1c. Including the total resistance R, the energy dissipated by the charging and the discharging of a single gate is as:

$$E_{ALPCN} = 2\frac{RC}{T}CV_{DD}^2 \quad (5)$$

(5) is valid as long as the adiabatic condition $T >> RC$ is met. Otherwise, it will lead to non-adiabatic losses which lower the energy saving.

B. Voltage and Energy Loss Equations

This section describes the capacitor voltage and the energy consumed by an adiabatic logic gate regardless at the ramp time. The capacitor voltage follows the first order differential equation:

$$RC\frac{dV_C(t)}{dt} + V_C(t) = V_\Phi(t) \quad (6)$$

1) Evaluation Phase

During the evaluation phase, V_Φ is ramping up to reach V_{DD} at time by T_1. Using (6) and $V_C(T_0) = 0$, V_C is defined as:

$$V_C(t) = \underbrace{\frac{t-T_0}{T_{EV}}V_{DD}}_{V_\Phi(t)} + \frac{RC}{T_{EV}}V_{DD}\left(e^{-\frac{t-T_0}{RC}} - 1\right),\ T_0 \le t \le T_1 \quad (7)$$

where T_{EV} is the duration of the evaluation (shown in Fig.1d). Then, the energy loss during the evaluation time, calculated between T_0 and T_1, is as:

$$E_{EV} = \frac{RC}{T_{EV}}CV_{DD}^2 - \frac{3}{2}\left(\frac{RC}{T_{EV}}\right)^2 CV_{DD}^2 + \left(\frac{RC}{T_{EV}}\right)^2 CV_{DD}^2 e^{\frac{-T_{EV}}{RC}}\left(2 - \frac{1}{2}e^{\frac{-T_{EV}}{RC}}\right) \quad (8)$$

If T_{EV} is not long enough, V_C cannot reach V_{DD}. So we have introduced V_{EVF} which is V_C voltage level at time T_1:

$$V_{EVF} = V_C(T_1) = V_{DD} - \frac{RC}{T_{EV}}V_{DD}\left(1 - e^{-\frac{T_{EV}}{RC}}\right) \quad (9)$$

2) Hold Phase

The hold phase occurs between T_1 and T_2. If the circuit is not in an adiabatic condition, the capacitor will charge while V_Φ will stay at V_{DD}. Thus, using (6) and $V_C(T_1) = V_{EVF}$, V_C is as:

$$V_C(t) = \underbrace{V_{DD}}_{V_\Phi(t)} - (V_{DD} - V_{EVF})e^{-\frac{t-T_1}{RC}}, \quad T_1 \le t \le T_2 \quad (10)$$

Then, the energy loss during the hold phase, E_H is as:

$$E_H = \frac{1}{2}CV_{DD}(V_{DD} - V_{EVF})(1 - e^{\frac{-2T_H}{RC}}) \quad (11)$$

where T_H is the duration of the hold phase. In the worst case, capacitor is not fully charged after the hold phase, we introduce V_{HF} representing the capacitor voltage at T_2:

$$V_{HF} = V_{DD} - (V_{DD} - V_{EVF})e^{\frac{-T_H}{RC}} \quad (12)$$

3) Recovery Phase

The recovery occurs between T_2 and T_3. During the recovery phase, the power supply voltage ramps down. Using (6) and $V_C(T_2) = V_{HF}$, V_C is determined as:

$$V_C(t) = \underbrace{\frac{T_3 - t}{T_{REC}}V_{DD}}_{V_\Phi(t)} + \frac{RC}{T_{REC}}V_{DD}\left(1 - e^{-\frac{t-T_2}{RC}}\right) - (V_{DD} - V_{HF})e^{-\frac{t-T_2}{RC}}, \; T_2 \le t \le T_3 \quad (13)$$

where T_{REC} is the duration of the recovery phase. It leads to consumed energy E_{REC}:

$$E_{REC} = k_1\frac{RC}{T_{REC}}CV_{DD}^2 + k_2\frac{RC}{T_{REC}}CV_{DD}(V_{DD} - V_{HF}) + k_3\frac{1}{2}C(V_{DD} - V_{HF})^2 \quad (14)$$

where $k_1 = 1 - \frac{3}{2}\frac{RC}{T_{REC}} + \frac{RC}{T_{REC}}e^{\frac{-T_{REC}}{RC}}\left(2 - \frac{1}{2}e^{\frac{-T_{REC}}{RC}}\right)$

$$k_2 = (1 - e^{\frac{-T_{REC}}{RC}}(2 - e^{\frac{-T_{REC}}{RC}}))$$

$$k_3 = (1 - e^{\frac{-2T_{REC}}{RC}})$$

As the capacitor might not be fully discharged when the recovery phase is over, we introduce V_{RECF} as the capacitor voltage at T_3.

$$V_{RECF} = \frac{RC}{T_{REC}}V_{DD}\left(1 - e^{\frac{-T_{REC}}{RC}}\right) - (V_{DD} - V_{HF})e^{\frac{-T_{REC}}{RC}} \quad (15)$$

4) Waiting Phase

The waiting phase occurs between T_3 and T_4. Finally, the capacitor is fully discharged during the waiting time. Using (6) and $V_C(T_3) = V_{RECF}$, V_C is determined as:

$$V_C(t) = V_{RECF}e^{-\frac{t-T_3}{RC}}, \qquad T_3 \le t \le T_4 \quad (16)$$

The difference between the others phases is that the final capacitor voltage is zero due to the reset which is mandatory in order to insure the logic function of the gate. Thus, E_W, the energy loss during the waiting phase is as:

$$E_W = \frac{1}{2}CV_{RECF}^2 \quad (17)$$

The dissipated energy for one clock cycle, E_{TOT}, is given by:

$$E_{TOT} = E_{EV} + E_H + E_{REC} + E_W \quad (18)$$

5) Model Validation

The model is developed in MATLAB and has been validated by comparing it to HSPICE simulations. In Fig.2, the model capacitor voltage is compared to the HSPICE capacitor voltage for a ramp time of $10^4 \times R_{GATE}C$ and a R_{PCN} of $0.1 \times R_{GATE}$ with R_{GATE}=10kΩ, C=1fF and V_{DD}=1V. These parameters' values have been taken randomly in order to validate the model regardless the adiabatic conditions.

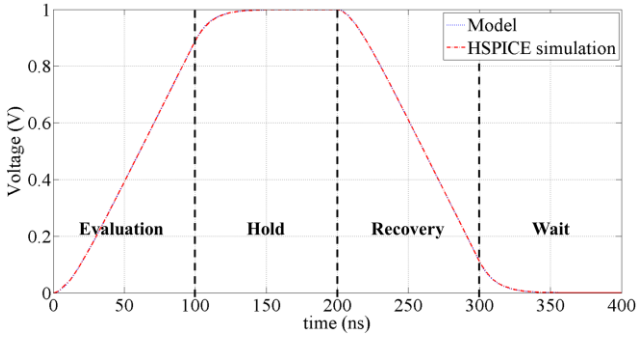

Fig.2: analytical equation resolution vs electrical simulation for the capacitor voltage

IV. PCN Impact on the Energy Efficiency

In this section, we derive the impact of PCN on energy efficiency for a single adiabatic logic gate. We use clock period parameters as $T = T_{EV} = T_H = T_{REC} = T_W$ in order to represent the clock properties of the most of the adiabatic logic families, V_{DD}=1V, R_{GATE}=10kΩ and C=1fF; to represent a gate model in 45nm-CMOS technology.

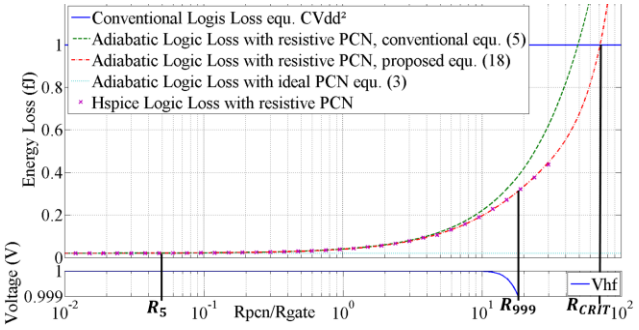

Fig. 3: Energy loss and V_{HF} against the total PCN resistance

In Fig.3, the energies calculated from different expressions are shown against the total PCN resistance for a ramp time of $100 \times R_{GATE}C$ i.e. T=10ns which is a usual value for adiabatic logic designs. For a given T, we introduce three boundaries in order to help designers to find the optimal resistance considering their constraints.

With R_5 as the maximum resistance, the total energy loss is 5% higher than the energy dissipated without power-clock network i.e. the expression defined in (3). Designers can change this constraint to operate at a higher frequency or to save more energy.

With R_{999} as the maximum PCN resistance, we impose a constraint on V_{HF} in order to have the load capacitor fully charged. As R_{999} is 19 times higher than R_{GATE}, this value is never reach in practice. It means the output will always be at V_{DD} during the hold phase which ensure the working of the adiabatic circuit.

With R_{CRIT} as the maximum resistance, the circuit will dissipate the same energy than using the conventional logic which means there is no point to use the adiabatic logic. The conventional logic energy loss is actually lowered by the activity factor of the circuit whereas the adiabatic logic energy loss is not. This is why designers have to pay a particular attention to the activity factor of the circuit in order to ensure that the circuit dissipate less energy than with conventional logic.

Regardless the chosen maximum resistance between these constraints, E_{TOT} defined in (18) is lower than E_{ALPCN} defined in (5) because the negative term $\left(\frac{RC}{T}\right)^2$ in (9) and (14) is predominant. It means E_{ALPCN} can be used as a worst estimation of the total energy loss. Using E_{ALPCN}, we directly derive an expression coupling the maximum tolerated PCN resistance, R_{PCNT}, R_{GATE}, and the maximum tolerated increase of the energy loss, A_{PCN}: $R_{PCNT} = A_{PCN}R_{GATE}$. A_{PCN} is linked to the constraint on the resistance, e.g. if designers choose R_5, A_{PCN} will be 0.05.

Despite the power mesh optimization to reduce the PCN, the maximum PCN resistance can be higher than R_{PCNT} given by the previous paragraph. In order to compensate a highest PCN resistance, the ramping time has to be increased. Using (5), we introduce the minimum needed ramping time, T_{MIN} which is defined as follow:

$$T_{MIN} = \frac{1}{1+A_{PCN}}\left(1 + \frac{R_{PCNM}}{R_{GATE}}\right)T \quad (19)$$

Once T_{MIN} is determined, the energy dissipated by one gate, E_{GATE} is as:

$$E_{GATE} = \frac{T}{T'}\left(1 + \frac{R_{PCN}}{R_{GATE}}\right)E \quad (20)$$

where T' is the maximum between T_{MIN} and T, R_{PCN} is the resistance of the PCN for this gate and E is the energy loss for one gate defined in (3).

This model validates the use of expression (5) as the total energy loss. (5) allows a quantitative answer on the tolerated parasitic resistance of the PCN without disrupting adiabatic conditions and gives the minimum ramping time in order to meet the adiabatic conditions for a given PCN resistance.

V. Conclusion

In this paper, we investigate the impact of the power-clock network on the energy efficiency of an adiabatic circuit. We present analytical models for computing the dissipated energy in order to determine the maximum resistance of Power-Clock Network (PCN) for a given frequency such that adiabatic conditions are met. This model gives the energy loss no matter i.e. the model is valid whatever the PCN resistance is. Based on mathematical simulations, we fix a constraint on the maximum PCN resistance in order to quantify the impact of the PCN on the energy loss. As the commonly used energy adiabatic logic loss (5) is always a worst estimation of the energy loss derived from the model (18), (5) can be used to directly derive the maximum tolerated PCN resistance and its minimum ramping time. Then, the overall impact of the power-clock network is the ratio between the sum of the gate resistance and the PCN resistance, and the gate resistance times the ratio between the targeted frequency and the actual switching frequency. In order to enhance the model, PCN parasitic and decoupling capacitors can be added in order to quantify their impact on the energy efficiency of the circuit.

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