FPGA based multi-channel TDC development*

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The FPGA based multi-channel TDC technology has been used by many detector prototypes and experiments in the past years and will continue to be used for further detector tests and data digitisation[1]. The TDC design has been implemented on many electronic boards (TRB3, TAMEX, CBMToF, etc.) and the success of the technology has opened gates for additional implementations (DiRich for CBM), which drives new features and specifications. In this paper two of these new features - double edge measurement in a single channel and new readout scheme for zero data loss - will be discussed.

Pulse width measurements are of special interest in many of the charge measurement (after encoding the pulse charge to a digital pulse width) and Time-Over-Threshold (ToT) measurement applications. In almost all of the FPGA-based TDC applications the pulse width is measured by using two of the channels for leading and trailing edge time measurements separately, which doesn't induce any extra dead time but requires double the number of channels. In the new version of the TDC the leading and trailing edges of a digital pulse is measured by a single TDC channel.

In order to measure both of the edges in a single channel, the trailing edge of the input pulse has to be delayed longer than the dead time of the TDC channel ($20\ ns$). This delay is achieved by stretching the pulse asynchronously in the FPGA by using the routing interconnections between the logic elements. After the successful measurement of the leading edge time, the delayed trailing edge is directed back to the channel in order to measure the trailing edge time. The type of the measured edge is marked in the data with a single bit.

The calculated time difference between the leading and the trailing edges - pulse width - contains a channel offset caused by the delay circuit, which needs to be calculated and subtracted from the result to find the real pulse width value. This value is different for each channel. This offset can be calculated by applying an external pulse to the TDC inputs with a fixed width and subtracting this fixed value from the measured width. As this is generally not possible in experimental setups, a pulse with a fixed width of $50\ ns$ is generated by the internal oscillator of the FPGA and is sent to each channel. The same generated pulse is also used to calibrate the channels. In Figure 1 on the right, the pulse width measurement of a $2\ ns$ pulse on a channel with an offset of $\sim 28\ ns$ is shown. On the left the leading edge measurement between two channels in the same TDC is depicted. As seen, the leading edge time and the pulse width can be measured with precisions as low as $9\ ps$ and $12\ ps$ respectively.

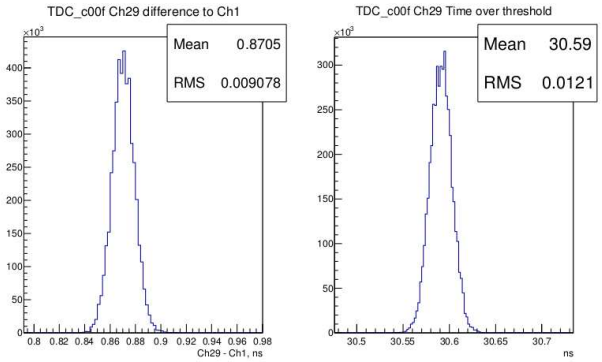

Figure 1: Leading edge (left) and pulse width (right) measurements of a pulse are done with the designed TDC.

The readout algorithm of the old TDC design was suitable only for triggered applications, as some of the hits after the trigger window could be lost during the readout of the data from the channel ring buffers. In order to adapt the TDC to trigger-less applications (such as PANDA) the readout scheme was changed.

In the new TDC a double buffer stage for each TDC channel is introduced. The first stage buffers, which are set as ring buffers, collect data as normal either until the end of the trigger window (in triggered applications) or the readout start signal from the system (in trigger-less applications). At this point the ring buffers are flushed directly to the second stage buffers, which are set as FIFOs. After flushing the first few words, the serialisation of the data from the second stage buffers begins. Any hit signal that might come during this process is saved in the relative ring buffer until the next trigger or readout start signal, hence no data is lost during the readout process.

The TDC development implemented in several electronic boards (TRB3, TAMEX, CBMToF, etc.) has been continued during the past year, introducing new abilities and features for better performance. These enhancements are being successfully tested in the laboratory as well as under beam conditions.

References

[1] C. Ugur et.al, "GSI Scientific Report 2013", p.89.

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