Bit Error Rate Tester

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For electronic components which transmit digital data the bit error rate is the figure of merit which has to be controlled. Electronics which will be installed in the field of reaction products in future experiments at FAIR has to be radiation hard. At present, selected electronic parts undergo exhaustive tests with use of intense minimum ionising particles' beams, mostly 3 GeV protons at Jülich synchrotron facility. To monitor data transmitting components during irradiation a Bit Error Rate Tester (BERT) has been developed.

BERT requirements

Randomly generated bit patterns are sent to the tested device and compared to the transmitted back bit series. In order to avoid spurious errors due to e.g. bit flips in the source or the receiver of the test data by ionising particles both of them have to be placed far away from the device under test. Moreover, the generated bit patterns have to be representative for the data to be collected in real high energy experiment and transmitted in a form of future data transmission (8bit/10bit and 64b/66b line coding). Transmission lines based on copper wires as well as on glass fibers as different carriers have to be tested with transmission frequency as high as planned for coming experiments. Block diagram of the Bit Error Rate Tester is presented in Fig.1. In the following some details of the construction of the bit pattern tester and its performance is described.

BERT construction

Figure 1: Simplified block diagram of GTP Transceiver

A standard PC as host (powering, programming environment) for the Spartan6 FPGA based card with GTP transceiver is used (Fig.2). Serial input and output of the card is using differential signalling via SFP interface or plane interface for transmission on copper line. Various parameter such as driver swing, TX pre-emphasis or receiver equalization might be adjusted to adapt this device to different standards. A random bit sequence generator implemented in the FPGA delivers patterns $2^7 - 1$ or $2^{31} - 1$ bit long according to polynomials $x^7 + x^6 + 1$ (PRBS7) and $x^{31} + x^{28} + 1$ (PRBS31) [1]. On receiver side incoming bits are stored into history shifting buffer and they are used to compute further expected incoming bits using the same PRBS algorithms.
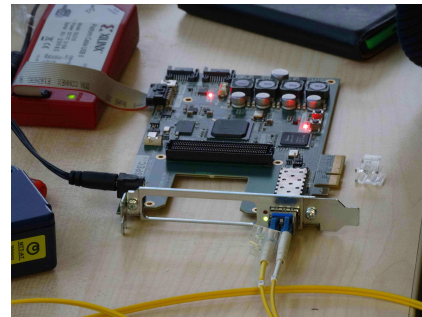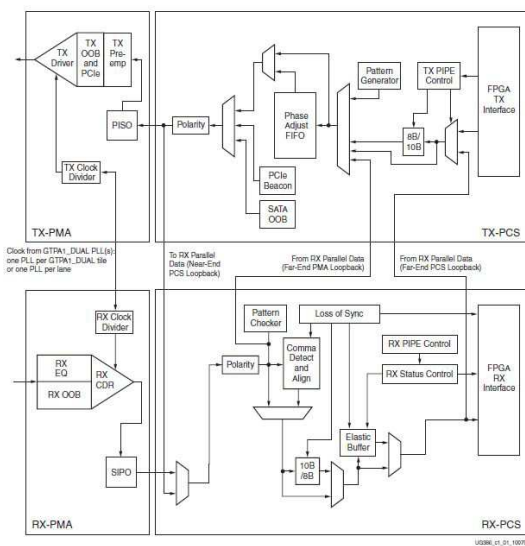

Figure 2: PC card with FPGA and I/Os.

BERT test results

An error-counter is incremented in case of discrepancy between sent and received patterns and monitoring software can display - apart of the test conditions - the error rate corresponding to certain transmission speed. Two lengths of transmission medium have been used (400 and 1000 m lines of glass fiber) for bit patterns generated with PRBS 31-bit with differential output swing of 200 mV and transmission speed of 2.5 Gbps In this particular configuration bit error rate was $1.42 * 10^{-14}$ after almost 8 hours of run. Transmission line has been disturbed mechanically to test proper detection of the transmission errors what resulted immediately in drastically increase of the bit error rate.

References

[1] http://www.xilinx.com/support/documentation/user_guides/ug386.pdf