A Front-end electronics test board for the CBM Silicon Tracking System*

V.Kleipa[1], *C. Simons*[1], *D. Soyk*[1], *C.J. Schmidt*[1], *J. Carpenter*[1], *the CBM collaboration*[1], *and the FAIR@GSI RBDL*[1]

[1]GSI, Darmstadt, Germany

The 896 modules of the CBM Silicon Tracking System will be equipped with two front-end electronics boards (FEBs) each, carrying per board eight STS-XYTER ASICs that read out the silicon micro-strip sensors of the modules [1]. The boards will be stacked at the top and bottom layers of the detector, mounted in a shelf structure that is in contact with a cooling plate to remove the power dissipated by the electronics. Due to the spatial contstraints there, the board dimensions are restricted to the limited size, as shown in Fig. 1. At the same time, the board has to provide the infrastructure for achieving the full output band width needed to read out the detector. This translates to realizing up to 5 LVDS pairs per final ASIC, a high-density challenge for the FEB design and prototyping.

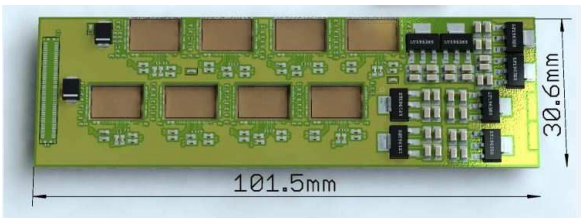


Figure 1: Rendering of the STS front-end electronics board comprising 8 STS-XYTER ASICs arranged in a fixed pattern on two double-rows of 4 ASICs each. Power supply section with LDOs on the right. The small components are decoupling capacitors to common and communication ground.

For assembly test purposes, a PCB was produced onto which 8 STS-XYTERv1 ASICs can be mounted but not having any electrical functionality. Only the top and bottom layers are covered with a gold layer for test bonding of ASICs and cables. During its layout, it turned out that only one of the four readout channels of each ASIC could be routed to the digital I/O connector, limited due to the available space in between the ASICs. This technological problem is the subject of current work.

In order to prepare a test equipment for a complete readout chain from sensor to GBTx boards, an intermediate FEB board has been designed that is not constrained to the small dimensions. The PCB, called FEB4, hosts only four ASICs. Its layout is shown in Fig. 2. This PCB comprises the required power supply LDOs. All I/O channels of each ASIC are linked to a connector. In addition, the required high-voltage capacitors (rated 250 V) for bias decoupling have been added to the differential LVDS connections. In Fig. 3(a) the board's assembly pads for passive devices are visible. For the devices' case size, the norm *0201[m]* had to be chosen in order to fit them between the ASICs. This board is currently being used for testing of the STS-XYTERv1 chips. One ASIC wire-bonded to the board is shown in Fig. 3(b).

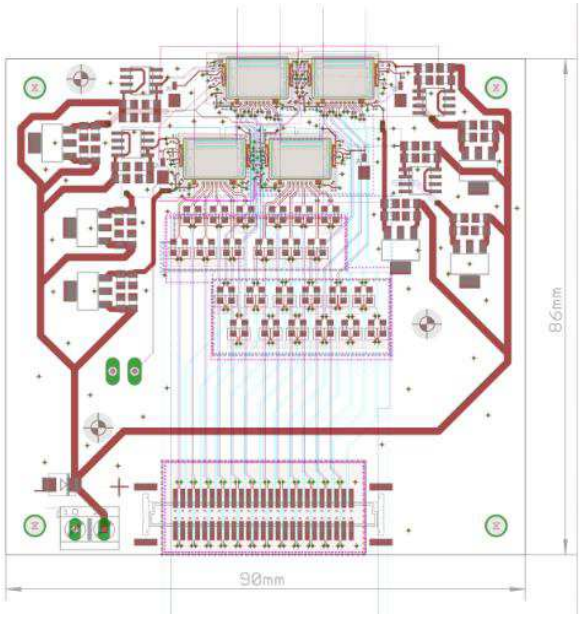
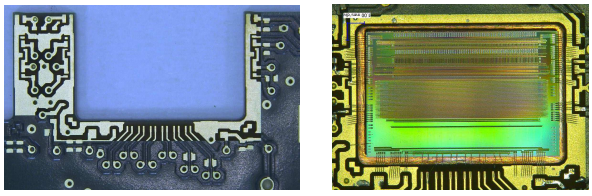


Figure 2: Layout of a front-end board comprising four read-out ASICs and all outgoing LVDS data lines on a somewhat relaxed geometrical footprint (FEB4).



(a) (b)

Figure 3: (a) High-density region in between the openings for the STS-XYTER ASICs on FEB4, filled with the full set of LVDS lines, micro-vias and connecting pads for high-voltage decoupling capacitors. (b) STS-XYTERv1 ASIC installed into FEB4 and wire-bonded to its power supply, control and outgoing data lines.

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References

[1] V. Kleipa et al., CBM Progress Report 2013 (2014), p. 36