# Towards the STSXYTERv2, a silicon strip detector readout chip for the STS

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STS-XYTER as a 128+2 channel full-size prototype IC dedicated for silicon strip detector readout for the STS was fabricated in 2013 [1]. Fig. 1. presents the test PCB developed at AGH used for functional verification. It provides on-board 5 separate power domains with dedicated low-noise LDO regulators, ERNI connector for sensor attachment, interconnects for test interface, test points and AC-coupled CBMnet interface (HDMI connector). The board is controlled by SysCore V3 (CBMnet) and NI FPGA (test interface) cards.

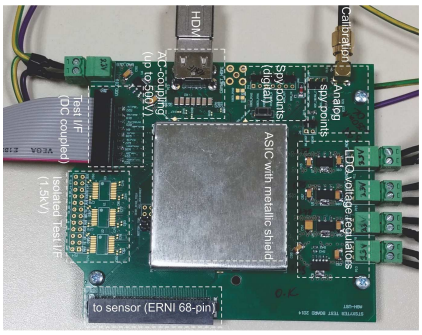


Figure 1: Test PCB for the STSXYTER ASIC.

The architecture details of the chip and test results were presented and published in [2]. Detailed tests using silicon sensors (e.g. CBM05) are currently being prepared. Using the same setup it was possible to further evaluate the chip. Fig. 2. shows the thermal image of the STS-XYTER chip on the test PCB. The thermal resistance was estimated to be approx. 52 °C/W, but it needs to be verified on the final FEB board in the environment similar to the final application as well. The temperature coefficients measured for various biasing points of of the ASIC evaluated for ambient temperatures of 7–85 °C are:

ADC_vdiscr_ref = -0.622 mV/°C,
ADC_ibias_corr = -0.312 mV/°C,
BG_iref = +0.154 mV/°C,
ADC_vref_n = -0.366 mV/°C,
ADC_vref_p = +0.286 mV/°C,
DISCR_bias_t = -0.435 mV/°C.

The STSXYTERv2 which will be an evolution of the STSXYTER prototype ASIC among the small fixes the changes include:

- new concept of the digital back-end (focused on the use of GBTx chip as a data concentrator), reaching hit bandwidths 9.4–47 MHit/s/chip,
- definition of the new communication protocol optimized for the conditions and requirements of the CBM experiment. The preliminary protocol was published [3] and is currently a subject of fine-tuning,
- configurable front-end (gain, bandwidth) for possible support of gas detectors (MUCH),
- new pad layout supporting quality test with pogo-probes and reduced connectivity required for regular operation,
- testability and temperature stability improvements of the in-channel ADC,
- further optimization of the analog front-end towards lower noise and better stability.

The STS-XYTERv2 ASIC is currently being under development. It is expected to be taped-out in Q2 of 2015 via Europractice services.

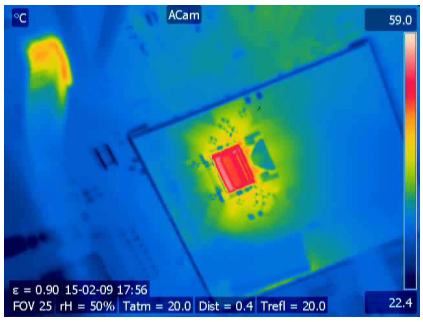


Figure 2: Thermal imaging of the operating ASIC on the test board.

## Acknowledgment

We would like to thank the colleagues from GSI and WUT Warsaw for the efforts towards verification and specification of the new requirements.

## References

[1] P. Grybos *et al.*, "STS-XYTER - a prototype silicon strip detector readout chip for the STS", CBM Progress Report 2012, Darmstadt 2013, p. 17.

[2] K. Kasinski *et al.*, "STS-XYTER, a High Count-Rate Self-Triggering Silicon Strip Detector Readout IC for High Resolution Time and Energy Measurements", IEEE NSS/MIC, 2014.

[3] K. Kasinski, W. Zabolotny, R. Szczygiel, "Interface and protocol development for STS read-out ASIC in the CBM experiment at FAIR", Proc. SPIE 9290, doi: 10.1117/12.2074883.


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