The GBT based readout concept for the CBM Silicon Tracking System

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The sensors of the CBM Silicon Tracking System (STS) are read out by frontend boards (FEB) with 8 STS-XYTER ASICs for 128 channels each implementing the analog frontend, analog-to-digital conversion and the readout of buffered hits via multiple serial links. A subsequent stage with data aggregation from several ASIC links and an electrical-to-optical interface is required before transfering the data to the FPGA based data processing boards (DPBs) located in some distance at the detector site where preprocessing and further data transfer occur. The aggregation stage is located in the cooled STS detector box inside the CBM magnet, which implies that the hardware must fulfill conditions in terms of radiation hardness, magnetic field, space contraints and thermal environment.

GBT Devices

A concept was devised for the STS readout to implement the aggregation and optical readout functionality on a separate readout board (ROB) using the GBTX, SCA and Versatile link devices [1] developed at CERN. The devices of the GBT project are mainly designed as interface between on-detector and off-detector electronics for future LHC experiment upgrades in a radiation environment up to tens of Mrad. The GBTX ASIC implements up to 56 SLVS links (E-Links) as electrical frontend interface with link speeds of 80, 160 or 320 Mb/s and a total bidirectional user bandwidth up to 4.48 Gb/s on the high speed serial link. Latencies of data throughput in the GBTX are fully deterministic. The Versatile Link devices are radiation hard optical transceivers and (twin) transmitters in SFP formfactor modules.

The STS Readout Chain

The ROBs for the STS will contain 1 GBTX device as master connected to an optical transceiver (VTRx), 2 GBTX devices connected to an optical twin transmitter (VTTx) and a GBT-SCA (Slow Control Adapter) device for I^2C based control of the 2 GBTX without optical downlink (see Fig.1). The GBTX uplinks will be operated in the widebus mode (without forward error correction) and therefore provide 3x14 frontend links at 320 Mb/s each. Fourty of these links are used to connect to the FEBs. Three types of FEBs will be used with either 1, 2 or 5 readout E-Links per ASIC depending on the local data load, resulting in a maximum of 5, 2.5 or 1 FEBs of the different types connected to a single ROB. With additional spatial contraints from system integration (no connections across quarter stations, no cable crossings) the total number of ROBs for the STS amounts to approx. 1000, with 3000 optical readout links and 1000 control links. For ASIC timing and control, one single E-Link output and one phase adjustable 160 MHz clock are connected from the master GBTX to each FEB; the control responses use any of the readout uplinks. All E-Links between FEBs and ROBs will be AC-coupled in order to allow the connection of a single ROB to multiple FEBs operated at different potentials together with their connected sensors. The ROBs will be located at the sides of the STS detector box outside the detector acceptance. Flexible flat cables of approximately 0.6 m length will connect the stacks of FEBs for a given quarter station of the detector to the corresponding stack of ROBs.

The version 2 of the STS-XYTER ASIC[2] will implement the GBTX E-Link interface with a configurable number of 1 to 5 readout links and a synchronous readout and control protocol that was specifically developed for the STS-XYTER readout via GBTX [3]. A demonstrator board with a single GBTX and Versatile Link components will be available from CERN for initial tests in early 2015 and a CBM ROB prototype with full functionality is currently being prepared. Larger quantities of the devices from the sole production run are expected end of 2015.

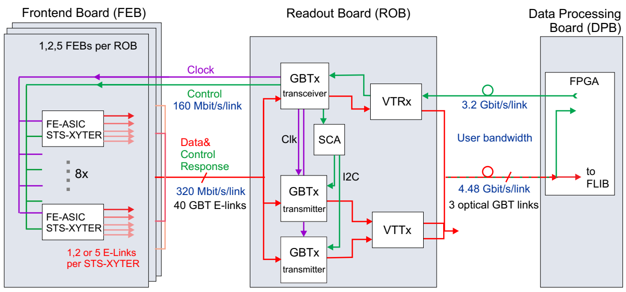

Figure 1: The STS readout chain with the readout board based on GBTX and Versatile Link components.

References

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