CBM FLES input interface developments*

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The First-level Event Selector (FLES) is the central event selection system in the CBM experiment. Its task is to select data for storage based on online analyses including a complete event reconstruction. To do so, the FLES timeslice building has to combine data from all input links to time intervals and distribute them to the compute nodes. To allow for efficient timeslice building, detector data streams are partitioned into microslices prior to combining them. Microslices are specialized containers covering a constant timeframe of real time, which is the same for all subsystems. This allows data agnostic, subsystem independent timeslice building. This partitioning will be done by the Data Processing Boards (DPB) as they are the last stage of the read-out tree which has to contain subsystem specific components.

The FLES input interface is realized by a custom FPGA PCIe card, the FLES Interface Board (FLIB). Its purpose is to provides the optical interface to the DPBs as well as the interface to the FLES input nodes. The current development is based on the commercial HTG-K7-PCIE board form Hitech Global. It features a Xilinx Kintex-7 FPGA, a 8x PCIe 2.0 interface, up to eight 10 GBit/s links and optionally 8 GB of DDR3 memory.

The FPGA design includes the protocol for receiving microslices, a pre-processing engine preparing microslices for timeslice building and a custom full off-load DMA engine. Once configured the DMA engine is capable of constantly transferring microslices and meta data to the PCs memory without involving the host CPU. The only task the CPU needs to perform is to acknowledge processed data segments occasionally to allow reusing buffer space. A measurement of the DMA performance for one to four 10 Gbit/s microslice streams is given in Fig. 1. For up to three steams, data is transmitted at full input speed. For four streams, the input data rate exceeds the available PCIe bandwidth. The achieved maximum data rate is 3345 MB/s, which matches the absolute maximum PCIe data rate for the given configuration.

For demonstration and testing the input interface concept in real live applications, the FLIB and flesnet software have been used for read-out in the CERN-PS 2014 testbeam at T9 beamline. In contrast to the final system, current setups lack the DPB layer and do not support the creation of microslices. A specialized FLIB prototype firmware therefore includes a mockup of the DPB design and is capable of directly receiving CBMNet messages as delivered by the CBM front-end electronics. Simplified microslices

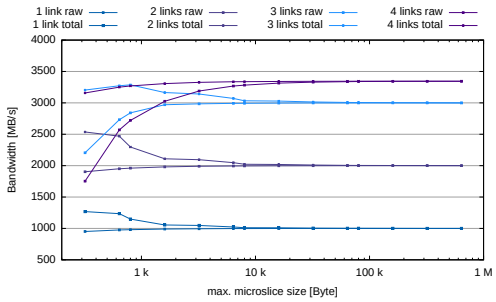

Figure 1: FLIB read-out bandwidth

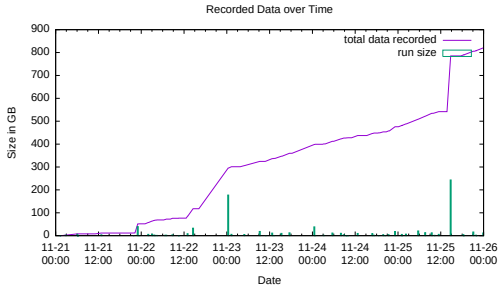

Figure 2: Recorded testbeam data over time

are generated inside the FLIB and subsequently handled in the same way as foreseen for the final setup. Thus the setup is capable of delivering fully build timeslices to any given consumer. In case of the testbeam, timeslices were written to disk and simultaneously published via a ZMQ socket to CBMroot clients for front-end calibration and online monitoring. In addition the firmware and software includes support for front-end configuration and synchronization over CBMnet which is accessible via a ZMQ interface or from within CBMroot.

During the testbeam a single FLIB in conjunction with the flesnet software was successfully used to read-out up to six detector setups in different configurations. Three different flavors of data sources have been employed, Syscore 2, Syscore 3 and TRB boards. Figure 2 shows an overview over five days of data taking. In total 888 GB of data in 84 runs was written to disk without any major read-out related problems. Online performed data consistency checks and first offline analysis did not reveal any issues with the data.

To support future setups including DPBs the FLES interface module is currently under development. It will provide a 10 GBit/s link transferring microslices to the FLIB enabling full featured microslice creation on the DPBs.

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