Towards the Data Processing Boards for CBM experiment[*]

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The Data Processing Boards (DPB)[1] are important part of the CBM readout and detector control systems, providing concentration (possibly combined with local preprocessing) of readout data, before they are sent to the First Level Event Selector (FLES). Additionally DPBs should provide fast and slow control for the Front End Electronics (FEE), distribute the reference clock, and time-critical information, like synchronization and flow control messages from the Timing and Flow Control system (TFC).

To allow testing of different possible implementations of listed functionalities, the versatile prototyping Open Hardware platform - AMC FMC Carrier Kintex (AFCK) [2] was created. The first version of AFCK is shown in figure 1.
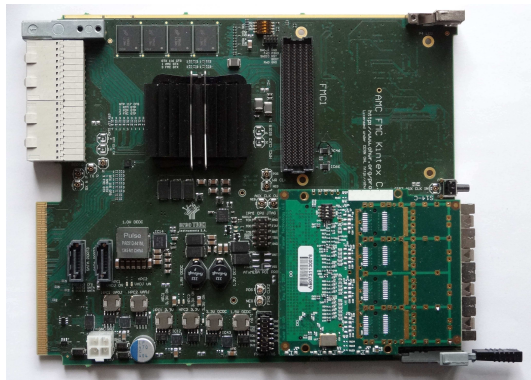

Figure 1: The AFCK board with an FMC card with 4 SFP+ cages connected to the FMC2 connector.

The AFCK board may be used in an MTCA crate or in stand-alone mode. The board is equipped with the XC7K325T FFG900 FPGA, containing 16 high speed GTX transceivers, which can be connected to 2 FMC slots (4 GTXs to each) or to the RTM connector. Another 8 GTXs may be connected to the MTCA backplane ports 0 to 11. This solution allows to test different transceivers mounted on FMC boards, without modifying the AFCK board itself. AFCK is also equipped with flexible clocking system allowing it operate with gigabit links of different speed and also to recover a jitter cleaned clock signal from a high speed receiver. The board is also equipped with 2GB of DDR3 SDRAM which may be used to store the processed data, but also for debugging purposes. Those resources make the AFCK board a suitable platform for development of data concentration and preprocessing algorithms.

First series of AFCK boards was manufactured and functionality tests were performed. High speed communication capabilities were tested with standard IBERT tests provided by Xilinx. Stable 10 Gbps transmission was achieved via GTXs connected to the FMC1 slot, while 5 Gbps transmission was possible via GTXs connected to the FMC2 and RTM (10 Gbps in FMC2 should be achievable in next revision of the board).

A few basic IP core blocks, suitable for use in the prototype DPB firmware were developed or ported and tested. These include the IPbus[3] core allowing to control board via 1 Gbps Ethernet interface and the GBT-FPGA[4] core used to communicate with GBTx ASICs. The Ethernet transmission of readout data at 10 Gbps rate was tested using the FADE IP core and protocol[5]. Stable transmission of 4x10 Gbps data streams was achieved using 4 SFP+ transceivers plugged in FMC board connected to FMC1. Porting of the White Rabbit[6] IP core to the AFCK board is currently in progress.

Results of tests performed with the AFCK board will be used to design the cost optimized version of DPB prototype.

Verification of the STS-XYTER communication protocol developed in collaboration with GSI and AGH [7] was performed in simulations and in hardware, using the KC705 evaluation board. The IPbus accessible controller, allowing to synchronize communication with the model of STS-XYTER (provided by the AGH team) and to control it, was developed and successfully tested. To achieve that, a dedicated environment for hardware-software cosimulation of IPbus connected IP cores was prepared.

Verified blocks used in controller will be used for development of prototype DPB firmware, after porting to the AFCK board.

References

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