Status of CBMnet readout and the prototype ASIC*

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Front-end read-out status

The CBMnet protocol is currently present in all stages of the CBM data acquisition (DAQ) network for the TRD and STS readout. Beside the two FEE ASICs using CBMnet links over HDMI cable, the cores are also integrated in the Read-Out Controller (ROC), the FLES Interface Board (FLIB) and further FPGA to FPGA interconnects. For these links Xilinx Gigabit Transceiver over SFPs are used. A typical setup is depicted in 1. To improve the link stability under influence of radiation, a reworked CBMnet Version 3.0 has been developed and implemented, containing a link layer, various physical layer implementations and more network related building blocks to deliver generally required features in CBM network devices. Implementations have been optimized for FPGA and ASIC use. The logic is built in such a way, that a malfunction triggered by a single event effect is detected and the corresponding functional blocks are reset. In this manner, the data acquisition over a long time is possible without any interruption. Larger test beam read-outs with up to three SPADICs per ROC have been tested in laboratory and under beam. The FLIB physical layer implementation has been tested intensively to work reliable under all conditions. The design can handle up to eight links now.

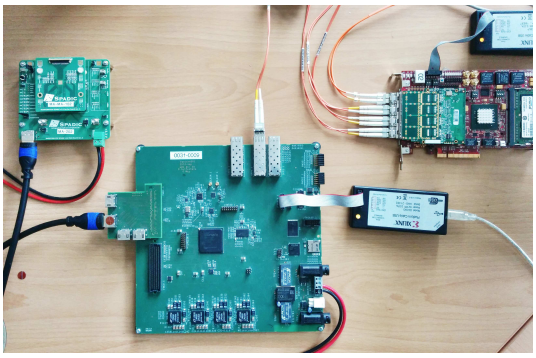

Figure 1: Read-out with FLIB, Syscore3 and SPADIC

Prototyping of a readout aggregation ASIC

A prototype of the readout and aggregation ASIC has been designed together with the Indian Institue of Technology Kharagpur (IITKGP). Therefore, an internship student from IITKGP was visiting the University of Heidelberg for half a year in 2014. This was possible because of successfully raised additional funding from the Heidelberg Center South Asia. This mixed-signal ASIC consists of a full-custom 5Gb/s serializer/deserializer, designed by the IITKGP including design elements such as phase-locked loop, bandgap reference, and clock data recovery, and a digital designed network communication and aggregation part designed by the computer architecture group of the University of Heidelberg.

In addition, there are test structures and an I2C readout integrated to ease bring up and monitoring. A specialty of this test ASIC is the aggregation of links featuring different data rates, running with bundles of 500 Mb/s LVDS [1]. This enables flexible readout setups of mixed detectors respectively readout of various chips. There are 1x, 2x, or 4x LVDS connections available enabling up to 2 Gb/s for a front-end connection. The prototype will be able to run in a mixed configuration, e.g. one 1x, two 2x, and one 4x. A prototype structure diagram depicting the link configuration possibilities is presented in figure 2. As communication protocol for the prototype, a unified link protocol is used including control messages, data messages, and synchronization messages on an identical lane. The design has been successfully simulated, verified, and hardware emulations using Spartan 6 FPGAs. The miniASIC mixed-signal design has been prepared and simulated together with the collaboration partners from the IITKGP. The first chance in 2015 for a submission using the TSMC 65nm LP Europractice process will be taken.

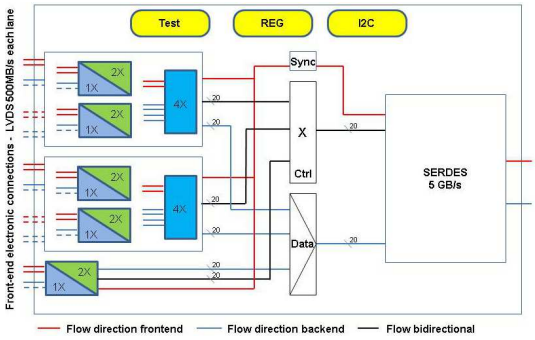

Figure 2: Link connection diagram for HUB ASIC

References

[1] S. Schatral, F. Lemke, U. Bruening, "Design of a deterministic link initialization mechanism for serial LVDS interconnects", Journal, doi:10.1088/1748-0221/9/03/C03022, VOL. 9, No. 03, pages C03022, March 2014.

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