Fast analog signal processor FASP-02 *

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A second version of FASP ASIC dedicated for high counting rate CBM TRD prototypes developed by Bucharest group [1] - [4] was designed and produced. Similar to the first version [5], it is based on AMS 0.35 μm N-well technology. The die size is 4.65 mm x 3.45 mm. Besides the main features of its previous version, new ones are implemented in FASP-02, considering the specific architecture of the fast TRD prototypes mentioned above and the results obtained in the tests carried out in the meantime. The most relevant new features are:

- 16 input channels
- selectable positive or negative polarity of the input signals
- multiplexed analog outputs, i.e. selectable semi-Gaussian or flat top
- channel wise clock synchronized logic time for individual ADC
- channel wise logic time signal generated at the selectable threshold level or at the signal peak detection, accordingly to the user setting
- selectable trigger of neighboring channels relative to the one with the signal over the threshold
- tilted and rectangular pairing of the triangular pads

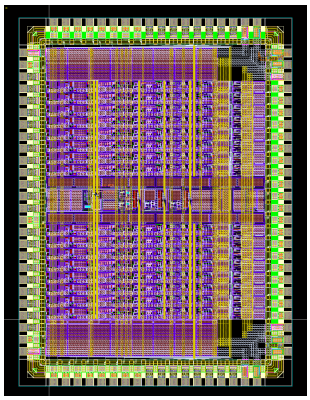

Figure 1: Photo of the FASP-0.2 ASIC

Good response to double pulse, to high pulse rate, fast recovery from positive/negative overload, base line restoration due to pulse rate shift, detector leakage current, temperature and voltage supply variations are also implemented to FASP-0.2 ASIC. Additionally the self trigger capability working with a new channel wise input/output interface enhances the performances of the new FASP-0.2 ASIC.

Table I

SPECIFICATION	FASP-0.1	FASP-0.2
Average pulse rate	>300kHz	>300KHz
Detector pad capacitance	25pF	25pF
Number of analog channel	8	16
Input polarity (1bit selection)	positive	Positive/negative
Channel pairing	no	yes
Charge input range	0.15fC...165fC	0.15fC...165fC
Input type	DC single ended	DC single ended
Channel gain	6.2mV/fC	6.2mV/fC
Shaping time /(1bit selection)	20ns and 40ns /yes	100ns/n.a
Analog output type (1bit selection)	semi-Gaussian or peak-sense	semi-Gaussian or peak-sense
Analog output polarity	Positive (single ended)	Positive (single ended)
Analog output voltage swing	0....1V	0....1V
Analog output DC voltage level base line (cont.adj)	0.2V....1V	0.2V....1V
Semi-Gaussian output FWHM	62ns/110ns	290ns
Peak-sense output plateau	typ. 400ns (cont. adj)	typ. 400ns (clock dependent)
Channel ENC (Cdet=25pF)	980e (St=40ns)/1170e (St=20ns)	940e
Crosstalk (max. signal in only one channel, no signals in others)	0.5%	0.012%
Crosstalk (max. signal in 15 ch. no signal in one channel)	0.7%	0.022%
Self trigger capability: variable threshold (cont. adj)	0....165fC	0....165fC
Logic common event output	negative 20ns width	negative 20ns width
External clock synchronization	no	max. 50MHz
Logic signal channel wise, clock synchronized, output	no	yes
Channel synchronized logic signal occurrence (1bit selection)	n.a	to threshold level / to maximum amplitude
Channel-wise synchronized logic signal for semi-Gaussian output	n.a	negative 20ns to threshold level/ to maximum amplitude
Channel-wise synchronized logic signal for peak-sense output	n.a	neg. 20ns to threshold level/ neg. 14 clock cycle to max. ampl
Channel neighbors trigger enable/disable	n.a	yes

The shaping time for FASP-0.2 is increased to 100 ns in order to accomplish the requirements of the new TRD prototypes with a drift region of 4 mm. The crosstalk is about ten times lover compared to FASP-0.1. The main specifications for FASP-0.1 and FASP-0.2 can be followed in Table I, where the new features and the modified specifications for FASP-0.2 can be followed.

References

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